Update on the HV-CMOS Sensors

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On behalf of the Silicon Tracker WG

Outline

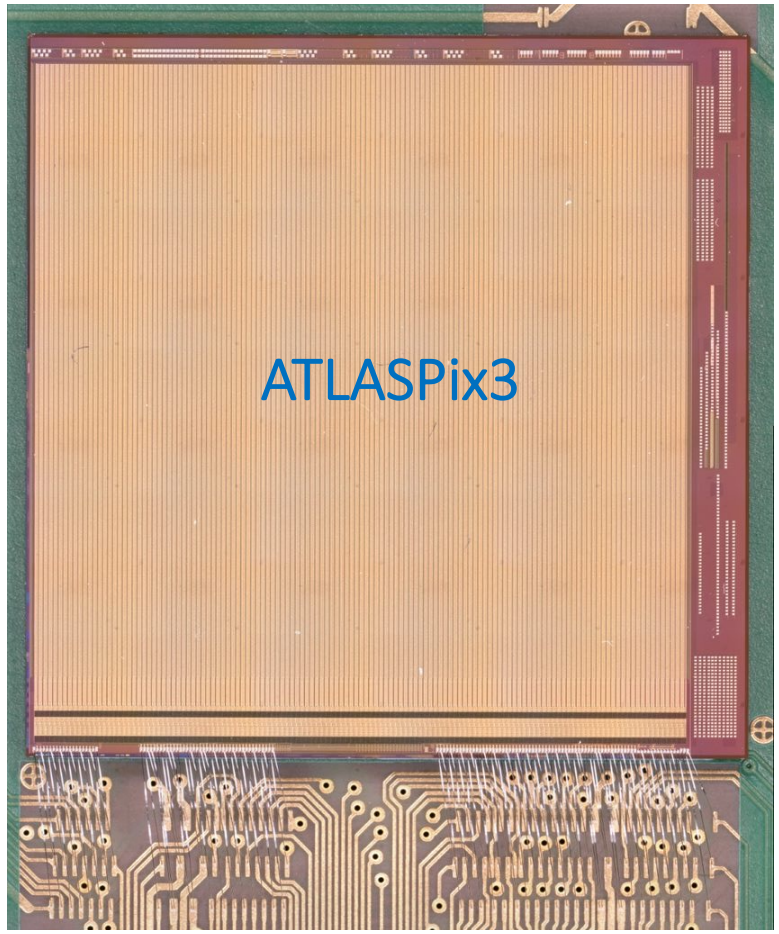
- ATLASPix3 characterization
- New sensor design

ATLASPix3

- Depleted CMOS sensor (HV-CMOS)
  - Fully integrated readout
  - Fast charge collection
  - Low material budget

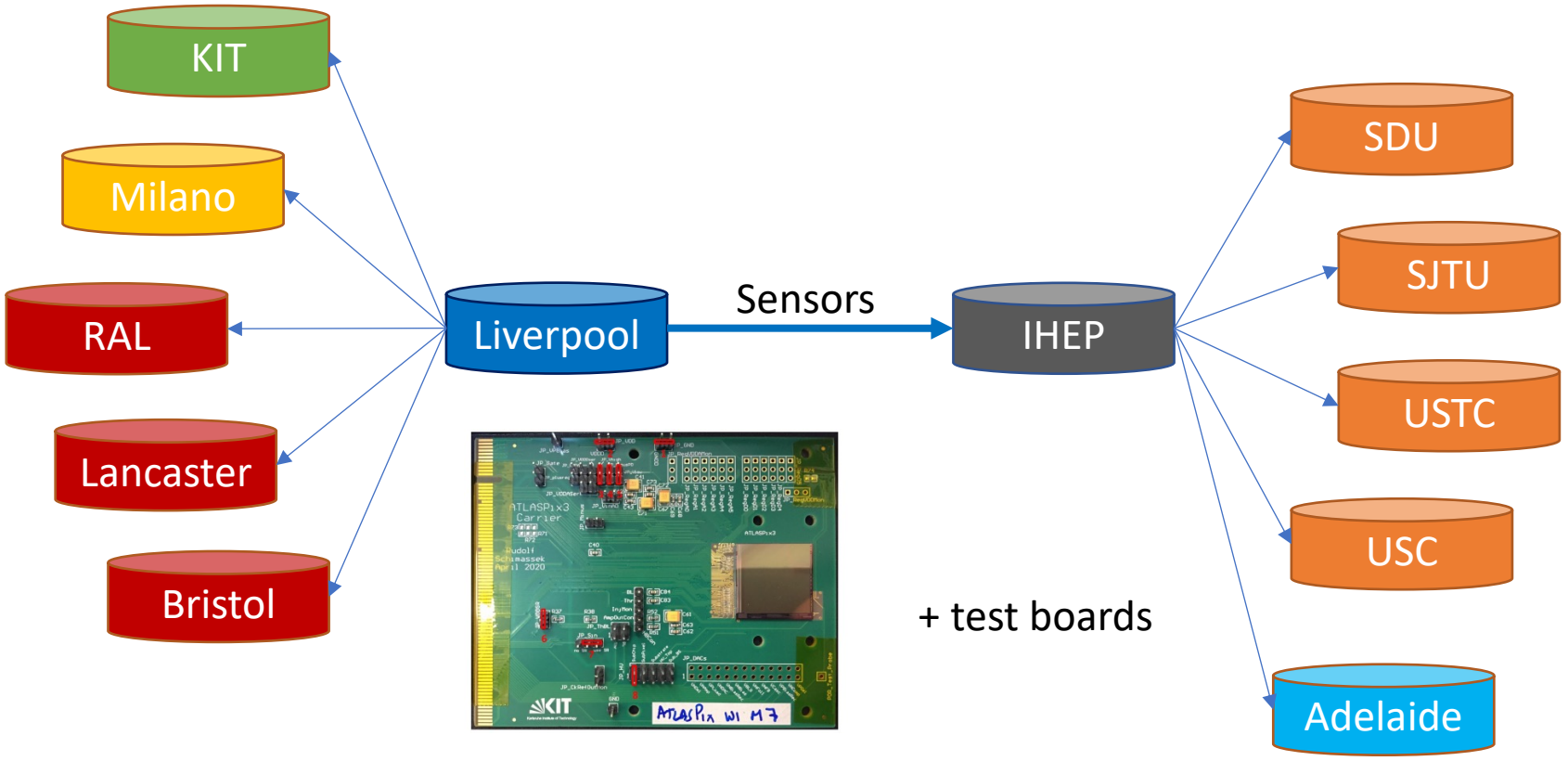
ATLASPix3 Features:

- Pixel size 50×150 μm^2
- Reticle size 20×21 mm^2
- TSI 180 nm HV process on 200 Ωcm substrate
- 132 columns × 372 rows
- Digital part of the matrix located on periphery
- Both triggerless and triggered readout possible
- Up to 1.28 Gbps downlink



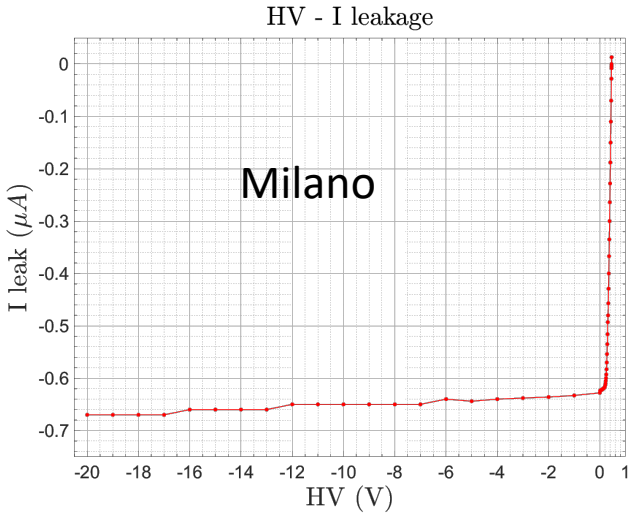
ATLASPix3 Distribution

- Wire-bonded ATLASPix3 sensors distributed to participating institutes
  - Liverpool & IHEP: wire-bonding and distribution centers



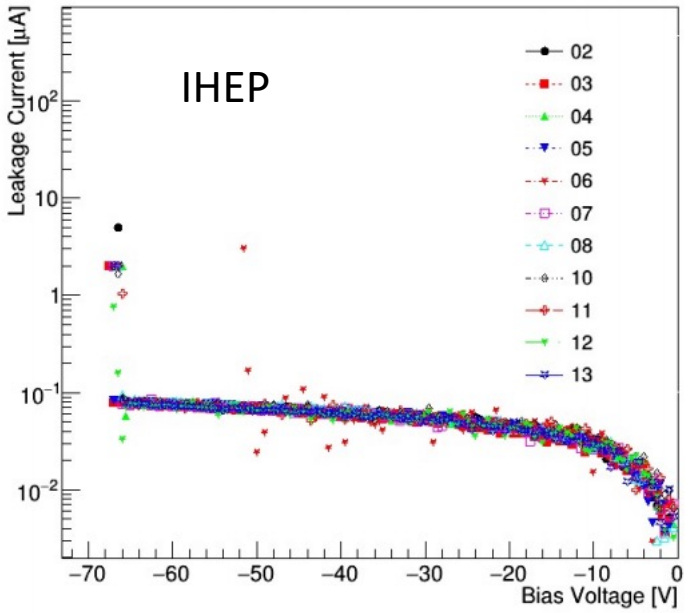
ATLASPix3 IV Scan

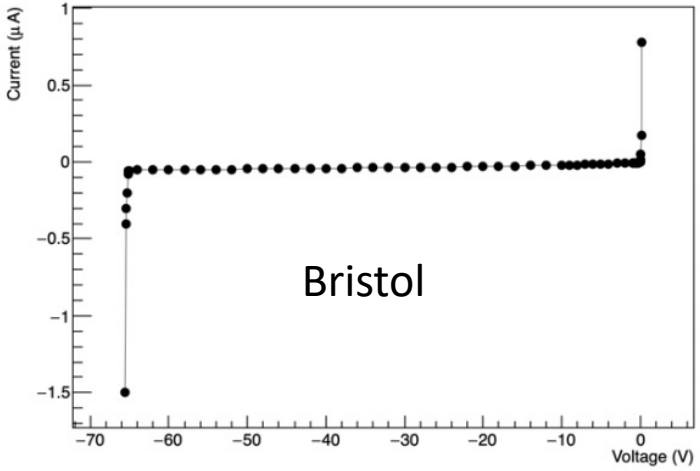
- IV scan to confirm sensor basic electrical characteristics



Most sensors showed consistent IV results

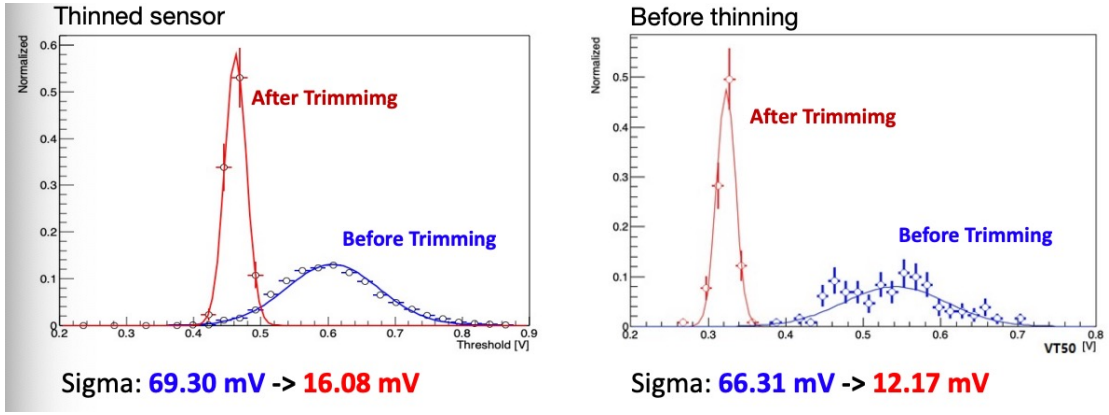
Low leakage current up to the breakdown voltage of 60 V





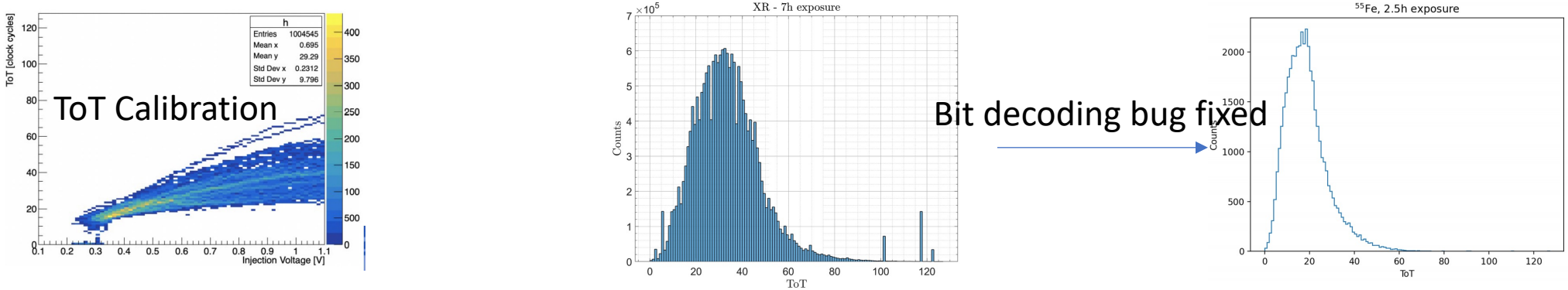
ATLASPix3 Tunings

- Trimming: threshold voltage for each pixel tuned to achieve homogenous sensor response



Consistent trimming results obtained by different institutes (minor variation from chip to chip); no significant change for thinned sensors

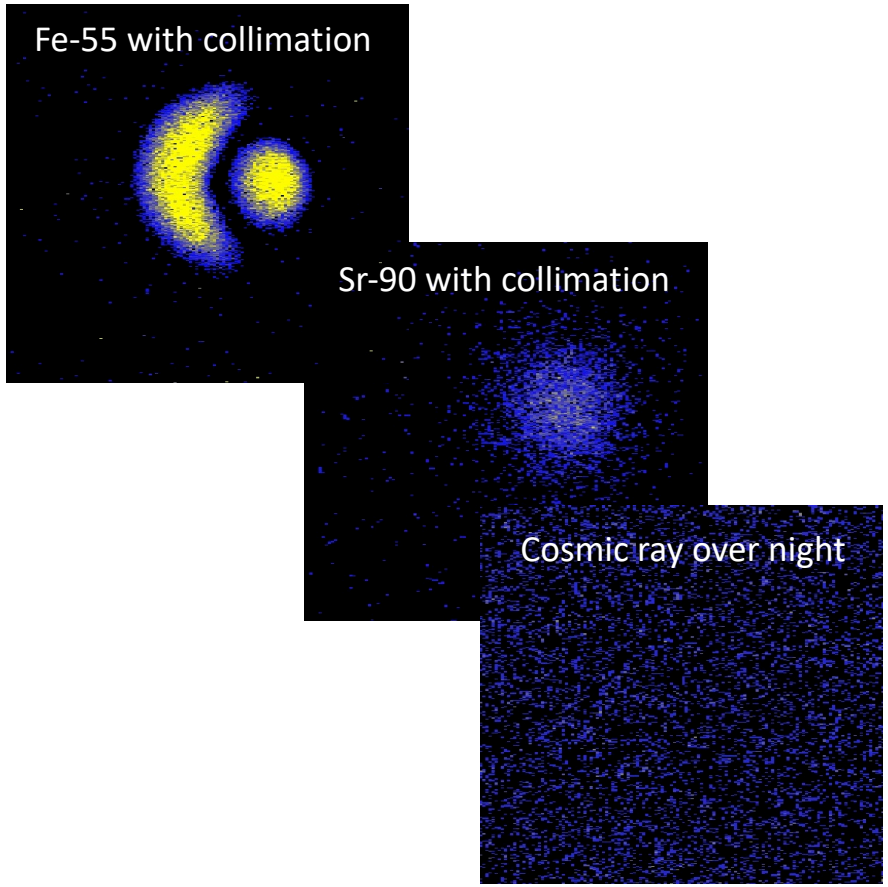
- Time-over-Threshold (ToT): to measure deposited energy



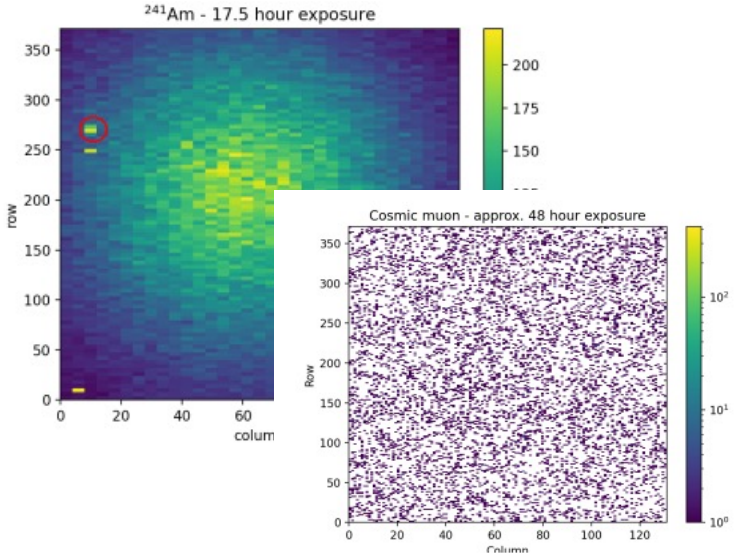
Response to Radioactive Sources

- ATLASPix3 tested with radioactive sources at different sites

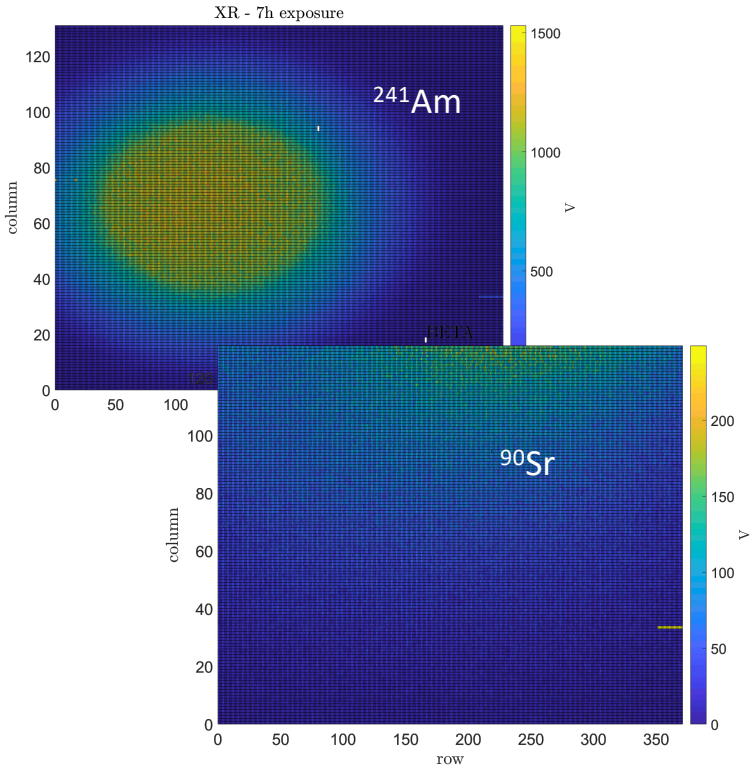
IHEP



Edinburgh/Bristol/Lancaster



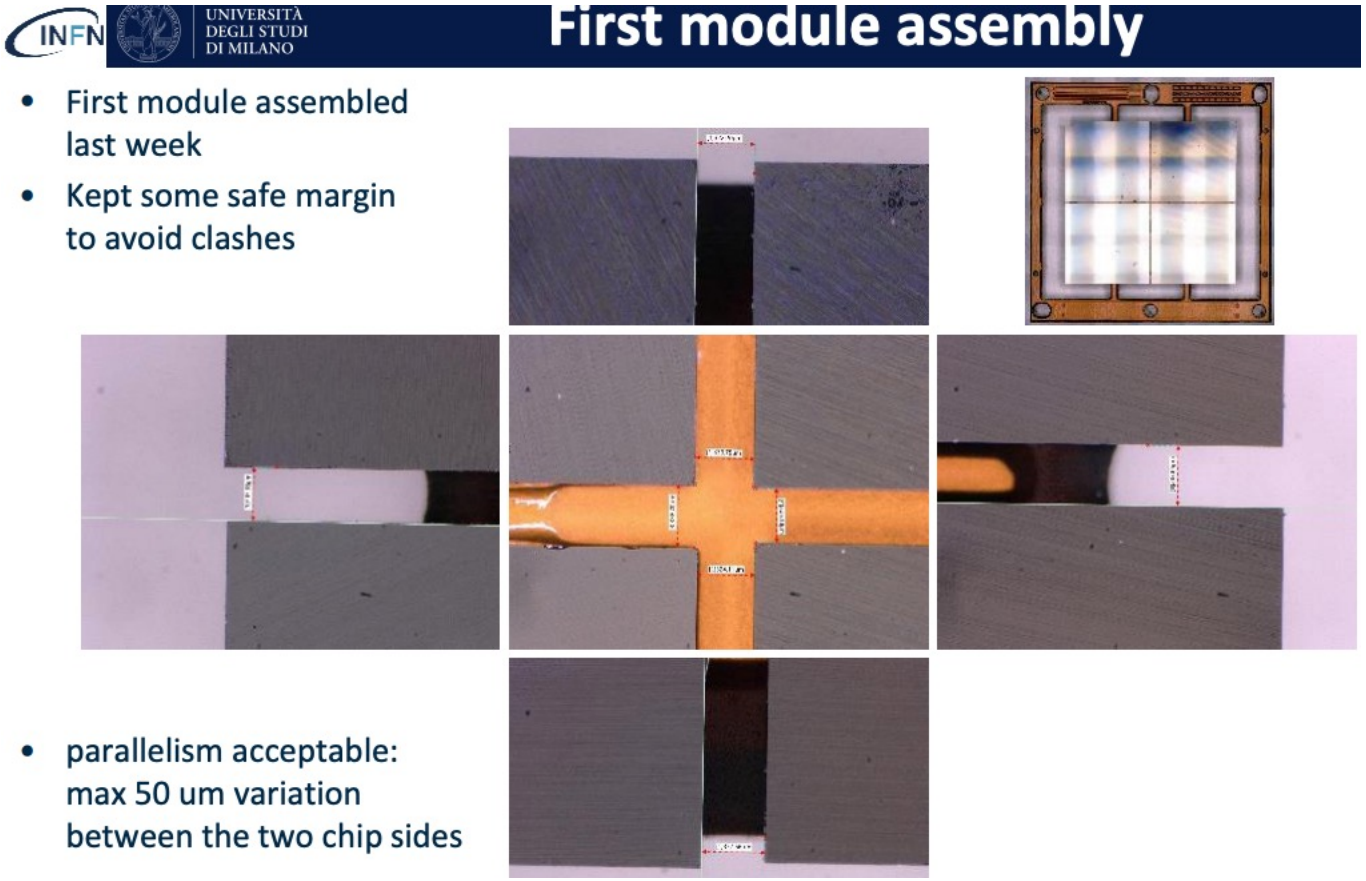
Milano



QuadModule Assembly

Milano

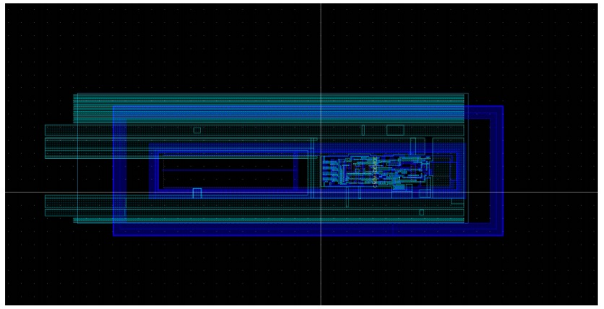
- QuadModule flex PCB electrically tested; module assembly underway

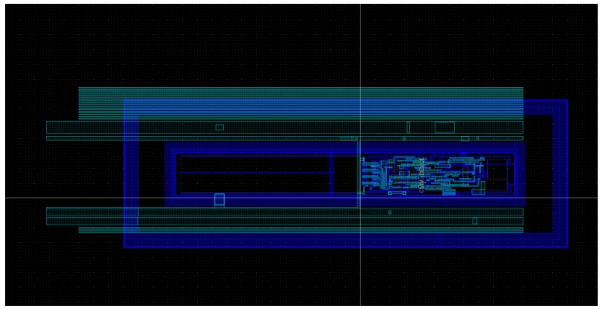


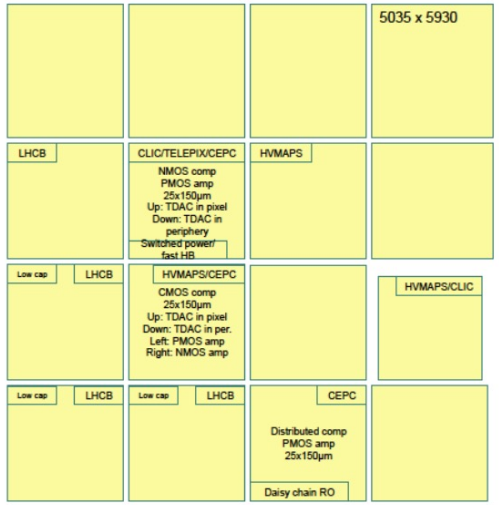
- Defined wire bonding options; to prepare for the test firmware & Software (command decoding configuration fully tested)

More on ATLASPix3

- ATLASPix3.1 (back from foundry)
  - Reduced detector capacitance by replacing M2 shield with M3 shield (250 fF to 130 fF)
  - Modified design of the guard ring
  - Larger distance between DN and PW ring
  - M1 ring disconnected from PW
  - Idea set substrate to -120V and M1 ring to -60V
  - Added stability capacitor to the power regulator
- Optimization for the CEPC tracker (submitted)
  - Smaller pixel size (25µm) in φ direction
  - Lower capacitance
  - Amplifier and comparator design
  - Electronics in pixel or periphery
  - Daisy chain of readout





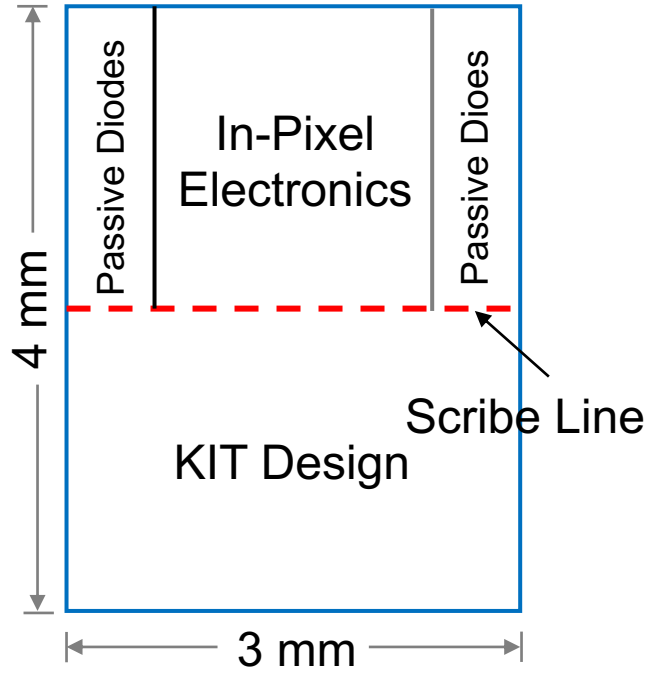


Migration to New Process

- Started new sensor design with the HLMC 55 nm HV-CMOS

- MPW: 3×4 mm^2, 50 dies; caveats: low bulk resistivity wafers (10 ohm), no deep P-well

- Engineering run: deep P-well possible (being tried out for their CIS process of the same feature size); high resistivity wafers to be negotiated



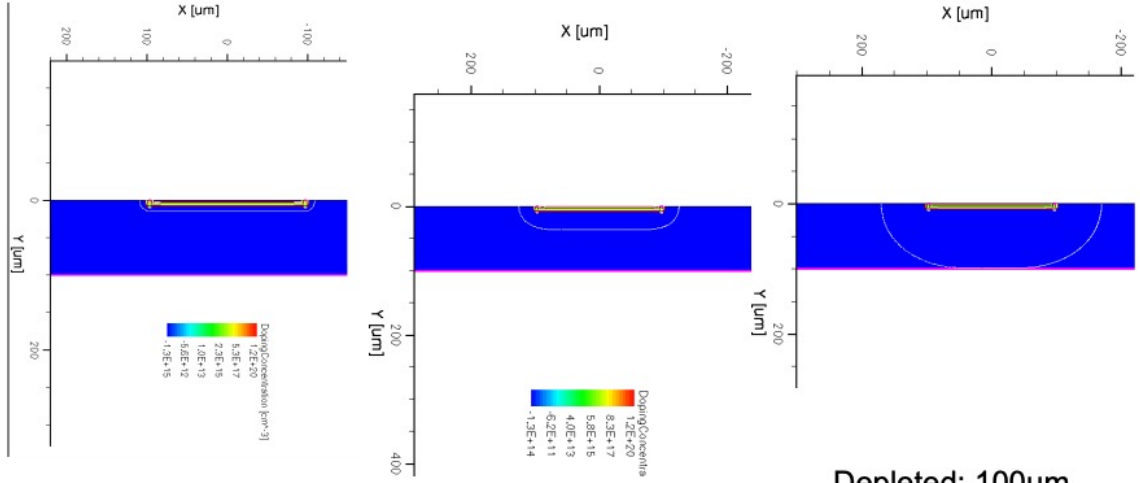
MPW submission date: 16 August, 2021

Sensor Design

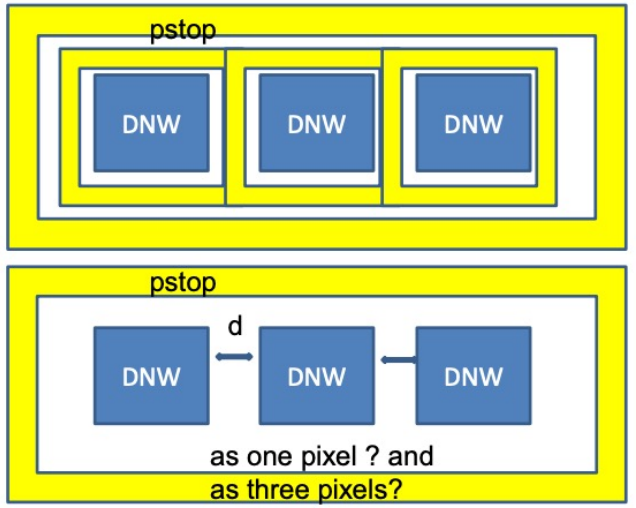
Biweekly meetings to coordinate the design effort

- Pixel size: 25× 150 μm^2, to meet the spatial resolution requirement

Achievable depletion depth with different bulk resistivity



M. Zhao



- Design of in-pixel electronics, e.g. charge pre-amplifier, on-going
  - Simulation with Hspice (Spice model provided)

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