Silicon Tracker for CEPC

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On behalf of the CEPC Silicon Tracker WG

CEPC Detector & MDI Mechanical Design

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Si Tracker for CEPC

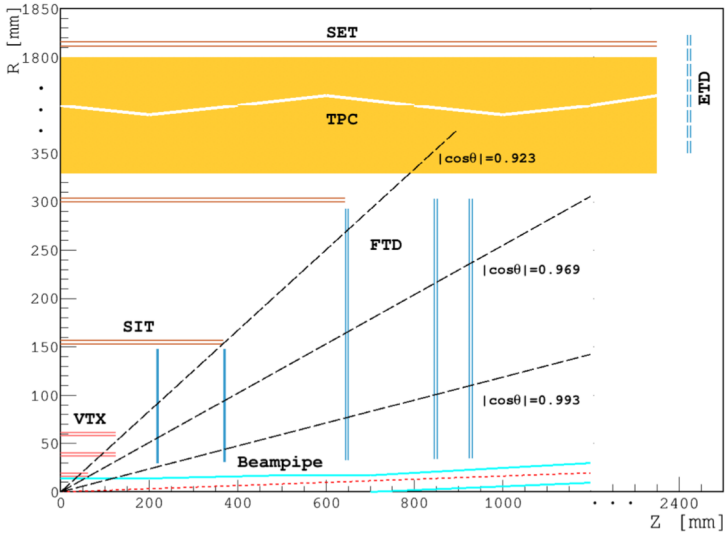
- CEPC requires a high-resolution and low-material tracking system
- Large area of silicon!
  - > 70 m^2 for baseline design: Silicon + TPC
  - ~ 140 m^2 for Full Silicon Tracker

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

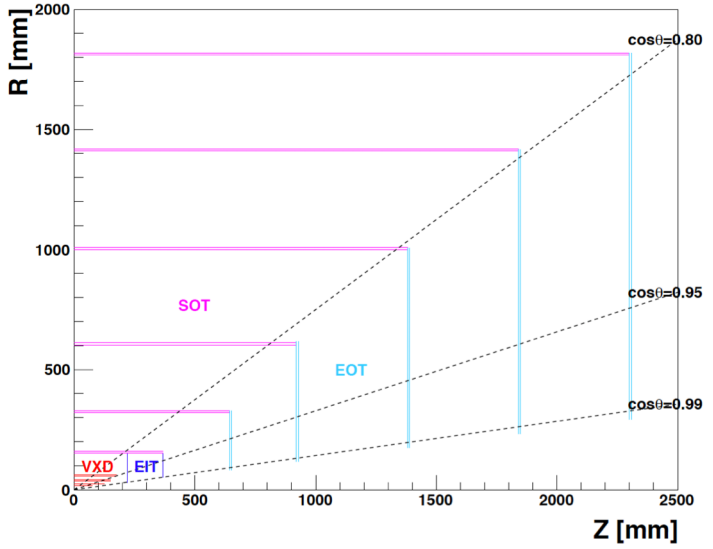
$$a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1}$$

$$b \sim 1 \times 10^{-3}$$

- CMOS is the promising technology for cost effectiveness and performance



Baseline design



Full Silicon Tracker

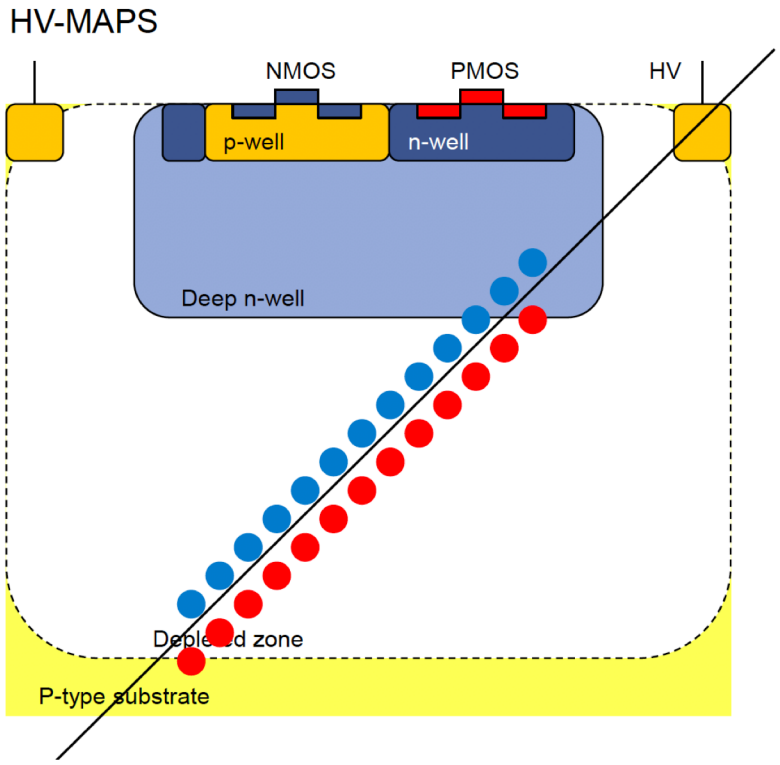
CMOS Si tracker collaborators

- Australia
  - University of Adelaide
- China
  - Harbin Institute of Technology
  - Institute of High Energy Physics, CAS
  - Northwestern Polytechnical University
  - Shandong University
  - T. D. Lee Institute – Shanghai Jiao Tong University
  - University of Science and Technology of China
  - University of South China
  - Zhejiang University
- Germany
  - Karlsruhe Institute für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisa e Università di Pisa
  - INFN Sezione di Torino e Università degli Studi di Torino
- UK
  - Lancaster University
  - Queen Mary University of London
  - STFC – Daresbury Laboratory
  - STFC – Rutherford Appleton Laboratory
  - University of Bristol
  - University of Edinburg
  - University of Liverpool
  - University of Oxford
  - University of Sheffield
  - University of Warwick

HV-CMOS sensors

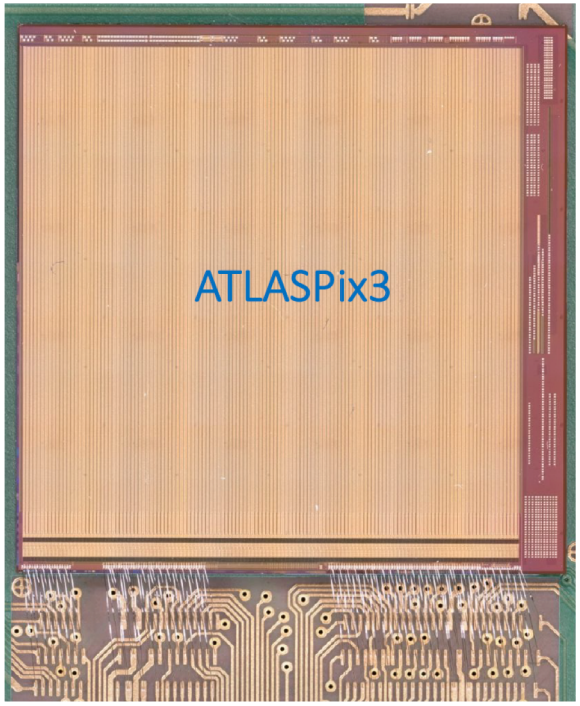
- CMOS
  - Low material budget, low power
- Depleted sensor
  - Fast charge collection
- Readout fully integrated

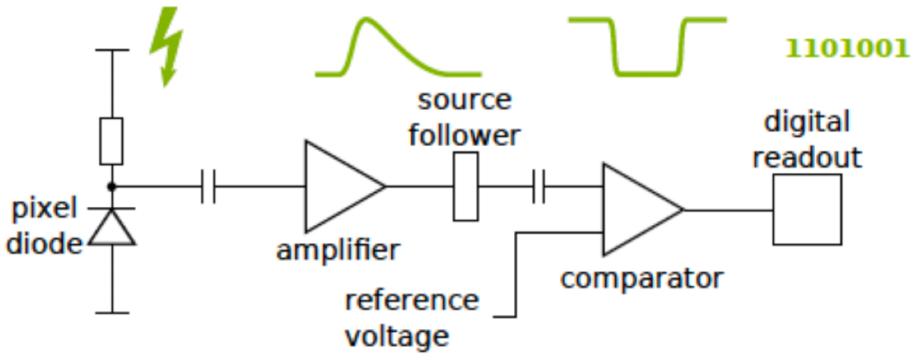
- High voltage monolithic active pixel sensors: deep n-well isolates electronics, allowing bias >= 50V
  - Depletion depth of 30~170 um

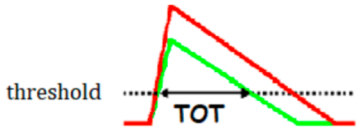


Sensor candidate: ATLASPix3

- ATLASPix3 features
  - TSI 180nm HV process on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 132 columns × 372 rows (20.2 × 21 mm^2 chip)
  - Triggerless/triggered readout possible
  - Binary with ToT information
- Designed at KIT



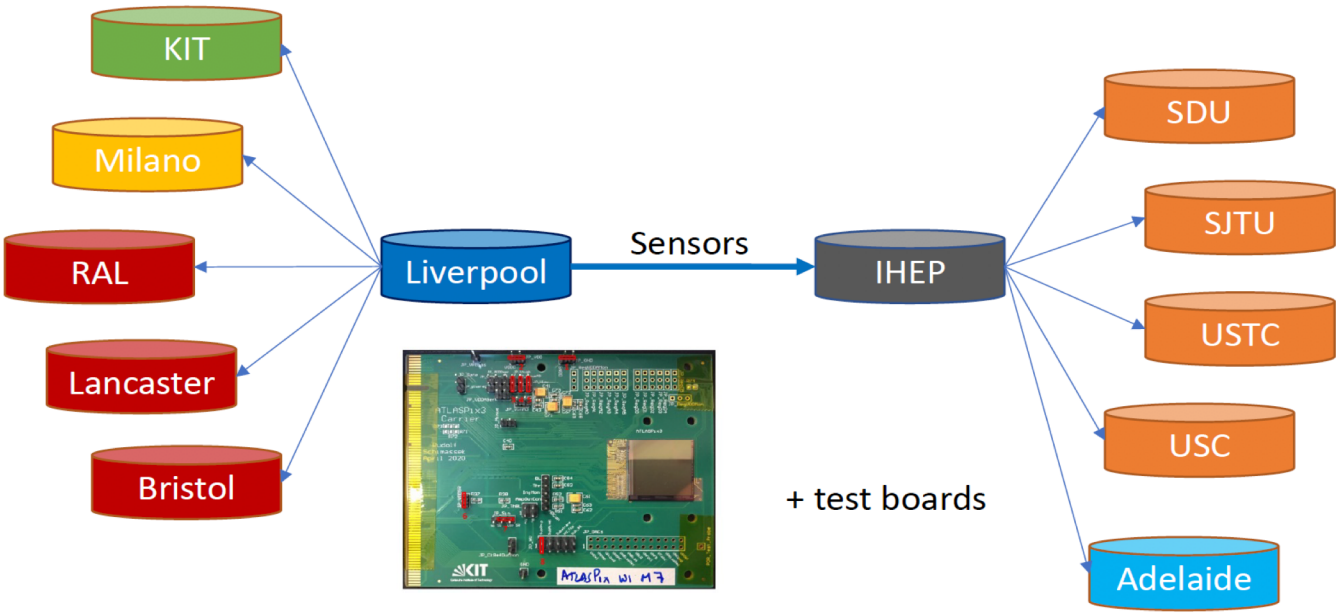




Time-over-Threshold (ToT) as proxy of signal amplitude

ATLASPix3 tests

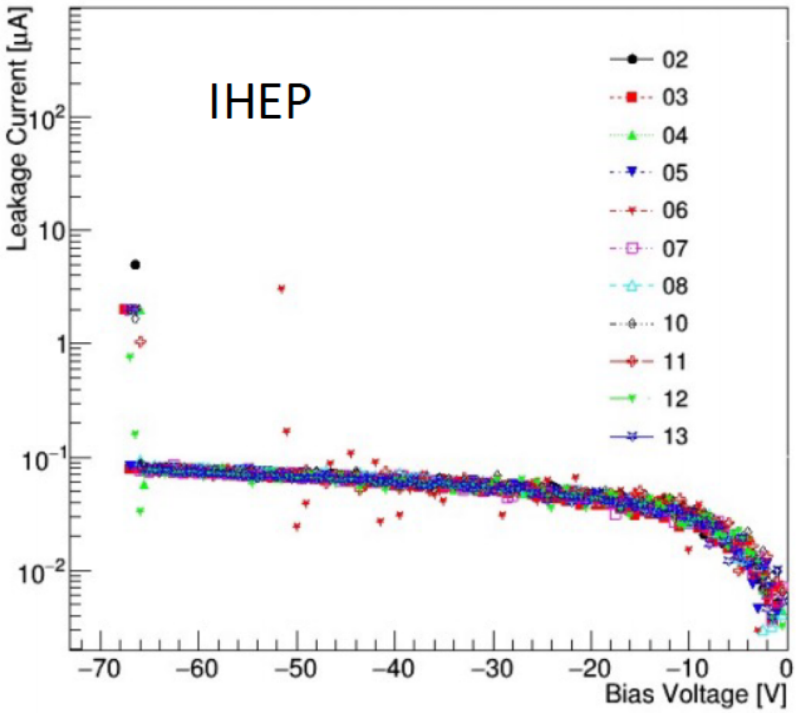
- Wire-bonded test boards distributed to multiple institutes



- Tests performed at various locations, with support from KIT

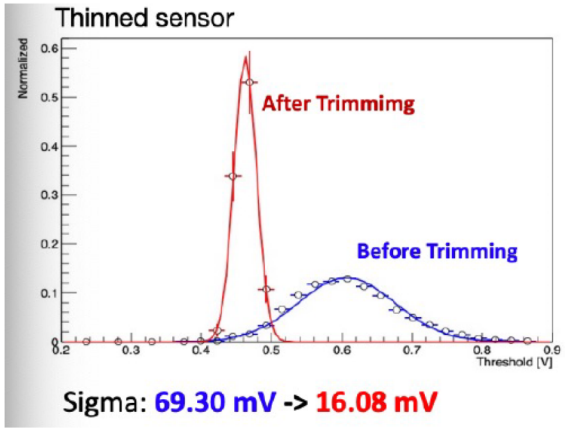
ATLASPix3 tests

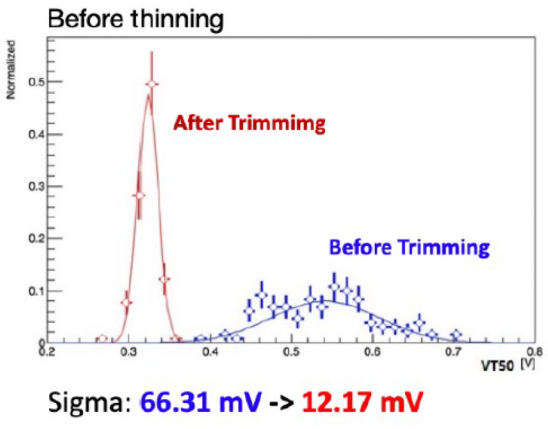
- IV scan confirms sensor electrical characteristics: breakdown up to 60V



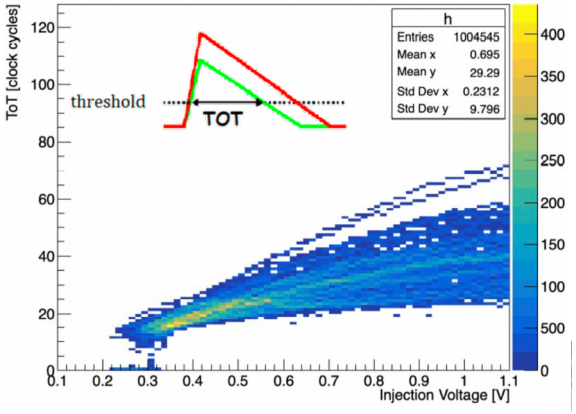
ATLASPix3 tests

- Trimming: tuning threshold for each pixel to gain homogenous response across sensor array





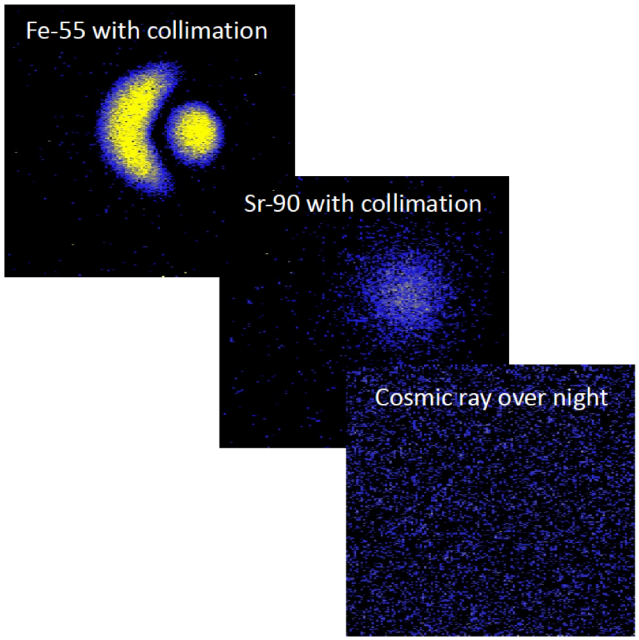
- ToT: a measure of deposited energy; calibration needed due to non-linearity



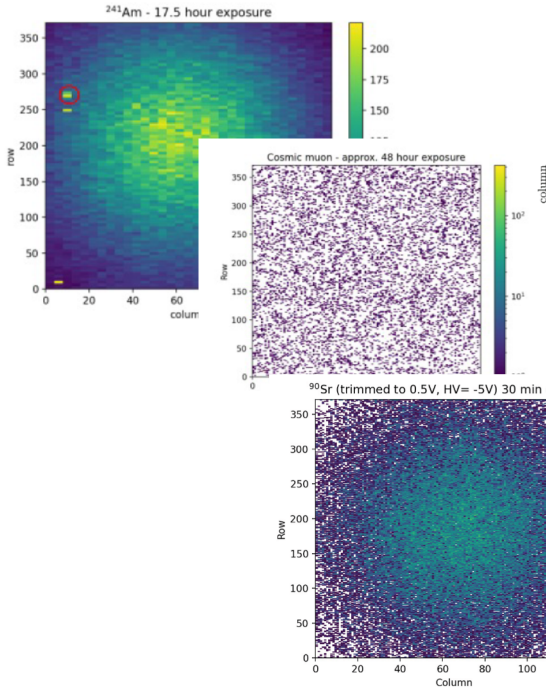
ATLASPix3 tests with radioactive sources

- ATLASPix3 responses to cosmic ray or various radioactive sources are observed at different sites

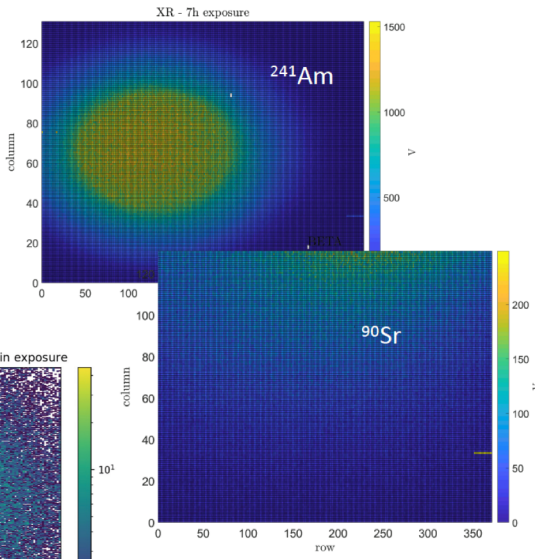
IHEP



Edinburgh/Bristol/Lancaster

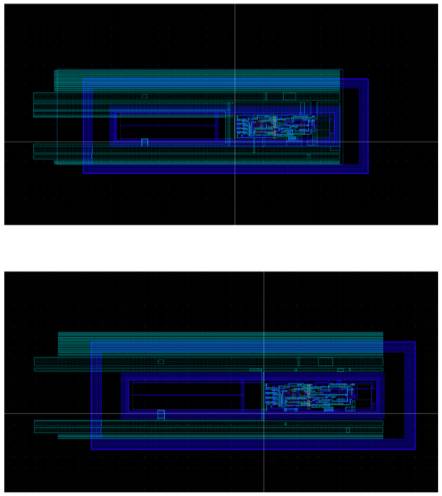


Milano



Further sensor development

- ATLASPix3.1
  - 12 wafers delivered in 02/2021
  - Reduced capacitance (250 fF → 130 fF)
  - Modified guard ring design

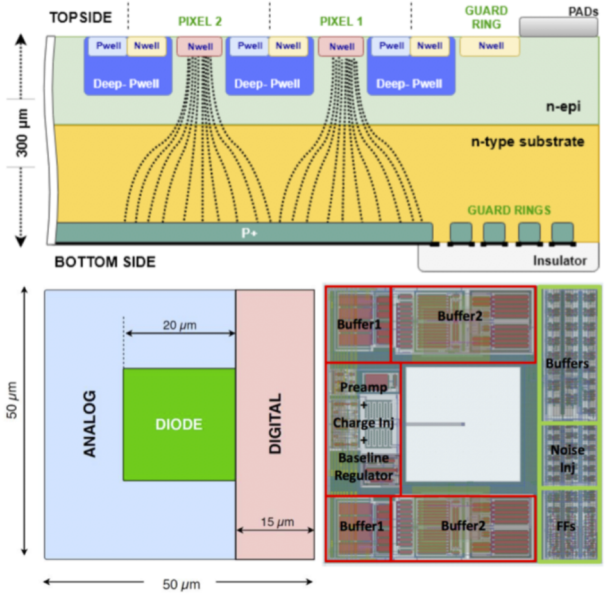


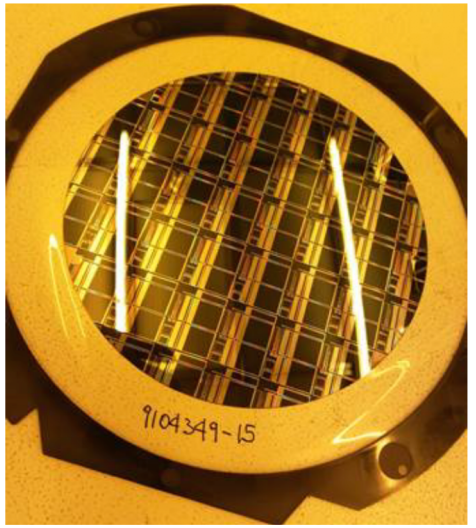
- CEPCPix
  - Smaller pixel size in $r\phi$: 50 µm → 25 µm
  - Low-power amplifiers and comparators
  - Daisy chain of readout reduces number of data links in case of low occupancy

New sensor design

- ARCADIA
  - 110 nm CMOS CIS technology at Lfoundry with high resistivity bulk
  - Main Demonstrator Chip (MD1): Pixel size 25 µm × 25 µm, reticle size 2.6 × 1.3 cm^2
  - First SPW by 11/2020, MD1 chip under characterization, 2nd run mid-2021
  - Triggerless binary readout
  - Design and fabrication towards CEPC since end 2019

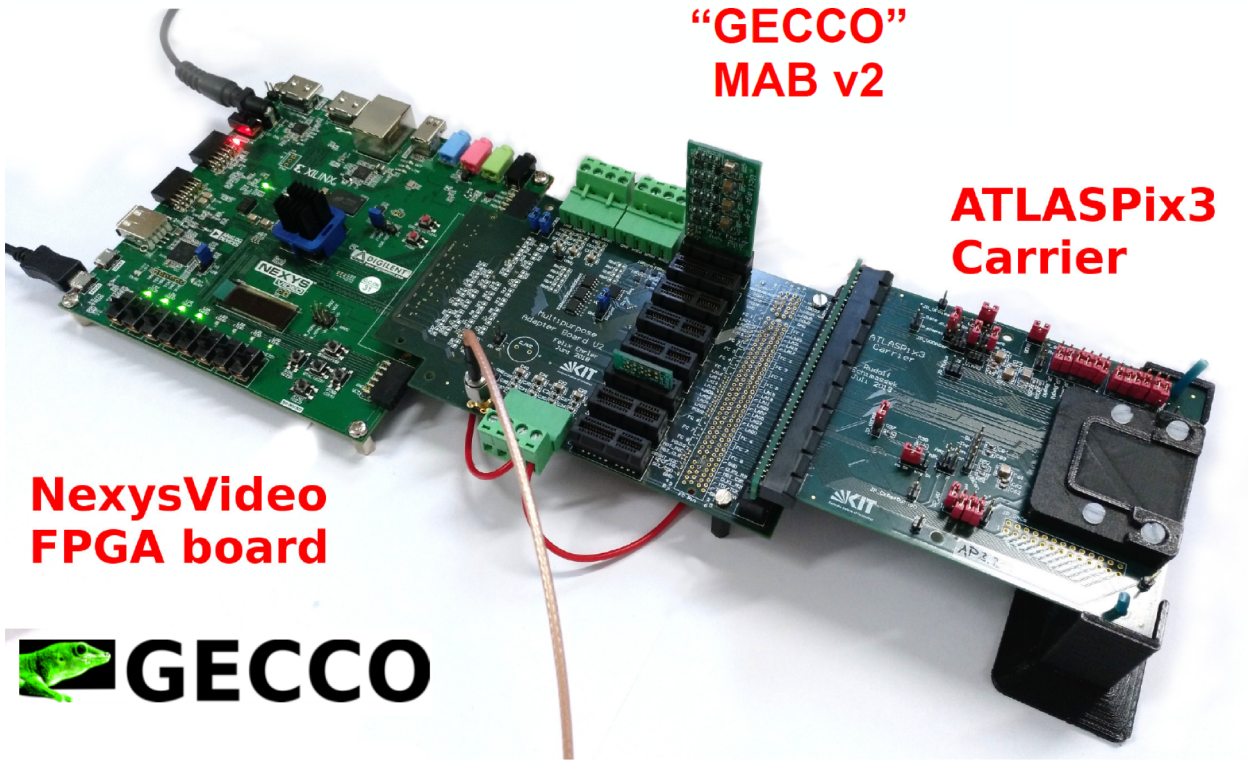
- Other possible foundry
  - HLMC: 55nm HV-CMOS from Chinese foundry, aiming at MPW early 2022





Readout system

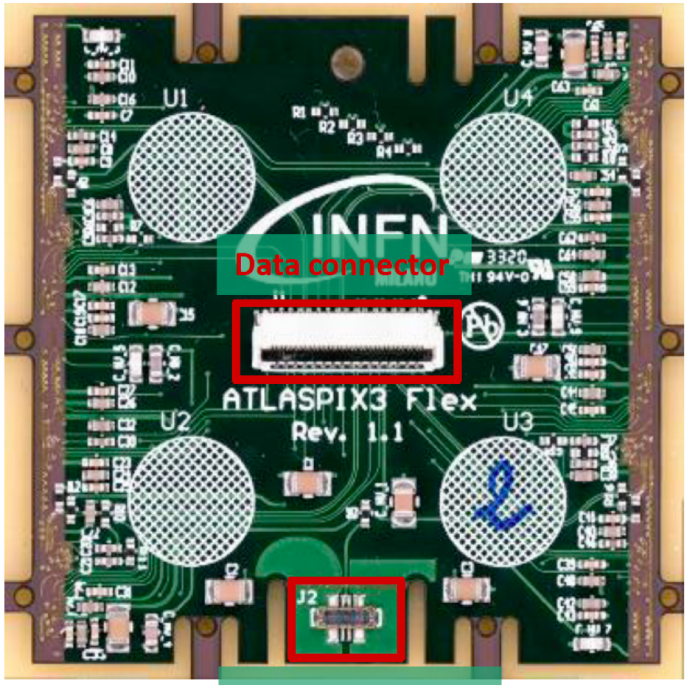
- GEneric Configuration and COntrol System
  - Versatile system for different applications designed at KIT
  - LFP-FMC connection to Nexys FPGA, PCIe x16 to DUT, allows extensive tests
  - Carrier board for ATLASPix3 single-chip
- YARR (a self-contained DAQ) is possible for ATLASPix3 with adaptation

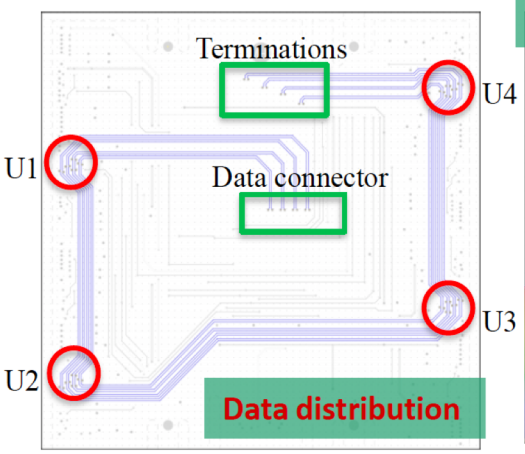


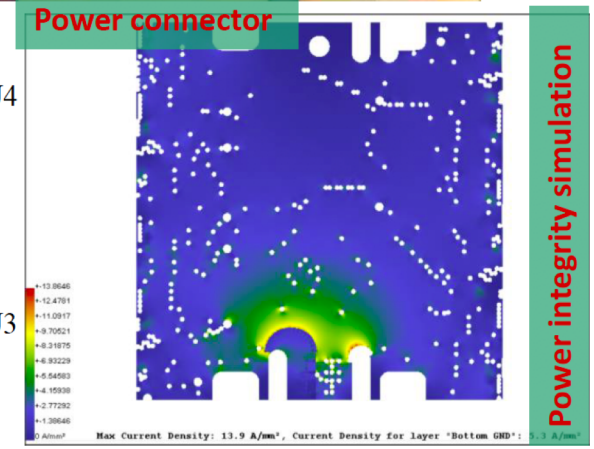
Module concept

- Readout unit based on 4 chips
  → “Quad module”

- Flex designed by INFN Milan
  - Shared service by common power connections and configuration lines
  - Avoid complication with stitching
  - PCB under verification

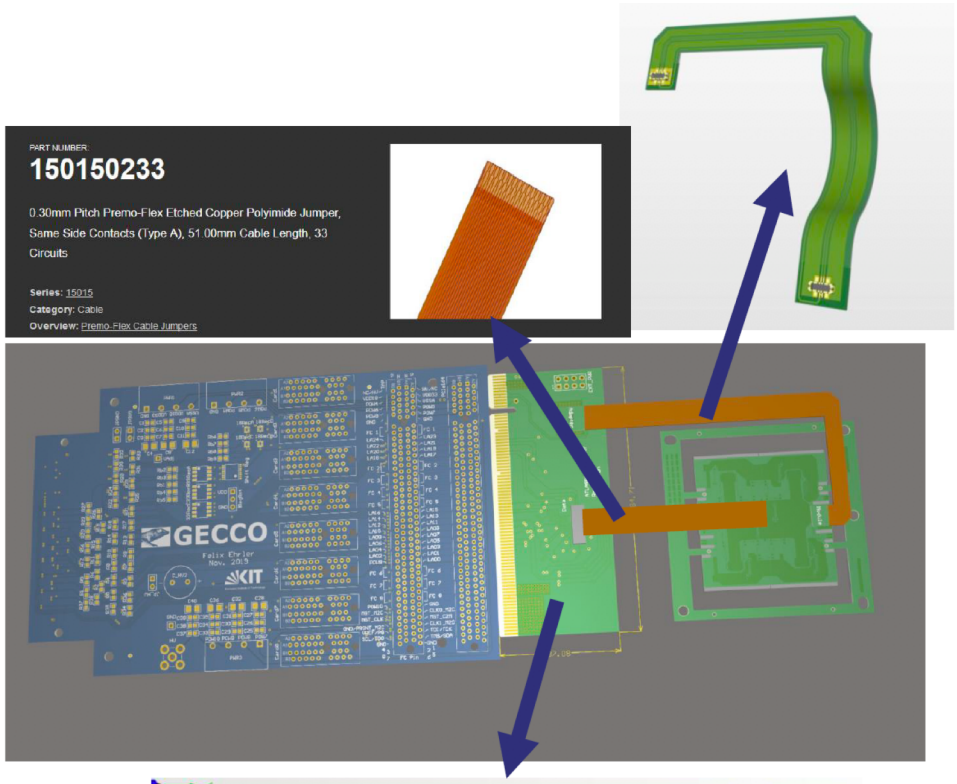


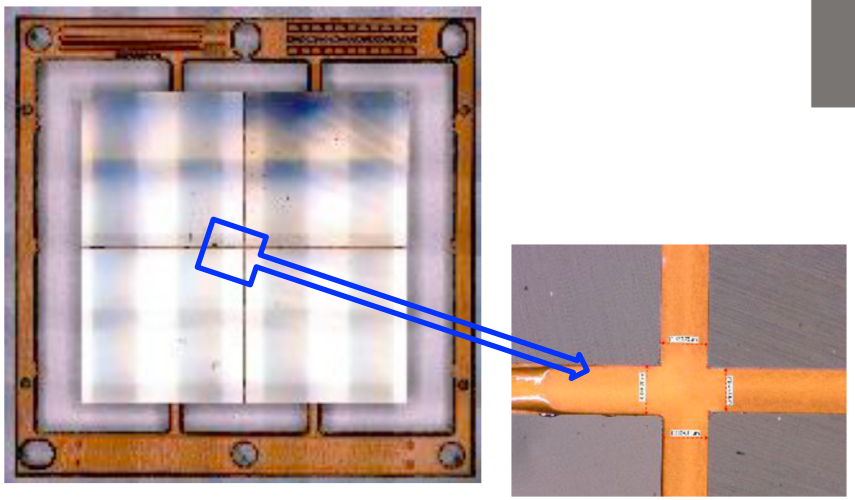


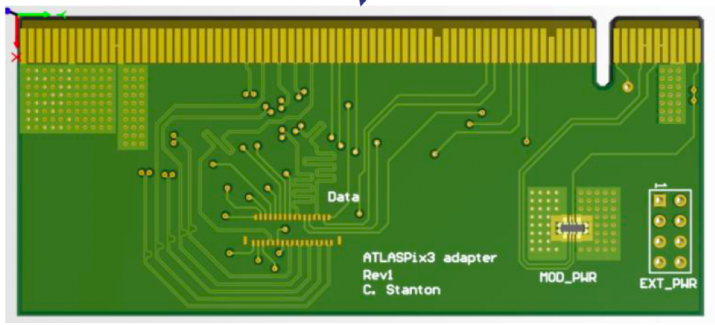


Quad Module

- First module assembled
- Adapter card for connection to GECCO system + commercial data pigtail + custom power pigtail
- Test on the quad ongoing

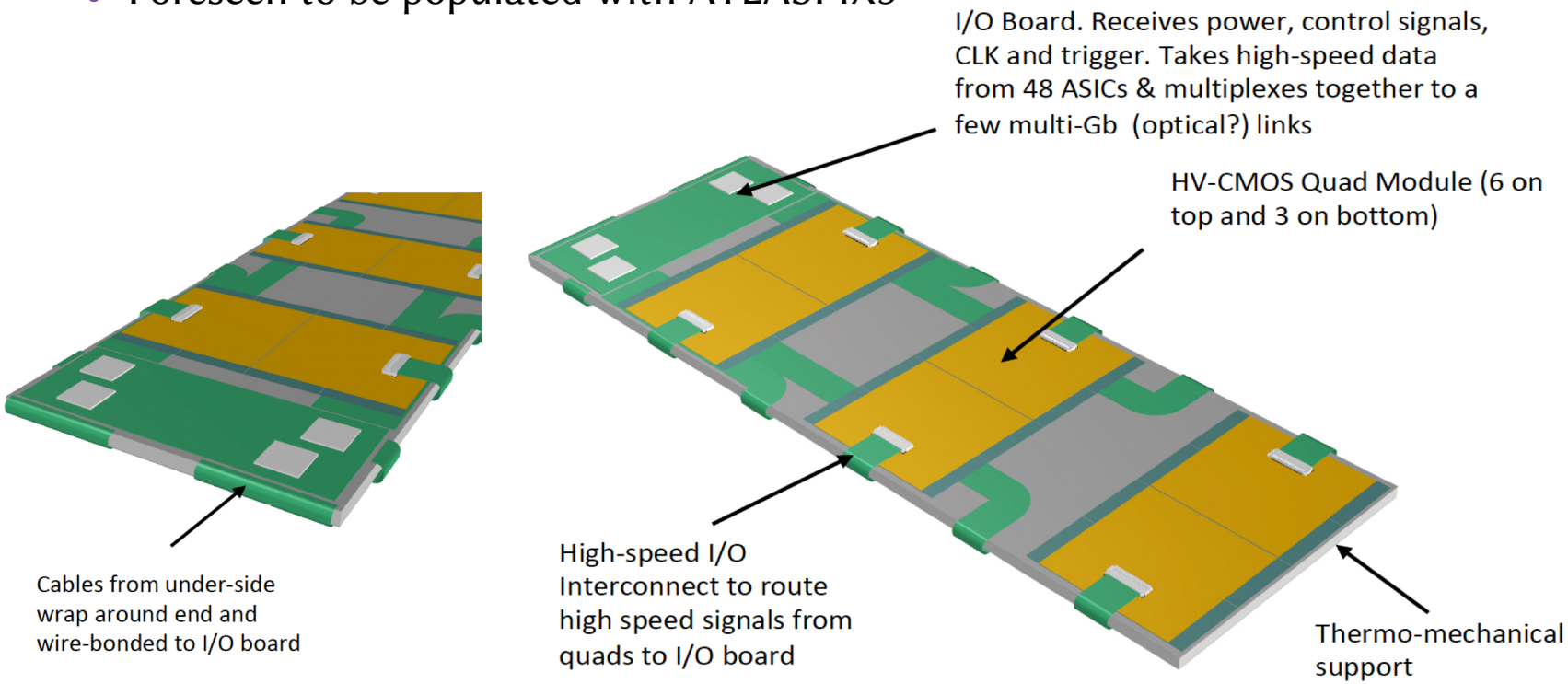


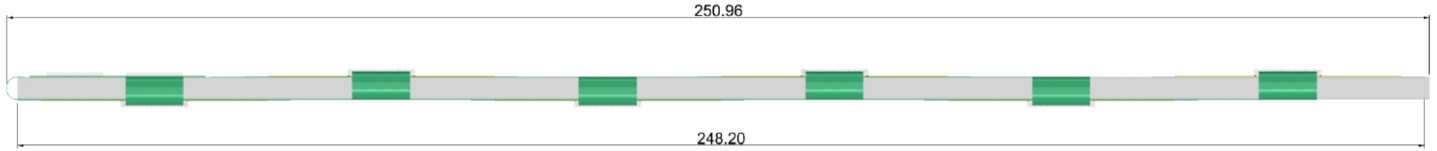




Stave demonstrator

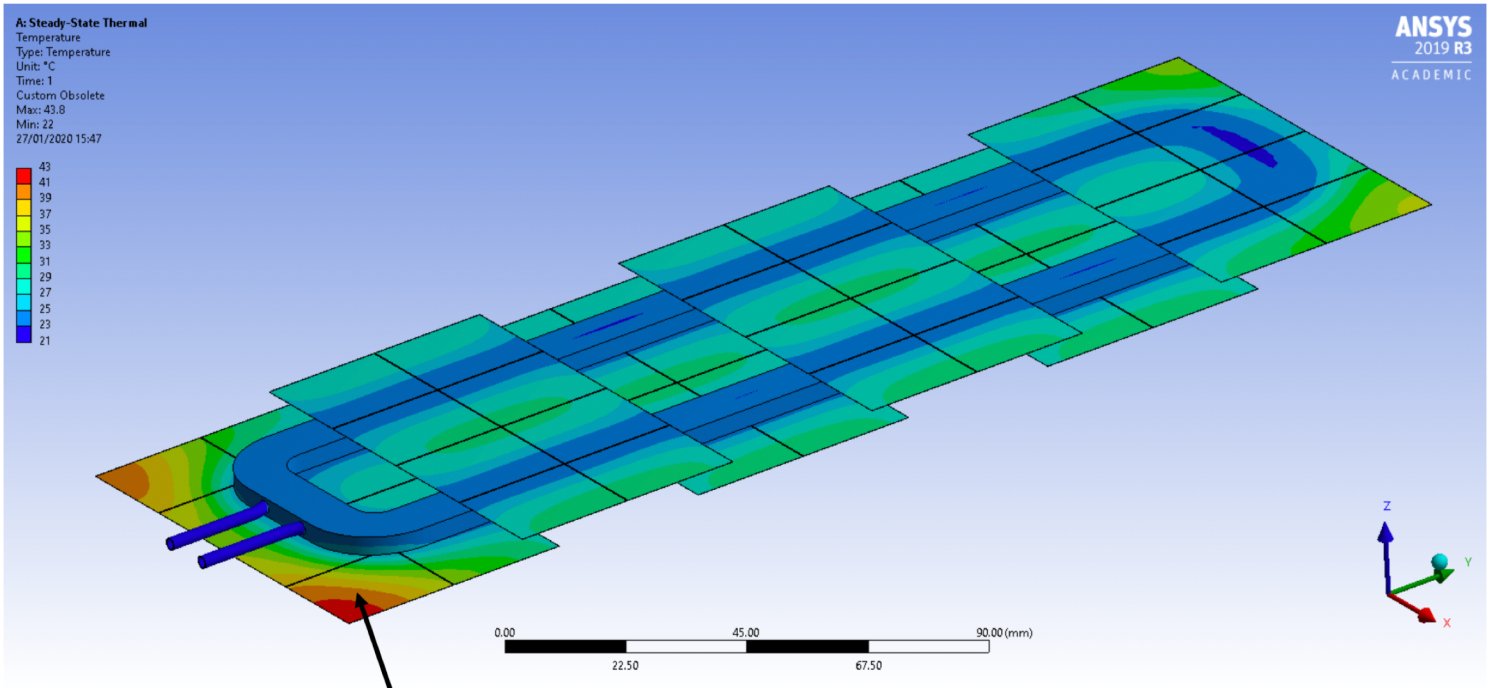
- A stavelet demonstrator with 12 quad modules under development
  - Aggregation of data + optical conversion at end-of-stave; serial powering
  - Foreseen to be populated with ATLASPIX3





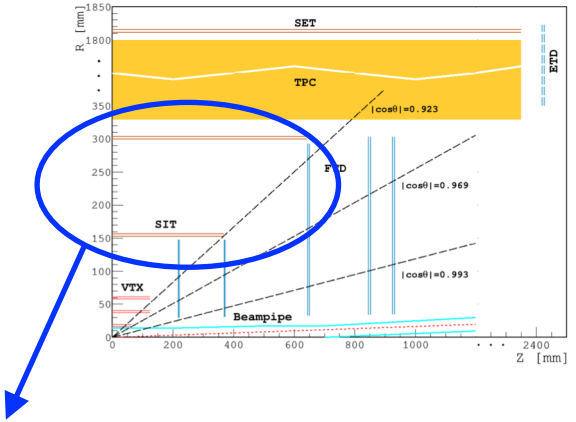
Thermal simulation

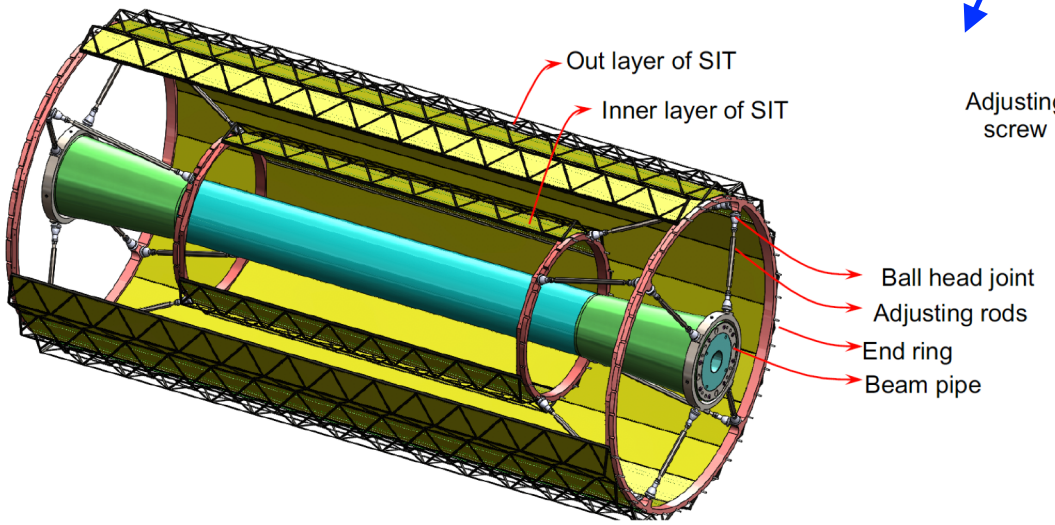
- ATLASPix3 power consumption 150 mW/cm^2 → 2.4 W/module
- This means ~0.5kW for half stave in layer 1, total FE ~100kW
- CO_2 cooling (or water cooling)

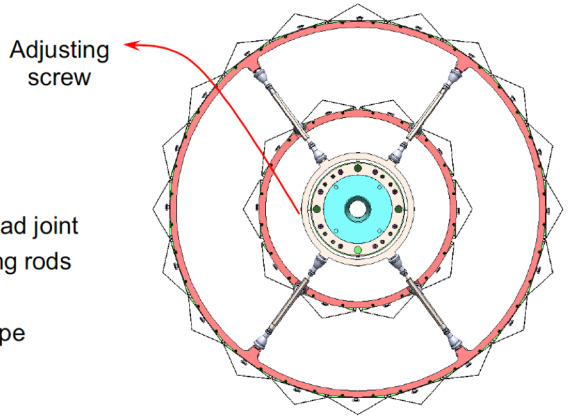


Mechanical design

- Design target: 0.65% X_0 for stave + modules
- CDR baseline design: 2 SIT layers
  - Stave concept: truss structure with cold plate







Similar to staves of ALICE Outer Barrel (0.8% X_0)

Mechanics R&D

- R&D ongoing for the system design
  - Long barrels vs. Endcaps?
  - Novel materials like SiC?
  - Assuming ATLASPix3 power consumption, air cooling might suffice but should consider liquid cooling as an option
  - …

Summary

- Development ongoing for CMOS based CEPC silicon tracker
  - Tests and prototyping with ATLASPix3 sensors, optimization for CEPC ongoing
  - Readout system for single-chip enables tests at various institutes
  - Quad module assembly and test progressing
  - System design and preparation of stavelet under way

http://cepc.ihep.ac.cn/~cepc/cepc_twiki/index.php/Si_Tracker