A 128-channel FPGA-based multi-phase sampling TDC for double-end readout RPC

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Outline

- Motivation
- Multi-phase clock sampling TDC
- Performance of the TDC with the signal generator
- TDC in a real RPC detector
- Summary

Motivation

❖Mass RPC production @ USTC

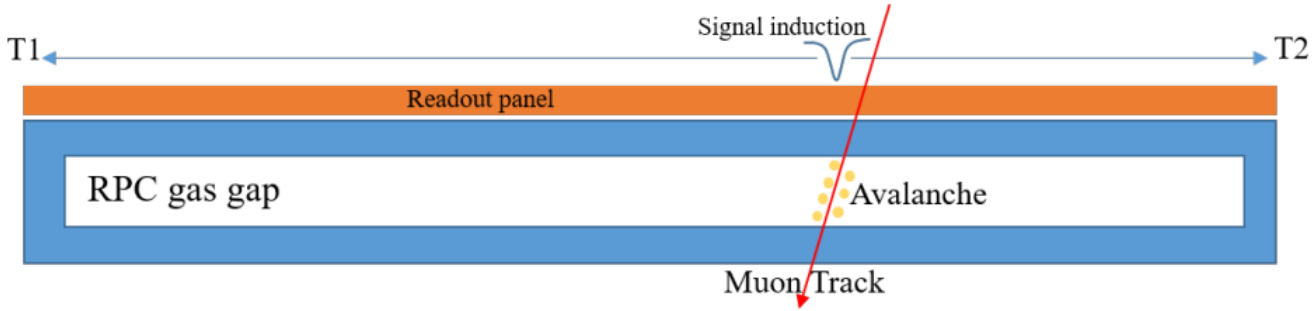
- Large number of TDC channels
- ~1000 channels with PXI, which provides 14 PXI peripheral slots

❖Double-ends readout method

❖$p = \frac{v}{2}(T_1 - T_2),\ \sigma_p = \frac{v}{2}\sqrt{\sigma_{T_1}^2 + \sigma_{T_2}^2}$

❖If $\sigma_p < 2cm$ and $v \approx 20cm, \sigma_T < 140ps$

❖$\sigma_T = \sigma_{FEE} \oplus \sigma_{\mathrm{TDC}} \oplus \sigma_{\mathrm{Avalanche}} \oplus \sigma_{\mathrm{T\_transmission}}$



❖TDC design goals

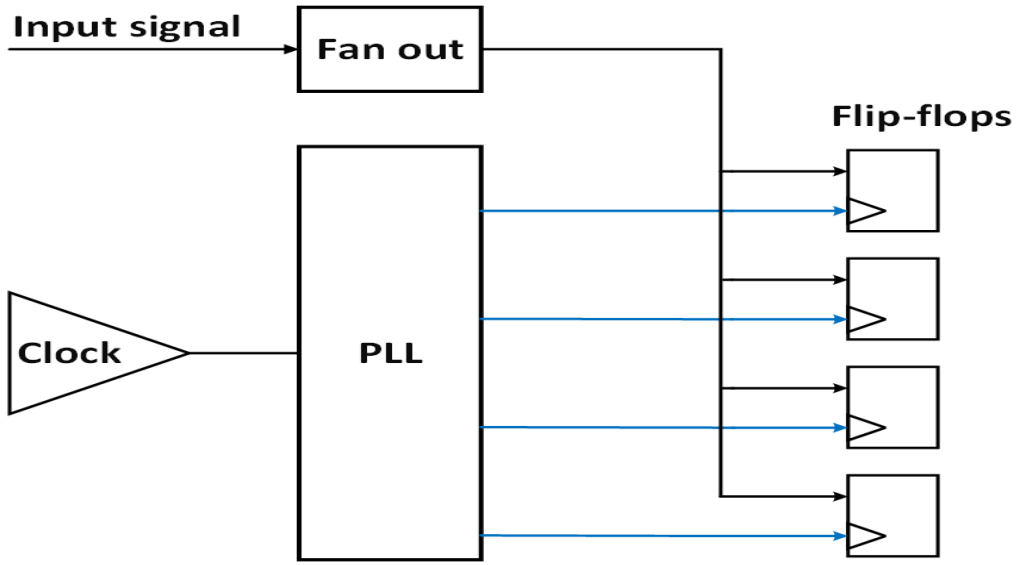
- 128 channels
- $\sigma_{TDC} < 70\ ps$
- Dead time $< 20\ ns$
- Power dissipation $< 100\ mW$

Commercial TDC	分辨率	通道数
V1290A	**35ps**	**32**
V1190A	**80ps**	**128**

Multi-phase clock sampling TDC

❖Theory

- Signal introduced to several flip-flops
- Generate equal-phase shift clocks by PLL structure
- Fine count by phase shift clocks after flip-flops



❖Characteristics

- Less resources occupancy
- Adjustable nonlinearity
- Bin width $\sim 100\ ps$
- Small dead time

❖Conclusion

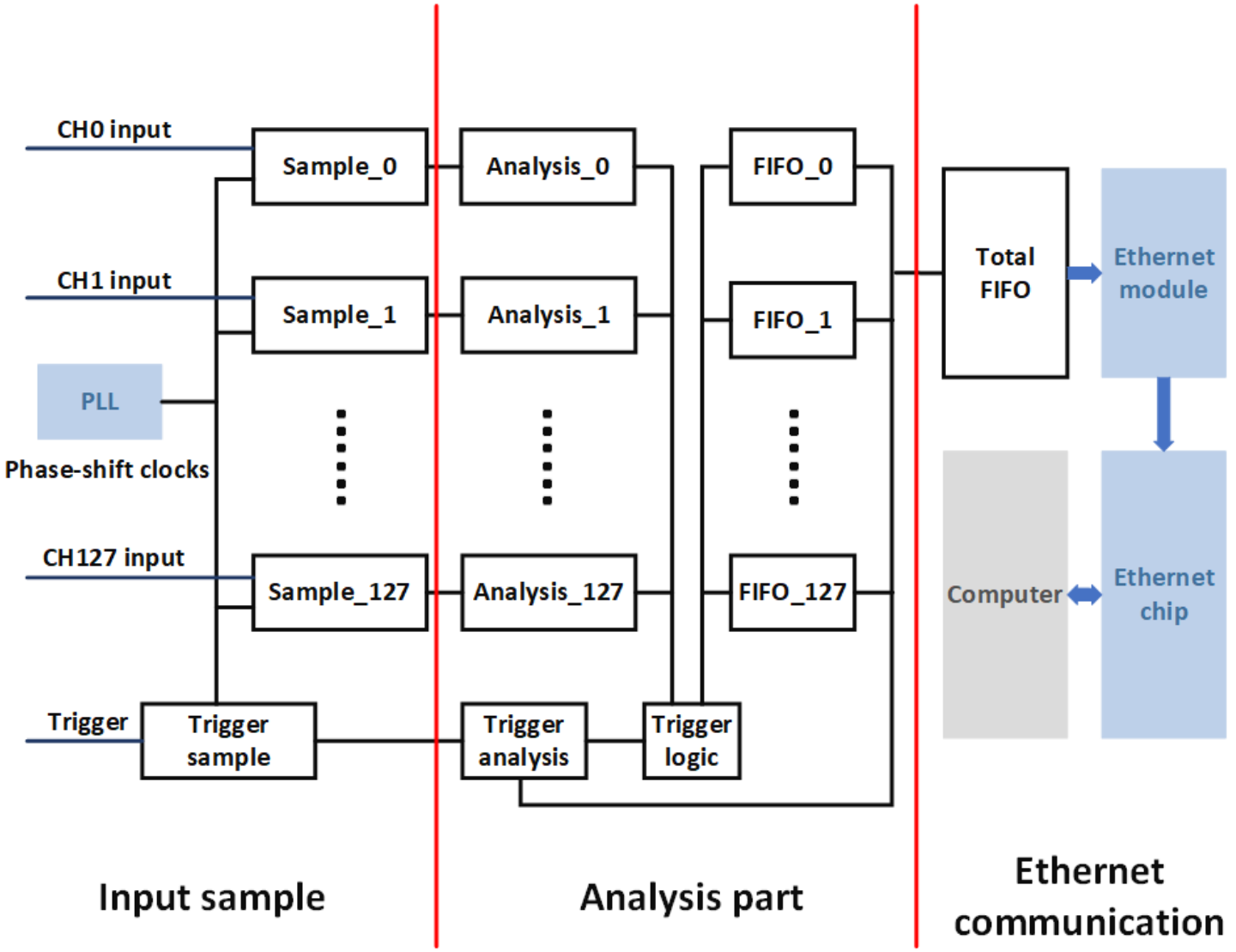
✓Multi-phase clock sampling TDC

✓Kintex-7: XC7K325T

Indicators	Requirements	Multi-phase clock sampling TDC
Channels	128	32~128
Time resolution (ps)	70	60~200
Dead time (ns)	20	Within 3 sampling clocks

TDC principle diagram

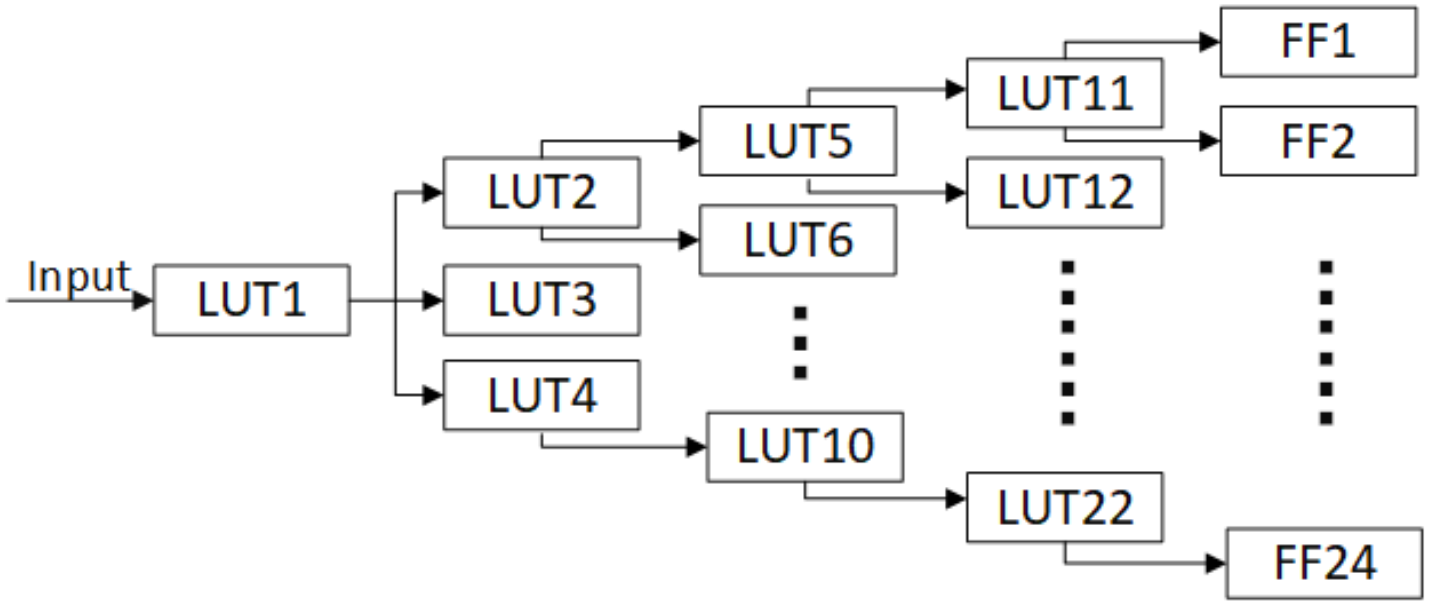
- Input sample part
  - Phase shift sampling clock
  - 24 bit thermometer code
- Analysis part
  - 24 bit → 5 bit fine count
  - Analyze edges
  - Store data based on trigger logic
- Ethernet communication part
  - Transfer the data to the total FIFO
  - Gigabit Ethernet



Input sampling module

❖Constrain routes

- delay of signal to FF
- delay of sampling clock to FF
- 22 LUT, 24FF



❖Clock design

Device	Setup	Clock
• Highest VCO frequency: $1.44\ GHz$ • External crystal oscillator: $200\ MHz$	• 2 MMCM • 12 phase-shift clocks • Phase shift 15° • $450\ MHz$ • Half of 24 FF in rising edge, other in falling edge	• 24 fine bins • Bin width: $92.59\ ps$ • Coarse counter clock: $450\ MHz$

PCB design

❖Parts

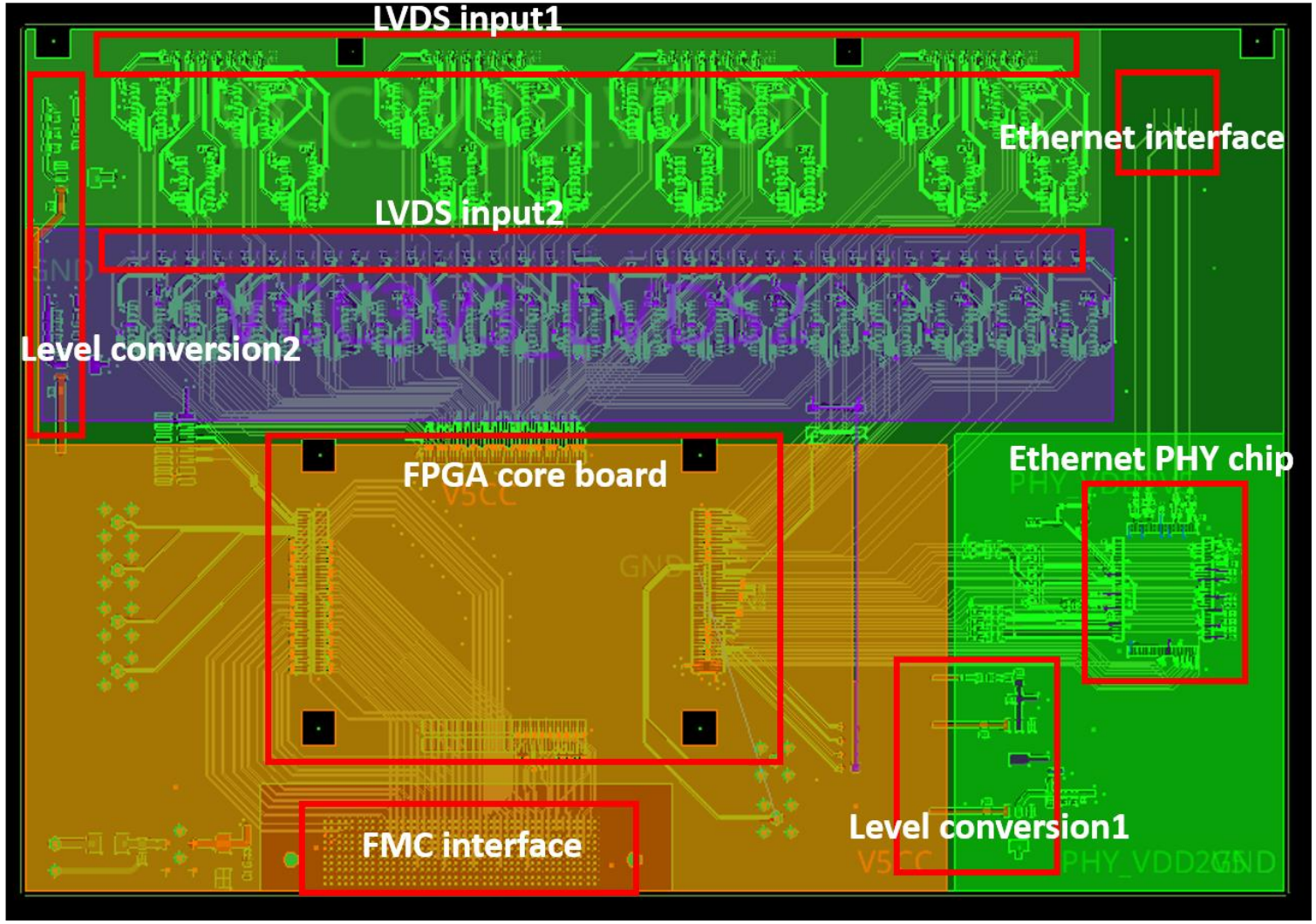
- Two LVDS input
- Ethernet PHY chip
- FPGA core board using kintex-7
- FMC interface
- Level conversion
- LVDS32B、88E1111

❖Working condition

- Voltage: 5 V
- Current: 1.8 A~1.9 A
- Power dissipation: 70 mW/ch

❖Board size

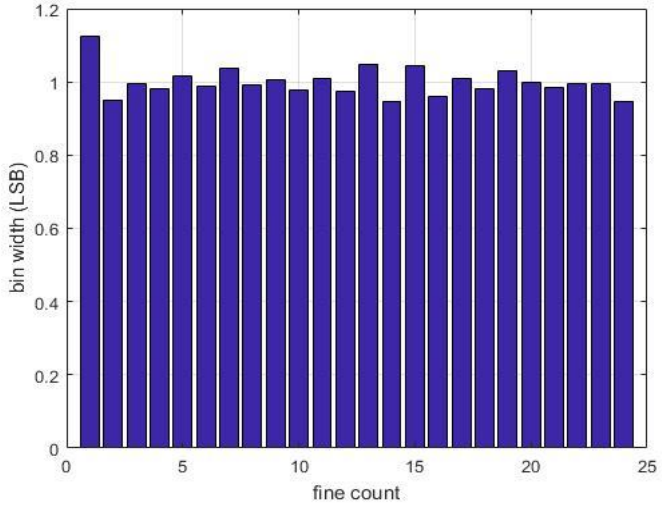
- $233mm \times 160mm \times 20mm$

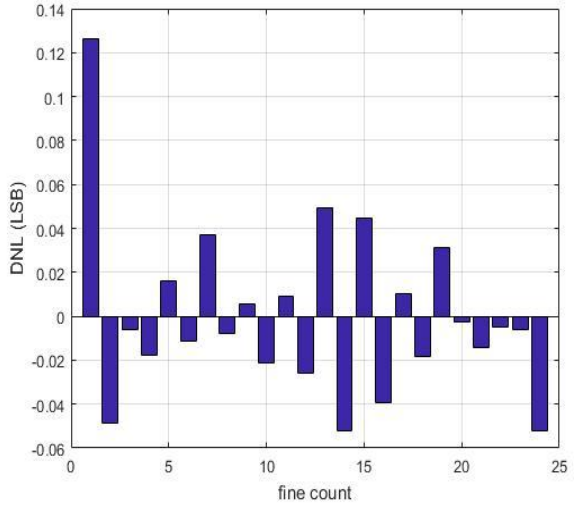


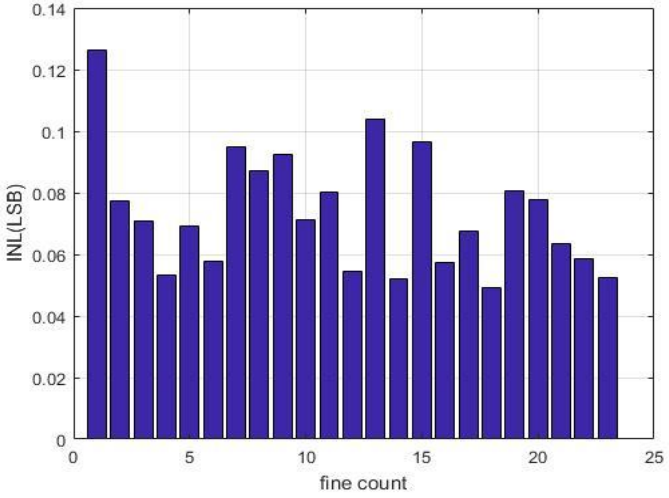
Performance with the signal generator: nonlinearity

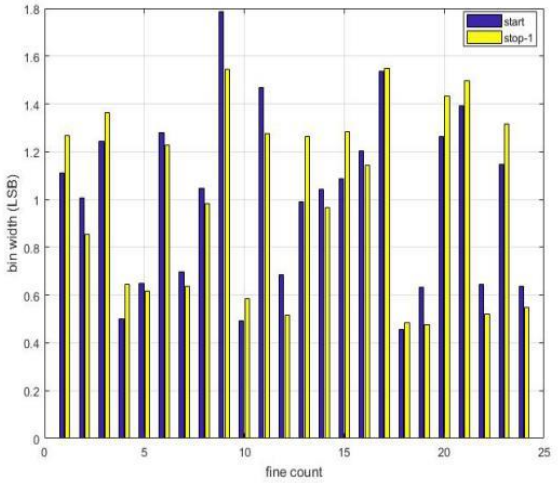
- Test setup
  - Dominated by fine counters
  - Two pulse signals as trigger and stop
  - Periods not correlated: 10μs and 23.14μs
  - Average distribution
- Test result
  - Bin width: $0.9477 \sim 1.1262\ LSB$
  - $DNL_{max} = INLmax = 0.1262\ LSB$
  - Deviation: within $18.59ps$
- Conclusion
  - Secondary contribution to σ
  - Convenient method: offline modification

$$\sigma = \sqrt{\frac{LSB^2}{12} + \sigma_{time}^2 + {\sigma_C}^2 + \frac{{\sigma_L}^2}{4}}$$









Performance: time resolution

Test setup

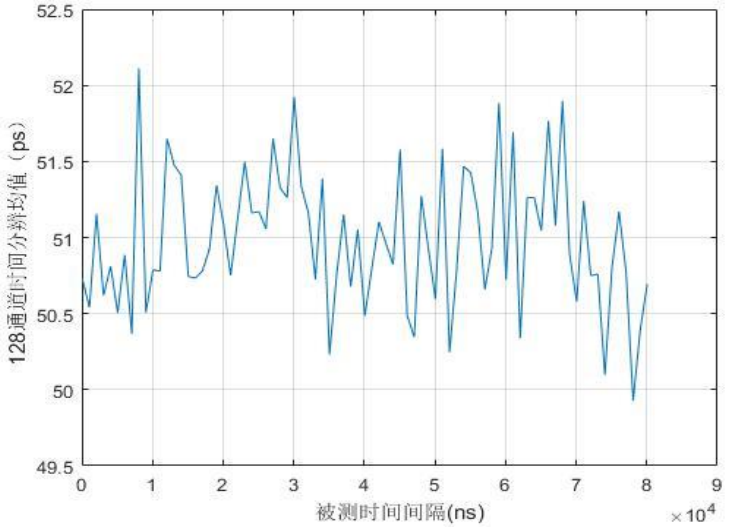
- Two pulse signals as trigger and stop
- Delay: $70ns \sim 7870ns$ at a step of $100\ ns$
- Standard deviation is the time resolution

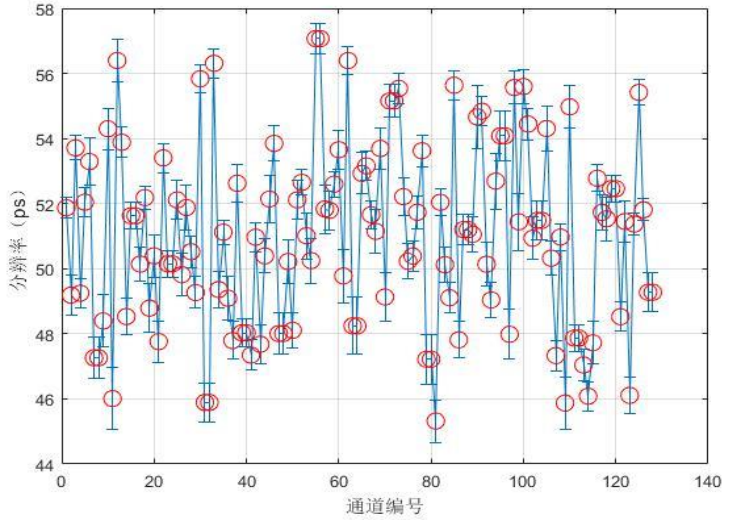
Test results

- Without periodicity
- Dual-channel σ_1: $45.3 \sim 57.1ps$,
- Single-channel $\sigma_2 = \frac{\sigma_1}{\sqrt{2}}$: $32 \sim 40.4\ ps$

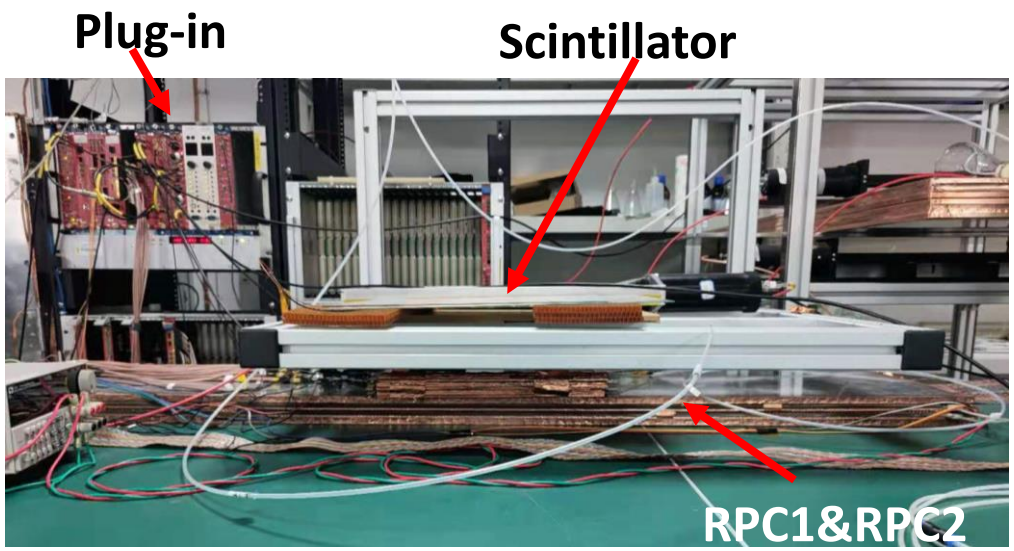
Conclusion

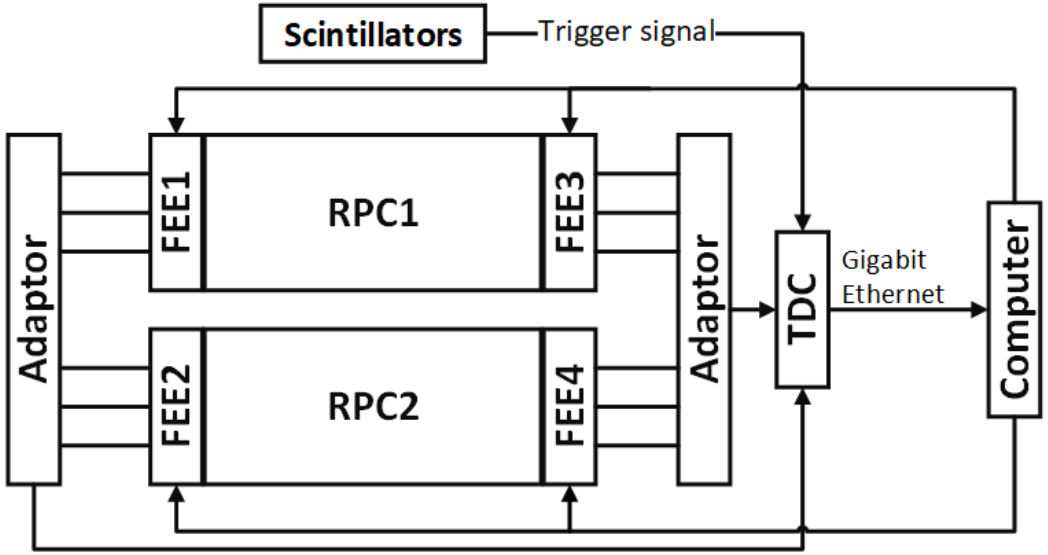
- Time resolution < $70\ ps$



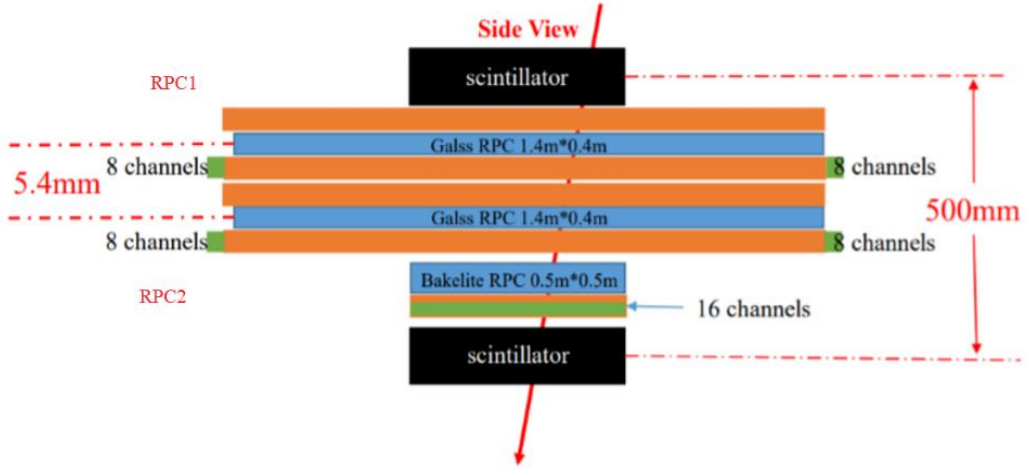


Performance in a real RPC detector: setup

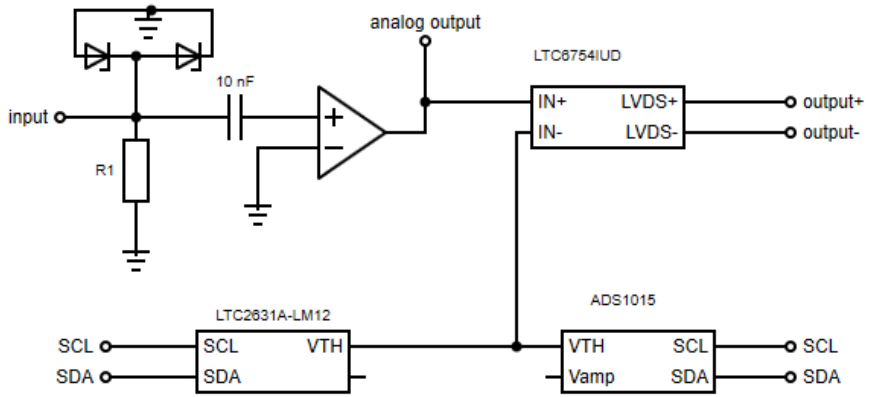




Double-end readout system structure



The structure of the cosmic ray test platform



The front end electrical (FEE) boards

Dark count

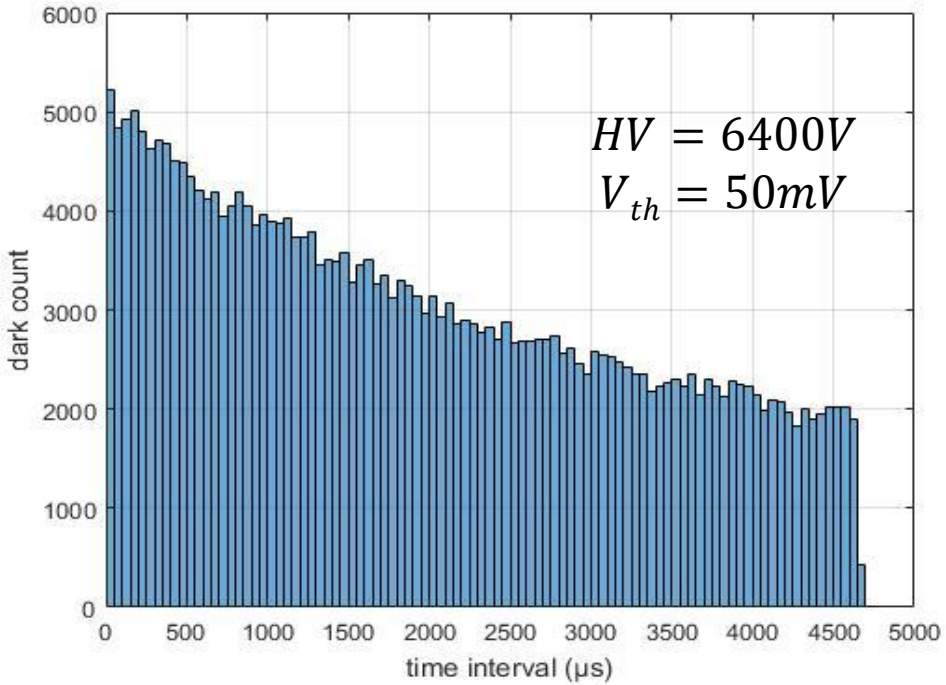
❖Test method

- Random trigger
- Time interval between dark count signal and trigger signal
- Average period of dark event: time constant of statistical distribution

❖Result

V_{th}(mV)	10	20	25	30	35	40	45	50
Rate (Hz/m²)	1.5×10^6	74194	32848	1858	1529	1465	1024	402

- Dark count rate related with V_{th}
- Testing time interval by using TDC also can get the data of dark count rate



Efficiency curve

Test method

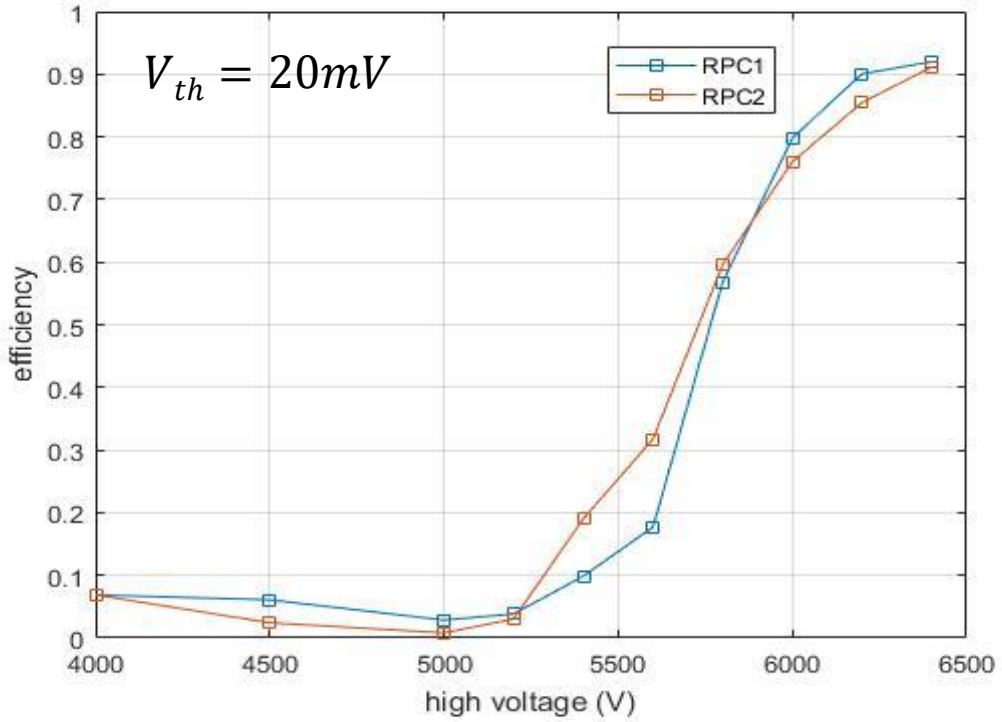
- External trigger mode
- Basic principle of conditional probability:

$$\begin{cases} p_1 = \dfrac{G_t \cap G_1 \cap G_2}{G_t \cap G_2} \\ p_2 = \dfrac{G_t \cap G_1 \cap G_2}{G_t \cap G_1} \end{cases}$$

- G_t: probability of trigger has output
- G_1: probability of RPC_1 has output
- G_2: probability of RPC_2 has output

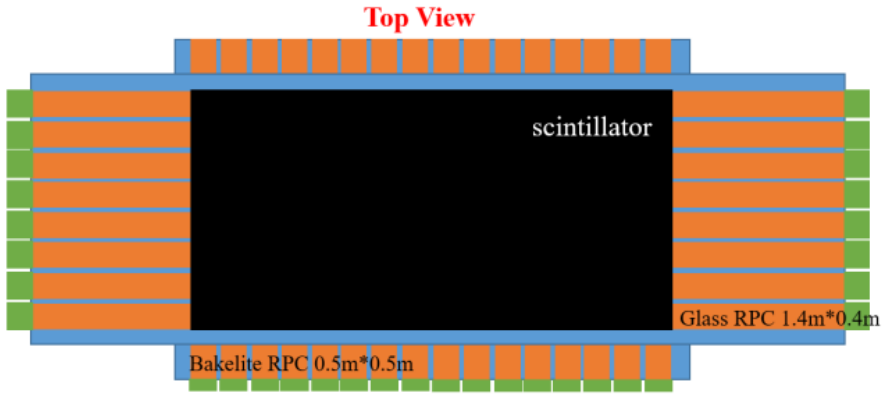
Result

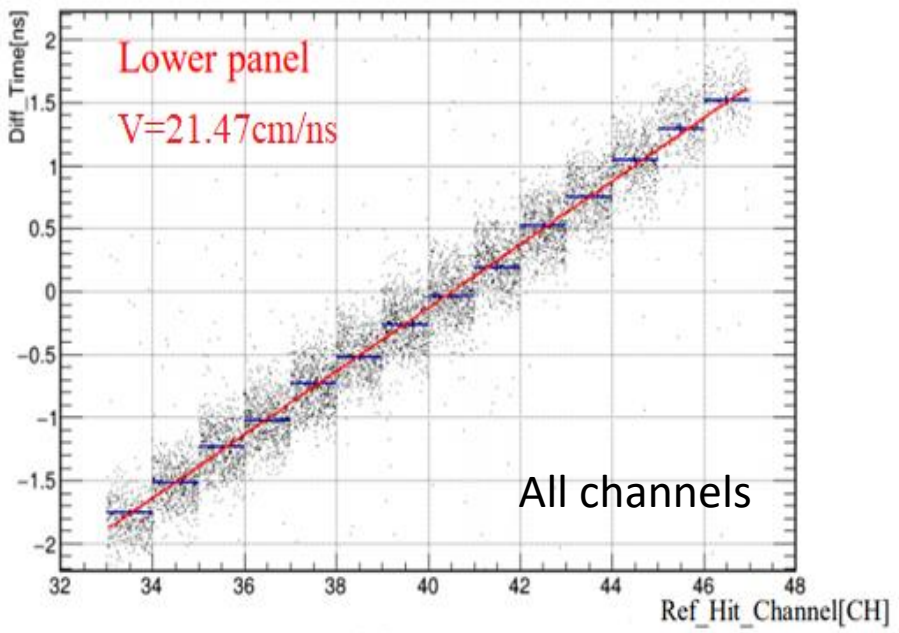
- $p1 = 93.2\%$ $p2 = 95.3\%$
- There are many factors that affect efficiency
- The results only prove that TDC works normally

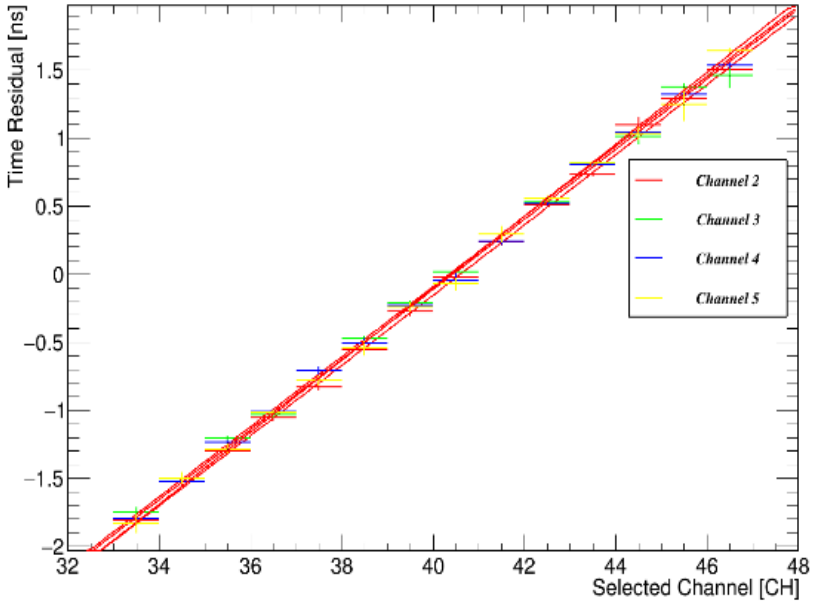


Calculate transmission speed

- Bakelite RPC with traditional readout method read signals from vertical strips
- Glass RPC with double-ends method read signal from horizontal strips
- Correlation between reconstructed hit position of the 2 gaps could be used for transmission speed calculation







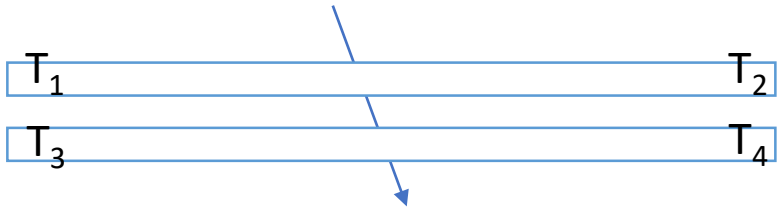
Spatial resolution

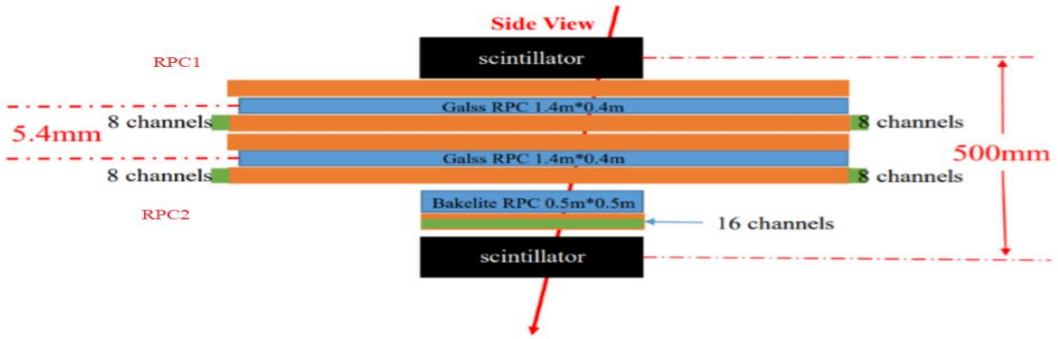
❖Test method

- Distance between RPC_1 and RPC_2 small enough
- Hit position should be in same location
- Time difference between them follows normal distribution

$$\Delta t = \frac{T3 - T4}{2} - \frac{T1 - T2}{2}$$

$$\sigma_T = \sigma_{\Delta T}$$

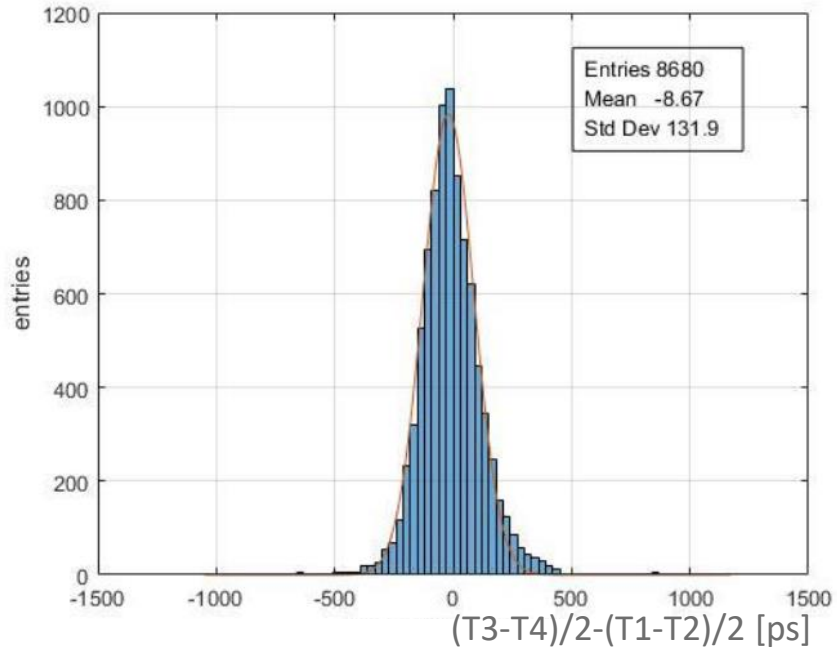




The structure of the cosmic ray test platform

❖Result

- Standard deviation: $131.9ps$
- $p = \frac{v}{2}(T_1 - T_2),\ \sigma_p = \frac{v}{2}\sqrt{\sigma_{T_1}^2 + \sigma_{T_2}^2} = \frac{v}{\sqrt{2}}\sigma_T$
- $\sigma_{space} = \frac{131.9 \times 21.47}{1000\sqrt{2}} \approx 2.00\text{cm}$



Summary

❖Index comparison:

✓Satisfy the requirement of ATLAS Phase II Upgrade

Design goals	Test result
• 128 channels	• 128 channels
• Time resolution < 70 ps	• Time resolution $28.1 \sim 52.3$ ps
• Power dissipation $< 100\ mW$	• Power dissipation $70\ mW$
• Spatial resolution $< 2cm$	• Spatial resolution $\sim 2cm$

❖Further work is ongoing

- Improve nonlinearity and time resolution
- Work with multiple TDC modules

Backup: dead time

- Test method
  - Two square wave
  - 10000 events
- Result
  - $f = 120MHz$, $\mathrm{d}ead\ time < 8.333ns$
- Conclusion
  - Dead time $< 20\ ns$

$f\ (MHz)$	10	20	40	60	80	100	120
interval(μs)	1000	500	250	166.67	125	100	83.333
deviation(ns)	0.89	0.46	0.22	0.15	0.1	0.1	0