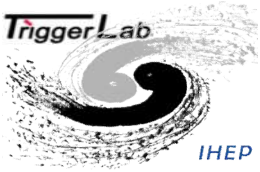

Firmware development of iRPC backend/trigger system

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TriggerLab/ IHEP Beijing

The 7th China LHC Physics Workshop

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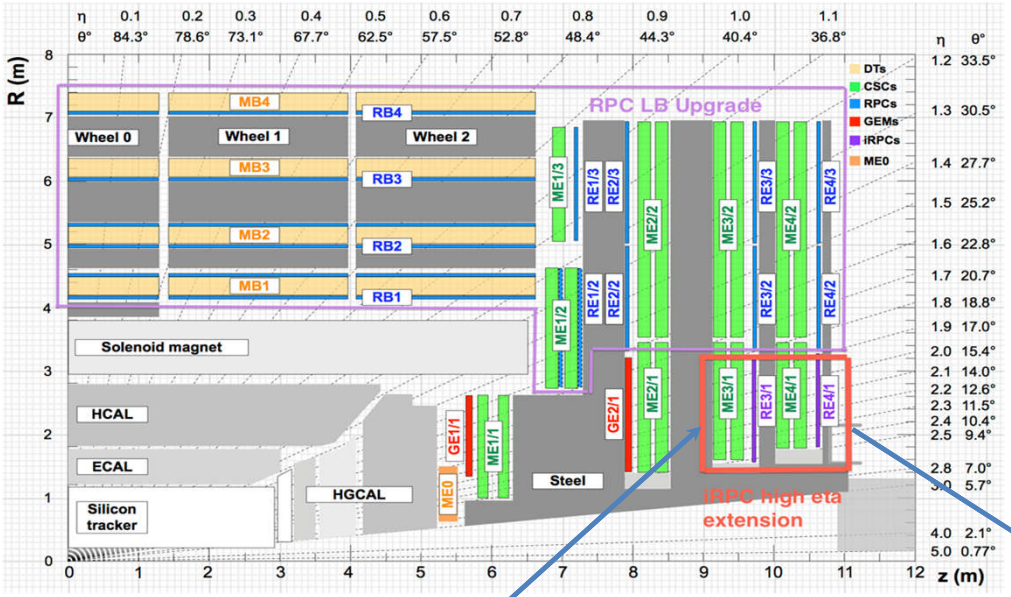
Outline

- Background
- Backend/Trigger System
- Firmware Development
- Functional Verification
- Summary

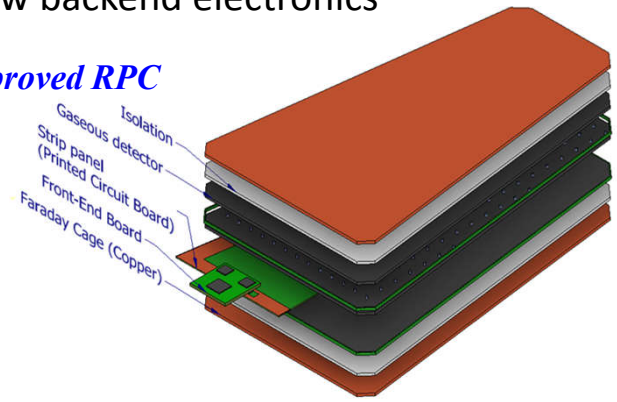
Background of iRPC



- **Main motivations/goals**:
  - Increase rate capability (2 KHz/cm^2)
  - Sufficient time resolution for background rejection
  - Sufficient space resolution for tracking
  - Improve contribution of RPCs to muon triggering in the forward region
- **Electronics:**
  - Two ends readout
  - GBT based transmission
  - New backend electronics

Extend the RPC coverage up to | η | = 2.4 to increase redundancy in high eta region in stations 3 and 4

RE 3.1 and RE 4.1 Improved RPC

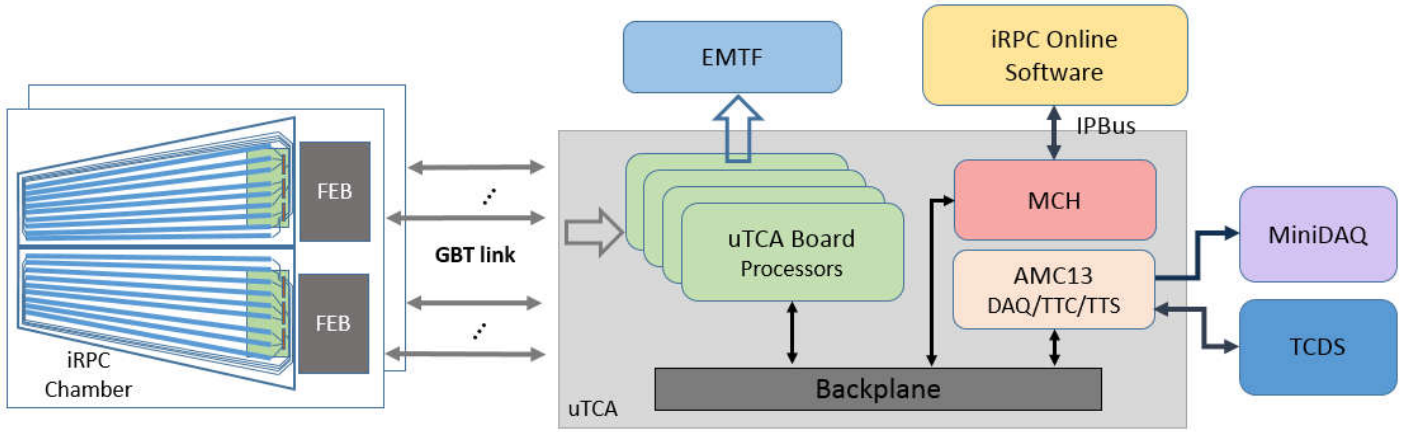


1 chamber ≈ **1.6 x 1.2 m^2 trapezoidal shape**

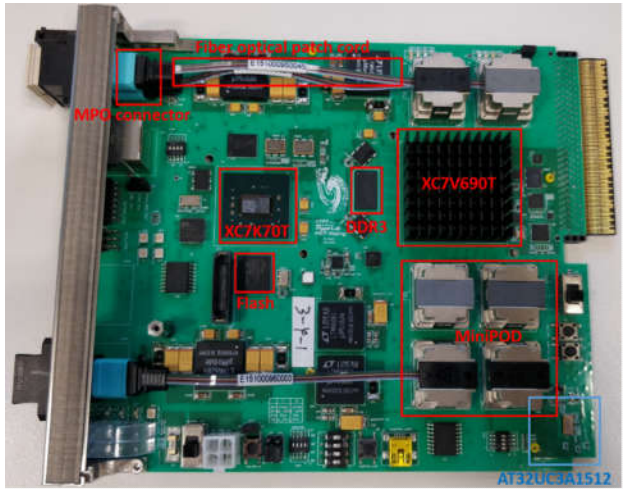
20° in φ ⟹ 18 chambers/disk ⟹ Total of 72 iRPC chambers

Backend/Trigger System

- BE prototype system：
  - µTCA compliant BEB
    - core board
  - a µTCA crate,
  - an AMC13 card,
    - system clock and fast control
  - a µTCA Carrier Hub(MCH),
    - manage the whole system
  - a sever PC.
    - slow control and DAQ

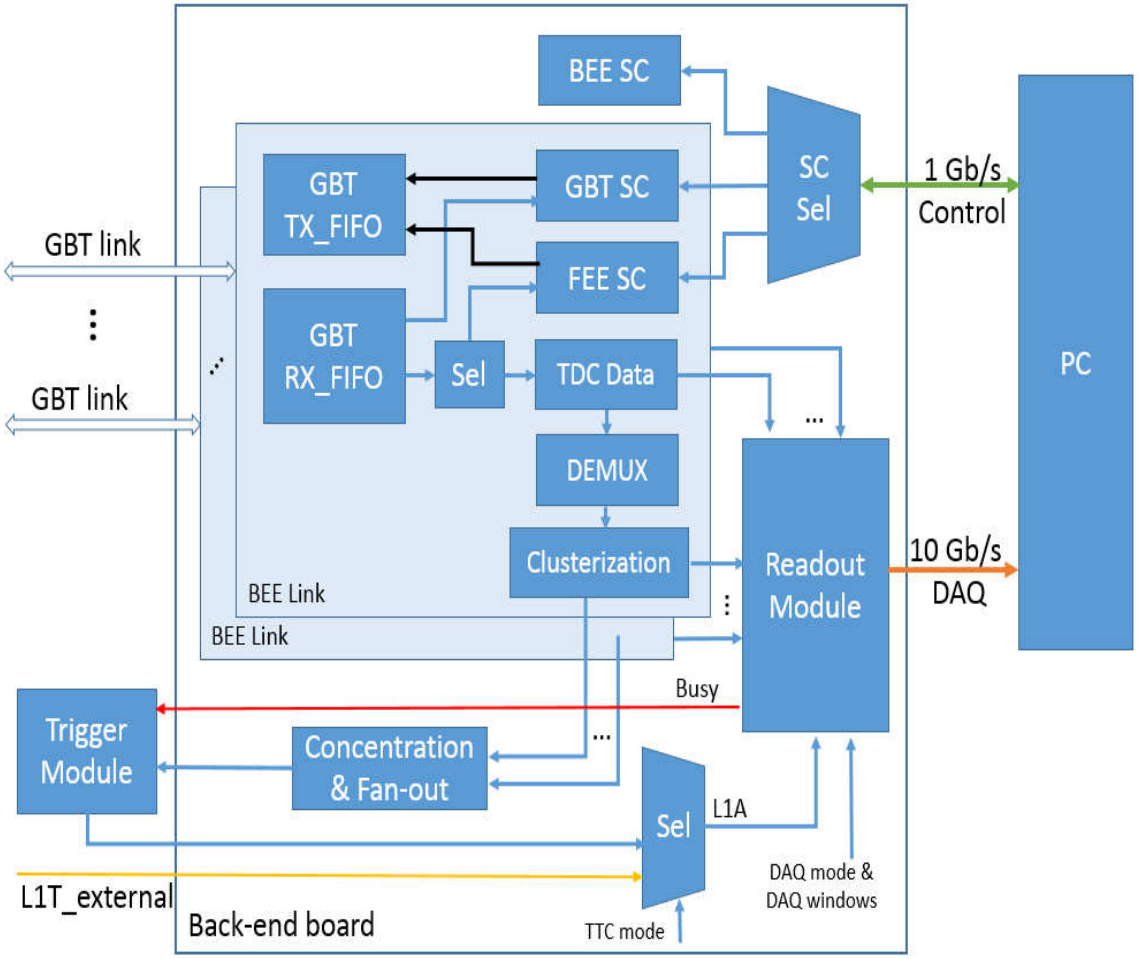


- Key hardware components
  - Virtex-7 FPGA： Core FPGA, to realize GBT link transmission and data processing;
  - Kintex-7 FPGA： Control FPGA, clock configuration



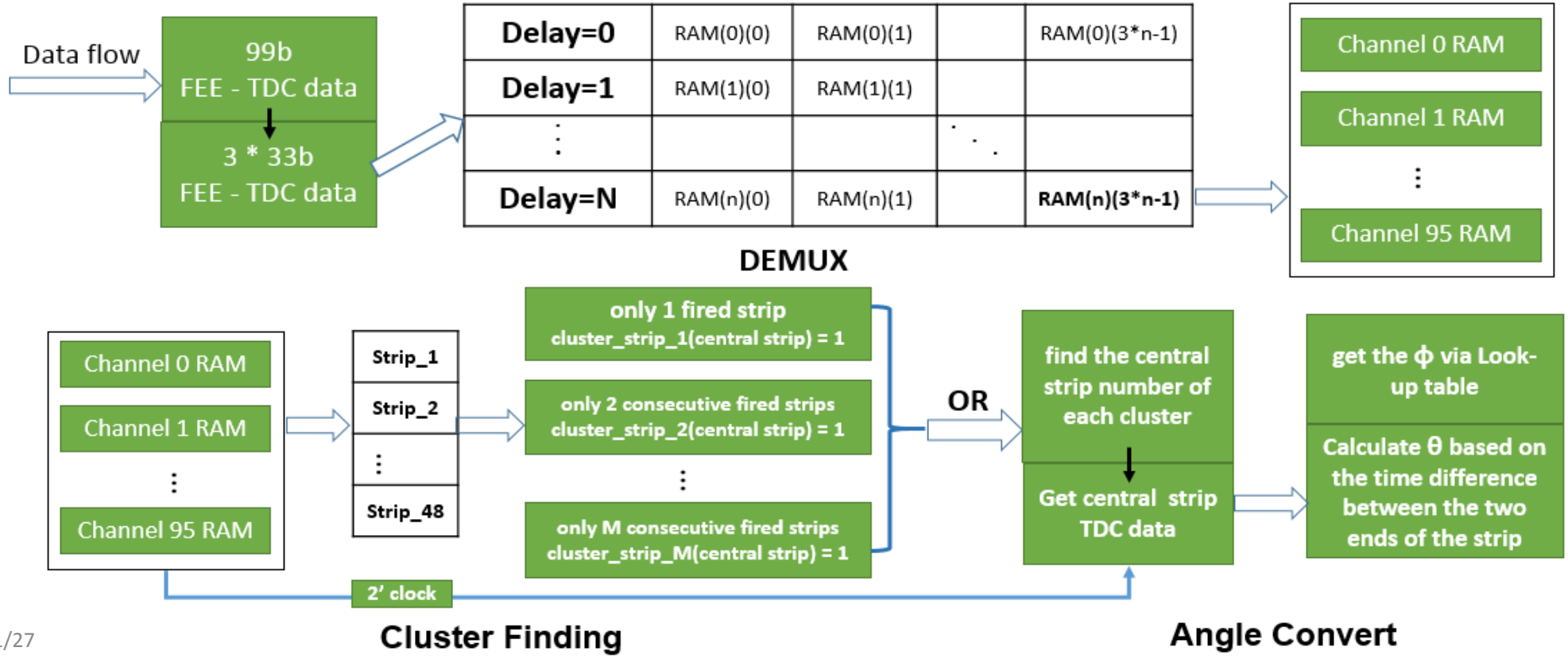
Firmware Development

- Functions：
  - Interactive link between FE and BE
    - GBT link(Bidirectional, 4.8Gb/s), iRPC data protocol
  - Fast control
    - FE interface, system protocol
  - Slow control
    - SiTCP(1Gb/s), GBT SCA, BEE SC, FEE SC
  - Trigger primitive
    - DEMUX, Cluster finding, Angle conversion
  - Data acquisition
    - Based on data storage architecture, Multi-channel input integration;
    - TCP/IP(10Gb/s), Offline analysis



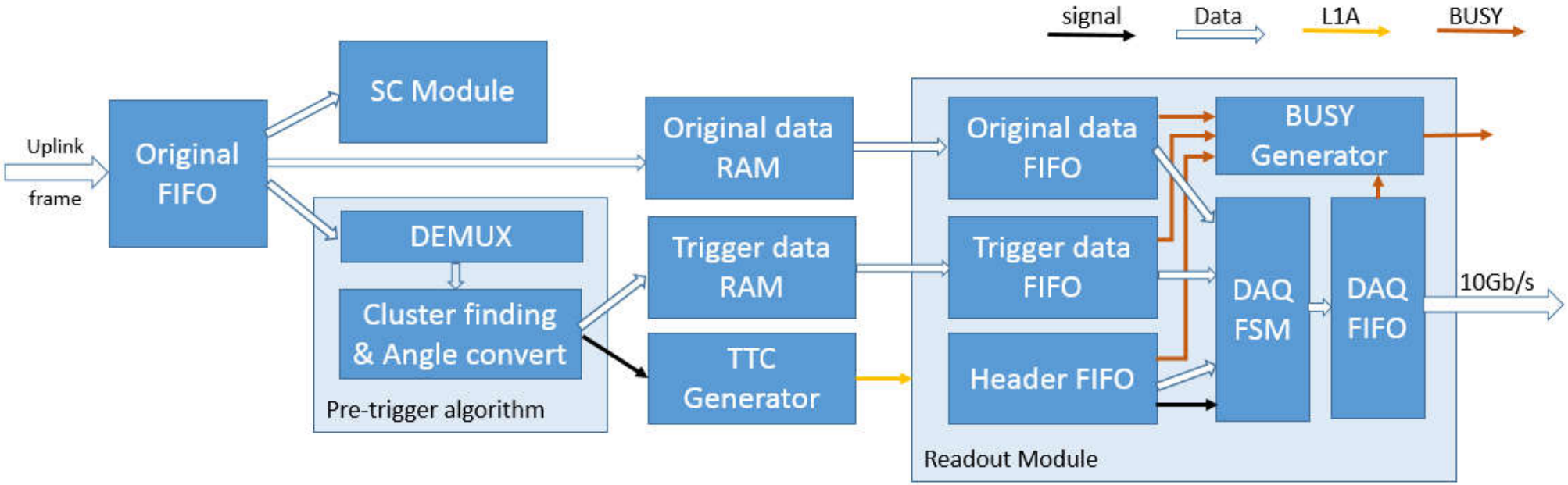
Firmware Development - trigger primitive

- Purpose :
  - Prevent the receiver buffer from overflowing; Recover the time relationship of the detector data; Get the hit position of the particle.
- Key point:
  - Pipeline, DEMUX algorithm, Cluster finding, Angle conversion.



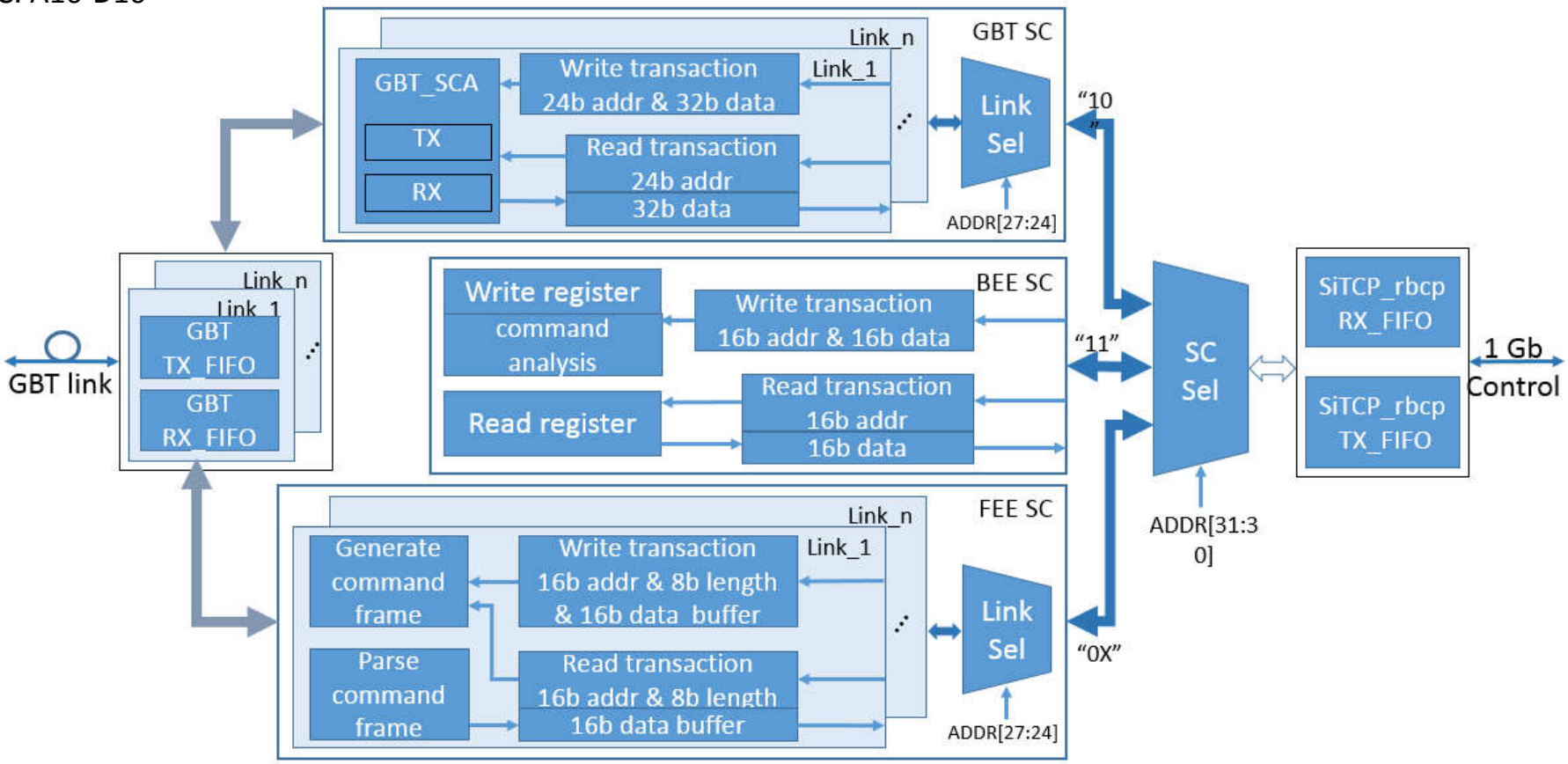
Firmware Development - Data acquisition

- Key point:
  - Search-Match algorithm: find out the data corresponding to the trigger signal.
  - Packing mechanism: all input links are packed, conforming to the data format.
  - Busy mechanism: prevent event loss caused by buffer overflow.



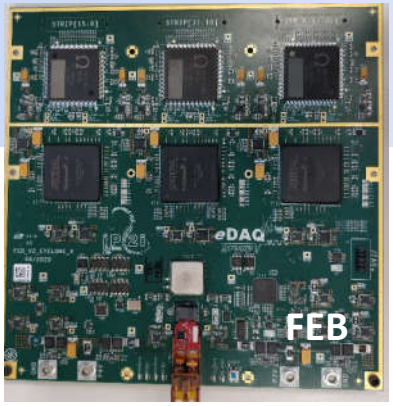
Firmware Development - slow control

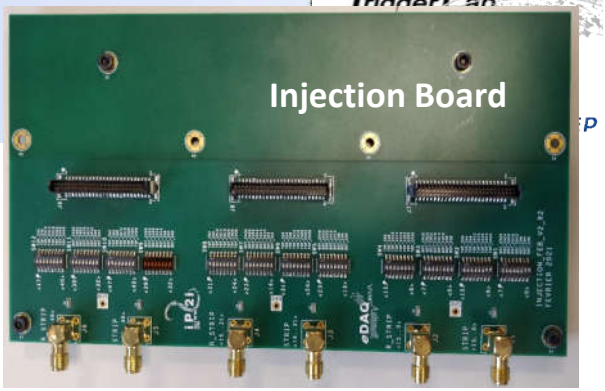
- Key point:
  - Realize the conversion of multiple slow control protocols.
  - Sitcp: 32-bit address and 8-bit data(A32-D8); FEE SC: 16-bit address and multiple 16-bit data(A16-D16*N); GBT SC: A24-D32; BEE_SC: A16-D16



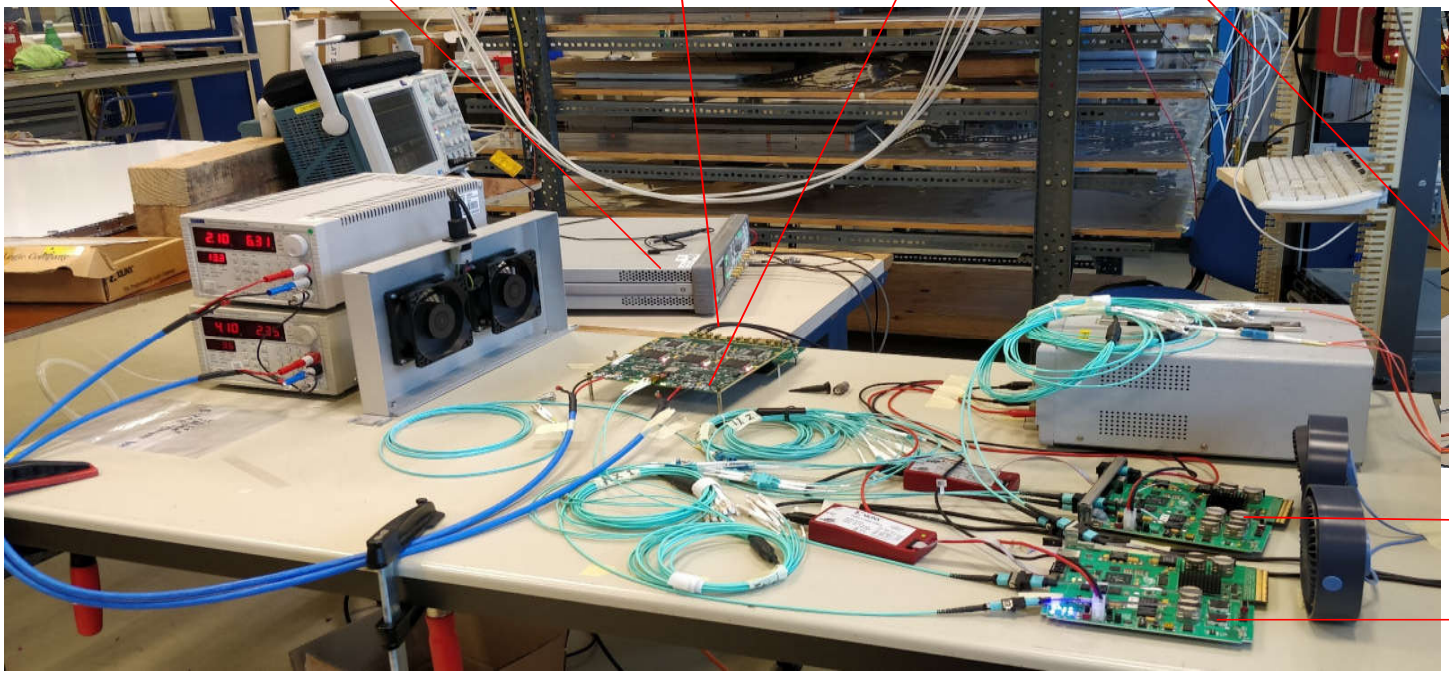
Functional Verification

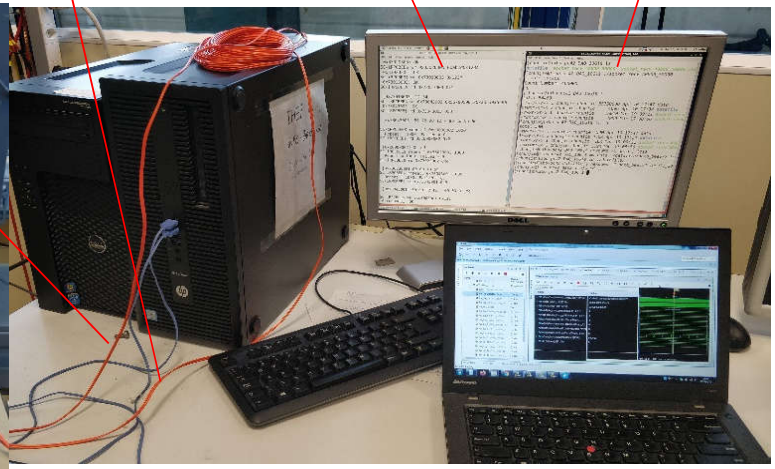
- Set up a joint test system between FEB and BEB
- Develop FEE emulator for cross-check





Signal Generator | Injection Board | FEB | 1Gb-link,SC | 10Gb-link,DAQ | SC Software | DAQ Software





FE-emulator

BEB

Functional Verification

Results list of FEE emulator – BEB joint test

- Check GBT link establish status √
- GBT link Long time stability test(> 1 week) √
- Bit Error Rate test for data transmission(< 2E-18) √
- Slow control protocol test of GBT SCA chip √
- FEE custom slow control protocol test √
  - Single Frame/ Burst/ Broadcast
- Slow control repeatability test (>10,000 times) √
- BE data process algorithm check √
  - DEMUX/Cluster Finding/Angle conversion
  - Data Acquisition/Offline Analysis

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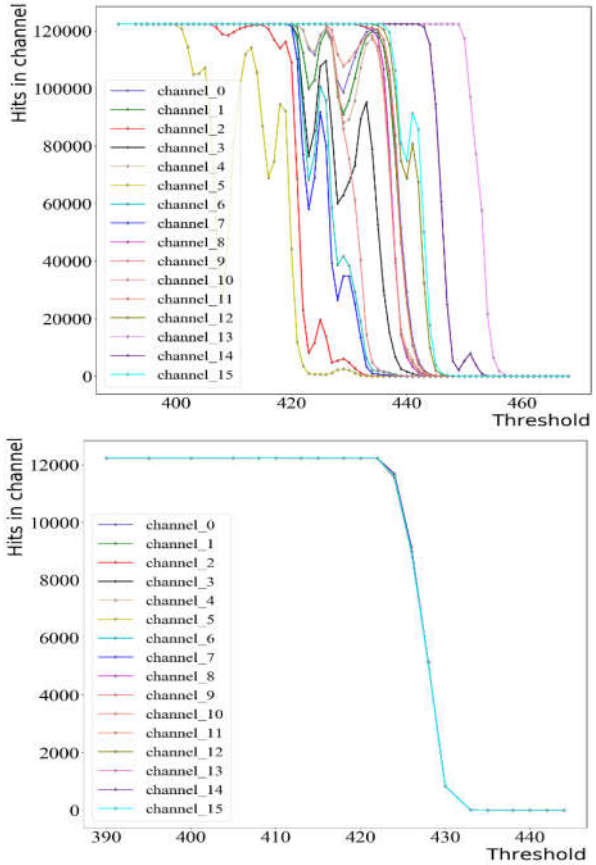
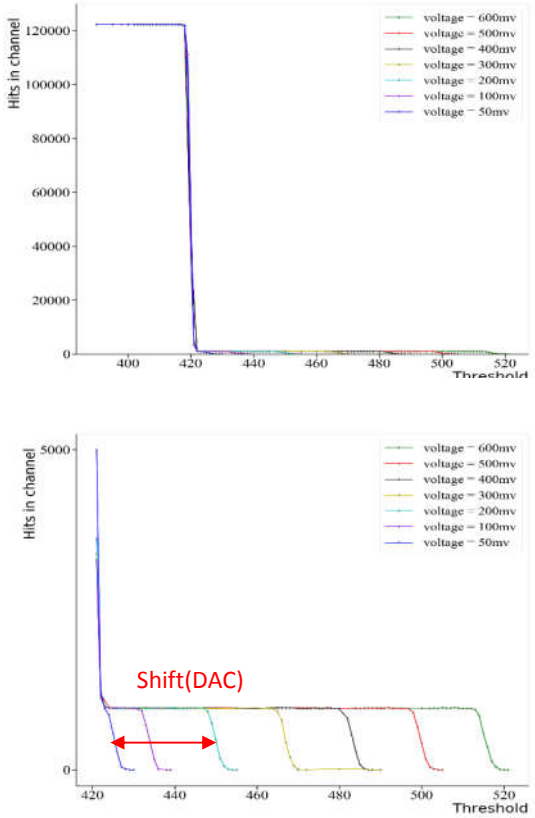
  - Single Frame/ Burst/ Broadcast
- Slow control repeatability test (>10,000 times) √
- TDC configuration of FEB √
- PETIROC configuration of FEB √
- PETIROC calibration of FEB √
- General functional test of FEB √
- Data transmission mechanism between FE and BE √
- BE data process algorithm check √
  - DEMUX(√)/Cluster Finding/Angle conversion
  - Data Acquisition/Offline Analysis √

Functional Verification - slow control

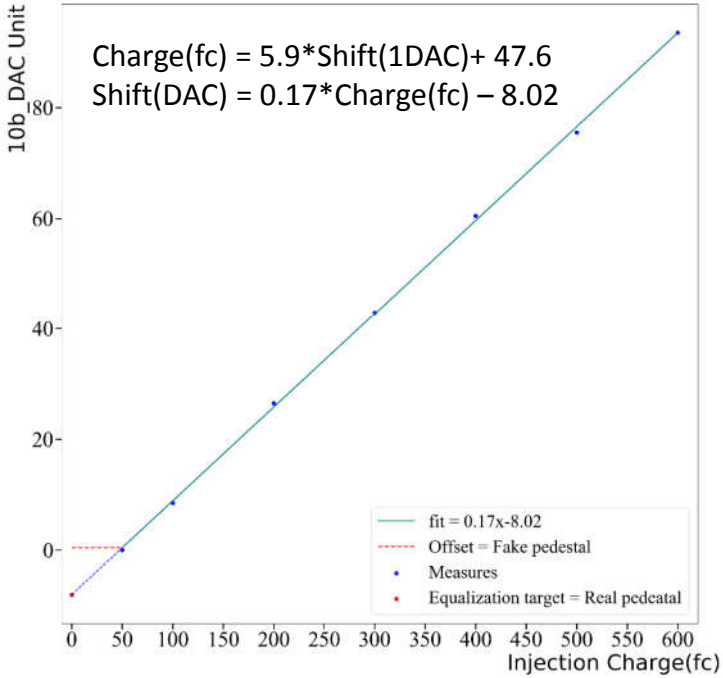
- Set Petiroc adjustment parameters channel by channel through slow control so that all Petiroc channels are aligned.
- By injecting different charges into Petiroc, the conversion relationship between the value set by the threshold(DAC) and the charge is obtained.



Align all channels of Petiroc



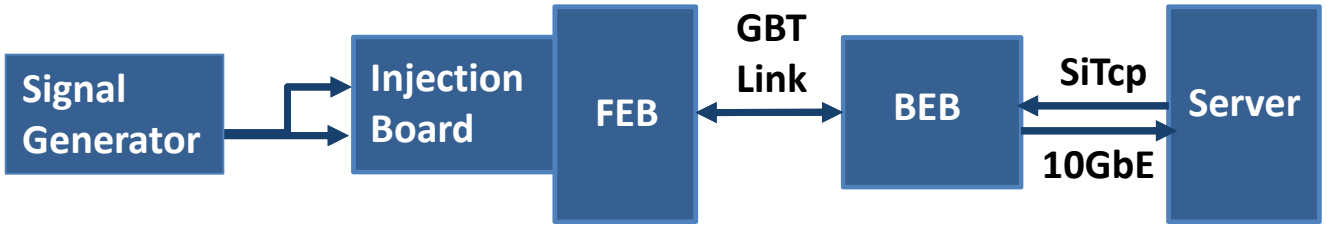
Inject different charges for SCurves



the conversion relationship between the DAC and the charge

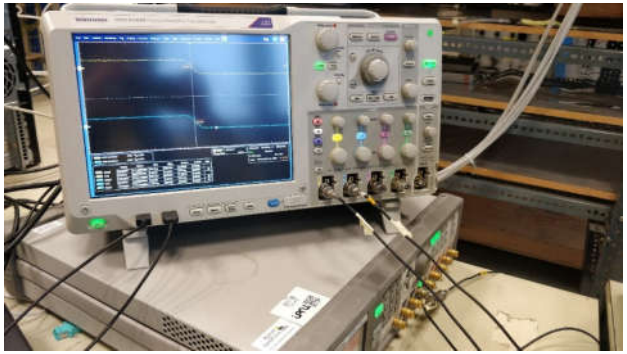
Functional Verification - data processing

- **Set up**: Use a splitter to fan out one output of the signal generator into two outputs. Ensure that all channels of Petiroc are aligned. The setting of Petiroc threshold can completely reject noise..
- **Test result**: The sigma of time difference is **36ps**. (The Jitter of TDC is 20ps, the Jitter of petiroc is 10ps, σ(X-Y) = 32ps). **Conclusion**: Verify that the entire test system is working properly.

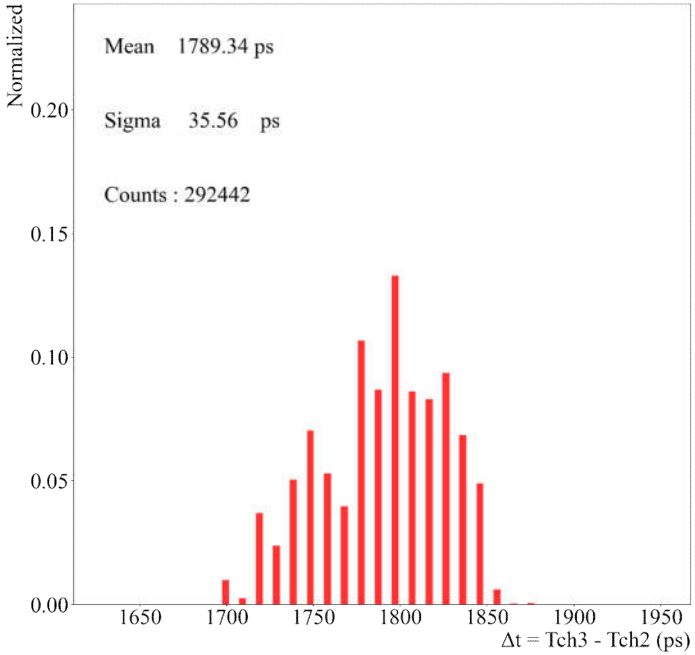


Test principle block diagram

FEB Injection signal



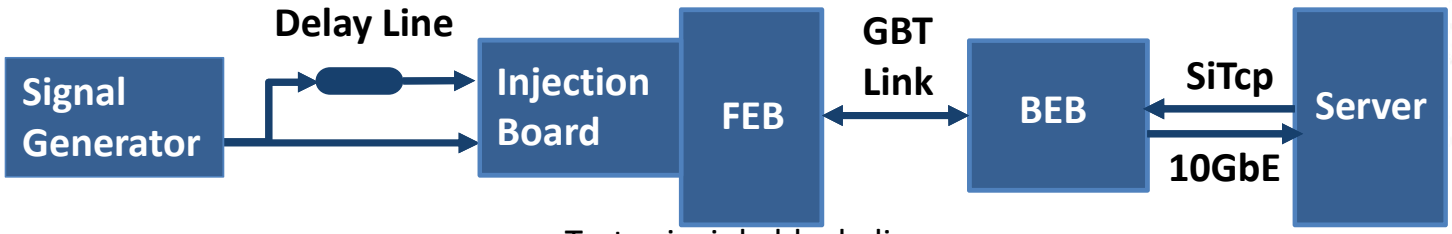
Oscilloscope confirms the output of the signal generator



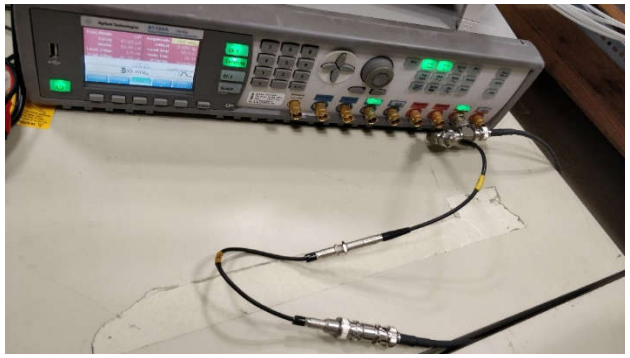
Distribution of time difference between test channel and trigger channel

Functional Verification - data processing

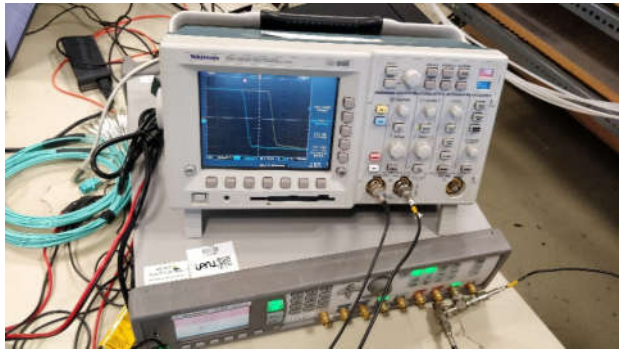
- **Test Methods**: Analyze the change regularity of the time difference between the test channel and the trigger channel by changing delay line.
- **Test results**: As the delay value of the test channel increases, the time difference between the test channel and the trigger channel increases linearly. The maximum deviation is **0.24ns** and the nonlinearity is **3‰**.
- **Conclusion**: Fully verified the backend function.



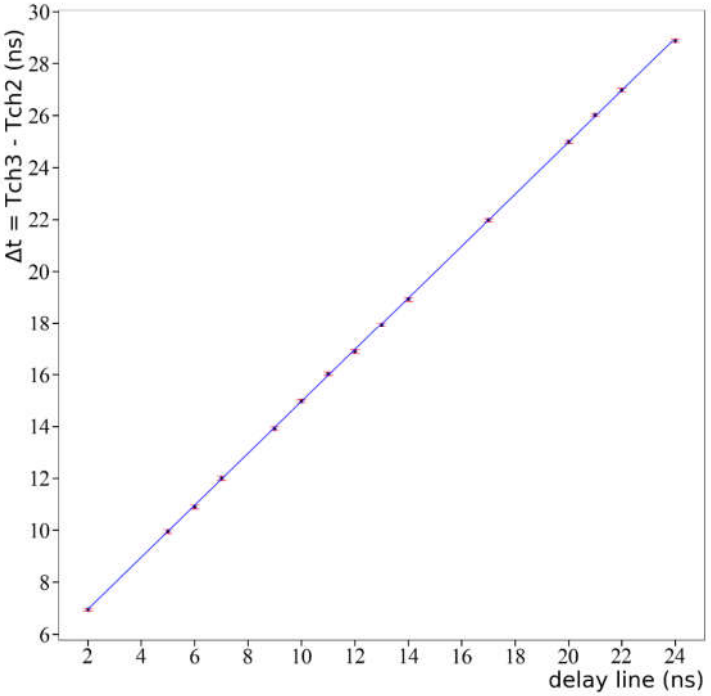
Test principle block diagram



Use delay line



Oscilloscope confirms the delay value



Time difference by measured VS delay line value

Summary

- Basic functional test of communication between FEB V2 and BEB was done and got a successful result.
- Part of the developed Backend/trigger functions and algorithms(slow control/DAQ) have been fully verified.
- The verification of the pre-trigger algorithm is in progress.

Thanks for listening!