Status of hardware development for iRPC Backend/Trigger system

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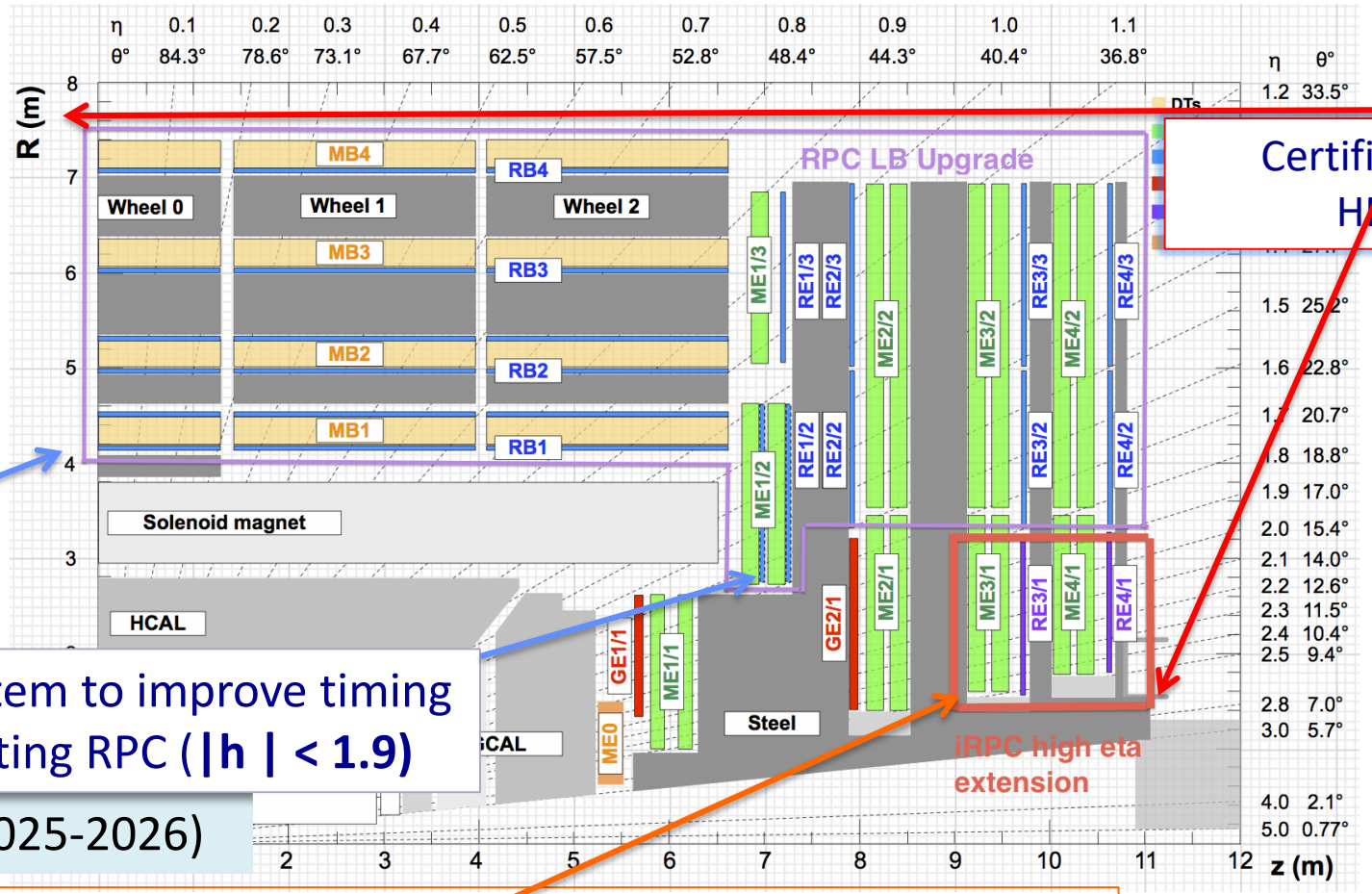
Phase II RPC Upgrade Project Overview

New RE3.1/4.1 (iRPC + FEBs)

New LinkBoard System for present RPC



Certification for HL_LHC

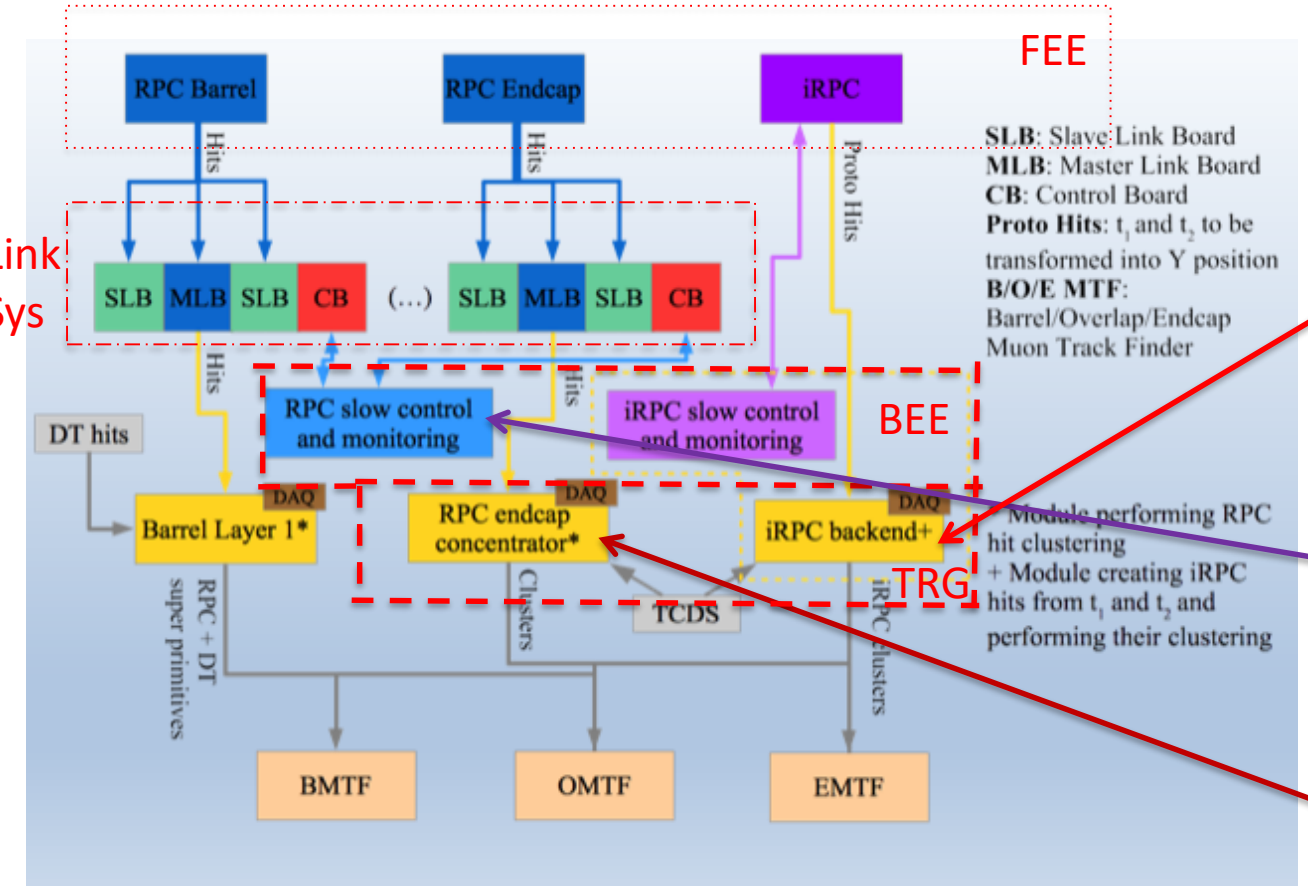
Upgrade of Link System to improve timing resolution for existing RPC (**|h | < 1.9**)

Installation in LS3 (2025-2026)

Extend the RPC coverage up to |η | = 2.4 to increase redundancy in high eta region in stations 3 and 4

Installation in YETS 2022-23 & YETS 2025-26

Tasks for RPC/iRPC TRIG/Backend Electronics



iRPC(RE3/1,RE4/1) Backend/Trigger

- Slow Control
- Monitoring
- Fast Control
- Trigger primitive (Cluster)
- Readout(DAQ)

Exiting RPC Backend(**|η | < 1.9),**Barrel and End cap

- Communication with LBS/CB
- Monitoring
- Slow Control

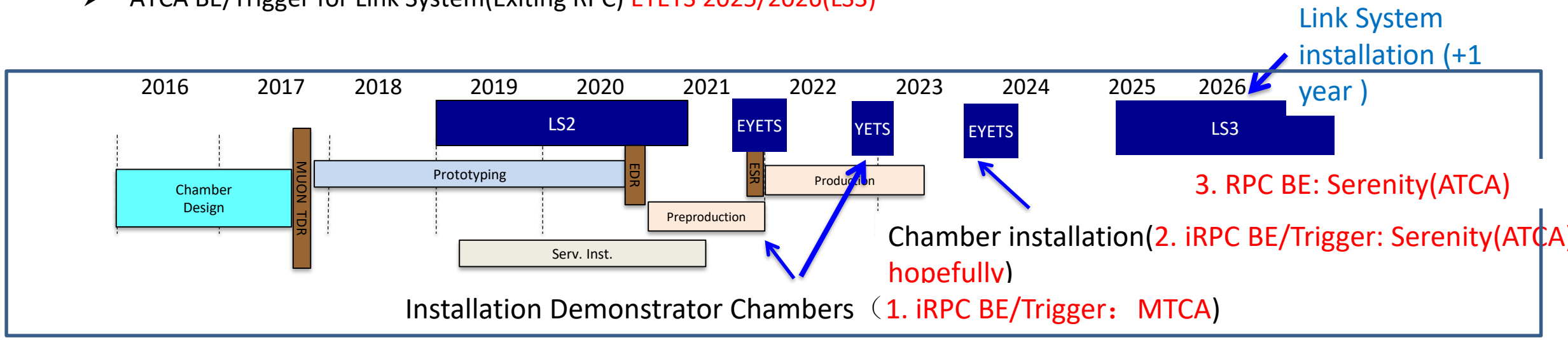
RPC Endcap Concentrator/Trigger

- Concentrator
- Trigger primitive(Cluster)
- Readout(DAQ)

BE/Trigger Roadmap and Schedule agreed in RPC

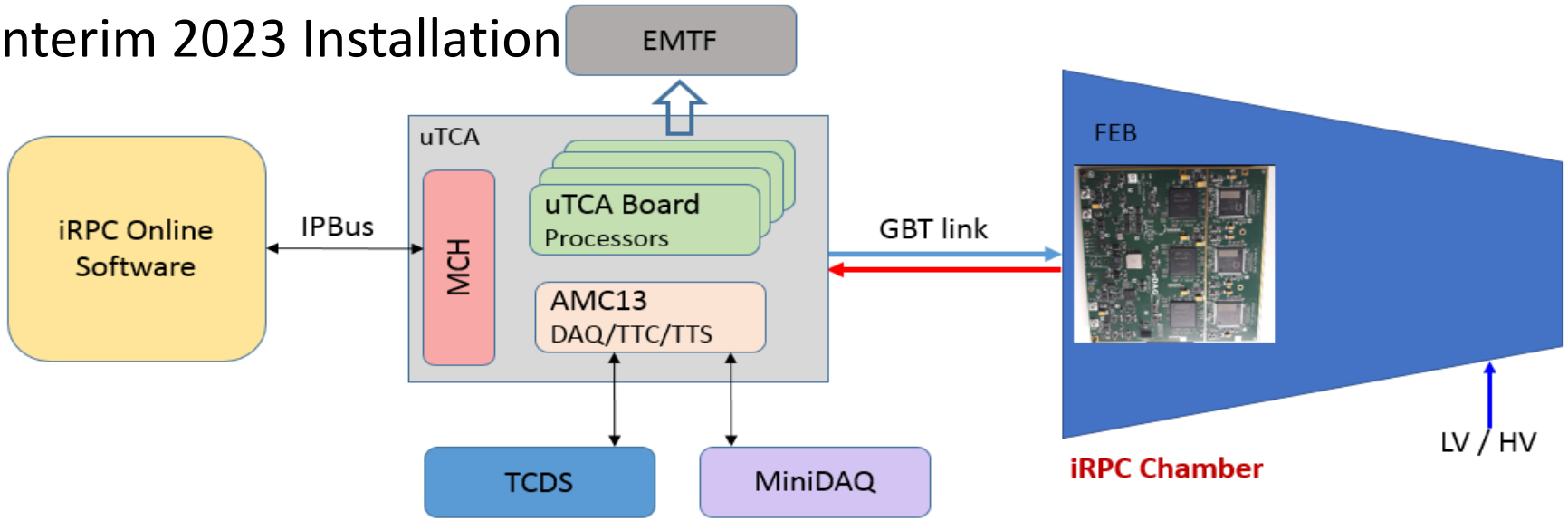
- **BE/Trigger installation Roadmap schedule**
  - ATCA installation late, IHEP propose two-step installation scheme.
- **2 Steps Installation Roadmap: MTCA+ATCA (4 periods)**
  - iRPC MTCA BE/Trigger for Demonstrator EYETS 2021/2022
  - iRPC MTCA BE/Trigger installation EYETS 2023/24
  - iRPC MTCA BE/Trigger merge to ATCA BE/Trigger EYETS 2025/2026
  - ATCA BE/Trigger for Link System(Exiting RPC) EYETS 2025/2026(LS3)

- **Hardware needed**
  - **MTCA Backend Trigger board**
  - **ATCA board**

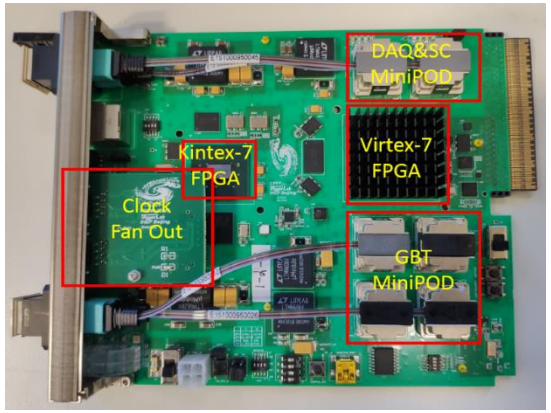


iRPC MTCA Demonstrator System

- For Demonstrator 2022 and Interim 2023 Installation
  - µTCA compliant BE boards
    - core board
  - a µTCA crate,
  - an AMC13 card,
    - system clock and fast control
  - a µTCA Carrier Hub(MCH),
    - manage the whole system
  - a sever PC.
    - slow control and DAQ



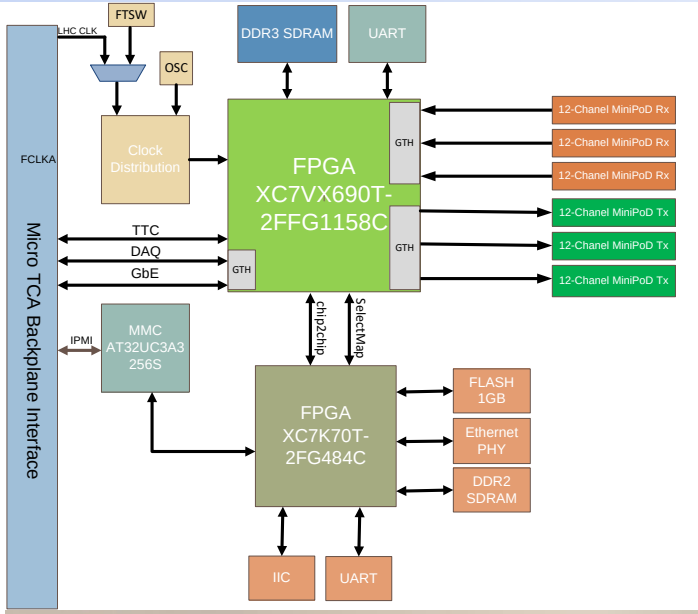
- Key hardware component for backend and trigger
  - Backend electronic and trigger board

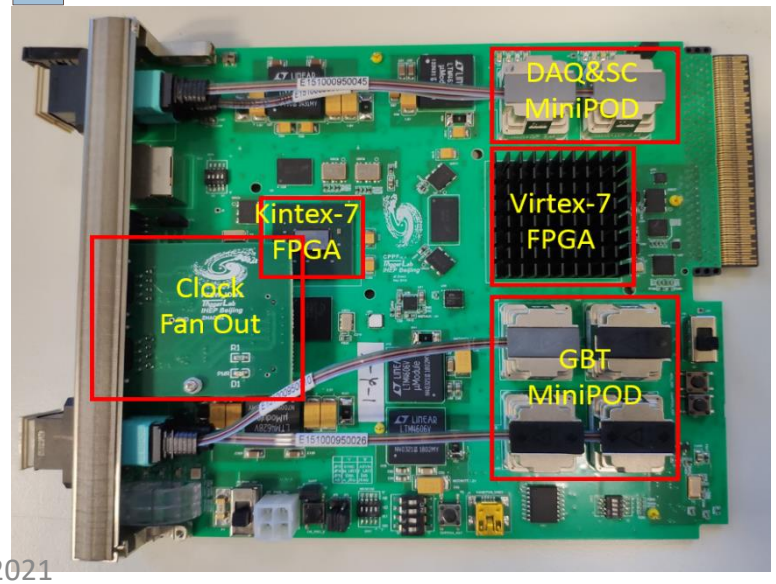


Backend electronic and trigger board designed by IHEP trigger team

BEB Hardware design

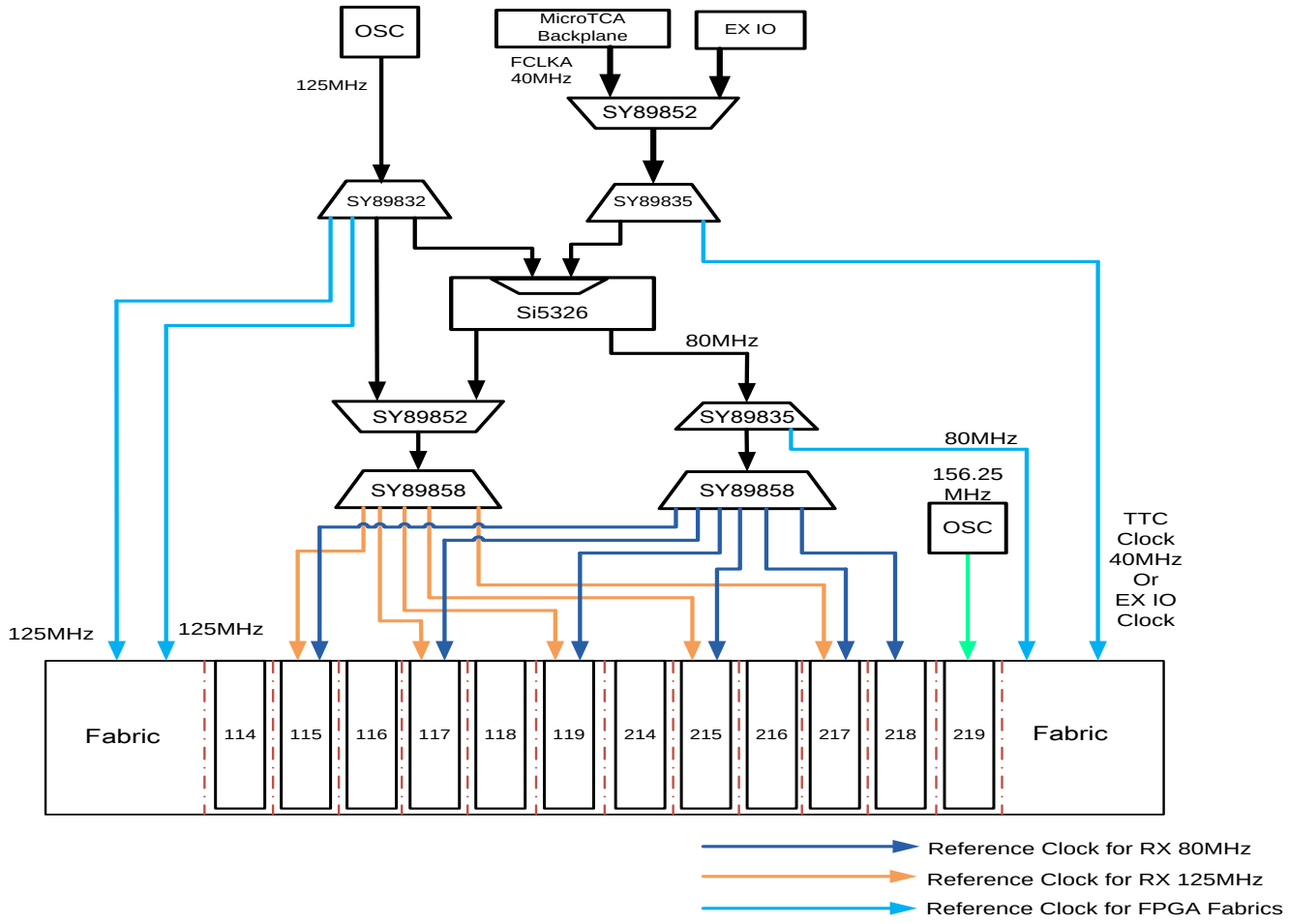
- Backend Electronics and Trigger Board
  - full-height double-width MTCA standard BEB
  - 36 links input/output, a total bandwidth of 400 Gb/s per board
- XC7VX690T-2(Virtex-7)
  - Core FPGA, data processing
  - GBT-FPGA
  - Cluster finding
- XC7K70T-2 (Kintex-7)
  - Ctrl FPGA, clock management and FPGA program
- AT32UC3A1512(Atmel)
  - Module Management Controller,
  - Power on/off, voltage, temperature information communicate with crate controller(MCH)
- Rj45
  - Clock in/fan out





Clock distribution on BE board

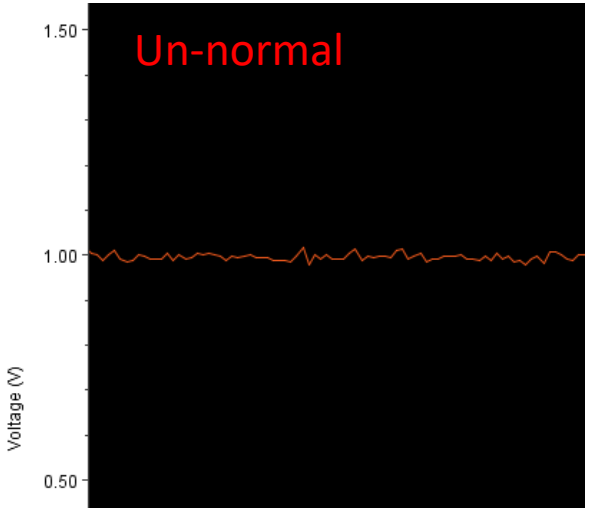
- Easy for system setup
  - Clock in
    - AMC FCLKA,
      - for LHC system clock(40MHz)
    - EX IO,
      - clock in without crate
  - Clock out
    - EX IO, provide 7 pairs lvds IO
  - Standalone clock for GTH TX and GTH RX
  - Standalone clock for 10GbE Quad

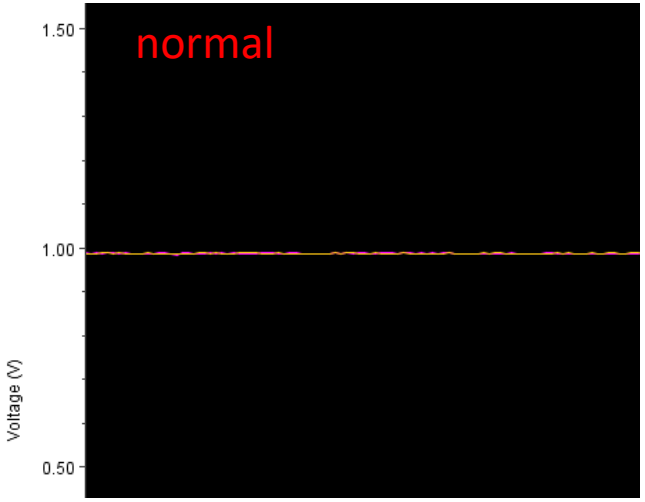


Power supply requirement study of GBT link

- GBT Link not stable on some Backend Electronic Boards.
- A series of test has been done between un-normal and normal to find the reason.
  - IBERT test
  - miniPods(Tx/Rx) replacement
  - Fibers replacement
  - Different versions of GBT-FPGA firmware (1link/4link)
  - Power supply

  …
- A interesting power ripple(Vpp) difference of VCCINT was founded.





Vpp max >= 30mv

- Voltages of both are within the recommended operating Conditions 0.97-1.03V (ds183_Virtex_7_Data_Sheet.pdf).
- No ripple requirement can be found in Xilinx or GBT user guide.

VCCINT for GBT-FPGA

- VCCINT is connected to Tx/Rx PCS in 7 series FPGA GTH.
- 8b/10b is not used in GBT-FPGA IP core.
- When GBT-FPGA IP core is used, more precise power of VCCINT is needed.
  - A preliminary requirement of ripple is obtained: Vpp <= 10mv.
    - GBT link then can be established and tested without error in 72h.

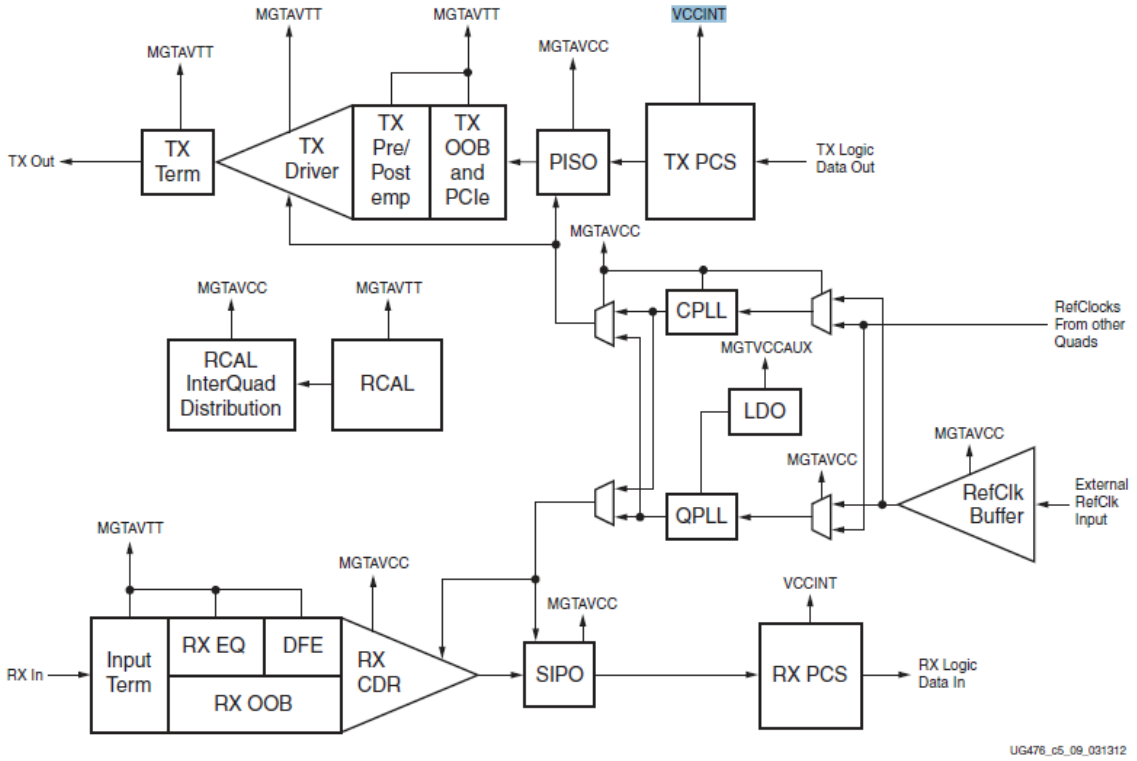
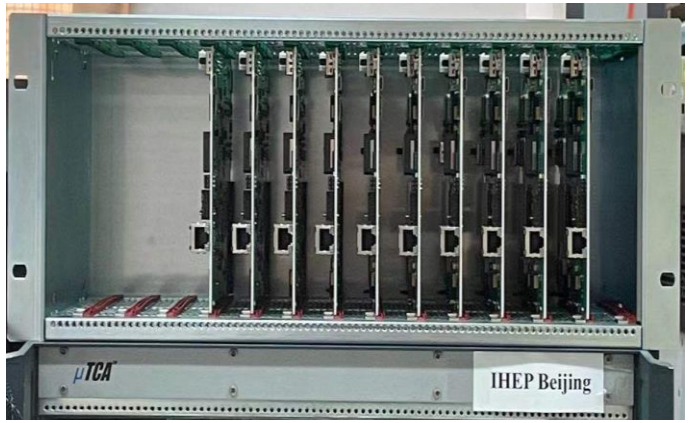
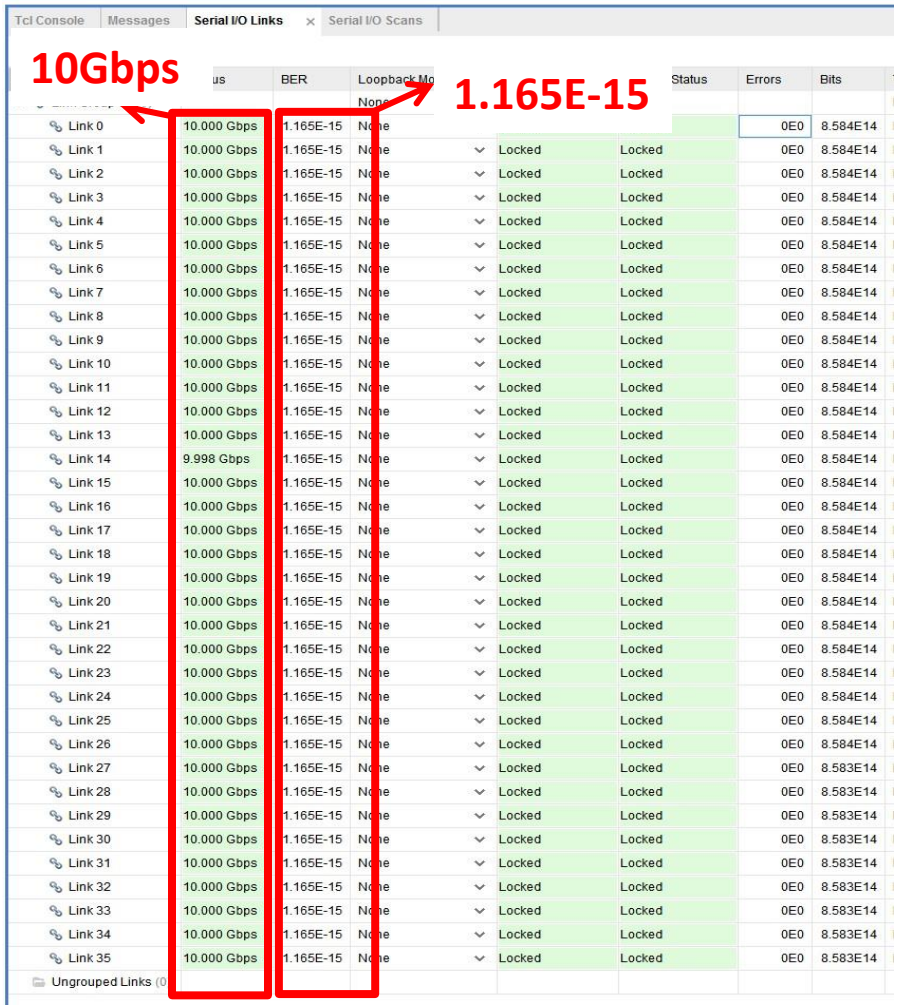


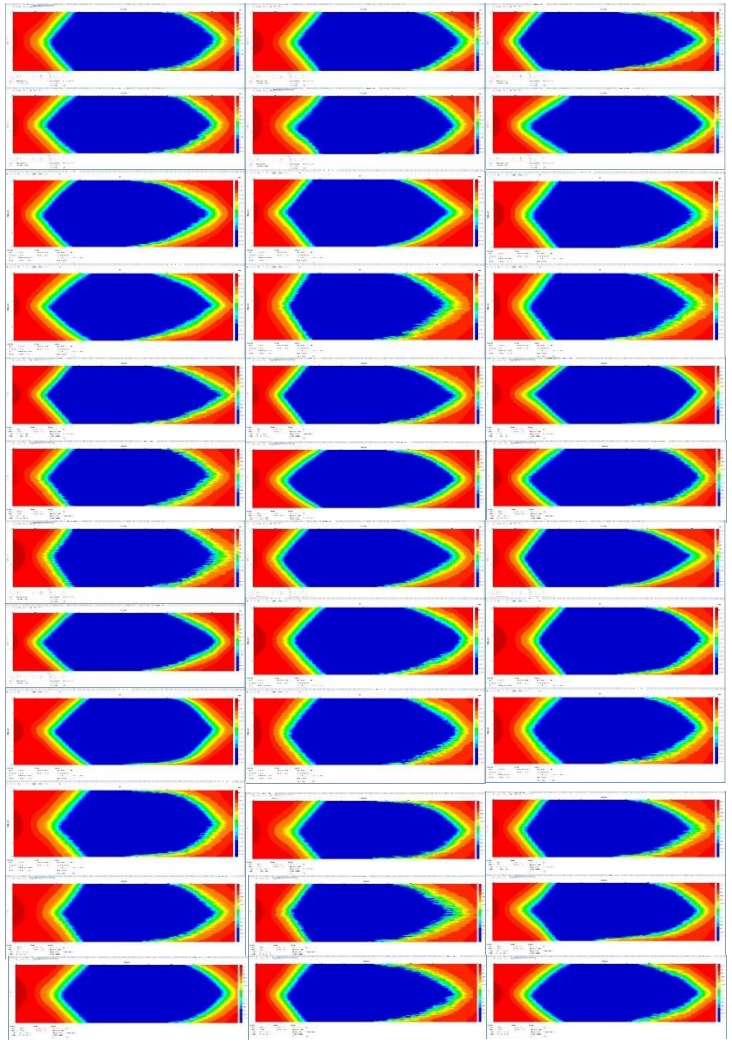
Figure 5-2: **7 Series FPGAs GTX/GTH Transceivers Internal Power Supply Connections**

MTCA Mini-Production for installation finished

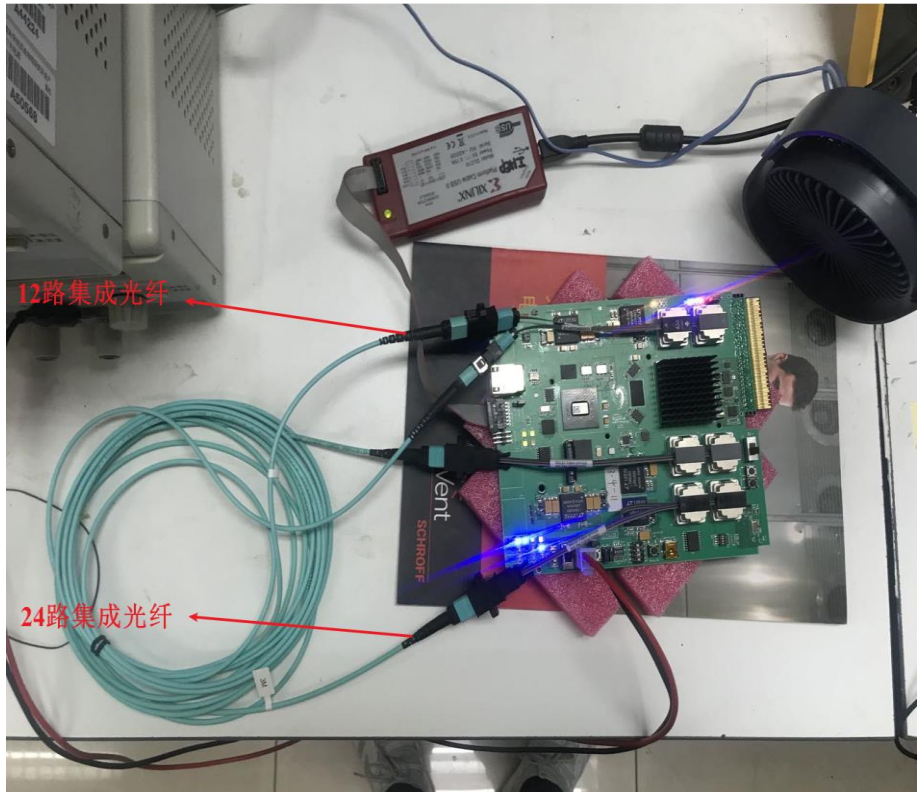
- Mini-Production for 2021/22 Demonstrator setup and 2023 Installation Finished.
- MicroTCA Qualification OK.
- Ready for transportation to CERN .







Quality Check list

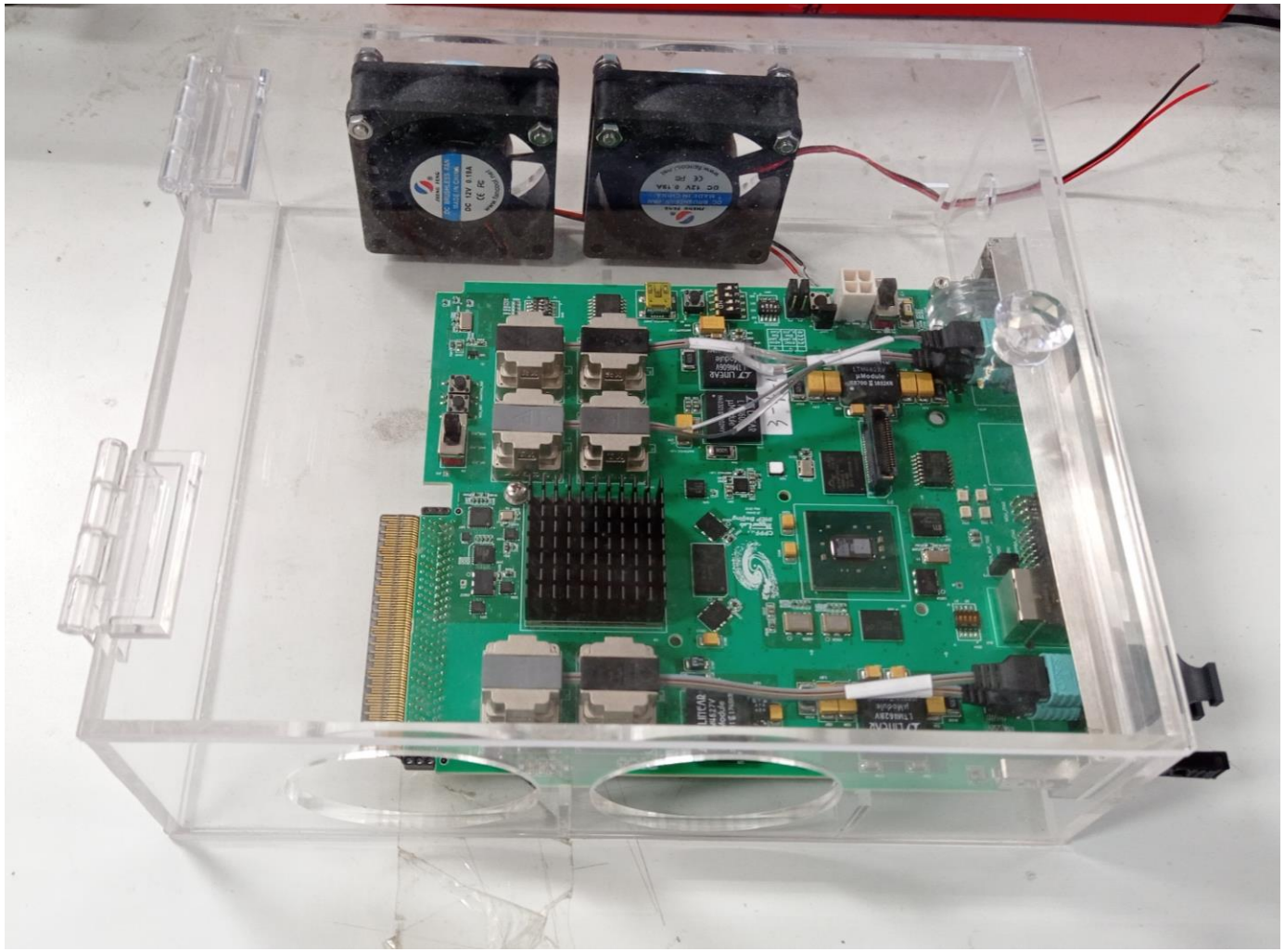


Mini-production QC list:

- 1. Number the boards, and check the appearance of the board.
- 2. Measure the grounding impedance and load impedance of the test point.
- 3. Install 0R isolation Resistor from power to payload.
- 4. Configure the switch to default position.
- 5. P6 to VCC_3V3 when standalone test, to MP_3V3 when install in crate.
- 6. Check the power status after first time power on(voltage value, power ripple).
- 7.MMC programming and MMC function test with crate。
- 8. Flash test.
- 9.DDR test。
- 10. GTH test using ibert。
- 11. GBT link test.

BE/Trigger Demo for iRPC chamber test

- BE/Trigger will be used for iRPC chamber test.
- Cooling box is designed for BE/trigger single board test system.
- 5 single board test system will be for chamber test.



Summary on iRPC Backend/Trigger

- Backend/Trigger Board based on MTCA is designed for iRPC Backend first step installation.
- MTCA BE board will be used for Demonstrator setup.
- Min-production is finished and ready for transportation to CERN .