中国科学技术大学

University of Science and Technology of China

Altiroc1 Test and LGAD Readout Electronics

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University of Science and Technology of China

Outline

- Background
- Altiroc1 test
  - Altiroc1V2
  - Altiroc1V3
- LGAD readout electronics of USTC
  - Analog front-end electronics(AFE)
  - Digital readout module(RM)
  - Common readout module(CRM)
- Summary and future plan

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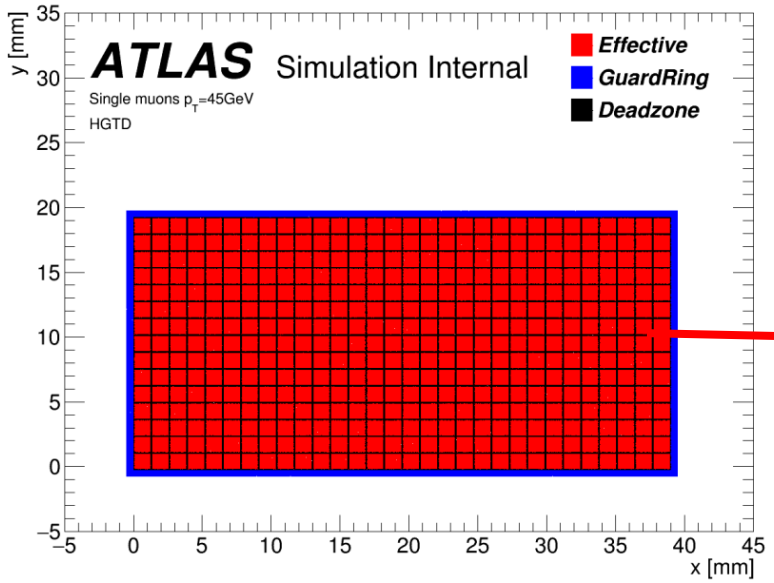
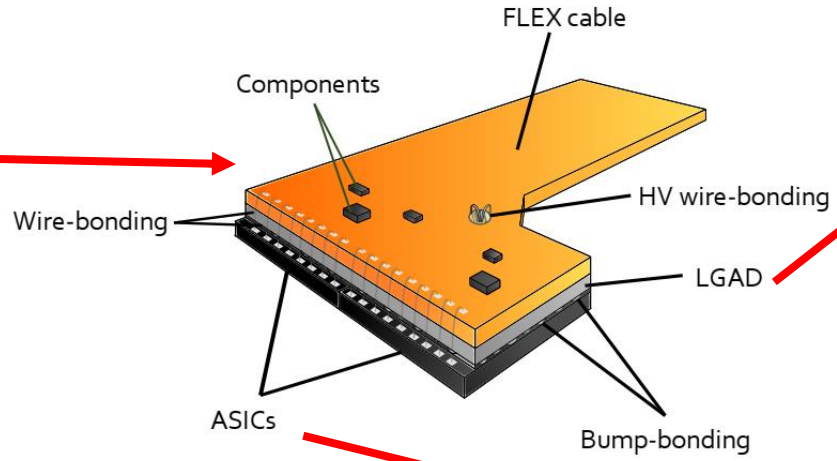
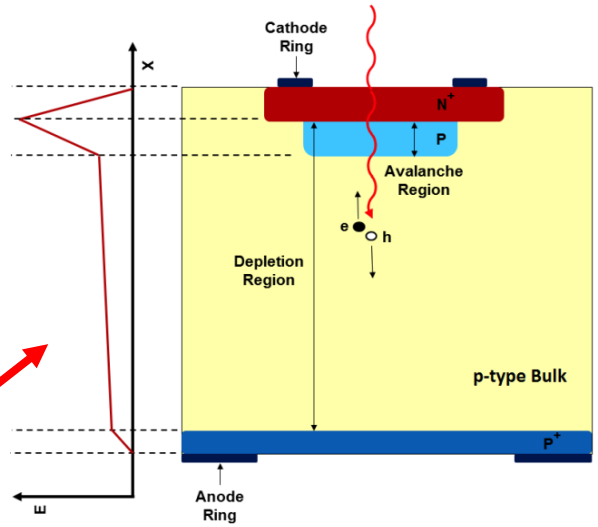
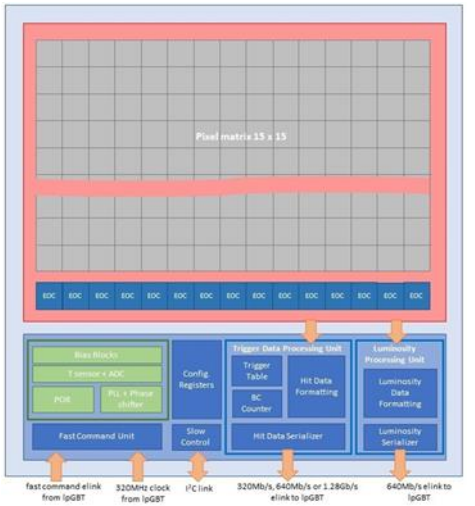
Background









- Low Gain Avalanche Detectors (LGAD). It has been chosen for the HGTD sensors.
- Altiroc, design by OMEGA, is a front-end electronics, low-noise custom ASIC used for LGAD readout.

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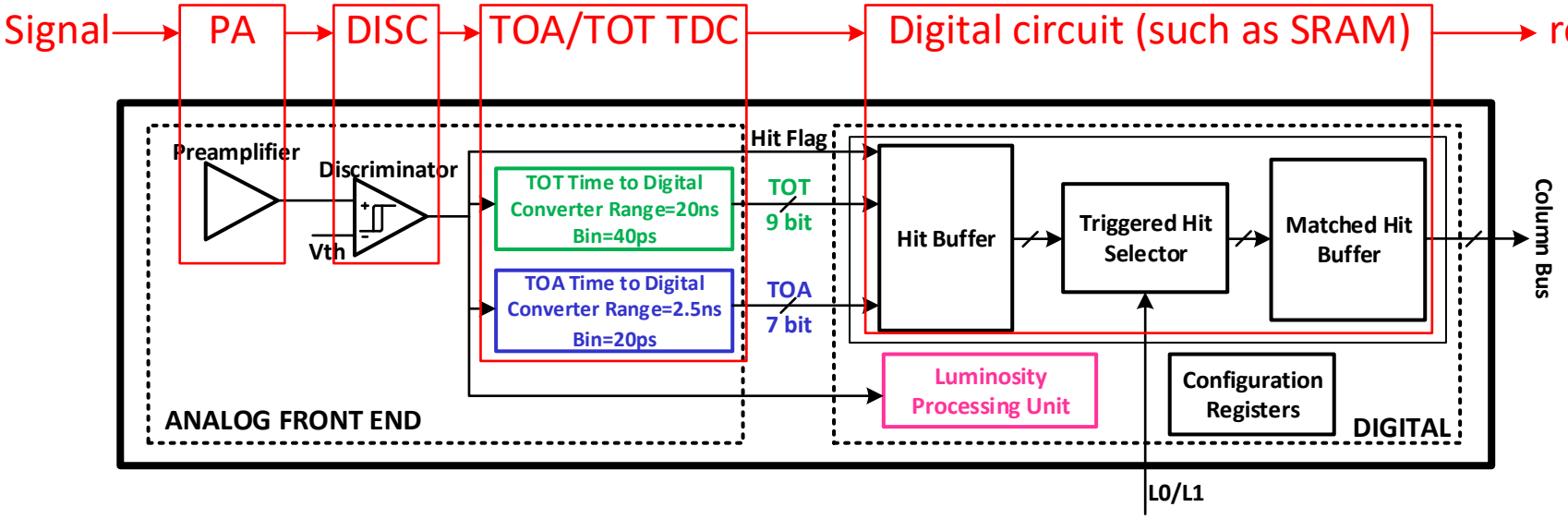
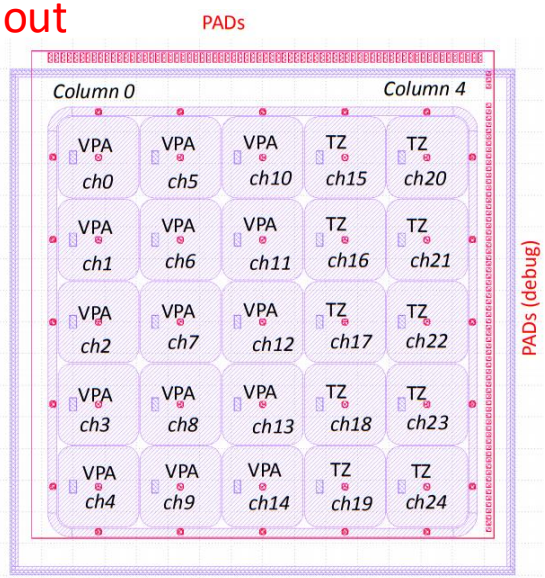
Structure of Altiroc1V2



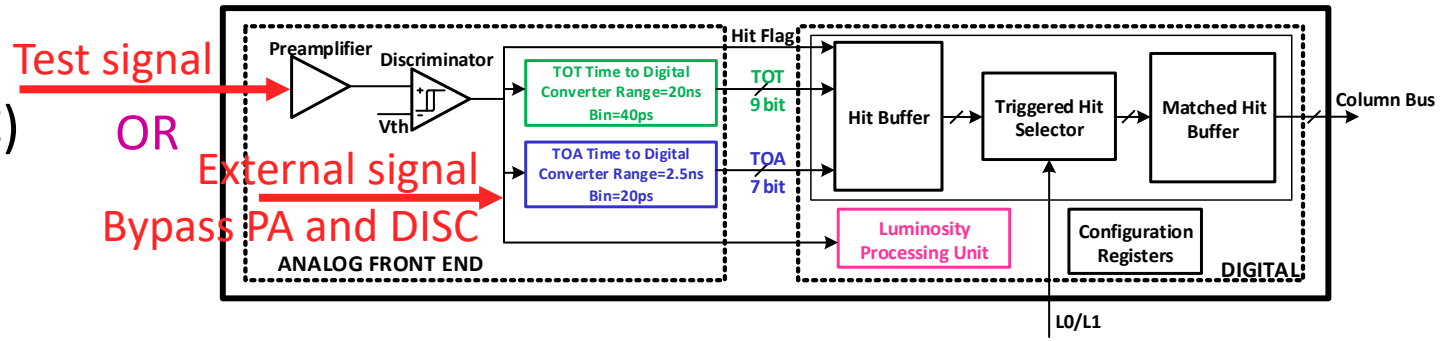


- Signal → Preamplifier(PA) → Discriminator(DISC) → TDC → SRAM → Readout

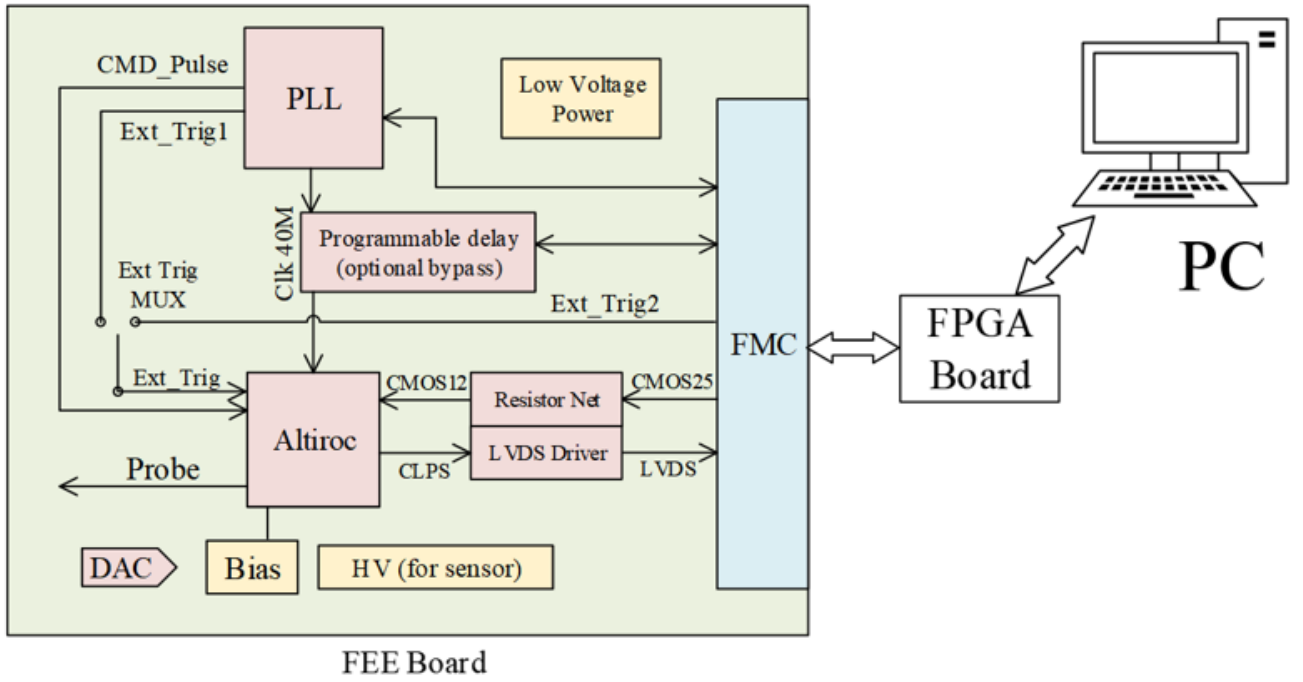
- Altiroc1V2 contains 25 channels
  - Channel 0~14 use voltage preamplifier(VPA) as PA
  - Channel 15~24 use trans-impedance amplifier(TZ) as PA
  - VPA performs better than TZ
  - Only channel 4, 9, 14 can add Cd, which simulates the parasitic capacitance of LGAD.

Altiroc1V2 test

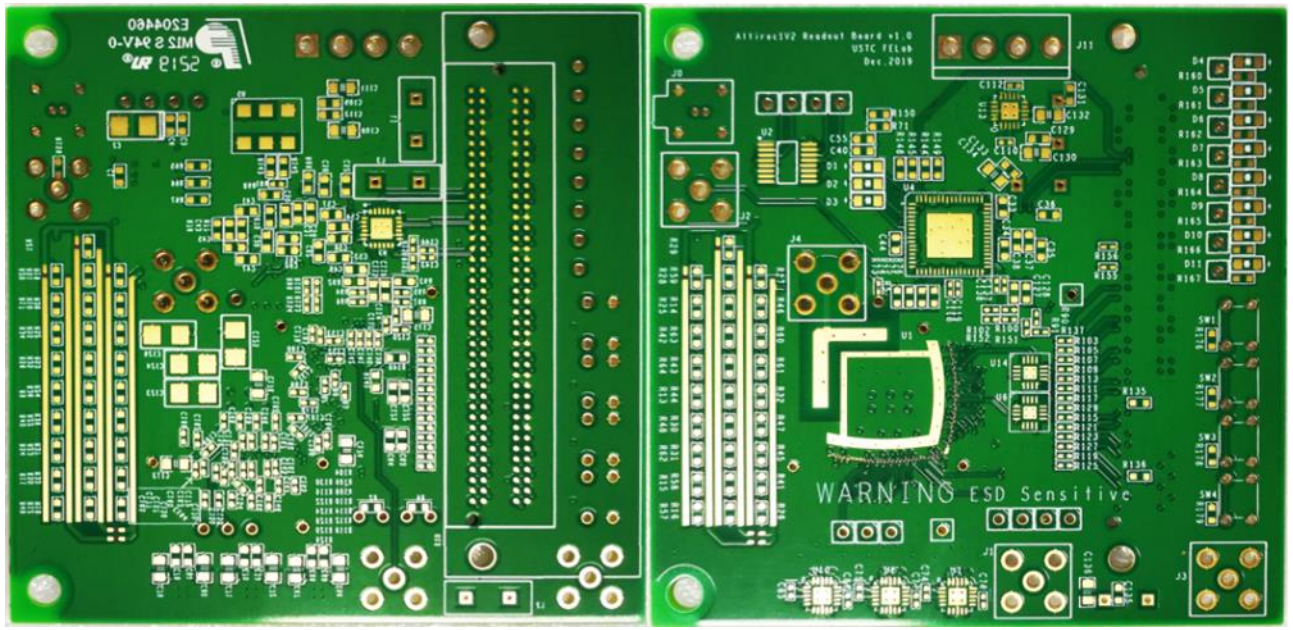
- Altiroc1 test contains
  - TDC test(bypass PA and DISC)
  - Complete channel test (PA+DISC+TDC)



- Test system main structure
  - PLL : provide high quality clock
  - Delay Cell : programmable delay
  - FMC Interface : transfer data and config
  - HV : prepared for sensor
  - DAC and Bias : Altiroc1V2 debug

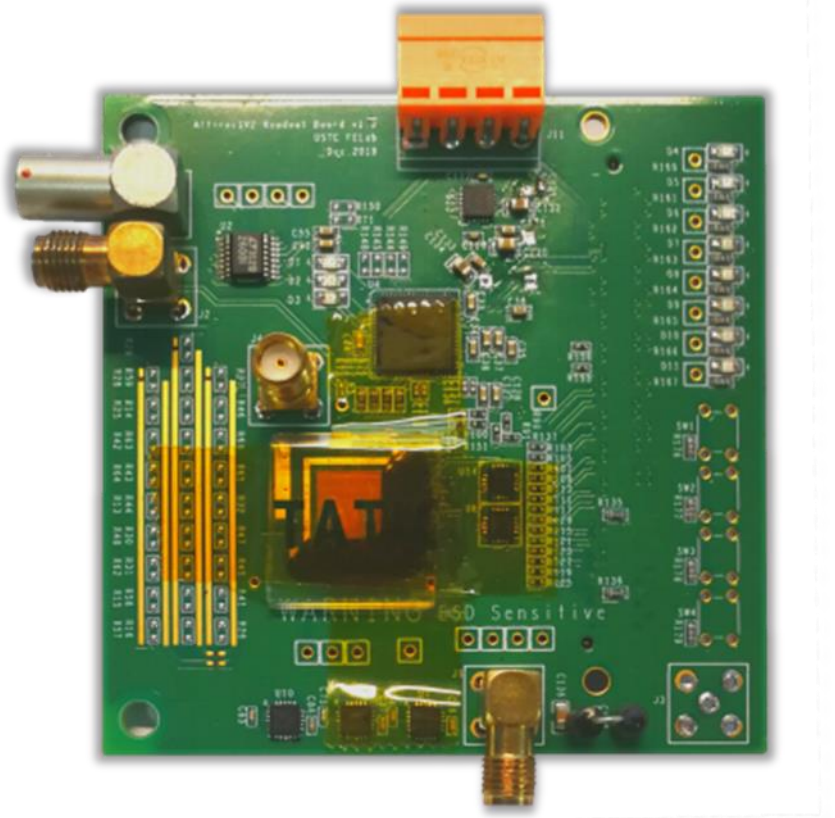


Altiroc1V2 test system



Bottom Top

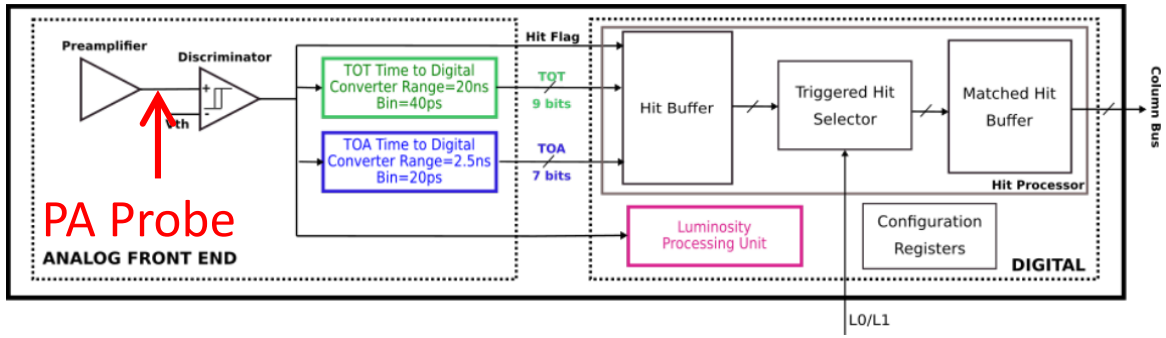
Altiroc1V2 test board (bare board)

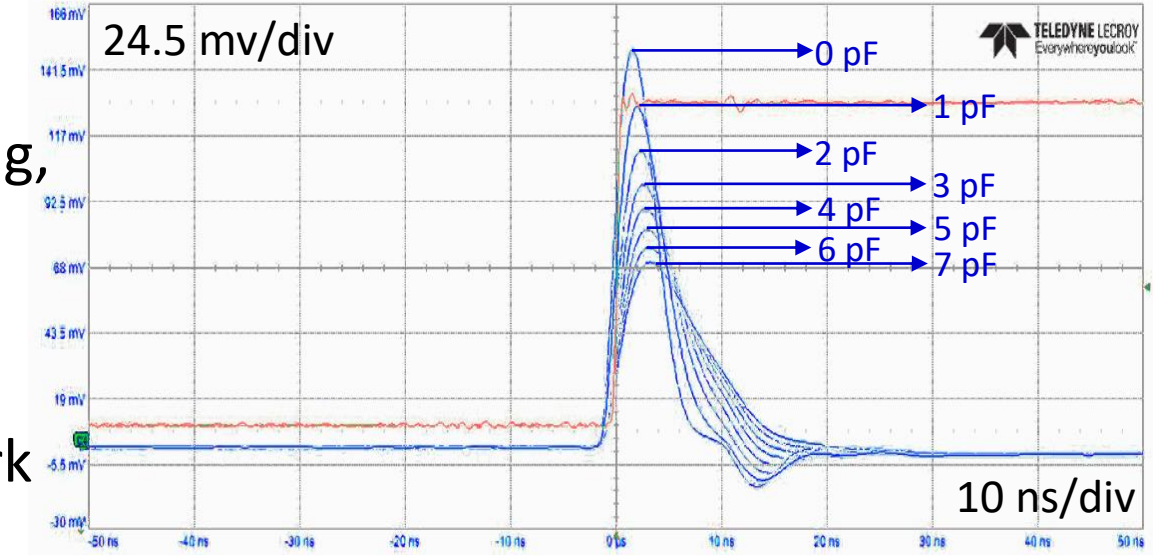


Altiroc1V2 test board

Altiroc1V2 PA Probe

- Observe the waveform through the PA Probe of Altiroc1V2
- Channel 4, 9 ,14 have configurable input capacitance
- with the input capacitance increasing, the amplitude of the PA output waveform decreases
- Slow control and analog circuits work as expected

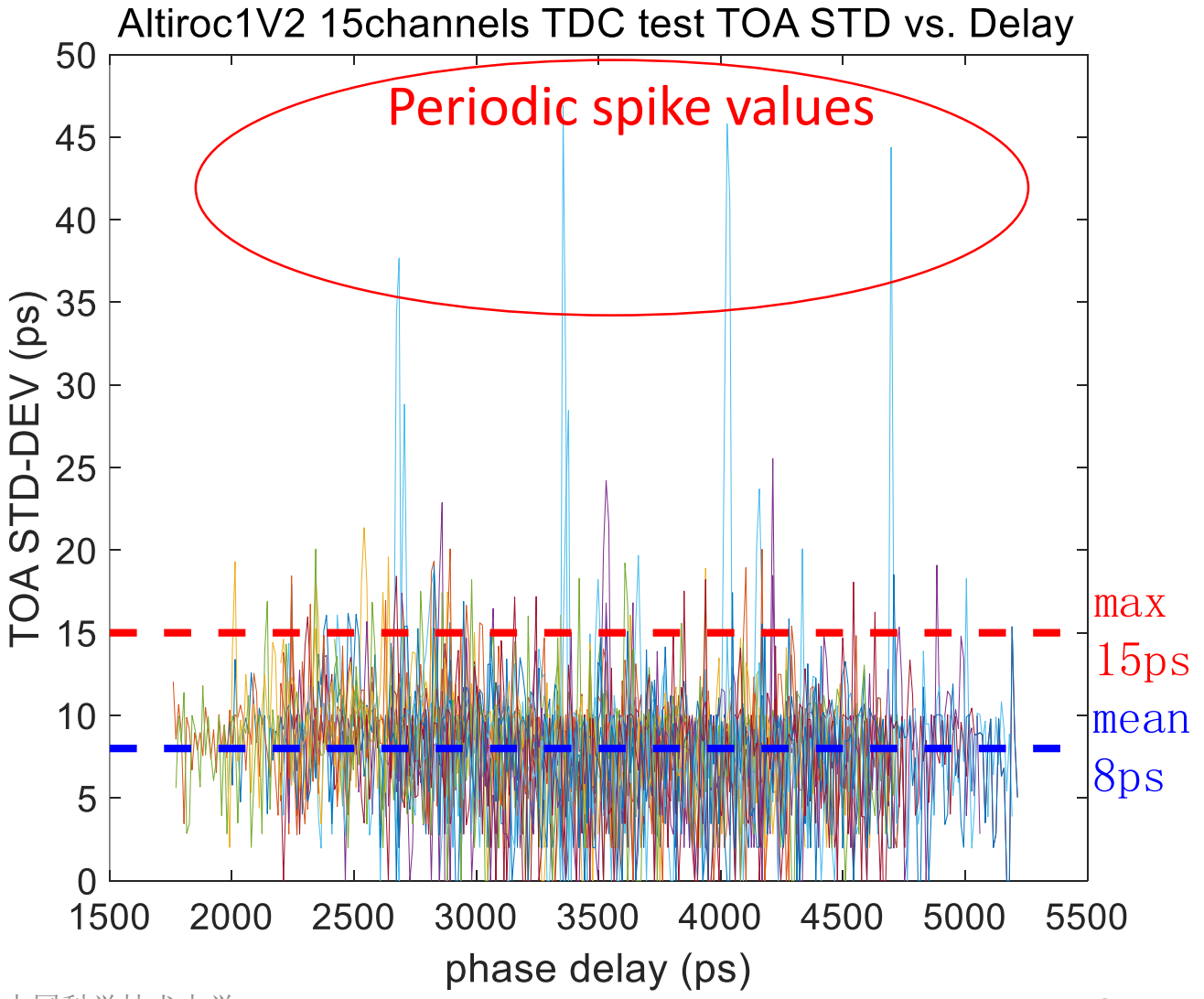




Waveform at different input capacitance 0~7 pF, input charge 10 fC

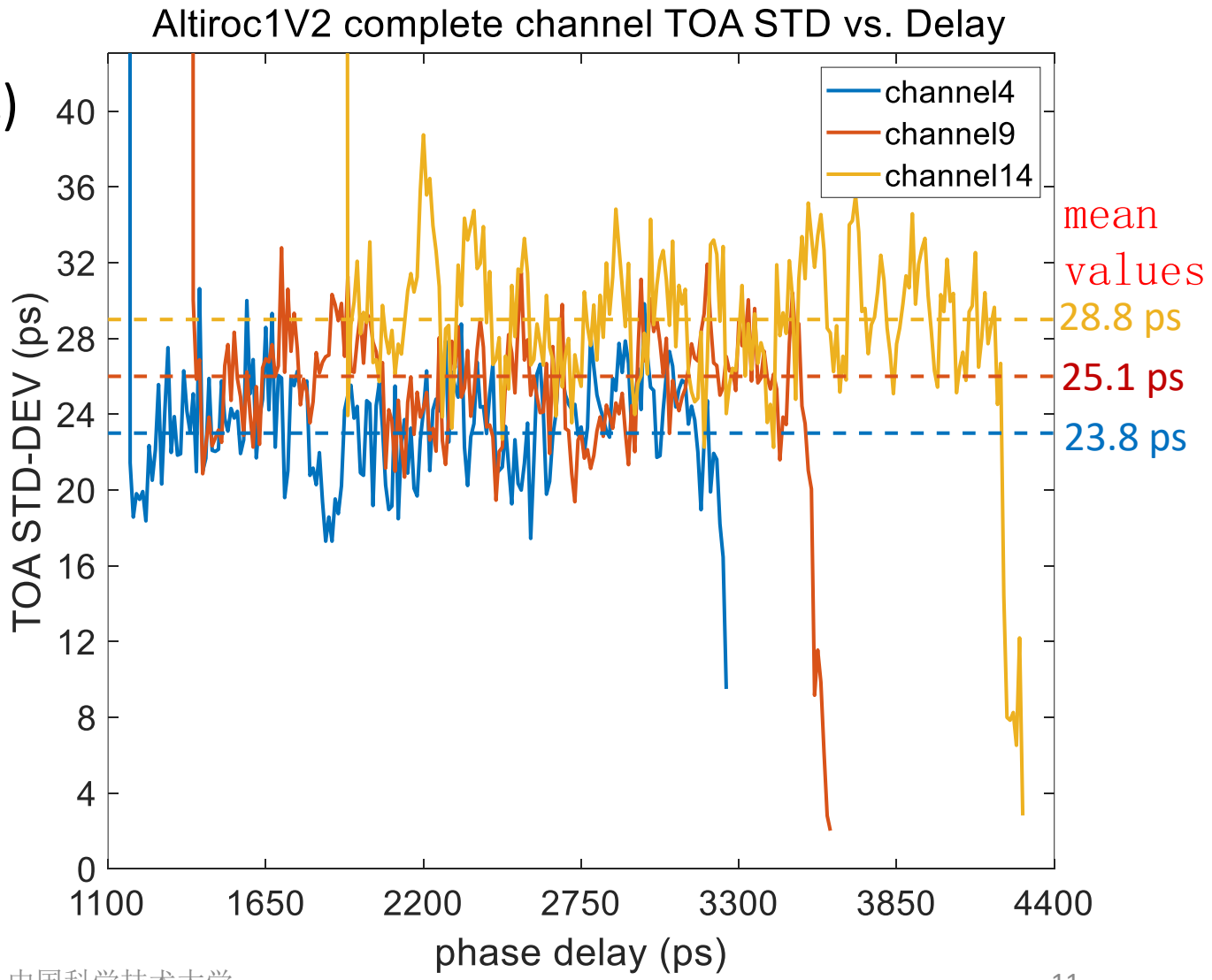
Altiroc1V2 TDC test

- TDC bin-size is around 20.3 ps. Detection range is 2.5 ns
- The mean value of TDC jitter is around 8 ps.
- Ignoring the abnormal channels, the maximum is around 15 ps.
- Periodic spike values appear
- According to the designer's reply, spike values appear probably due to some bugs in the digital part of Altiroc1.



Altiroc1V2 complete channel test

- 3 channels TOA jitter (PA+DISC+TDC)
  - Ch4 jitter mean value 23.8 ps
  - Ch9 jitter mean value 25.1 ps
  - Ch14 jitter mean value 28.8 ps
- The TOA measurement value close to the full range is inaccurate.



Change in Altiroc1V3 compared to Altiroc1V2：

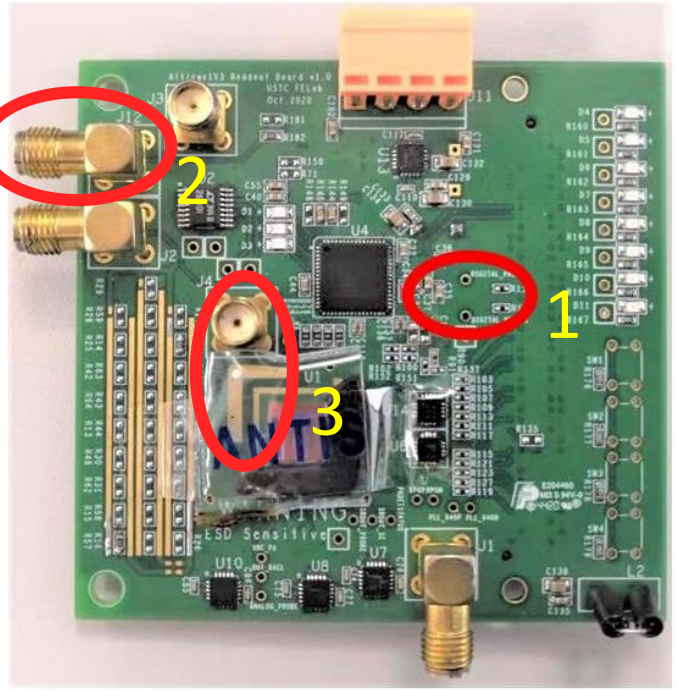
- 15 channels VPA +10 channels TZ → 25 channels VPA
  - According to the test the designer did, VPA works better than TZ.
- 4 channels can add Cd → 21 channels can add Cd
  - Cd can simulate the parasitic capacitance of LGAD.
- Add a new structure : leakage compensation.
  - It is used to adjust the binsize of TDC by adjusting the control voltage of DLLs of TDC.

Altiroc1V3 test system

Altiroc1V3 test system is similar to Altiroc1V2.

Major changes contain:

1. Add 2 new digital probe
2. Replace a LEMO with a SMA
3. Optimize the HV net
4. Fix some bugs in PCB design

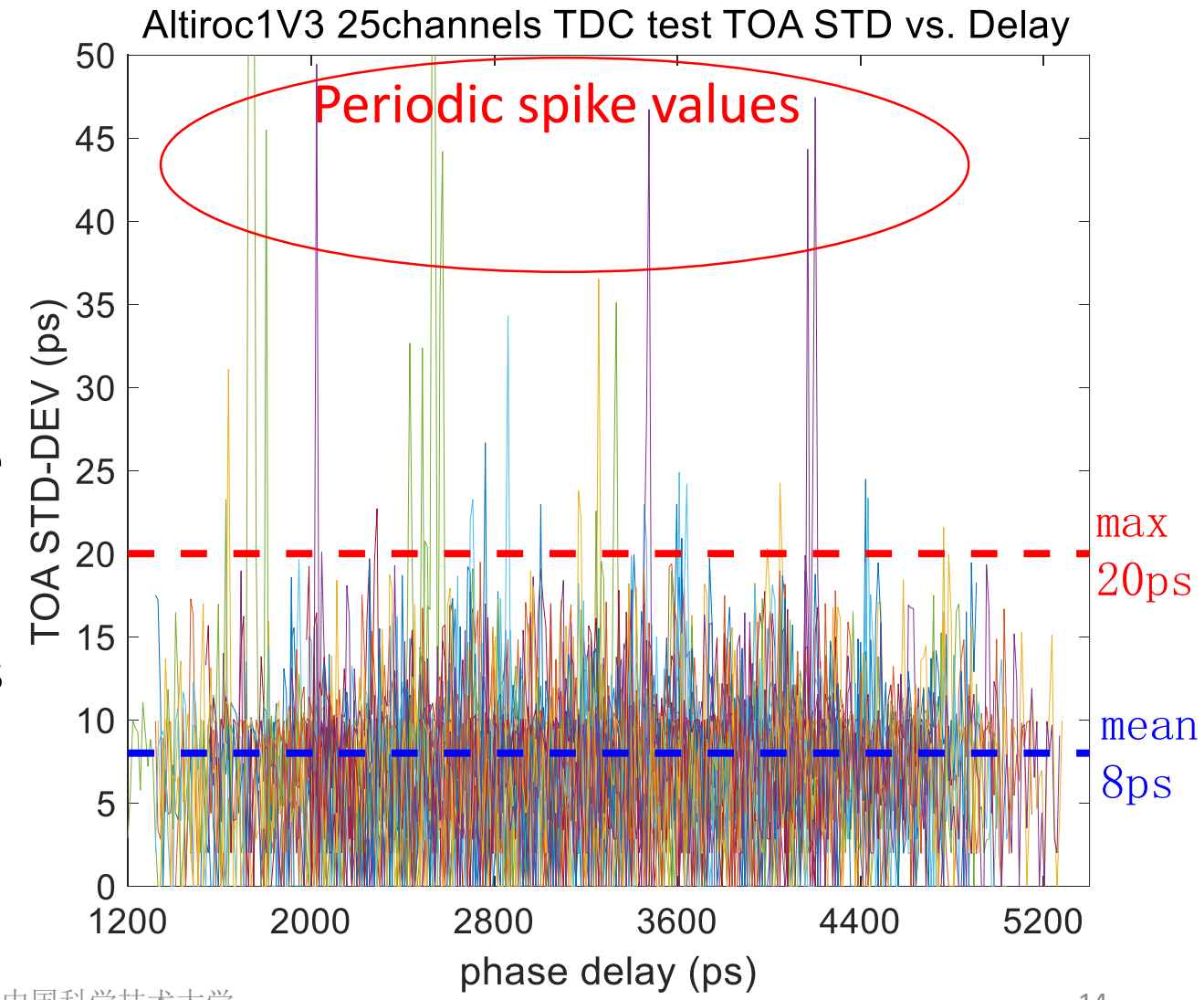


Test board for V3

Test board for V2

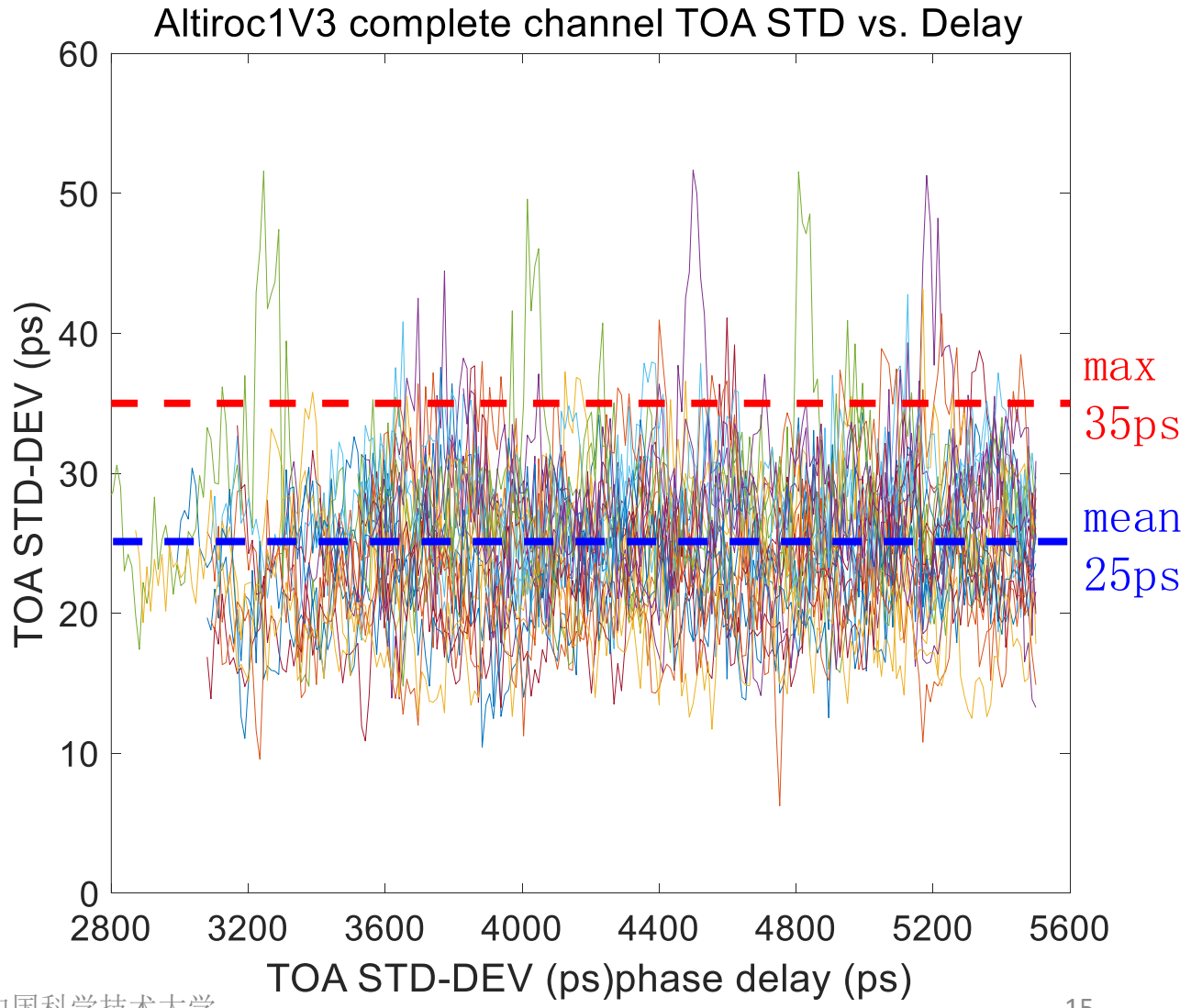
Altiroc1V3 TDC test

- The mean value of TDC jitter is around 8 ps.
- Ignoring the abnormal channels, the maximum is around 20 ps.
- Periodic spike values appear more frequently in V3 test .
- The designer planed to solve this problem in Altiroc2.



Altiroc1V3 complete channel test

- The mean value of channels jitter is around 25 ps.
- Ignoring the abnormal channels, the maximum is around 35 ps.
- Periodic spike values that appear in TDC test affect the results of complete channel test obviously.



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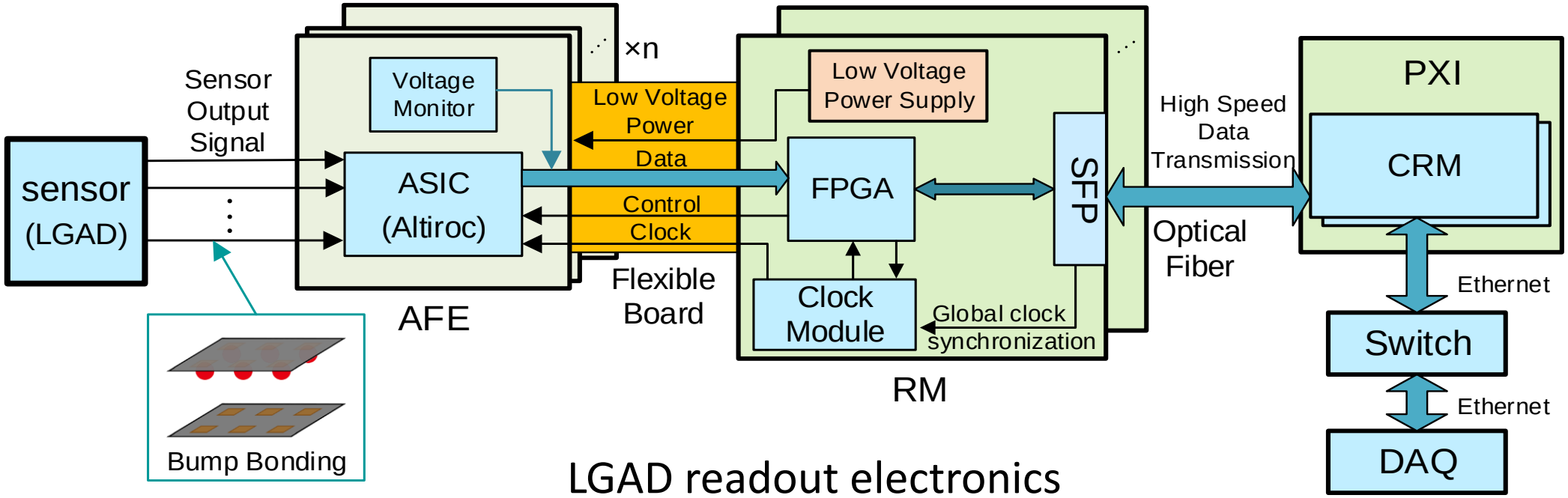
LGAD readout electronics of USTC



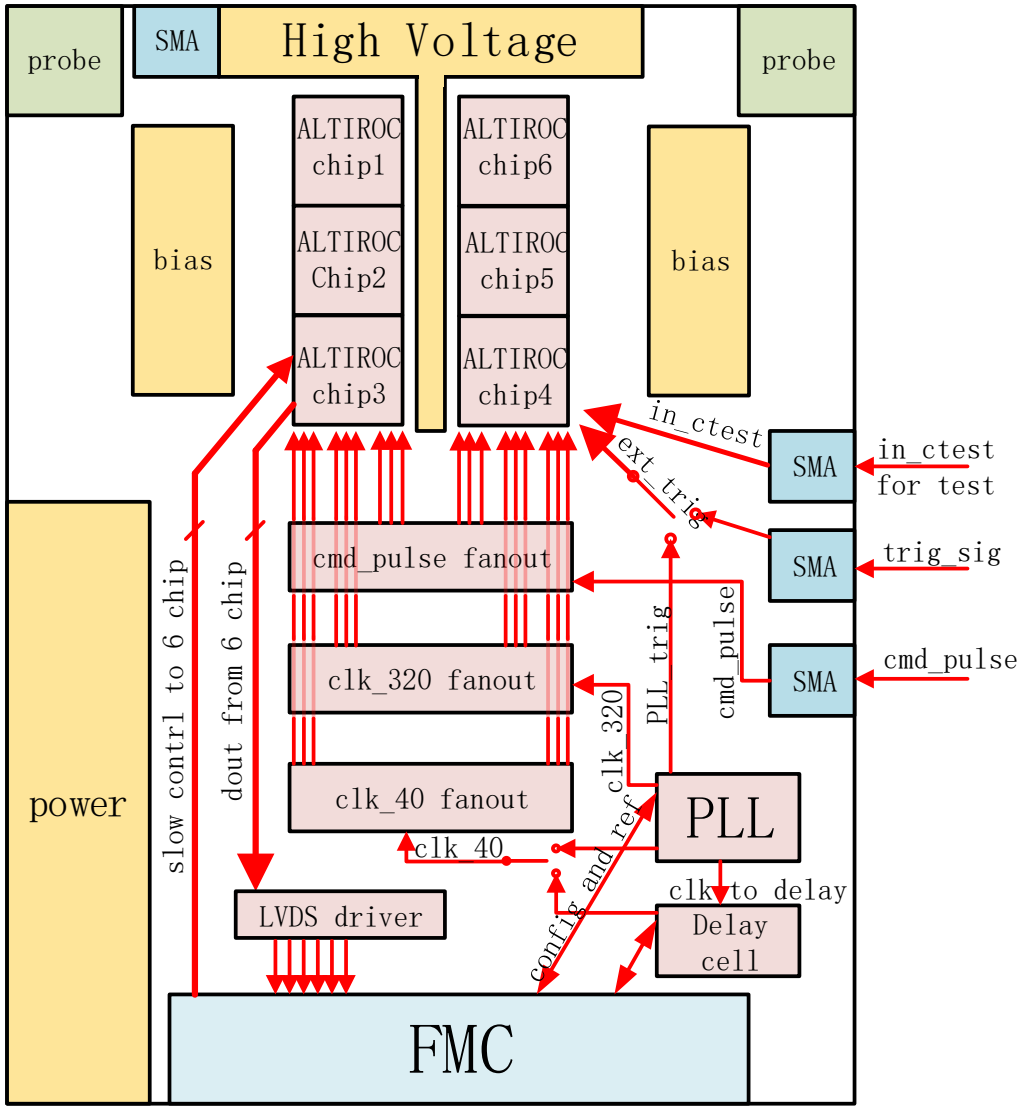
LGAD readout electronics

- We design this LGAD readout electronics for the verification of USTC LGAD.
- Analog front-end electronics(AFE) is based on Altiroc1v2/Altiroc2.
- Readout modules (RMs) transfer data from AFEs to the CRM.
- Common readout module (CRM) collects data and sends them to DAQ.

AFE based on Altiroc1

Main structure :

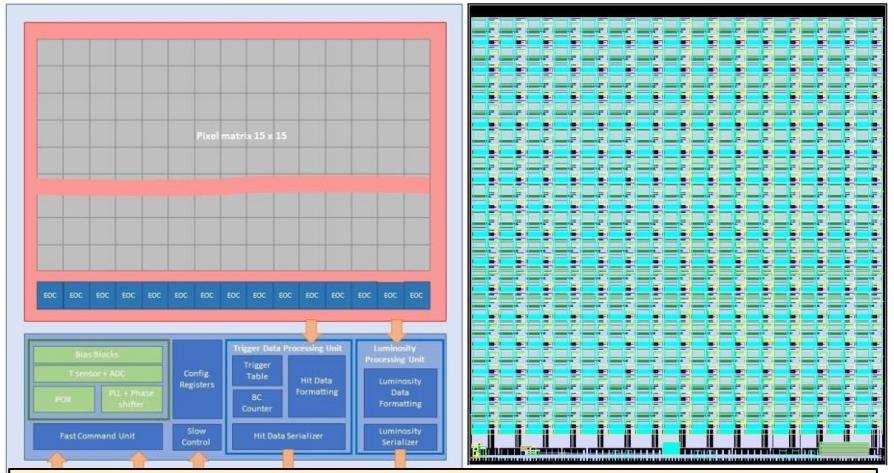
- Sensor+Altiroc1
  - Multiply chips(6 in this design)
- PLL/Delay Cell/Fan-out chip
  - delivery clock cleaning and fan-out
- FMC Interface
  - configuration and control command
- LVDS driver
  - data readout
- Probe holes:
  - calibration and debugging ports
- Power/Bias
  - low and high voltage bias circuits.



AFE based on Altiroc2

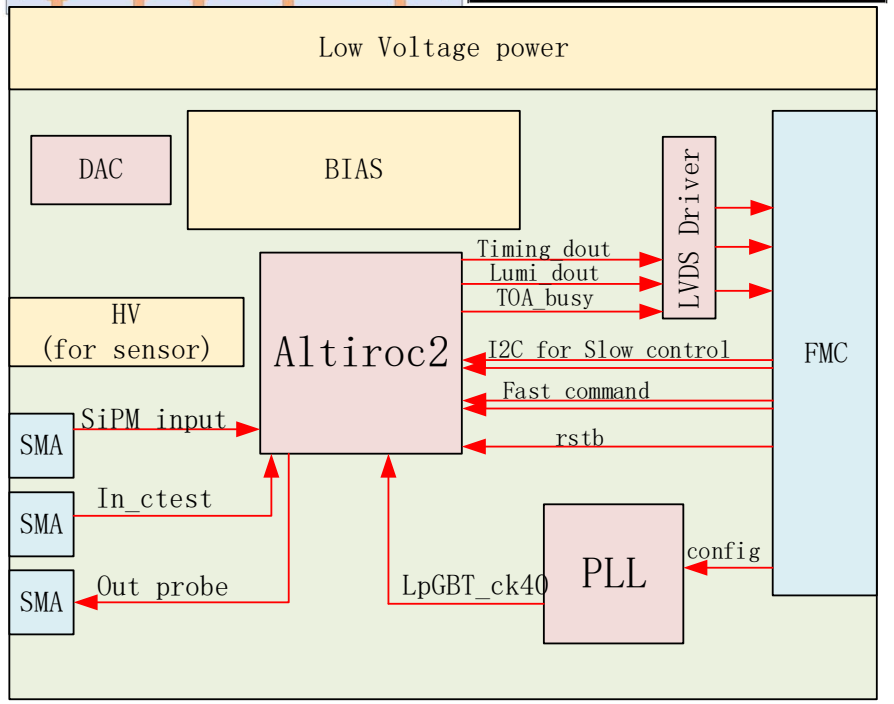
➢ Altiroc2

- latest version of the Altiroc series.
- contain 15×15 channels and complete readout function.



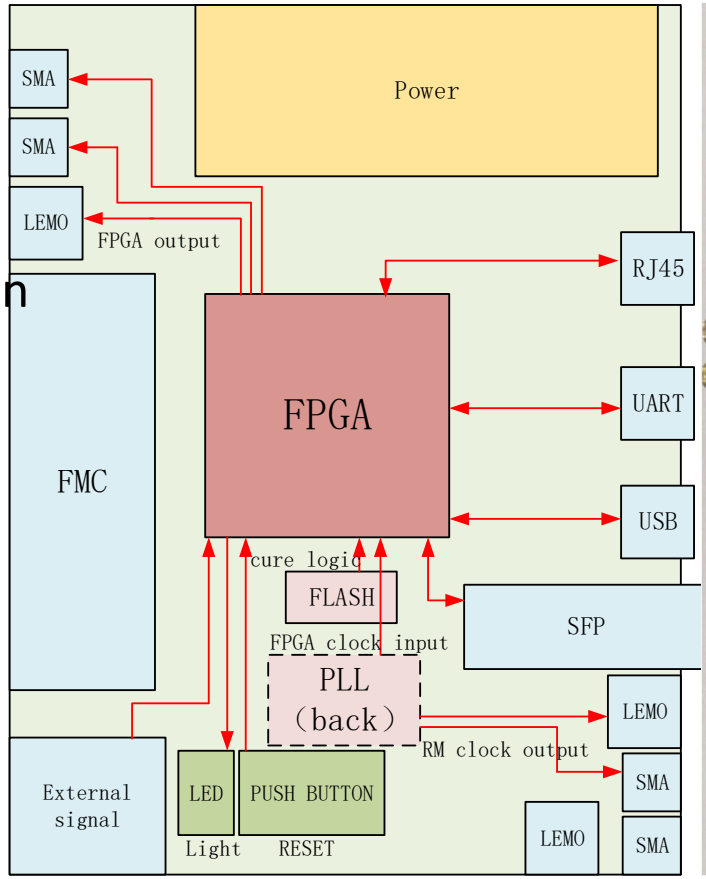
➢ Altiroc2-based AFE design

- Add measurement for hit count in Altiroc2.
- The slow control instruction is updated to the I2C interface in Altiroc2.
- Altiroc2 integrates more test modules
- Interface to RU is compatible with AFE based on Altiroc1.

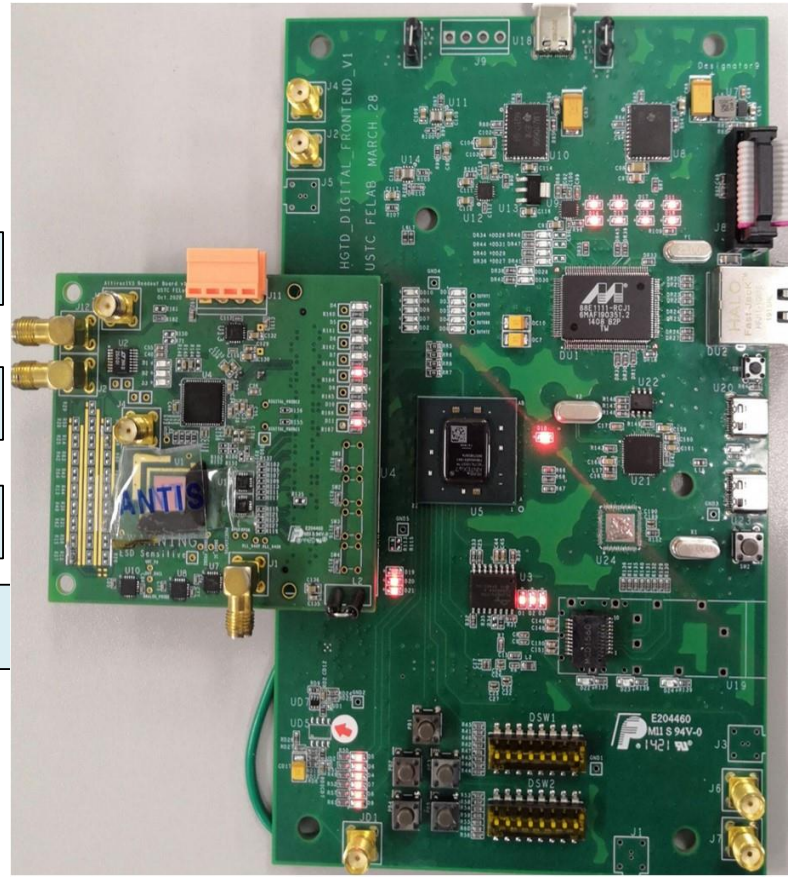


Digital readout module(RM)

- FPGA
  - data receiving and transfer
  - provide clock/trigger/control
- PLL
  - receive the global synchronization clock and clean delivery clock
- Power
  - low voltage power supply
- SFP
  - high-speed data exchange
- RJ45
  - The standby interface of SFP
- UART
  - debug

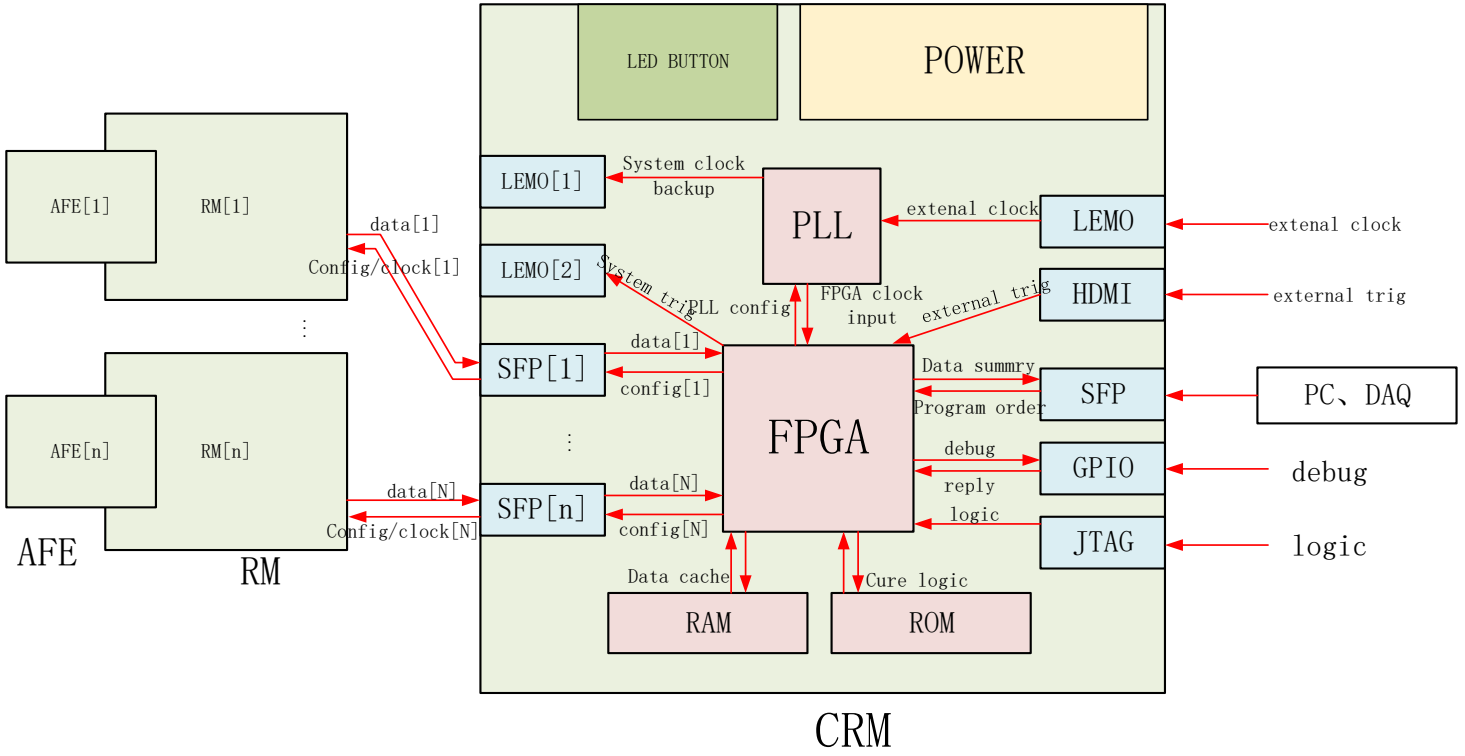


Schematic diagram



Digital readout module(RM)

Common readout module(CRM)



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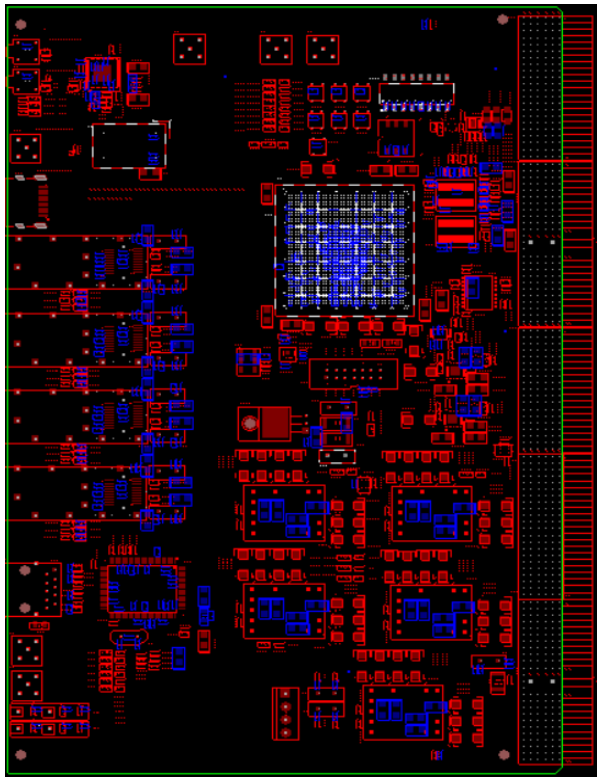

PCB design

- Data collection and packaging
- Receiving external clock and trigger
- Clock and trigger distribution

- Have finished the PCB design

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- Altiroc1 test
  - Altiroc1v2 test channel jitter mean values: Ch4 23.8 ps ; Ch9 25.1 ps ; Ch14 28.8 ps
  - Altiroc1V3 test channel jitter: mean values 25ps ; maximum 35ps
  - Periodic spike values due to digital circuits bugs
- LGAD readout electronics of USTC
  - Analog front-end electronics(AFE) based on Altiroc1/Altiroc2
  - Digital readout module(RM)
  - Common readout module(CRM)

Future plan

- Altiroc2 test
- Bump bonding module
- Complete system fabrication and debugging