# Emulator System of the HGTD Peripheral Electronics Board (PEB) for ATLAS Phase II Upgrade

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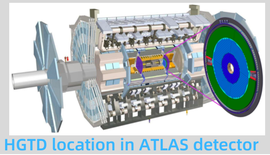
## Motivation

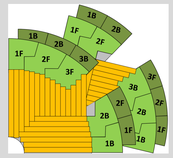
In order to mitigate the pileup effects caused by the increasing luminosity of proton-proton collision at HL-LHC, a High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase-II upgrade. There will be six types of Peripheral Electronics Boards (PEB), 1F, 2F, 3F, 1B, 2B, 3B, which are designed to cover the peripheral area of the HGTD.

Prior to the PEB prototype, a PEB emulator system has been developed to help us verify some concerns in advance. It can serve as a flexible platform where we can perform many kinds of tests and validations, such as:

- Validate some manufacturing techniques of PCB, some mechanical parameters
- Exercise the data transmission of the versatile link (lpGBT + VTRx+)
- Exercise the assembly and integration of the peripheral electronics parts to the cooling plate
- Verify the strategies of connectivity between modules and lpGBTs, test power blocks……



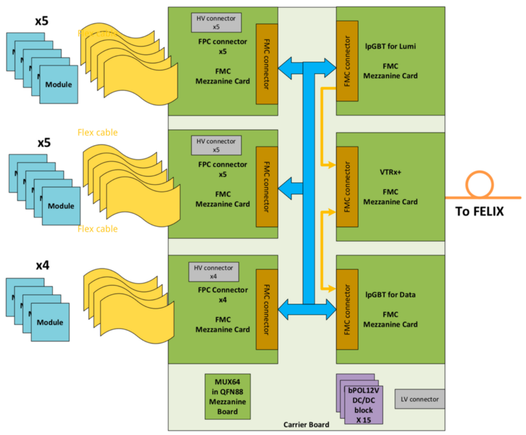
HGTD location in ATLAS detector




PEB layout in one quadrant

## PEB emulator system design

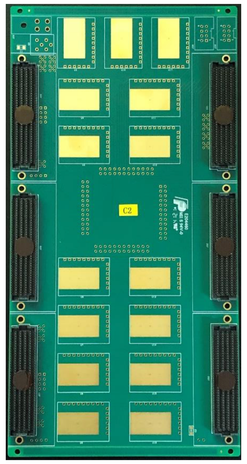
### Overview




The PEB emulator system is actually a simplified version of PEB prototype, and it still uses the same ASICs like lpGBT, VTRx+, bPOL12V, Mux64, but in a small quantities. Design highlights:

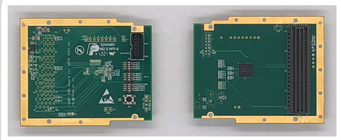
- **Modular design makes ASICs replaceable**: Those key ASICs are modularized into different kinds of daughter boards while the PEB emulator itself serves as a carrier board. Specifically, the system includes a carrier board, 1 VTRx+ daughter board, 2 lpGBT daughter boards (for Lumi and time data processing), 3 FH26 connector daughter boards, 15 bPOL12V daughter boards and 1 MUX64 daughter board
- **Compatible with commercial ASICs**: In case those key ASICs are in shortage, we can still operate the emulator system with some commercial ASICs. For that, we can use FPGA and SFP+ daughter boards to replace the lpGBT and VTRx+. We also designed a commercial ASIC power block to replace the bPOL12V.
- **Dedicated wire routing between modules and lpGBTs**: This kind of wire routing can help us verify different lpGBT data rate settings. The carrier board can support up to 14 modules whose signals will go to the 2 lpGBTs. We designed module emulator since modules are not available at the moment.

### Carrier board



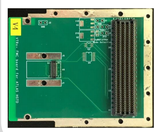
It can host all the daughter boards together to realize the functionality of PEB. Basically, all the components on this carrier board are passive connectors, including FMC connectors, QFN88 socket and header pin rows. The main role of this board is to implement specific connectivity among those connectors

### lpGBT daughter board



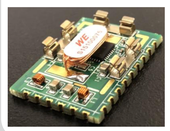
Basically all the lpGBT pins are routed to the FMC connector, which will make sure that the carrier board can have full communication with the lpGBT once the lpGBT daughter board is plugged. It can be tested with a Xilinx evaluation board before integrated into the carrier board. Compatible with v0 and v1.

### VTRx+ daughter board



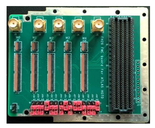
The signals on the VTRx+ connector are re-routed to the FMC connectors. It can be tested with a Xilinx evaluation board before integrated into the carrier board.

### bPOL12V power block



The bPOL12V power ASIC is mounted on this board, which can be covered with a shielding case to reduce output ripple.

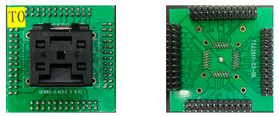
### FH26 connector daughter board



It is actually an adapter board. There are only connectors used on this board.

The 5 FH26 connectors are used to hold 5 modules through flex cables while the FMC connector brings in all the signals of FH26 connectors.

### MUX64 daughter board



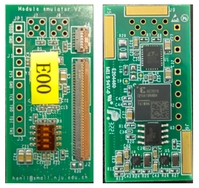
The MUX64 is wrapped in the socked and its pins are routed to the connectors on the back side.

### Daughter boards with commercial ASICs

The FPGA daughter board can be used to replace the lpGBT with some related logic implemented inside the FPGA.

The SFP+ daughter board can be used to replace the VTRx+ in case the VTRx+ is in shortage.

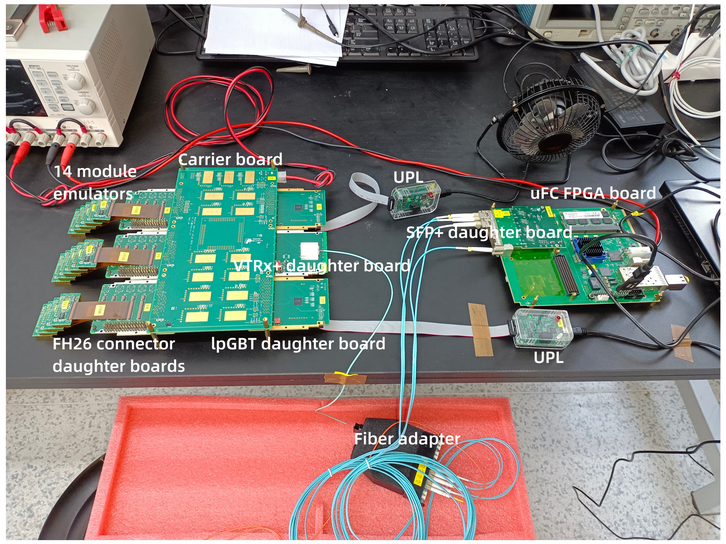
The power block, mounted with a commercial ASIC TPS56428, can replace the bPOL12V.



The module emulator can mimic the module both in dimension and functionality if some related logics are implemented in the FPGA located on the back of the board.

## Joint test

### PEB emulator system setup



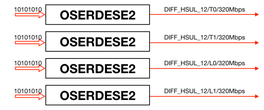

In the setup, all the boards are integrated together into a functional system.

- At the leftmost part, 14 module emulators are connected to the carrier board through the flat cable and the FH26 connector daughter boards.
- On the carrier board, 15 power blocks are mounted on the back side to provide power for this system. As well, 2 lpGBT daughter boards are plugged to respectively process the Lumi data and time data from module emulator.
- The VTRx+ daughter board is also plugged in the carrier board to transfer the data from both lpGBTs into optical signal. Then a fiber adapter is used to adapt the 5 MT-terminated fibers of VTRx+ to 5 LC-terminated fibers.
- A microTCA board uFC is used to do the data acquisition. It is a FPGA-based board where the lpGBT backend counterpart logic can be implemented to decode data from the lpGBTs.
- The 2 lpGBTs are configured with 2 programming boards UPL, which is a dedicated board for lpGBT configuration.

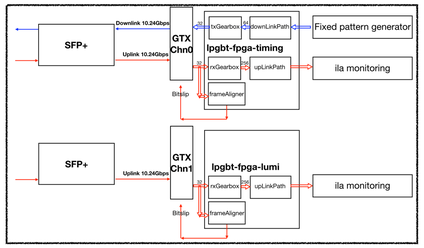
### Firmware

Firmware should be prepared for both the module emulator and the microTCA DAQ board.

- Firmware on module emulator can generate pseudo signals (fixed pattern) with a specific transmission speed.



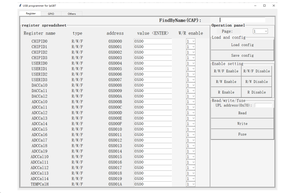

- Firmware on microTCA DAQ board is mainly used to decode and monitor the data from lpGBT.




### lpGBT configuration

Dedicated configuration toolkit was developed to configure the lpGBT through its I2C slave interface. The toolkit includes:

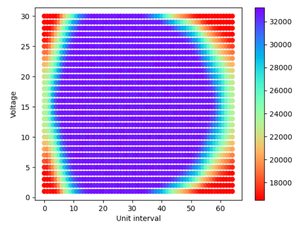
- A programmer board UPL
- Graphic user interface(GUI)
- Configuration with script is also available



### Results

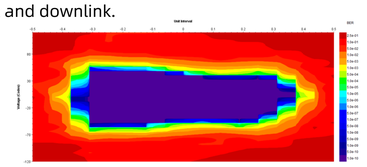
With the PEB emulator system setup, many features of lpGBT are configured and tested. The time lpGBT is configured as a transceiver while the lumi lpGBT is configured as a simplex transmitter.

- All the 28 uplink ePorts are enabled for both the time and lumi lpGBT and work at the speed of 320Mbps. They are all stable after setting the pre-emphasis of the high speed output
- The time lpGBT distributes 14 40MHz clocks to the 14 module emulators. They are all stable after increasing the drive strength of the eLink clocks.
- The 40MHz reference clock of lumi lpGBT comes from the phase shifter clock of the time lpGBT. It stays stable.
- The ADCs and GPIOs are configured and tested as expected. The ADC needs calibration in the future.

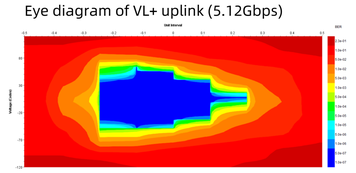



Eye diagram of VL+ downlink (2.56Gbps) measured by the EOM circuit of lpGBT

The versatile link (lpGBT + VTRX+) transmission was also tested in the case of uplink and downlink.



Eye diagram of VL+ uplink (5.12Gbps)



Eye diagram of VL+ uplink (10.24Gbps)

## Conclusion

The PEB emulator system is a simplified version of the future PEB prototype to help us verify many important factors in advance. The system was set up and communication from module emulator up to the DAQ FPGA board was successful established, many features of lpGBT were successfully configured and tested, which indicates that the hardware design and production, lpGBT configuration, versatile link are quite reliable. The system will be integrated into cooling plate for further test. The experience we got from the PEB emulator system will help us have a better and effective design for the PEB prototype. It is worth mentioning that, the PEB emulator system can serve as a platform for many other related tests, such as module tests, bPOL12V power block noise test, power consumption estimation, and etc.