Fast Timing Readout Electronic based on PETIROC ASIC

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Abstract

Semi-Digital Hadron Calorimeter (SDHCAL) prototype for CEPC is a PFA-based hadron calorimeter which has showed good energy and position resolution with CERN test beam. Considering signal time of hadronic shower formed by neutrons is delayed, comparing with that from charged hadrons, high-precision time measurement, requiring at least 100ps orders, helps improve separation between neutrons and charged hadrons and further improve the jet energy resolution.The readout electronics with four PETIROC ASIC chips have been designed to validate the high time resolution with $tens\ of\ ps$.

Keywords: CEPC, SDHCAL, PETIROC, ASIC, High Time Resolution.

Motivation, Targets & Methods

Motivation: CEPC, *Higgs factory*, was proposed to measure the Higgs properties with unprecedented precision and the largest ratio for Higgs decay into hadron final states. The design of high-performance hadron calorimeter is crucial, one of which is SDHCAL based on Glass Resistive Plate Chamber (GRPC) has achieved good energy and position resolution with CERN test beam. With **at least 100ps orders** as shown in Fig 1, it could improve separation between neutrons and charged hadrons and further promote the jet energy resolution.

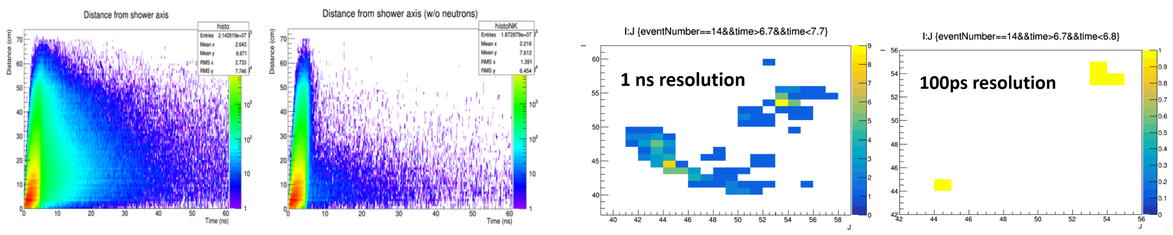
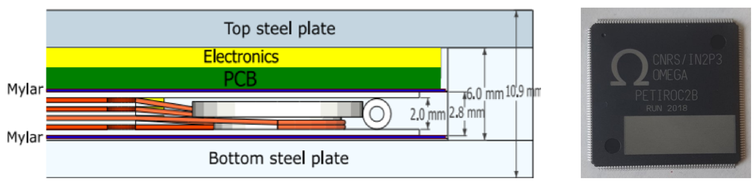


Figure 1: With and without neutrons(left two) and shower separations under 1ns or 100ps(right two).

- ***Timing information could be:***
- An important factor to identify delayed neutron and better reconstruct their energy.
- Conducive to separate close by showers to reduce the confusion for a better PFA application.



- With multigap RPC (MRPCs) with a time resolution better than 60 ps.
- Petiroc ASICs with a Jitter<20ps RMS from OMEGA (Collaborator) applied.

References

[1] Liu Z. et al. Timing performance study of multigap resistive plate chamber with different gap size. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 927:396–400, 2019.

[2] https://www.weeroc.com/products/sipm-read-out/petiroc-2a.

Hardware & Firmware

- ***Hardware:***
- FEB prototype containing four ASIC chips and 128 readout pads at the PCB bottom side with the blind/buried via technology.
- DIF card designed to power supply and clock jitter for FEB and the communication between FEB and FPGA.
- Xilinx ZCU102 FPGA integrated with programmable logic (PL) and ARM processing system (PS) is used to implement DAQ system including Petiroc2B configuration and data transmission with the Ethernet.

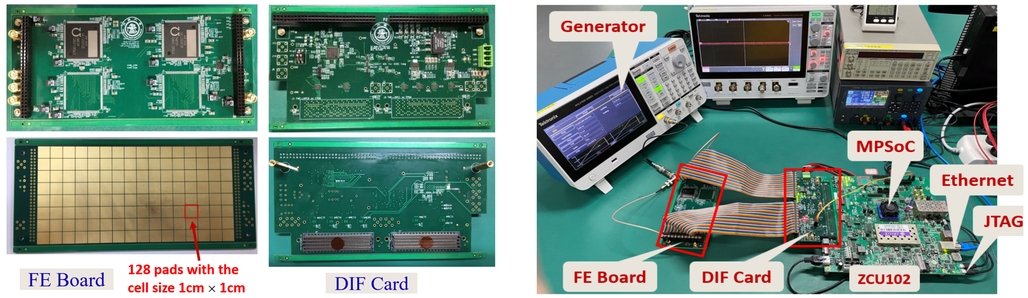


Figure 2: Hardware: Front-End Board, Detector Interface Card and signal injection test setup (right).

Firmware: DAQ is developed by the embedded design that incorporates firmware on PL and software on PS.The Ethernet communication programmed on Vitis and the PC host designed by QT Creator application, which are still ongoing promoted. The signal injection setup has been built. Data can be taken from the FEB through the injected signal.

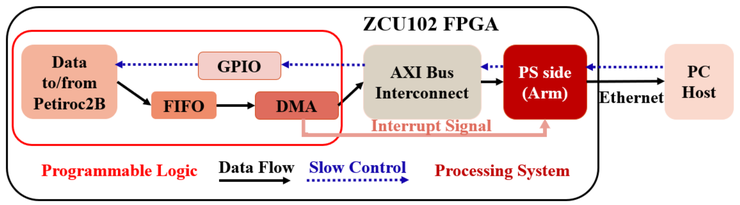


Figure 3: Block diagram of DAQ system

Test, Results & Future Plans

- The design of FEE prototype and DIF card with FMC have been finished.
- DAQ finished to design including the daisy-chain configuration of Petiroc2B by checking time and charge threshold.
- Output data taken by injecting one signal from the generator,and the preliminary time measurement is hundreds of ns due to larger noises.

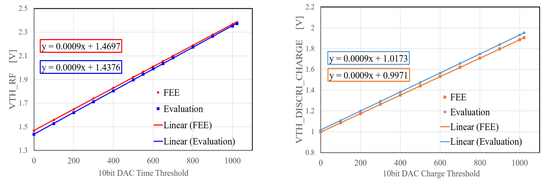


Figure 4: 10-bit time and charge threshold DAC.

- Decrease the noise level in the next future.
- Perform precise time measurement.