Status of LHCb Upstream Tracker

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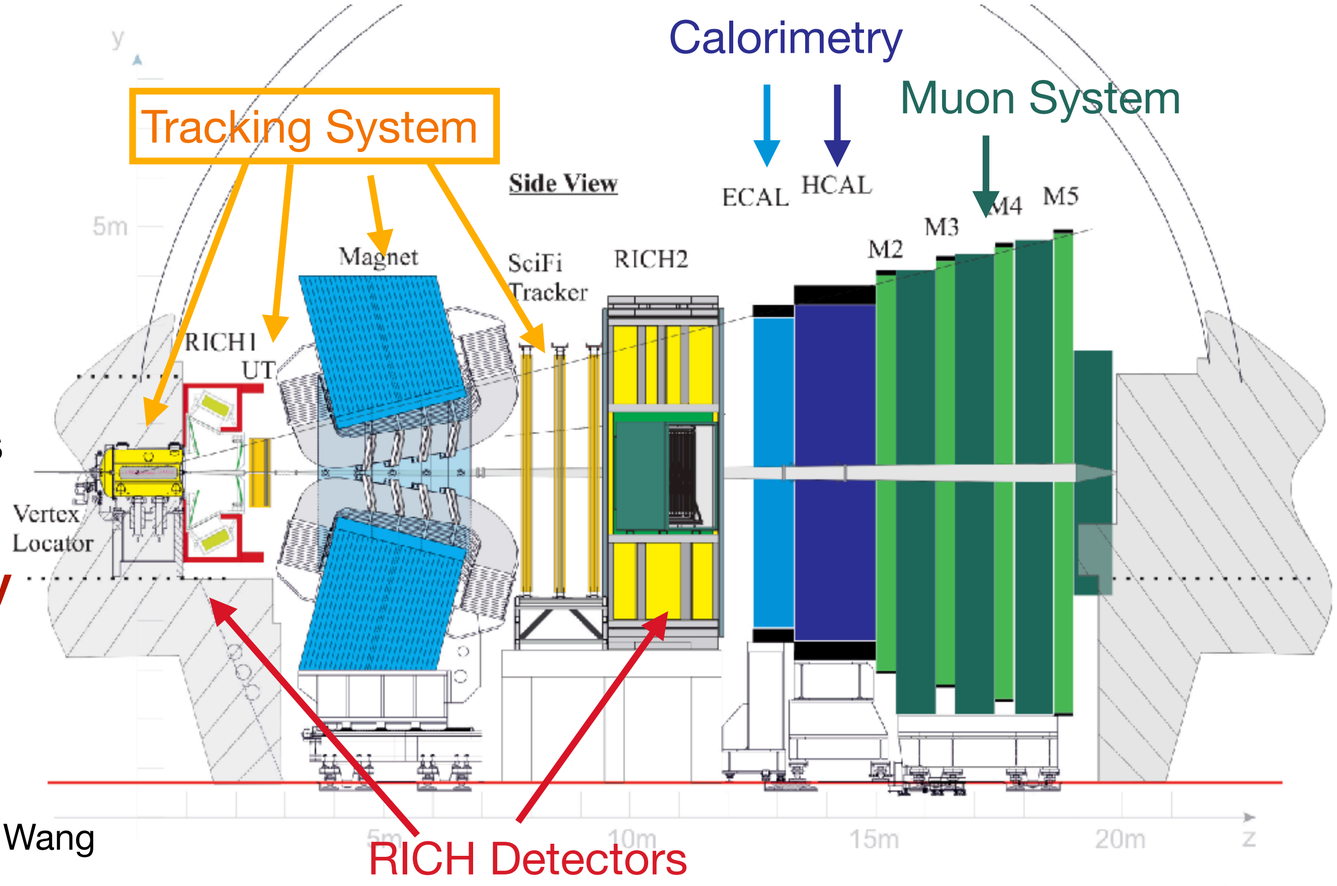
中国科学院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

LHCb Upgrade I

➢ LHCb Phase-I upgrade during LS2:

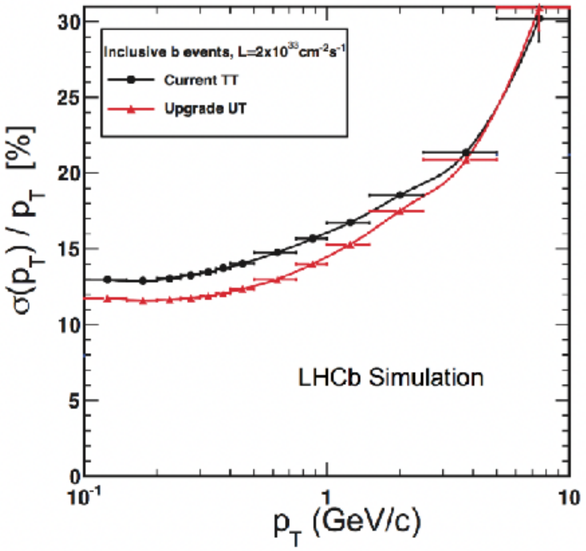
- ❑ $\mathcal{L} = 2 \times 10^{33} cm^{-2} s^{-1}$, **5 times higher** than run1&2, expected $\mathcal{L}_{int} = 50 fb^{-1}$
- ❑ Replacing with **new tracking detectors**; at least upgrade electronics for other sub-dectectors
- ❑ New electronics with **40MHz** readout, **software-only trigger**

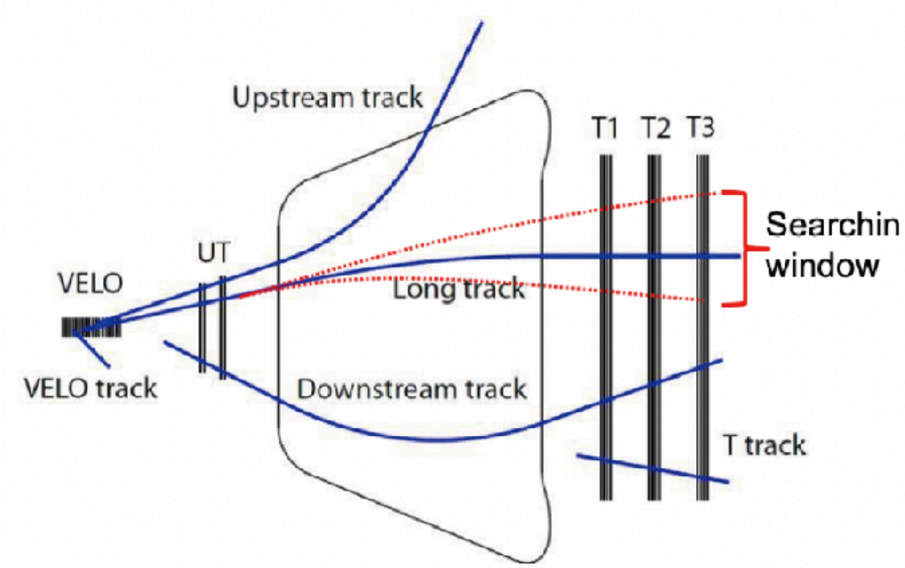


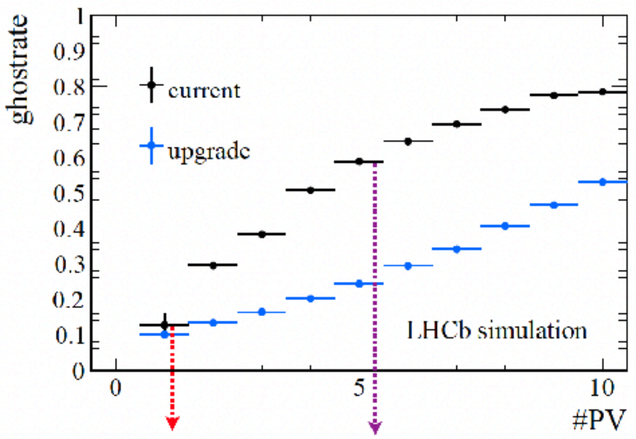
For general LHCb Upgrade, please see the plenary talk by Professor Jike Wang
For UT front end ASIC study, please see the presentation by Shuaiyi Liu

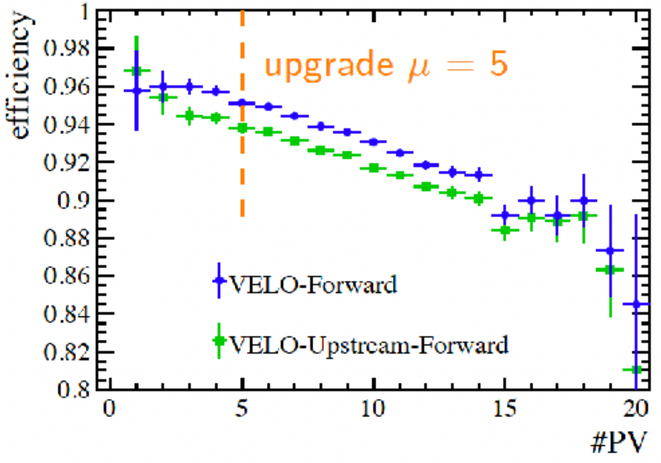
Role of UT in Tracking

- Provide **fast track reconstruction** to speed up trigger decision
  - Tighten searching window in SciFi
  - Charge determination
- Reduce **ghost rate** in long tracks
- Improve **momentum resolution**
- Increase **reconstruction efficiency** of long lived particles: e.g. K_S^0



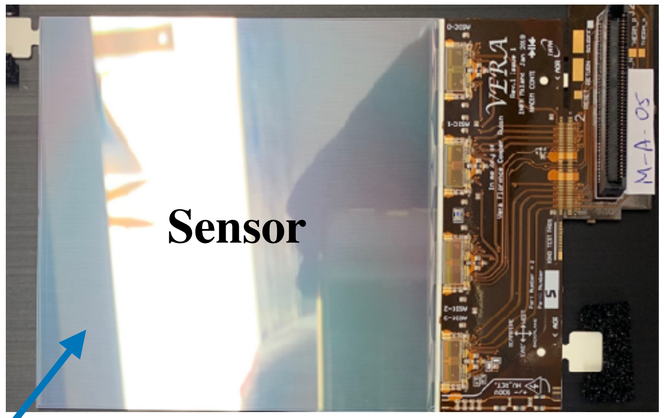


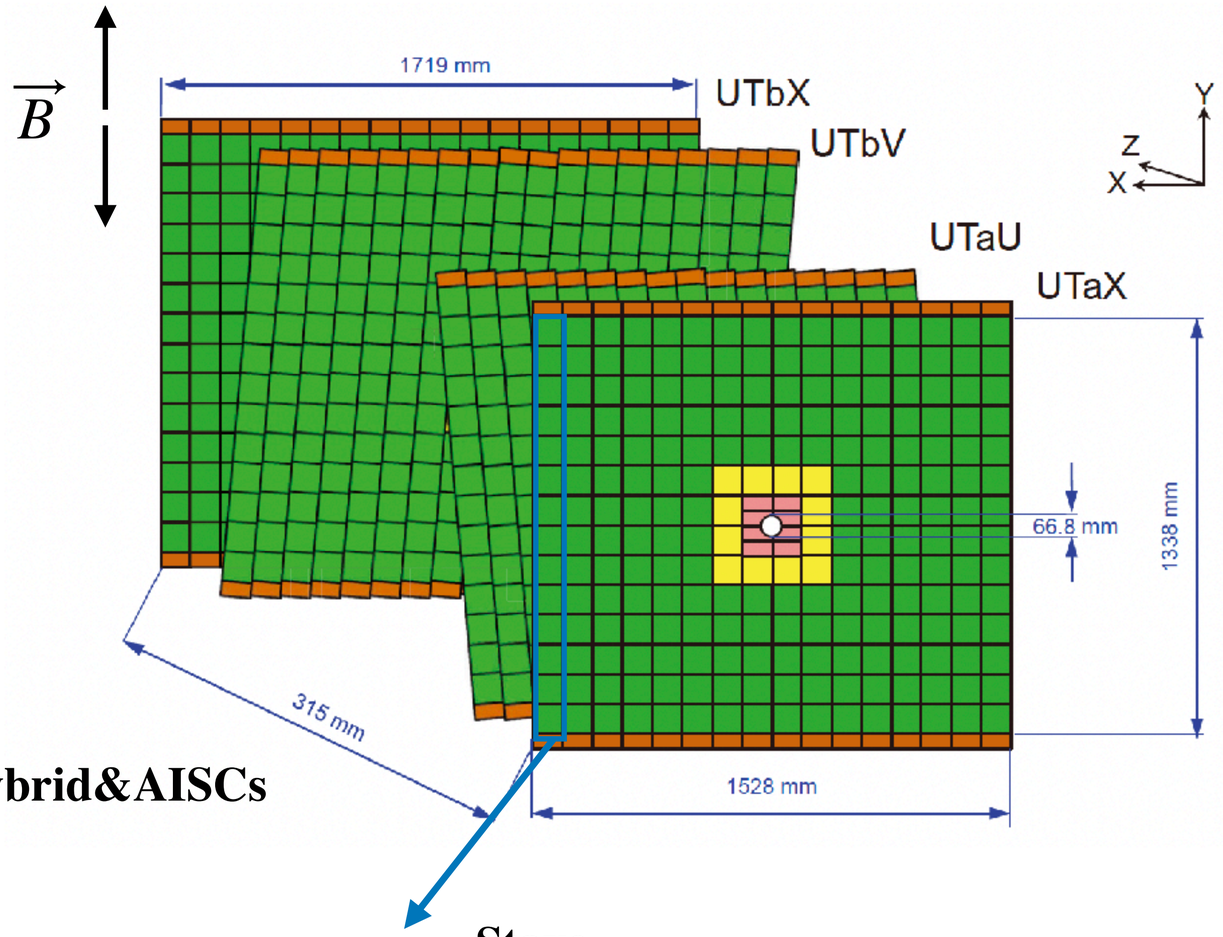




UT overview

- **4 planes** of silicon strips (X,U,V,X)@(0˚,5˚,-5˚,0˚), providing stereo measurements
- **16/16/18/18 staves** for layer (X,U,V,X)
- **Modules** mounted on both sides of the stave
- Improved features comparing to previous TT
  - **More radiation resilience for sensors**
  - **Larger coverage**
  - **Finer granularity**

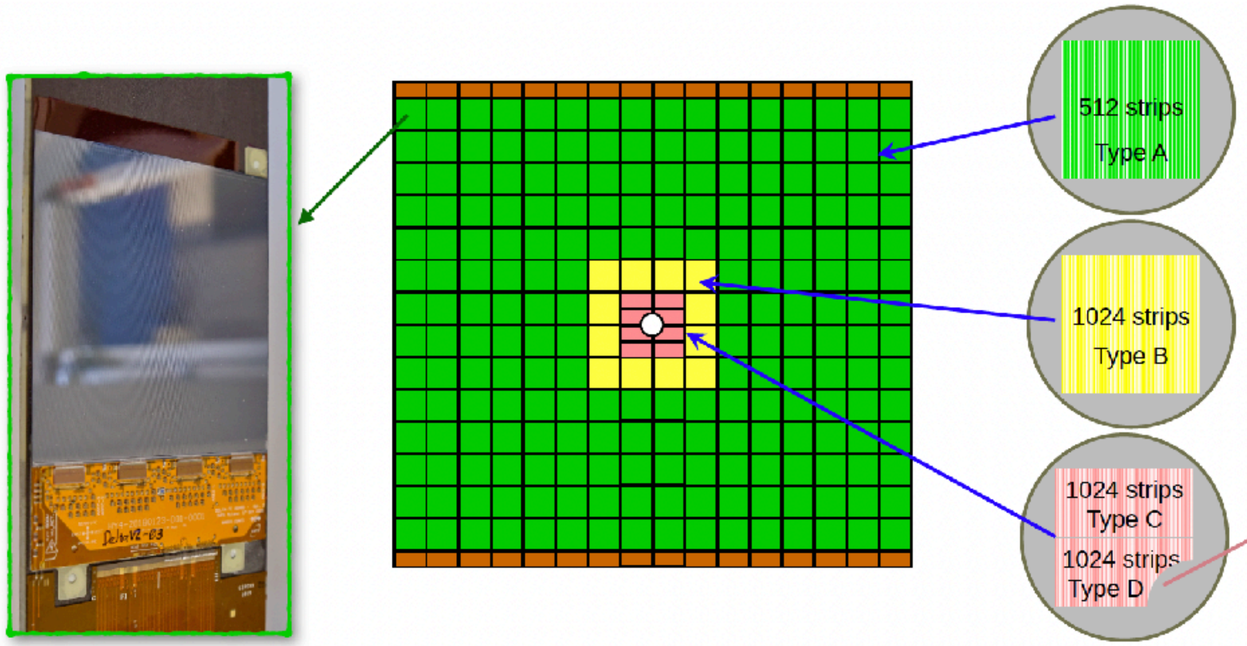


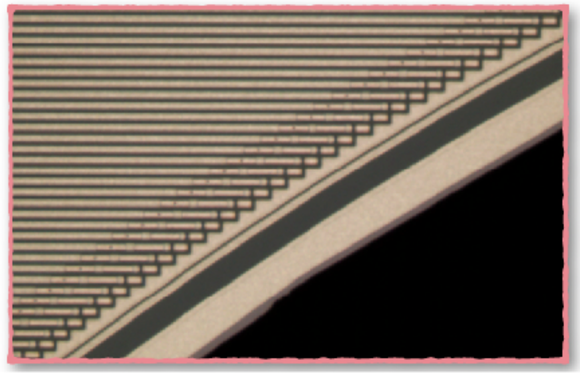


Silicon Sensors

Sensors	Type	Pitch/μm	Length/mm	#Strips	#sensors
A	p-in-n	187.5	99.5	512	888
B	n-in-p	93.5	99.5	1024	48
C	n-in-p	93.5	50	1024	16
D	n-in-p	93.5	50	1024	16

- **Four types** of the silicon sensors, 968 in total.
- **Finer granularity** and **radiation hardness** in inner-most region
  - ❑ Outer region with p-in-n,187.5μm pitch, cost effective
  - ❑ Inner region with n-in-p, 93.5μm pitch, radiation-hard

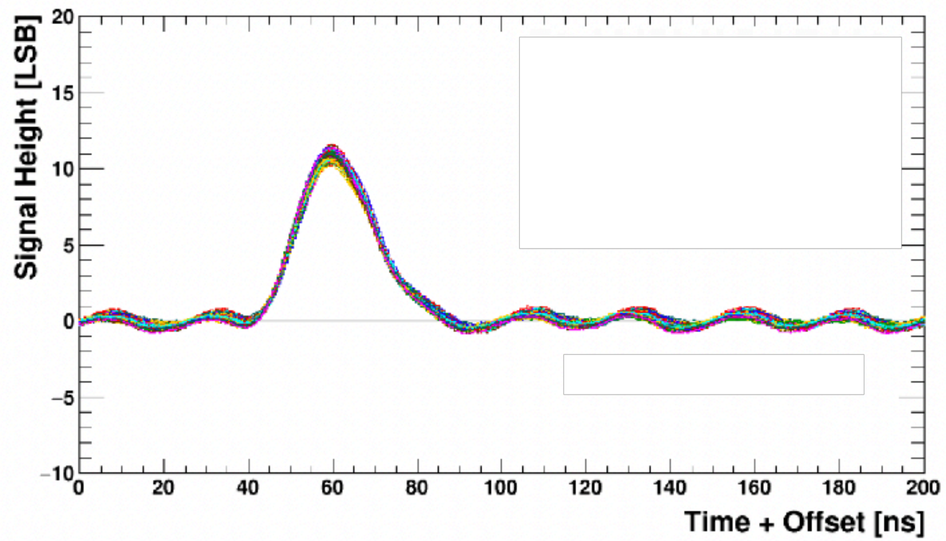


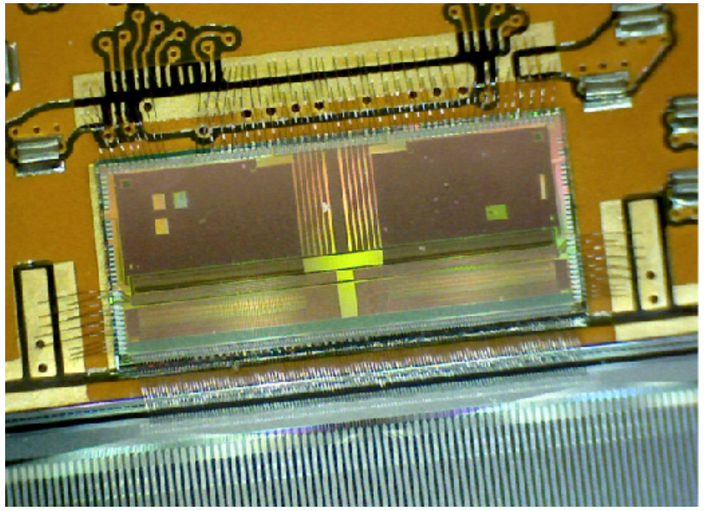


Circular cutout near the beamline

SALT: Silicon ASIC for LHCb Tracking

- **128 channels** with 6-bit ADC (1-bit for polarity), **40MHz** readout, **4192 ASICs** in total
- Wire-bonded to the sensor
- Fast shaping time/return to baseline
  - T_{peak} ≦25 ns, less than 5% after 2 T_{peak}





- DSP[1] features
  - Per channel TrimDAC correction
  - Pedestal and common mode subtraction
  - Zero suppression
  - Data formatting…

[1] DSP: Digital Signal Processing

Sensor & ASIC combined test

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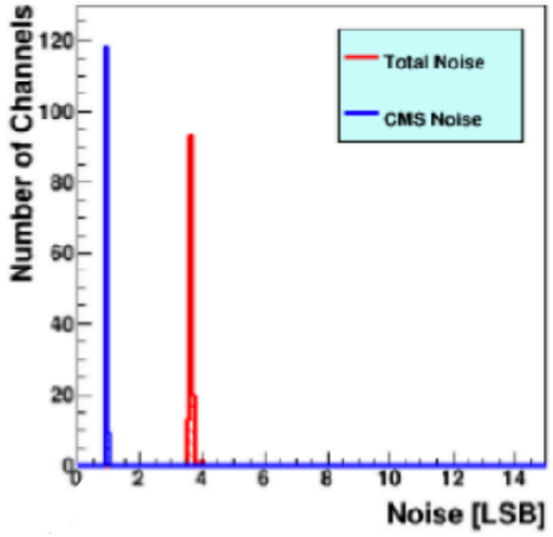
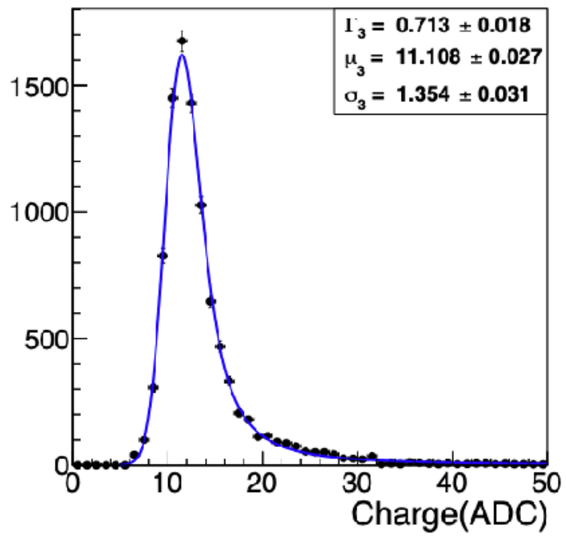
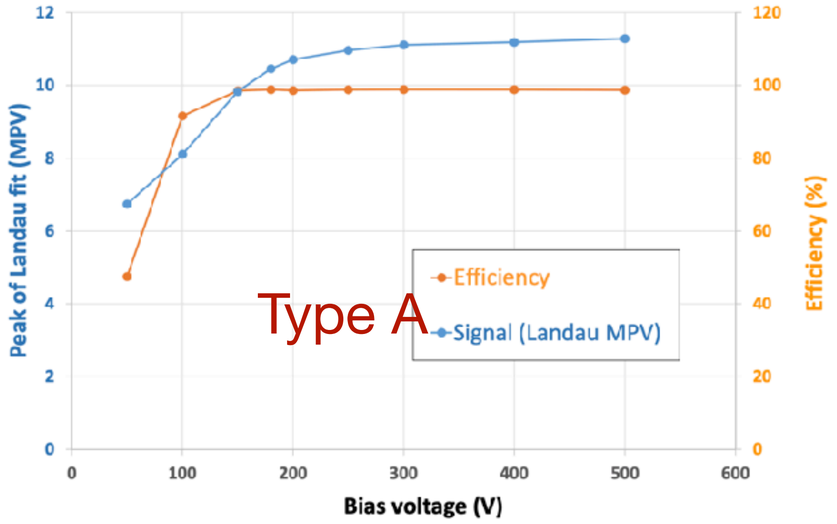
➢ Beam test at Fermilab in March 2019

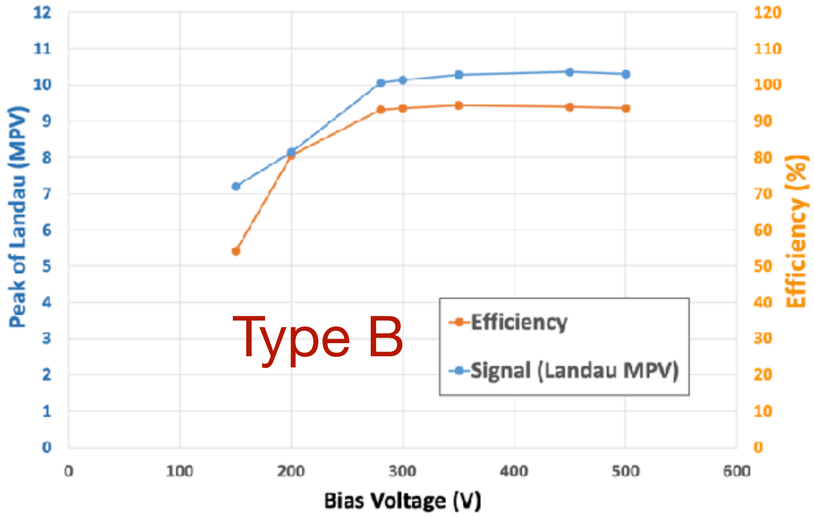
- ❑ Type A unirradiated sensor: **99.5%** efficiency and **S/N~12**
- ❑ Type B sensor irradiated to 2x maximum dose, **94%** efficiency and **S/N~11**, partially due to readout limitation

Final system expected to have single-hit **high efficiency (> 99%)** and **good signal-to-noise ratio** throughout experiment lifetime



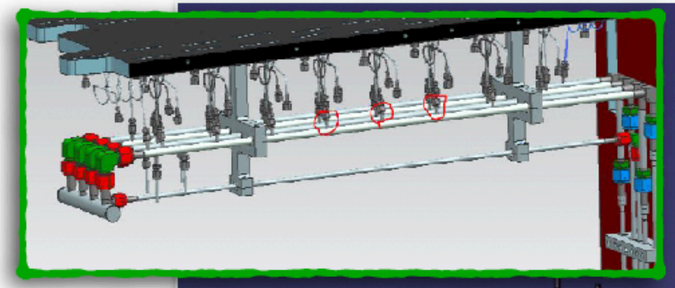






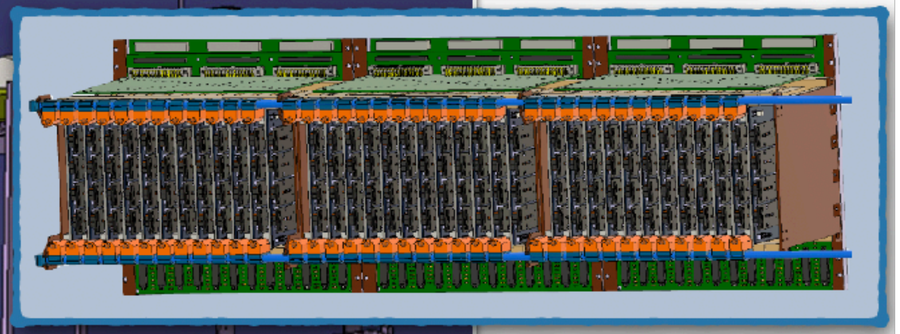
M. Artuso et al, "First Beam Test of UT Sensors with the SALT 3.0 Readout ASIC" (2019) DOI:10.2172/1568842

UT integration



Staves cooled by **CO_2**, tested between -30° and 20°

PEPI cooled by **water**, boxes sit directly on top and below staves



PEPI boxes

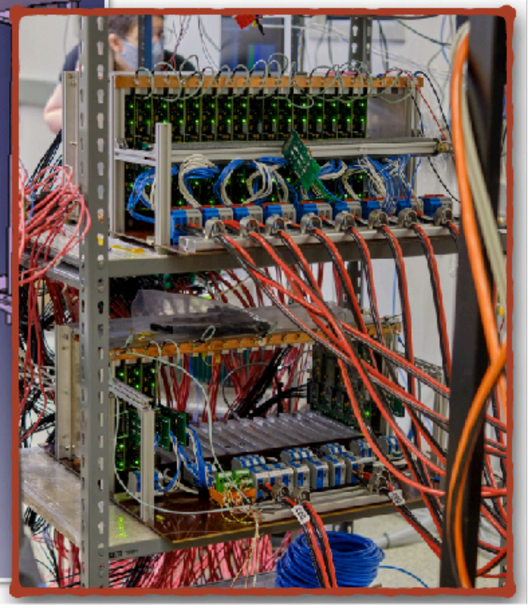
UT Box

Rails

Cable chains

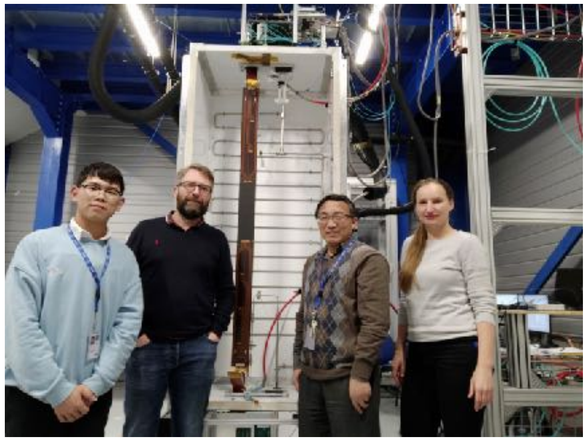
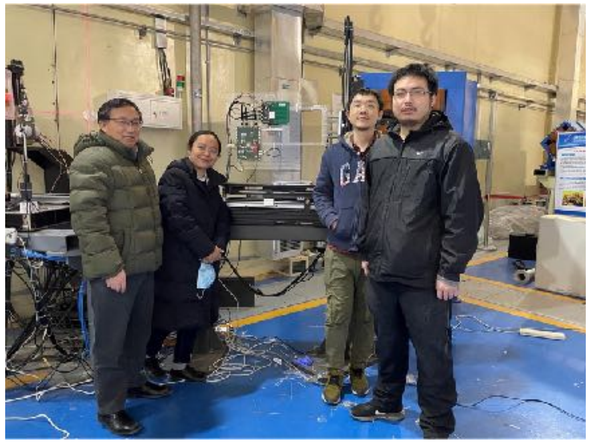
Service Bays

LV and **HV** regulation at the service bays



Chinese members contributing to UT

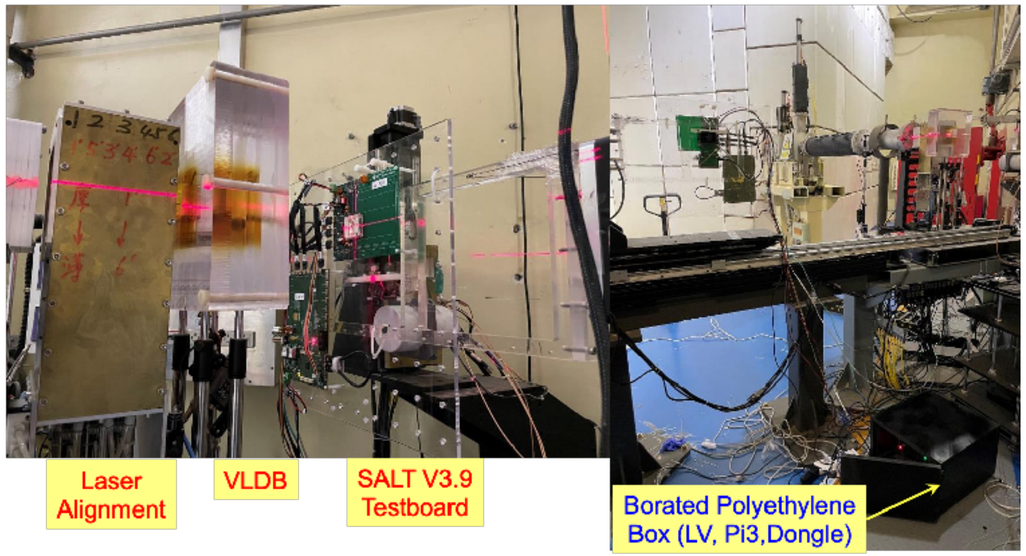
- **3 staff:** Jianchun Wang, Yiming Li, Shanzhen Chen
- **2 visiting scientists:** Mark Tobin, Petr Gorbounov
- **4 postdocs:** Nathan Grieser, Yu Lu, Ina Carli, Baasansuren Batsukh
- **PhD students:** Quan Zou, Shuaiyi Liu, Shuqi Sheng, Xiaojie Jiang, Zan Ren*, Feihao Zhang**, Bo Chen**

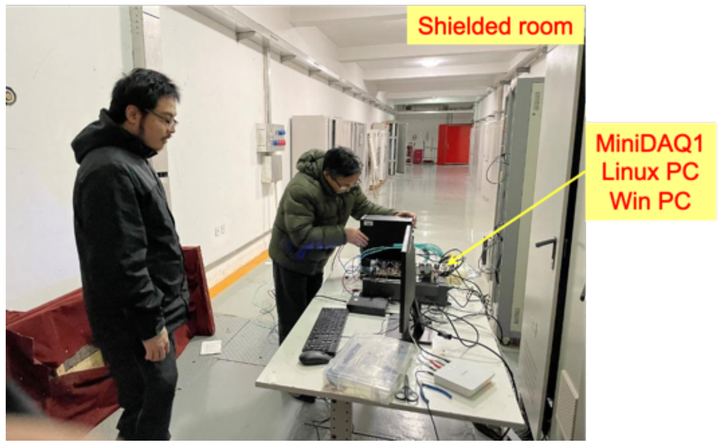



* Tsinghua University
** Hunan University

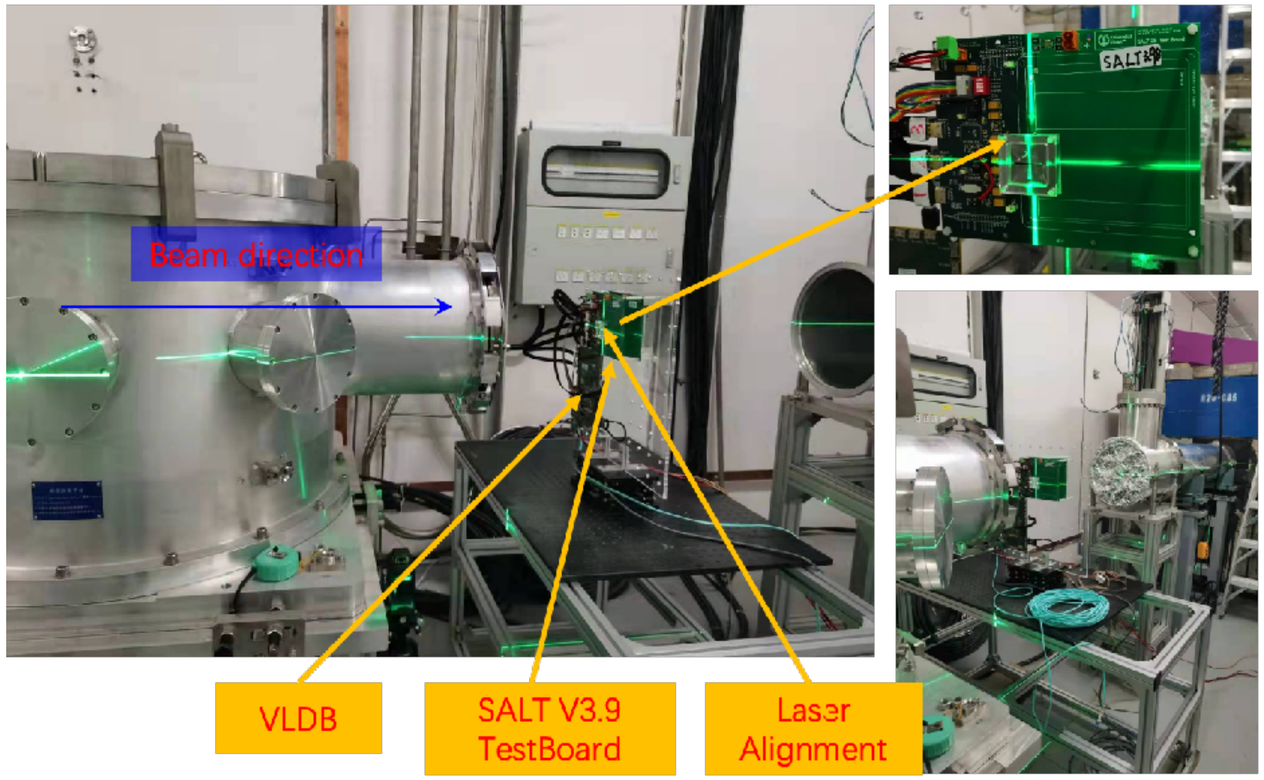
Beam test

- At CIAE (China Institute of Atomic Energy) Beijing, in December 2020
- At CSNS (China Spallation Neutron Source) Dongguan, in October 2021





At CIAE



At CSNS

For more details, see Shuaiyi's talk

ECS[1] & DSS[2] development

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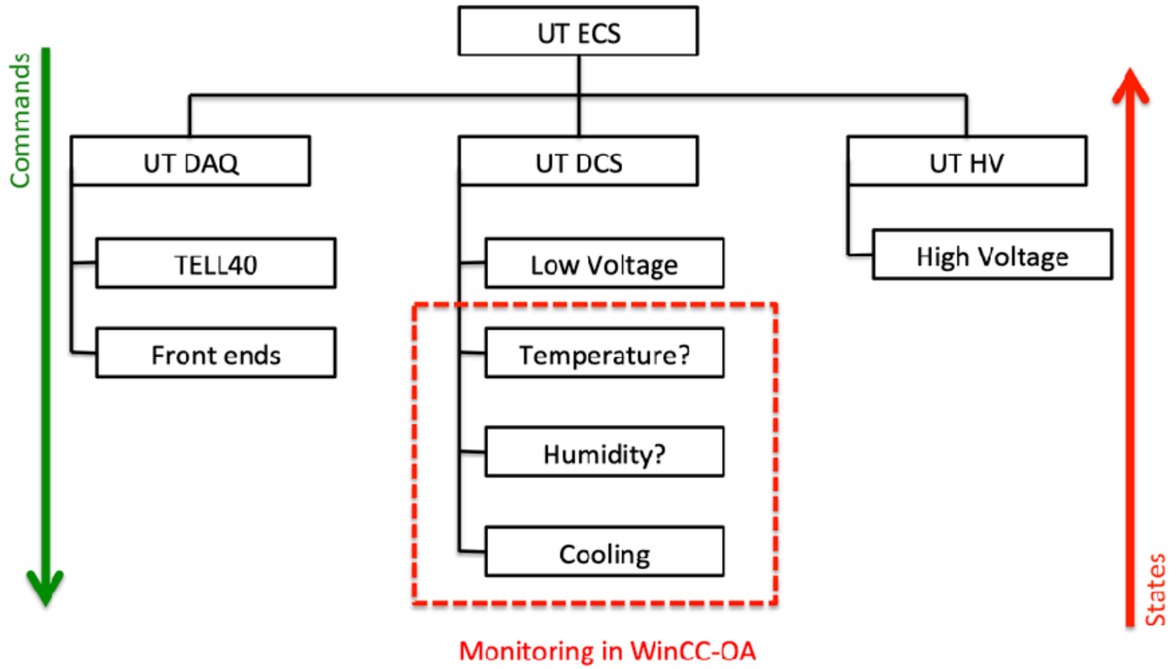
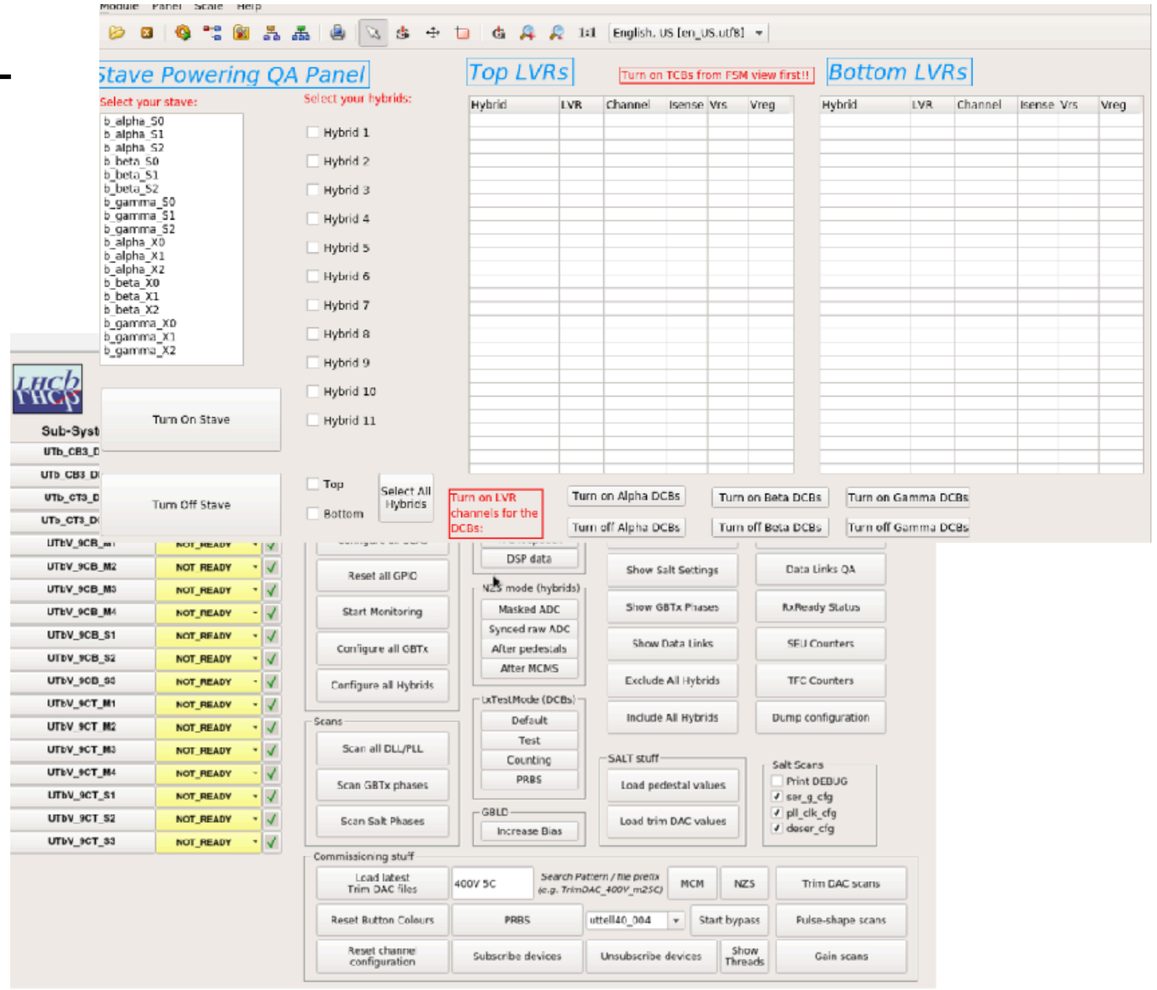
- Developing control system for slice test
- Developing DAQ and control system for final UT



LV QA panel for slice test



DCBs&hybrids configuration

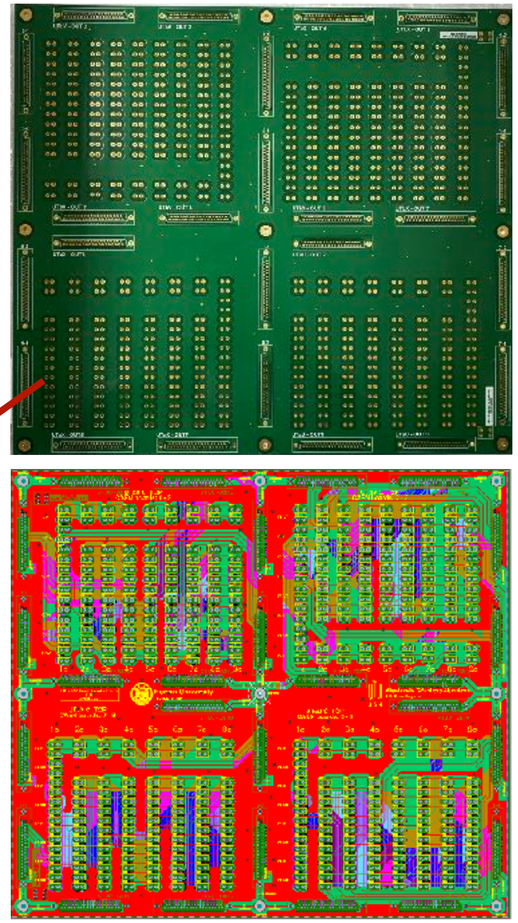
[1] ECS: Experiment Control System
[2] DSS: Detector Safety System

Panel Design

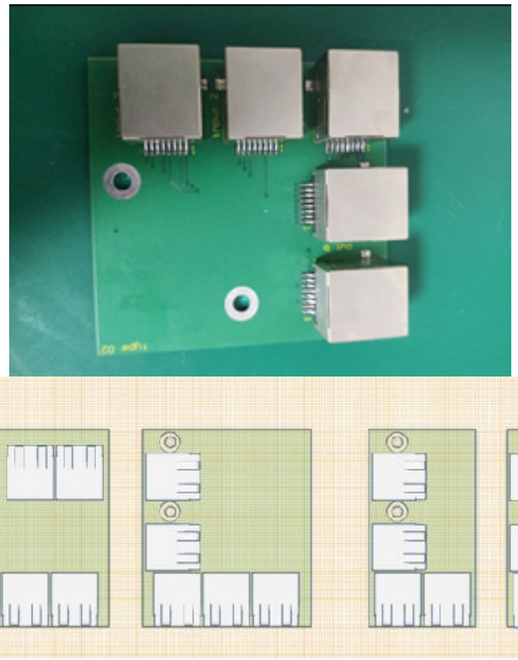
- HV patch panel in D3 region
- LV spliter in SBC region

HV power supply in D3 region

HV patch panel



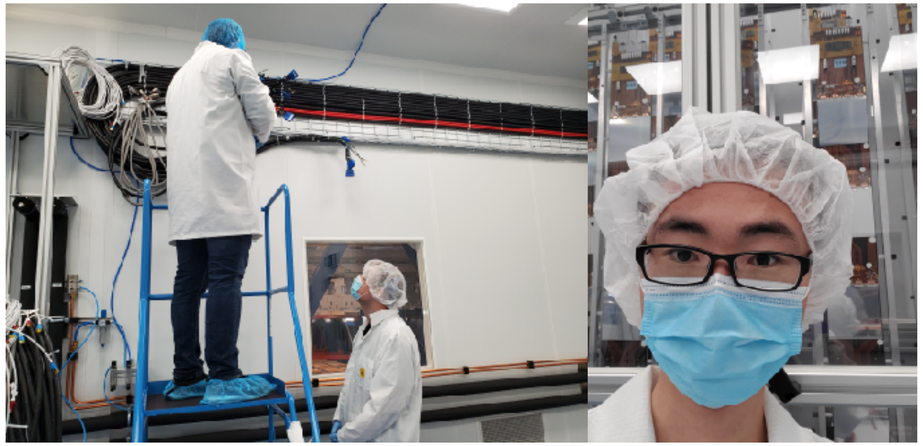
LV spliter in SBC region

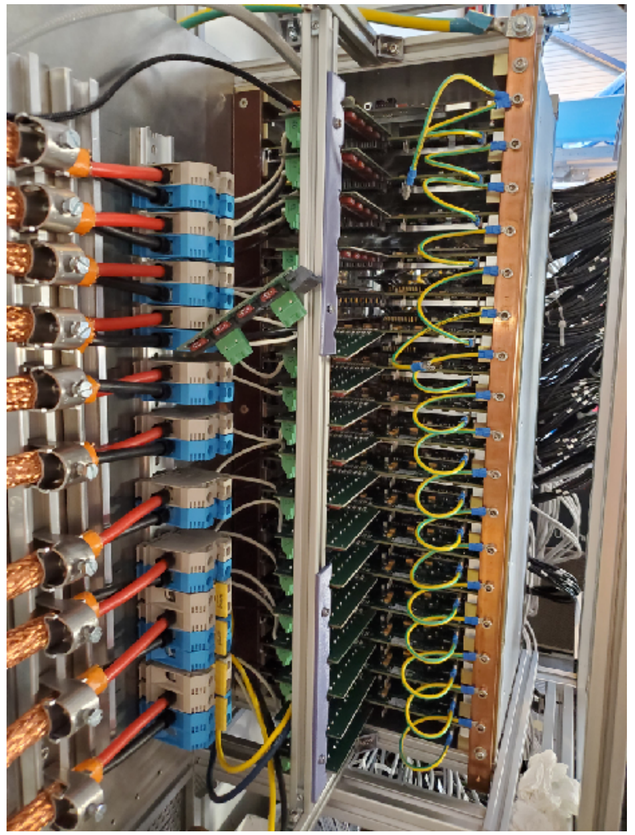


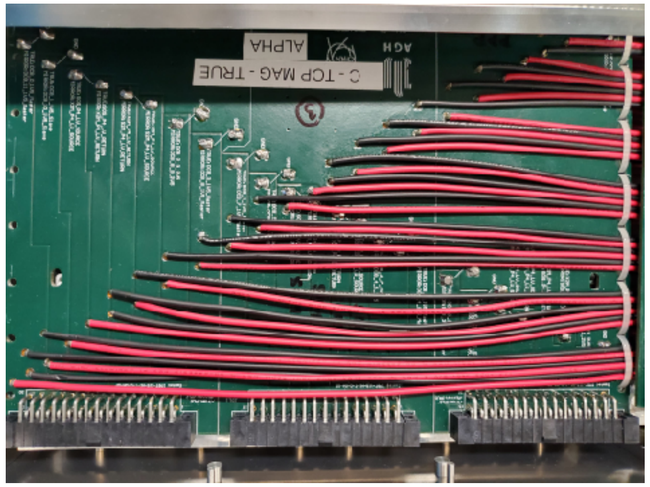
@Designed and produced by the HNU group

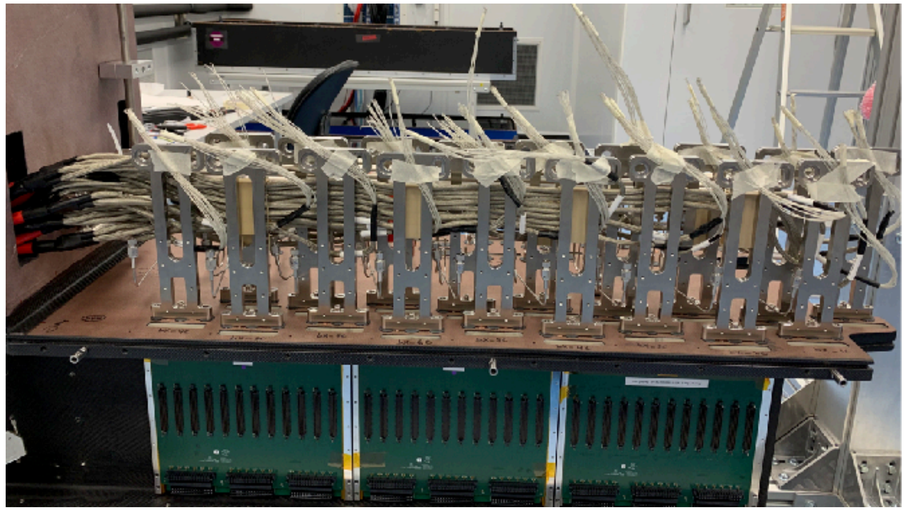
UT installation preparation

- Infrastructure preparation:cabling, soldering, splicing and mechanical tests



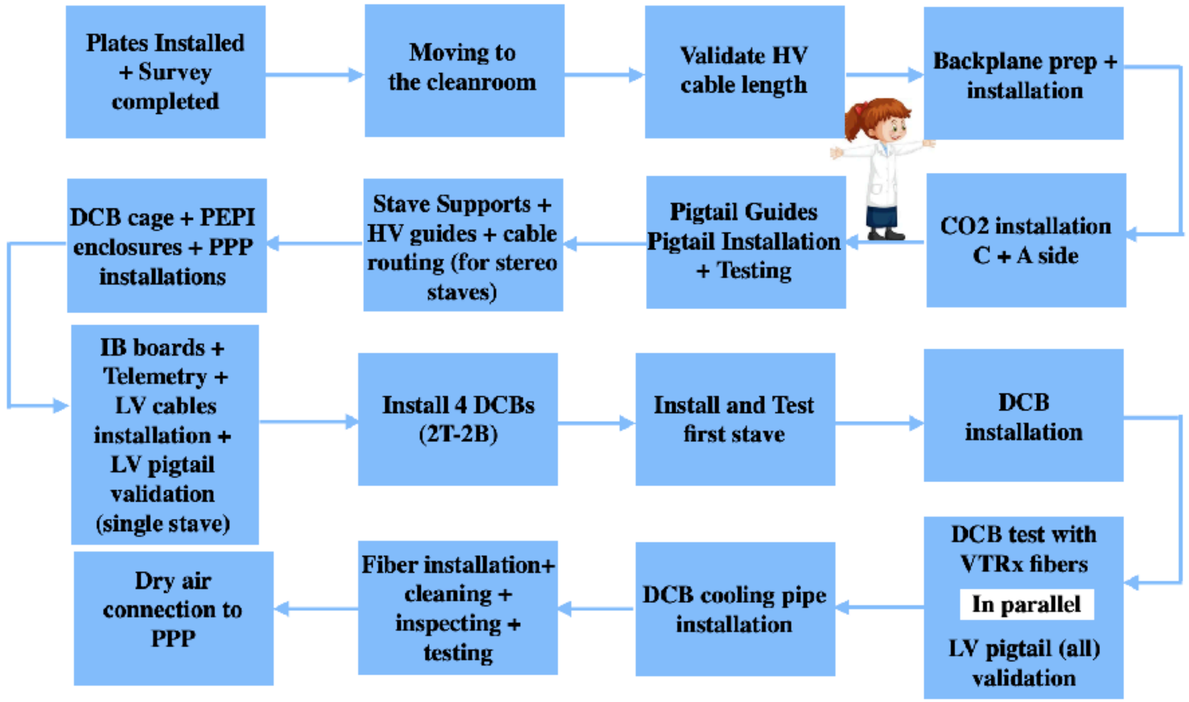




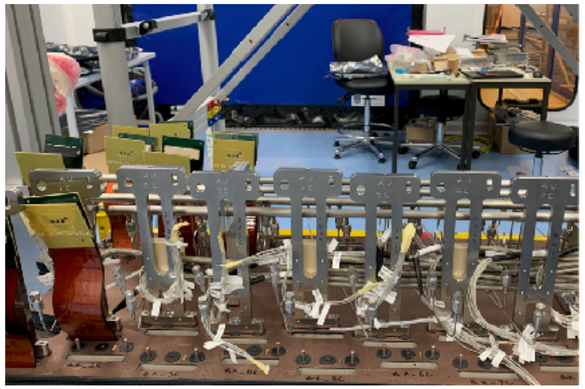


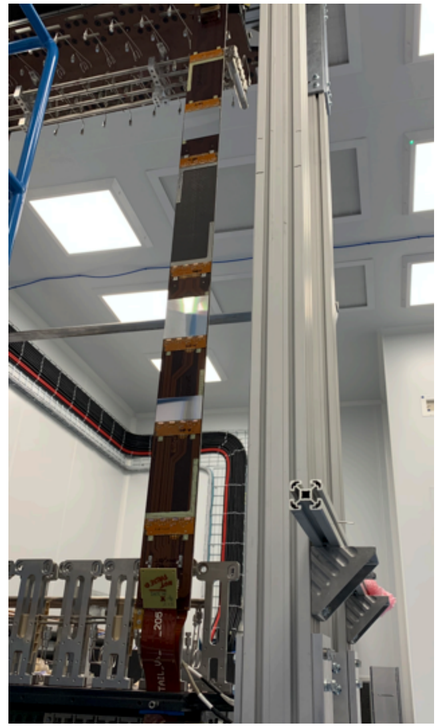
Status at CERN

- Most of the key infrastructures (LV, HV routing) have been processing well
- **25 staves** arrived at CERN (out of 68)
- Finished the essential DAQ and control system for surface test



@Dimitra





Summary

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  - $\mathcal{L} = 2 \times 10^{33} cm^{-2} s^{-1}$, $\mathcal{L}_{int}$= 50fb^{-1}, 40MHz readout with software-only trigger
  - UT: a new silicon strip detector is being constructed, as a key component of U1 tracking system
- Chinese members have made significant contributions in many fields
- The installation of UT is in critical period now

Thanks for your attention!