Radiation Study of the LHCb UT Readout ASIC

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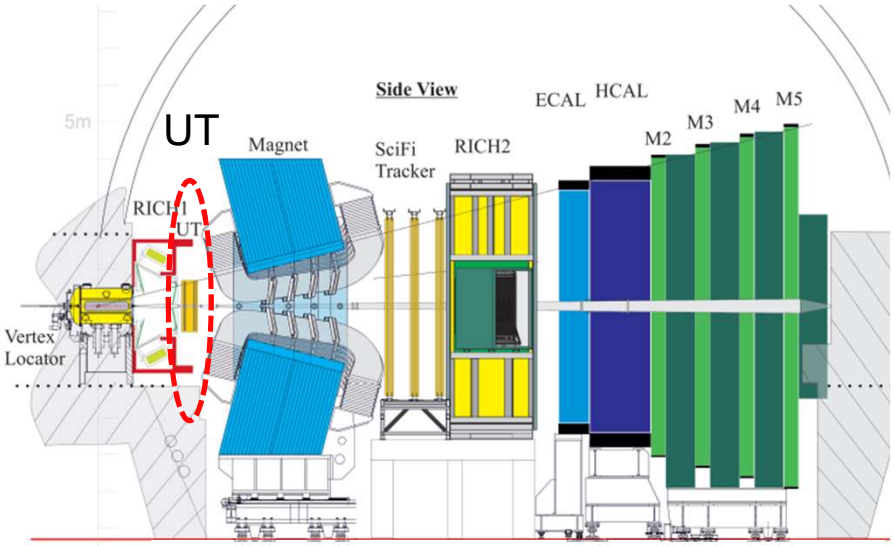
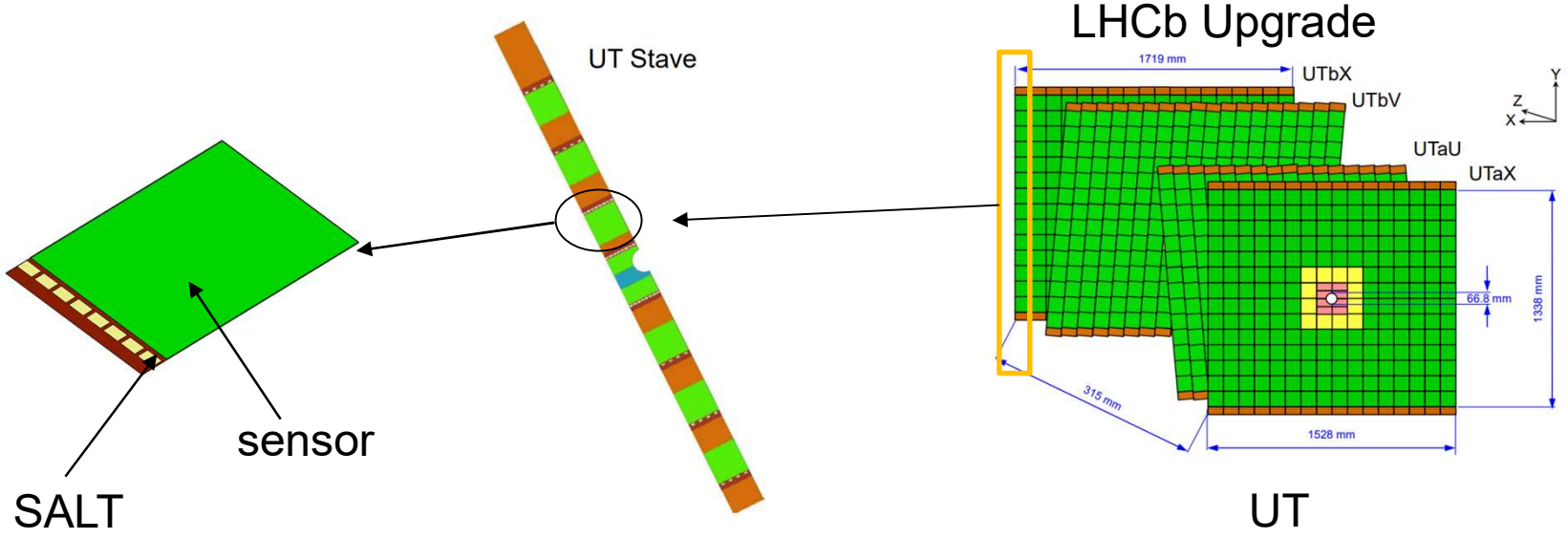
Introduction

- UT(upstream tracker) is a new silicon tracker in LHCb upgrade to replace the old tracker TT.
- It has 4 layers, each layer consists of 16/18 staves.
- SALT (Silicon ASIC for LHCb Tracker) is the front end readout ASIC of the UT system.



LHCb Upgrade



For UT installion, please see Quan Zou's presentation
For general LHCb upgrade, please see Professor Jike Wang's presentation

Motivation of radiation test

- SALT V3.5 is vulnerable to radiation in its TrimDAC and Pedestal registers.
  - This was first observed at the MGH radiation test on Aug 4th, 2019
  - It was further confirmed at the PSI radiation test on Nov 3rd, 2019.

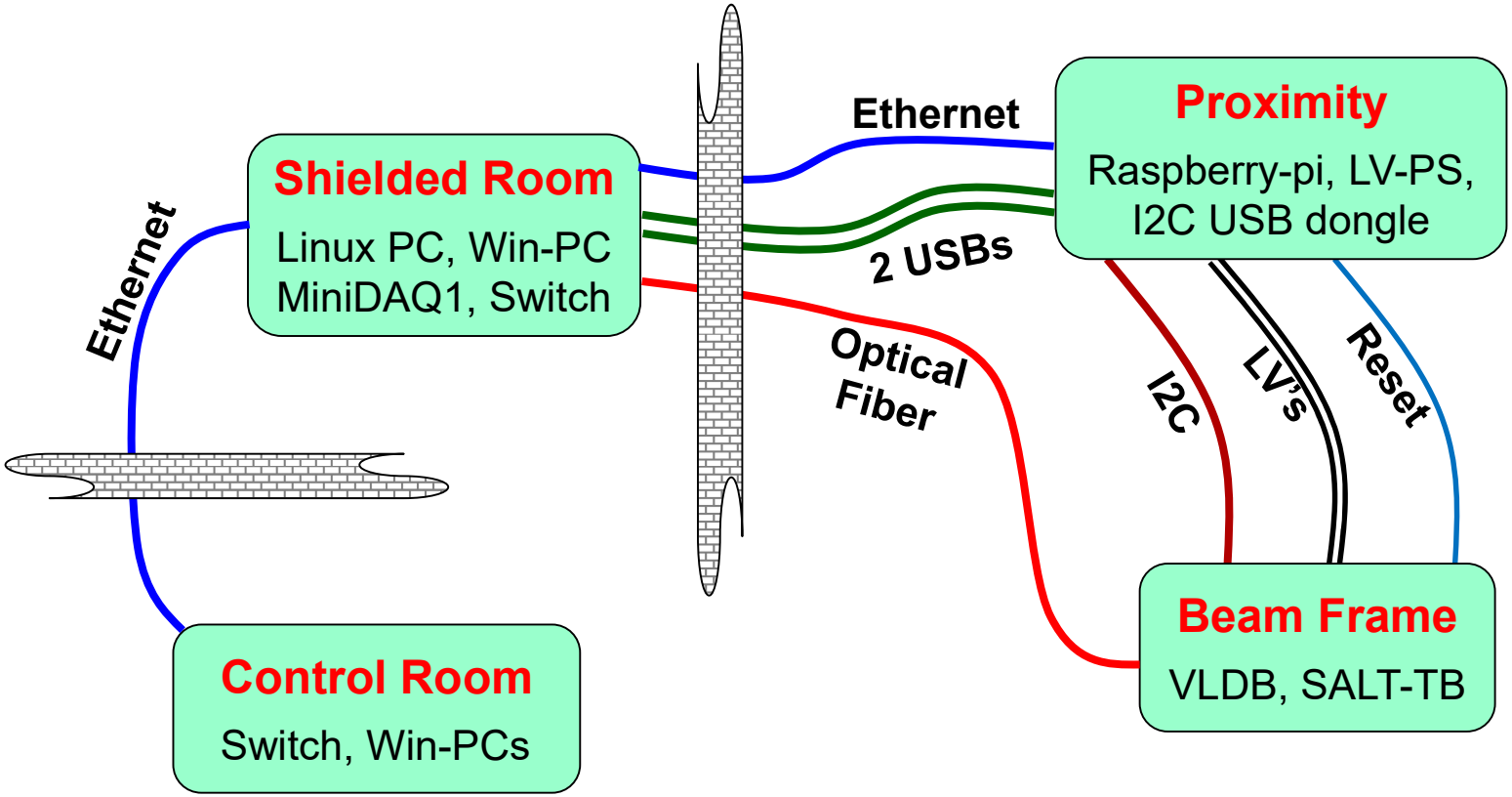
- After careful studies, a possible solution was found and implemented in a new design release, SALT V3.9. It needs to be validated in another test.

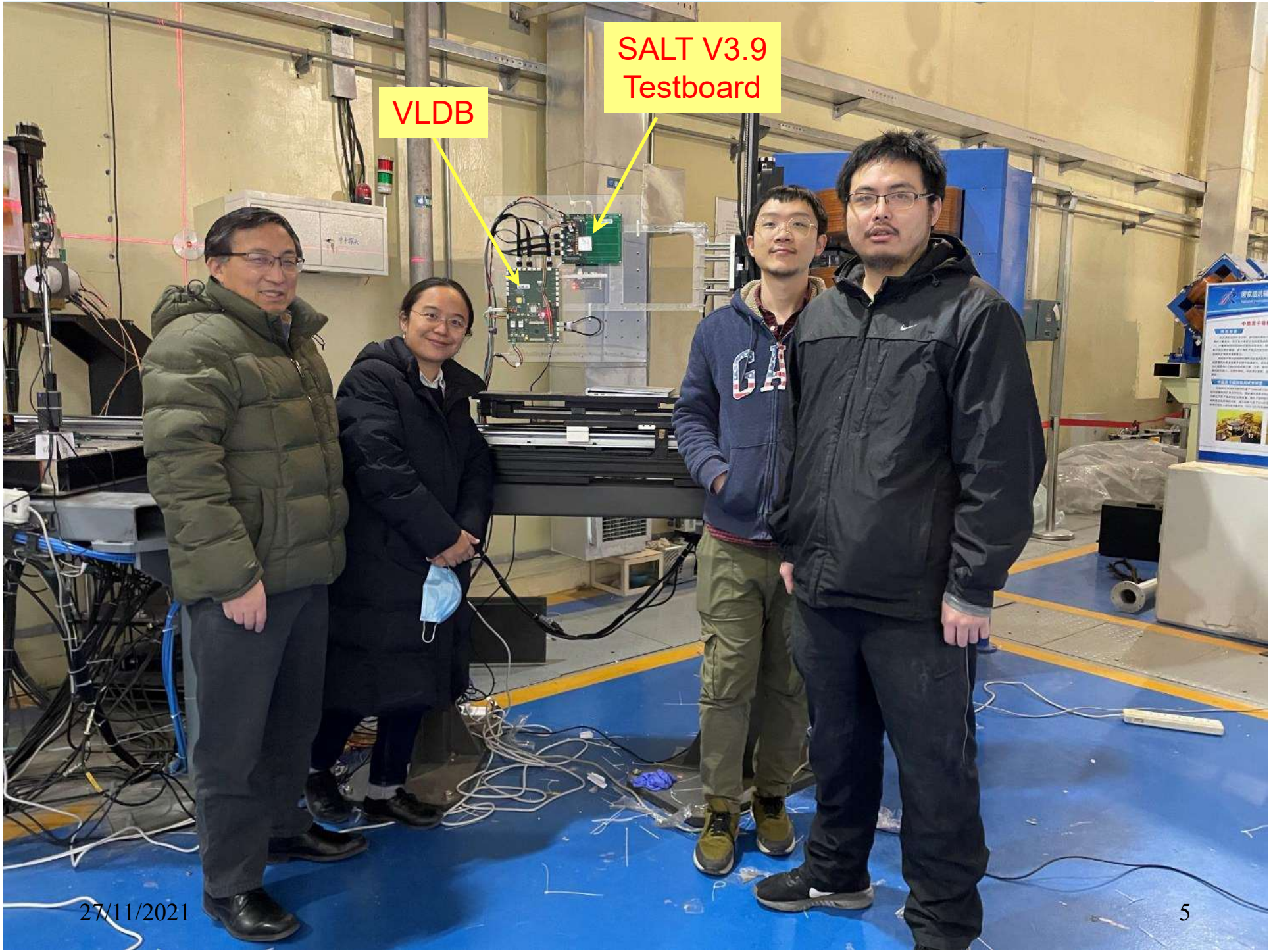
- Many thanks to the CIAE(China Institute of Atomic Energy, 原子能院) folks for squeezing their own test program and arranging one day for us on the last day of 2020.

- We did another beam test in CSNS (China Spallation Neutron Source, 散裂中子源) Dongguan for Memory SEUs(Single Event Upset) on the week of 18th Oct 2021. The data is under analyzing.

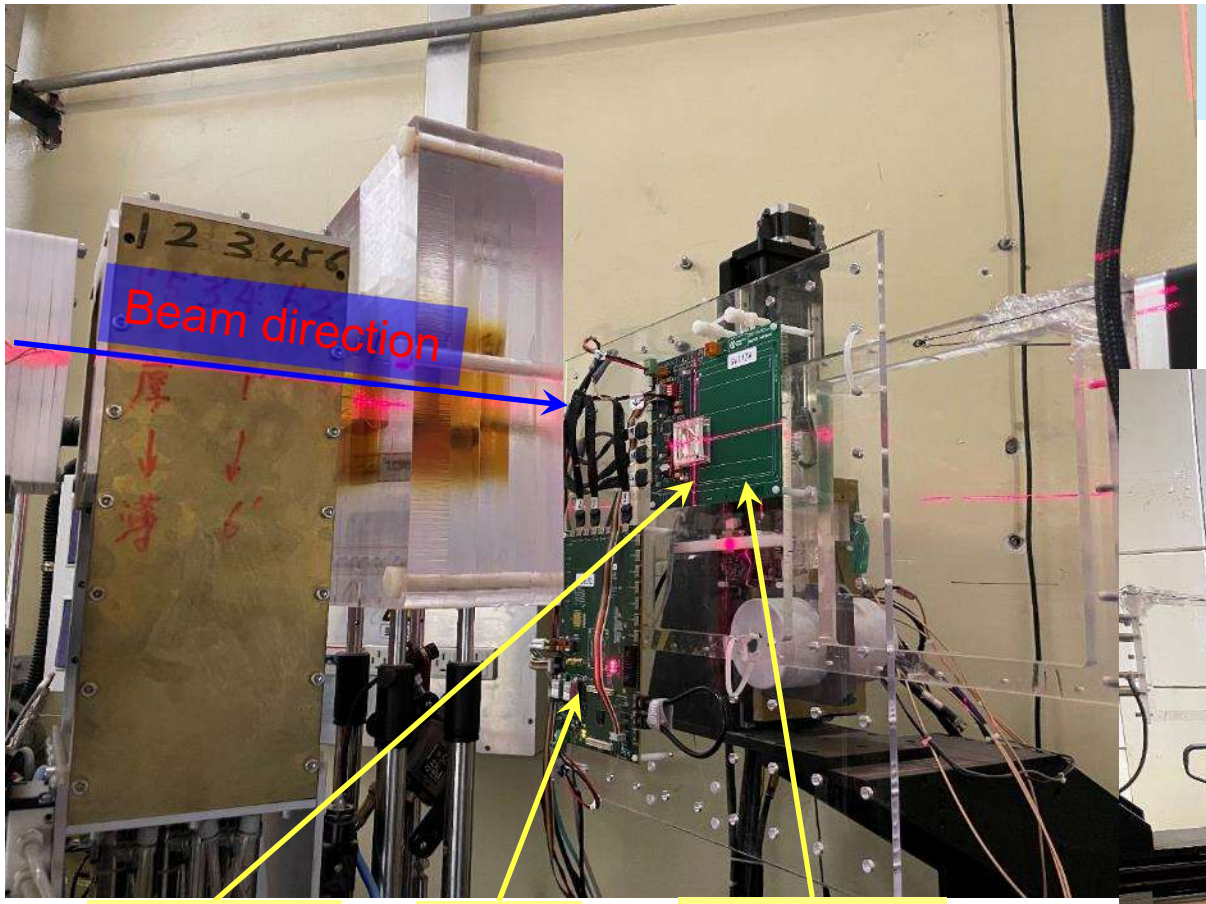
  (Thanks to everyone for helping setup a system at Beijing, especially Zhuoming Li, Federico Alessio, Paolo Durante, Ken Wyllie, Carlos Abellan, Will Parker)

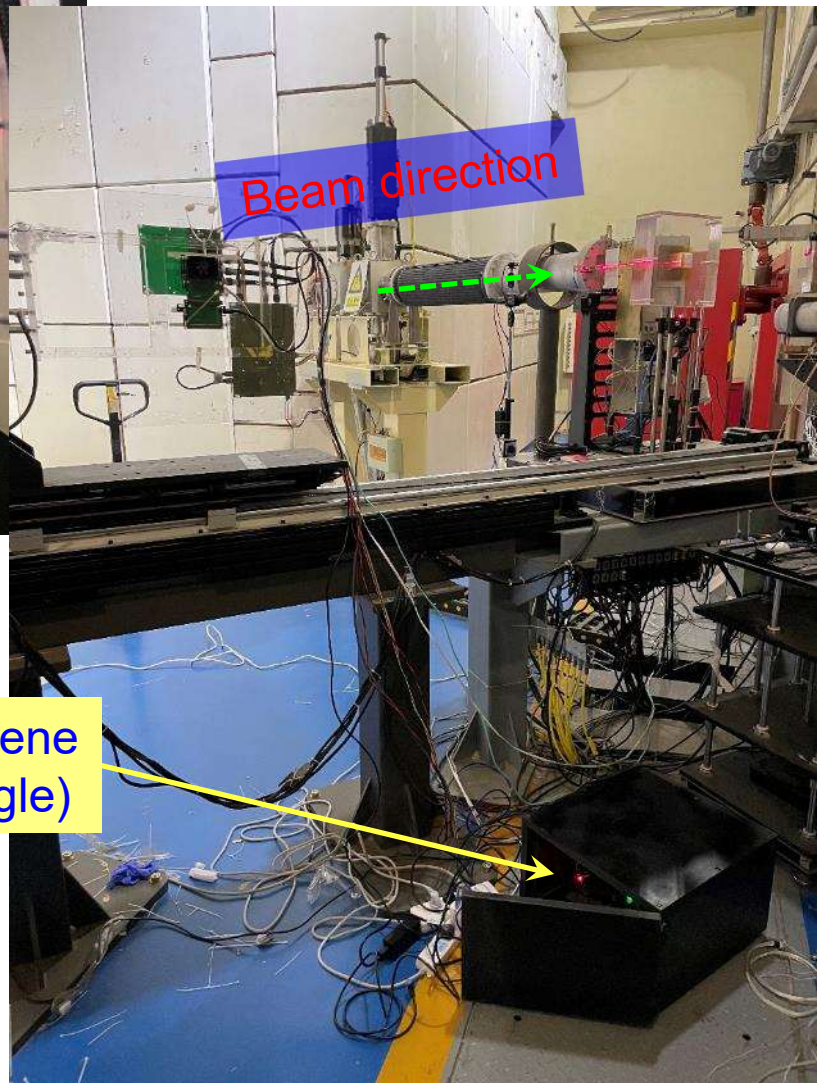
Layout of The Testbeam Setup at CIAE




SALT V3.9
Testboard
VLDB

Testbeam Setup





Raspberry-Pi3 died close to the end of the test, even though it was protected.

It recovered itself after several weeks.

Testbeam Setup

Register Configuration Value

- SALT V3.9 was set to a normal running condition.
- All TrimDAC, Pedestal, KillMask & InjectMask were set to 0×AA (b'1010 1010).
- In the last run KillMask = 0×00, so as to read out ADC value from all channels.

Address	Number	Value	Function
206-285	128	0×AA	TrimDAC
115-194	128	0×AA	Pedestal
105-114	16	0×AA	Kill Mask
307-316	16	0×AA	Inject Mask
205	1	0×AA	Global TrimDac
286-287	2	0×AA	TestChan TrimDAC

- All registers were checked frequently, including
  - **291** registers listed in the table have in total **1164 / 1164** bits of value **1 / 0**. when the KillMask is disabled, 1100 / 1228 bits are 1 / 0.
  - **53** other configuration registers, 96 / 328 bits of 1 / 0.

Runs of The Register SEU Test

Run	Starting Time	Flux [$cm^{-2}s^{-1}$]	SEU			TMR						
			Ped	Trim	Ext	SER	DSP	ANA	MIS	TFC	MEM	GLB
1	133201	3.12 E7	0	0	0	3	6	3	0	4	0	28
2	140203	1.35 E8	0	0	0	0	10	6	4	5	0	59
3	143436	1.03 E9	1	0	0	5	71	81	17	25	7	-
4	145750	1.12 E10	removed due to a mechanical issue									
5	155531	1.03 E9	1	0	0	7	59	66	17	38	2	-
6	160824	1.12 E10	4	3	1	63	-	-	214	-	56	-
7	162440	1.12 E10	3	4	1	64	-	-	x	-	51	-

KillMask = 0×00 → 7

- The beam flux was adjusted ~3×10^{7}-10^{10} $cm^{-2}s^{-1}$. Calibration with a Faraday cup was performed for each intensity value.
- A run lasts 600s. Total 7 runs were taken. Run 4 was invalid due to a mechanical issue. In the last run the Kill Mask was disabled, to test ADC readout.
- The total fluence for SEU test is 1.48×10^{13} cm^{-2}, 45.5% with KillMask disabled.
- In total 18 register value changes were observed: 9 from Pedestal, 7 from TrimDAQ, and 2 from other configuration registers.

All SEUs in The Configuration Registers

Run	Regi	Vset	Vnew	Nbit	Ch
3	154	AA	00	4	3F
5	190	AA	8A	1	7B
6	26F	AA	8A	1	69
	144	AA	08	3	2F
	14F	AA	A0	2	3A
	26D	AA	A2	1	67
	214	AA	A2	1	0E
	14D	AA	00	4	38
	11E	AA	00	4	09
	114	AA	00	4	-
7	245	AA	88	2	3F
	217	AA	8A	1	11
	130	AA	00	4	1B
	182	AA	02	3	6D
	214	AA	80	3	0E
	204	0C	08	1	-
	21D	AA	82	2	17
	172	AA	00	4	5D

Chronological order

KillMask = 0×00

- 18 register values changed during the whole test.
  - 9 from 128 Pedestals (in).
  - 7 from 128 TrimDACs (in).
  - 1 from 16 KillMasks (in).
  - 1 from the S2D register (in).
- Total 45 bit values changed.
  - 29 in Pedestal, ~3.2/register (max=4).
  - 11 in TrimDAC, ~1.6/register (max=4).
- Similar as observed at MGH & PSI, there were only bit changes of "1→0", no "0→1".
- Every time only 1 register was changed. There is no clustering of 16-channel group, unlike at PSI.
- The overall rate is significantly reduced. Pedestal registers seem slightly more vulnerable.

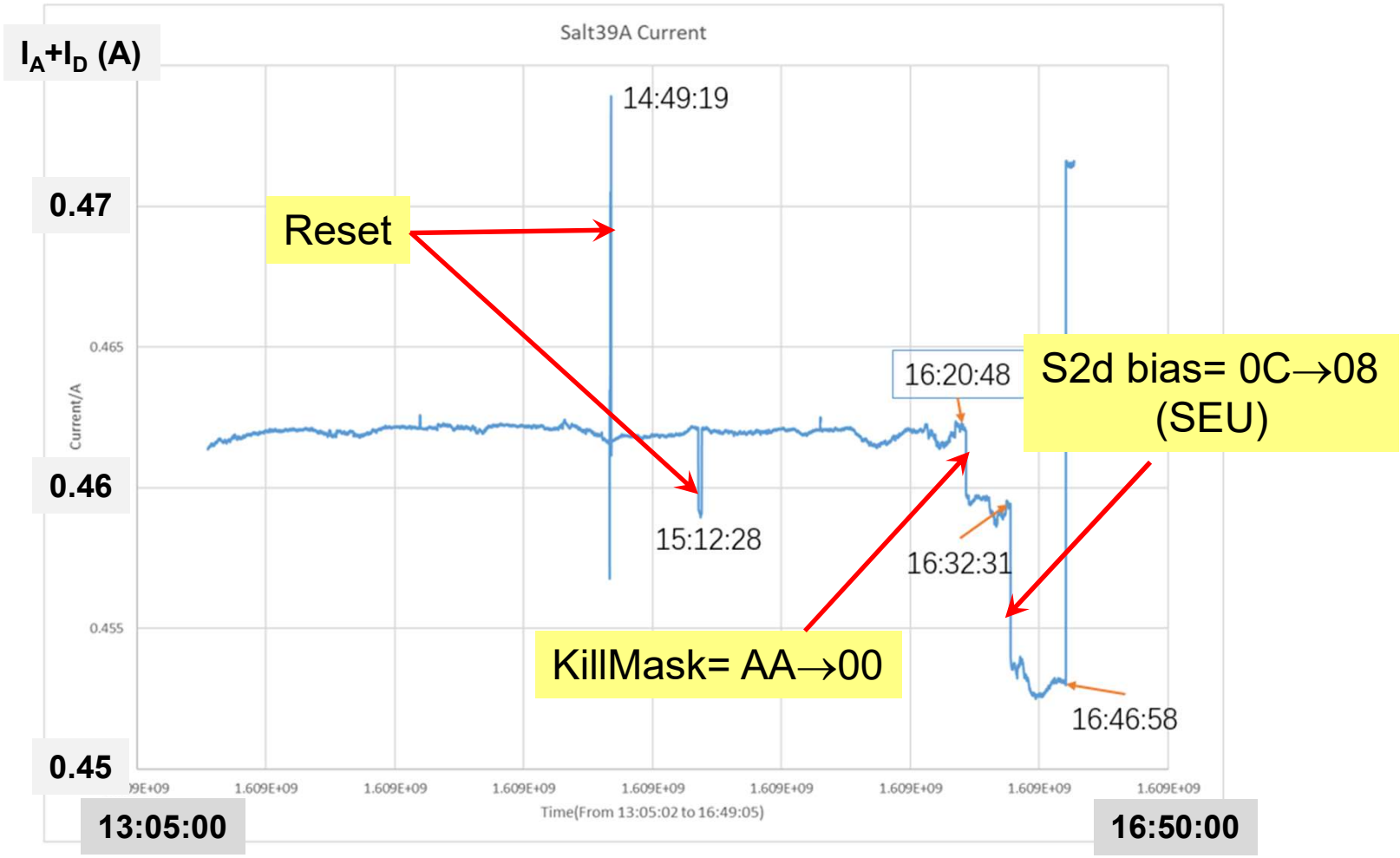
For comparison : **PSI test result**

TrimDAC: 12.3 registers / group, 3.4 bits / register
Pedestal: 7.0 registers / group, 1.8 bits / register

Rate of The Register SEU

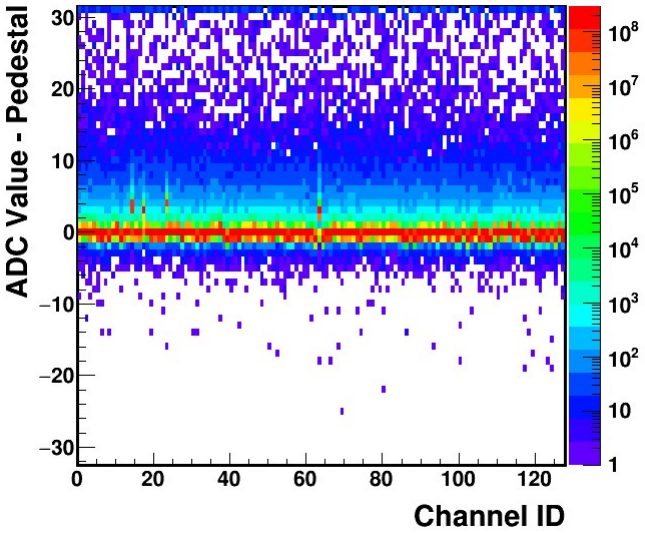
- Total particle fluence for the register SEU test: 1.48×10^{13} cm^{-2}
- The SEU rate of the per channel TrimDAC register.
  - Total **7** register changes $\Rightarrow$ cross section = 4.7×10^{-13} cm^2.
  - In comparison, test @ PSI measured 7.8×10^{-11} cm^2, a factor of **~165** higher.
  - Frequency of the inner-most ASIC = 0.6×10^{7} cm^{-2}s^{-1} $\times$ 4.7×10^{-13} cm^2 = 2.8×10^{-6} Hz.
  - If the UT uses all SALT V3.9 ASICs, the frequency = 4192 $\times$ 0.029 $\times$ 2.8×10^{-6} Hz = 0.34 mHz, i.e. **1.2 / hour** TrimDAC changes.
- Pedestal register per channel SEU rate.
  - Total **9** register changes $\Rightarrow$ cross section = 6.1×10^{-13} cm^2.
  - In comparison, test @ PSI measured = 1.3×10^{-11} cm^2, a factor of **~21** higher
  - If the UT uses all SALT V3.9 ASICs, the frequency = 4192 $\times$ 0.029 $\times$ 0.6×10^{7} $\times$ 6.1×10^{-13} = 0.44 mHz, i.e. **1.6 / hour** Pedestal changes.
- Note that the calculation assumes average 4 bits of “1” and 4 bits of “0”.

Monitoring The Current



All current changes match with actions or SEU, and are confirmed in a bench test after the radiation test.

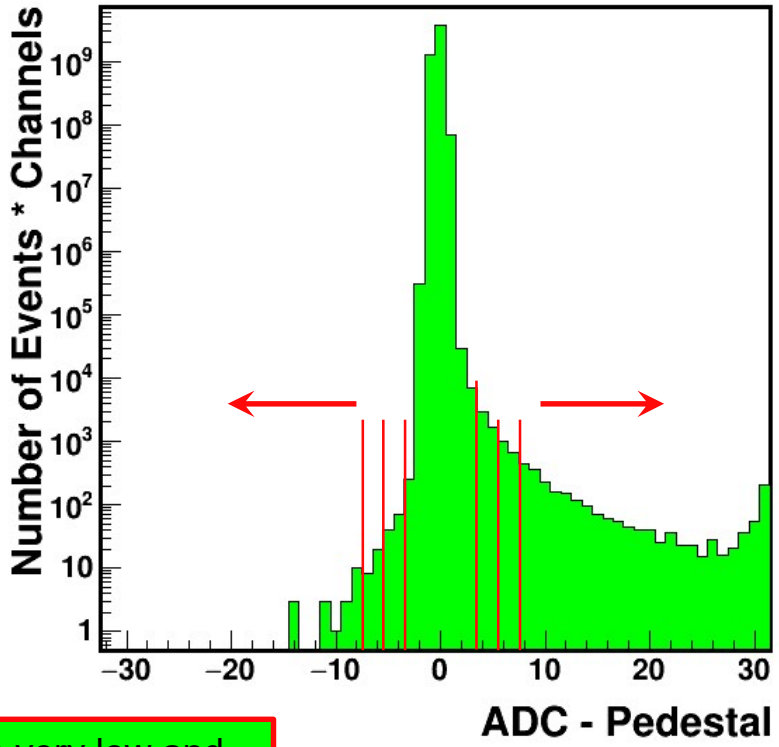
ADC SEU



Flux = 1.12×10^{10} $cm^{-2}s^{-1}$

~140 M NZS(non-Zero Supressed) events, remove channels **14,17,23,& 63** that TrimDAC registers changed.

ADC – Ped	Rate
> +7	4.8×10^{-7}
> +5	8.1×10^{-7}
> +3	1.7×10^{-6}
< –3	3.5×10^{-8}
< –5	9.1×10^{-9}
< –7	4.2×10^{-9}



ADC SEU rate is very low and not a problem in the real system.

Memory SEU

163043	
Expected	**Readout**
452 0F0	452 0F0
5D2 0F0	5D2 0F0
6D2 0F0	6D2 0F0
752 0F0	652 0F0
852 0F0	852 0F0
9D2 0F0	9D2 0F0
AD2 0F0	AD2 0F0
B52 0F0	B52 0F0

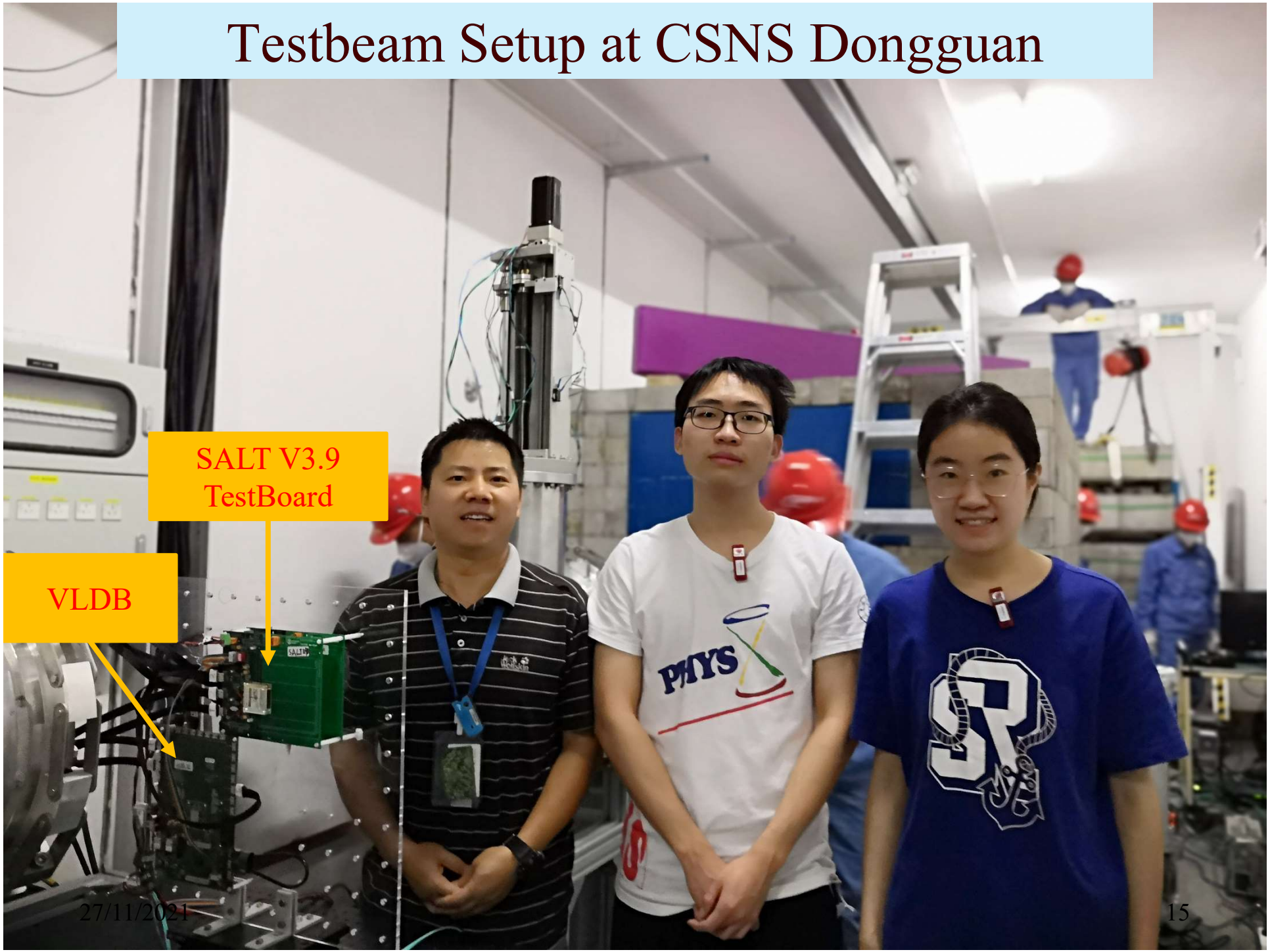
0111→0110

163314	
Expected	**Readout**
6D2 752	6D2 752
852 9D2	852 9D2
AD2 B52	AD2 B52
CD2 D52	CD2 D56
E52 FD2	E52 FD2
0D2 152	0D2 152
252 0F0	252 0F0
3D2 0F0	3D2 0F0

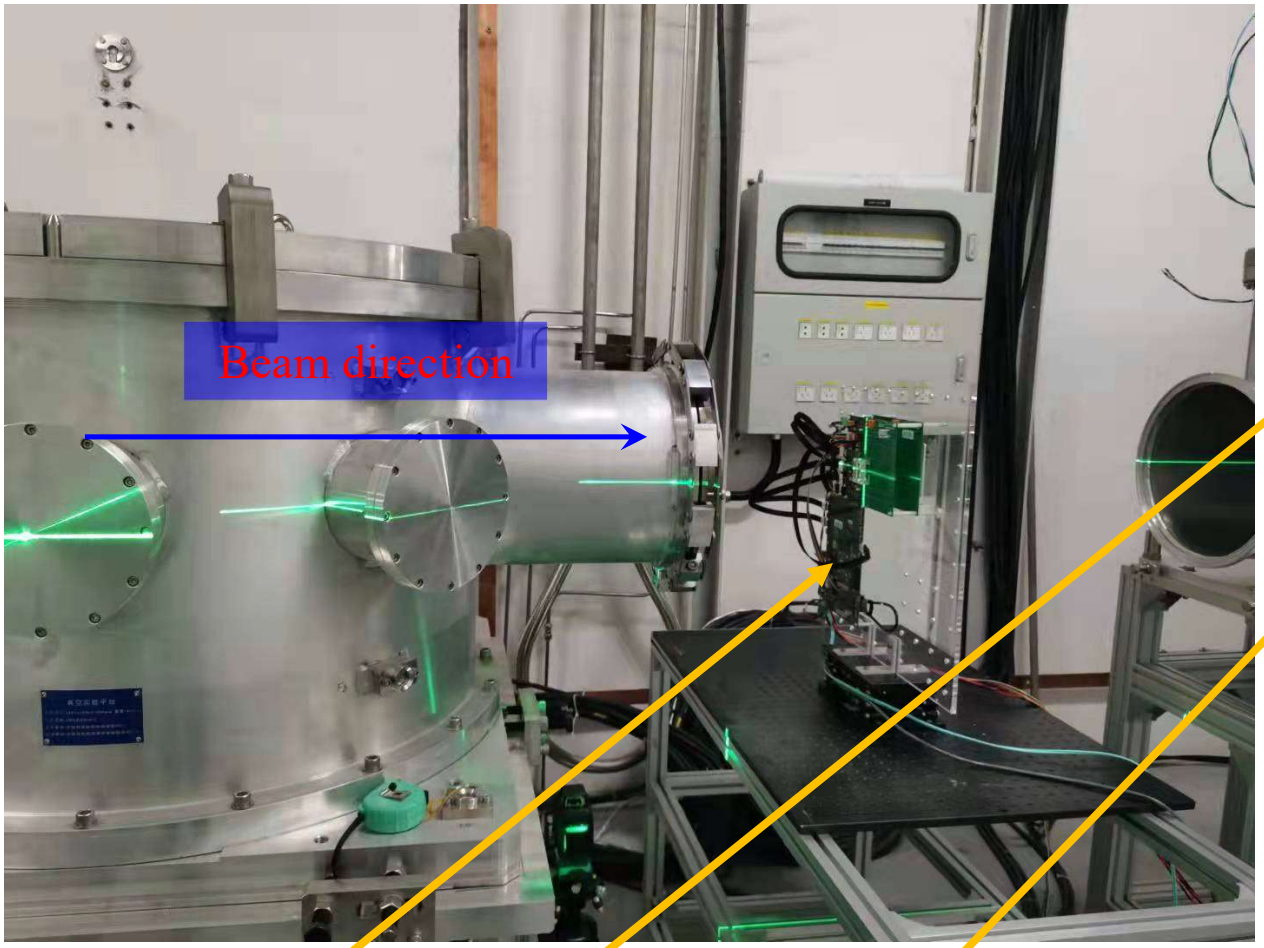
0010→0110

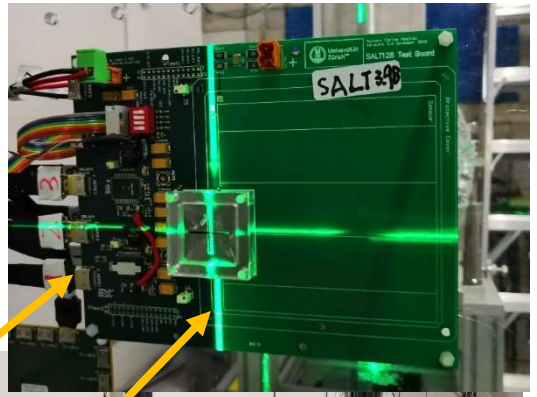
- The system is stable enough that we are able to check the memory SEU.
- In total ~18 billion bunch crossings were checked, 1/128 are NZS events, and 127/128 are HeaderOnly events.
- 2 memory SEUs were observed, that correspond to 2 HeaderOnly events. One has a bit change of “1→0”. The other has a “0→1”.
- Too few events for a meaningful Memory SEU study. We further explore this at CSNS, Dongguan in the week of Oct 18th, 2021.

Testbeam Setup at CSNS Dongguan



Testbeam Setup at CSNS Dongguan





VLDB

SALT V3.9 TestBoards

Laser Alignment

The same board that was used at CIAE is tested at CSNS. The 2nd board failed and could not be corrected once the cavern is closed.

Summary

- A SALT V3.9 ASIC was tested at CIAE in an 100 MeV proton beam. The particle flux is ~ 10^{7}-10^{10} $cm^{-2}s^{-1}$.
- SEUs in TrimDAC and Pedestal registers were observed. But the rates of V3.9 compared with V3.5 reduced by factors of **165 & 21**, respectively. Projecting to the whole UT at LHCb nominal luminosity, there will be **~1.2** TrimDAC and **~1.6** Pedestal SEUs per hour.
- The front end current was monitored. All significant changes are understood, and not problem in the final system.
- ADC SEUs are also observed. The rate measured is very low. In the final UT system they will contribute to noise hit only. It is not a problem.
- We observed 2 SEUs in the memory buffer or data transferring. Since the registers are much more stable than before, we could have a designated study this lower probability issue, to model the real condition of the LHCb running.

- Another radiation study took place at CSNS, Dongguan, Oct 18-23, 2021. Currently the data are being analyzed.

Thanks