LHCb Upgrade Status Report

- Mainly focus on the Chinese groups' contributions, including Upgrade I and II
- **Outline:**
  - Upgrade I activities: RTA, FPGA-tracking, DPA, SciFi, UT
  - Upgrade II activities: UT, ECAL

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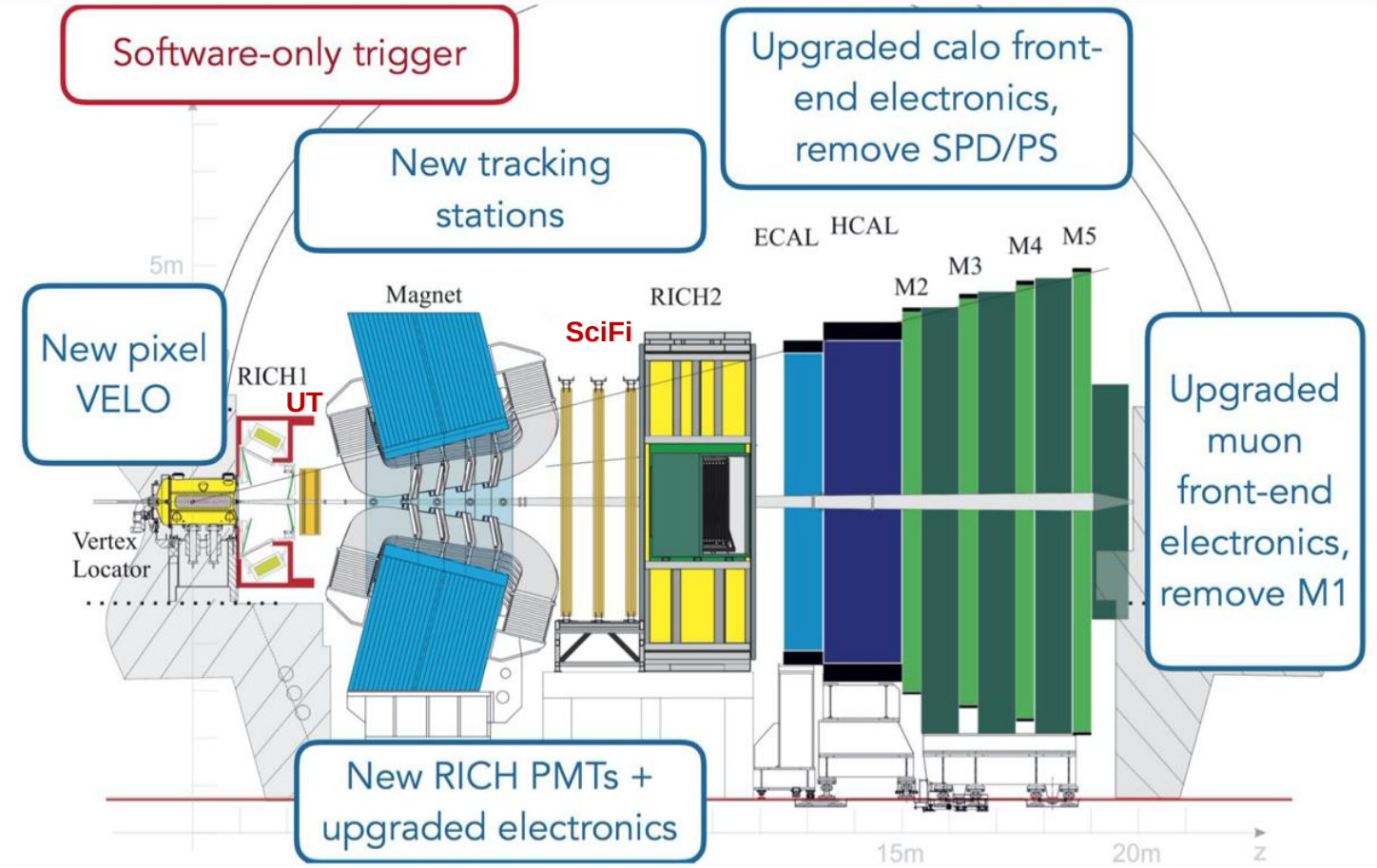
LHCb Upgrade Timeline

'Upgrade Ib'

- Currently 'Upgrade I' is under installation and commissioning, and is the next challenge for LHCb
- Upgrade II is another major upgrade planned for 2032

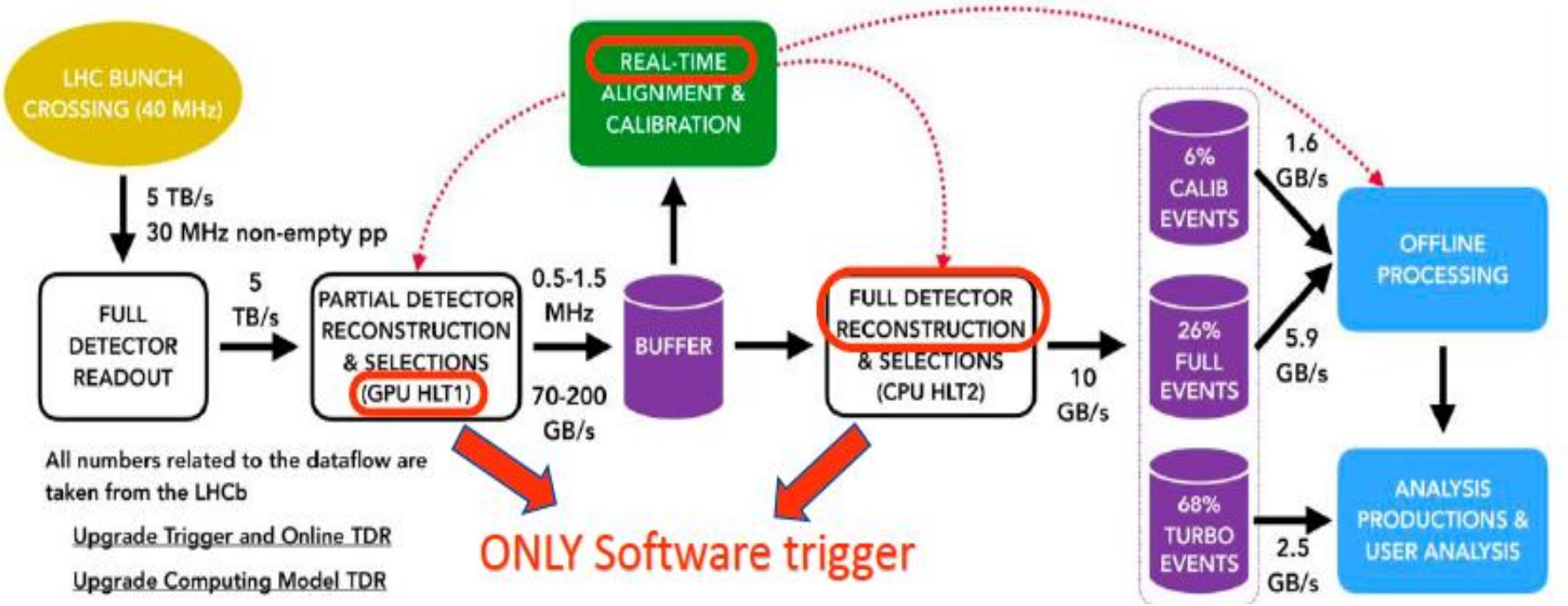
General Status of Upgrade-I

- Chinese groups focus on the **software trigger, UT and SciFi**



- Reference: LHCb-TDR-012

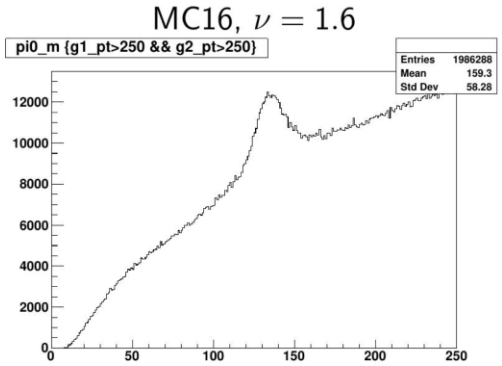
Real Time Analysis Project

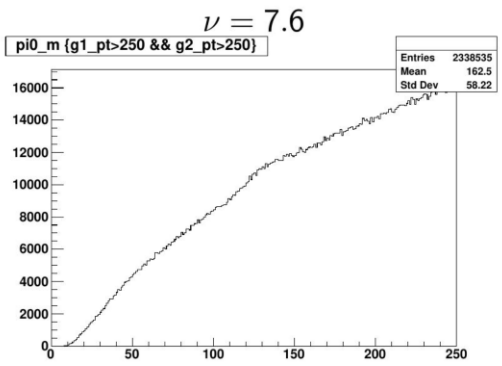


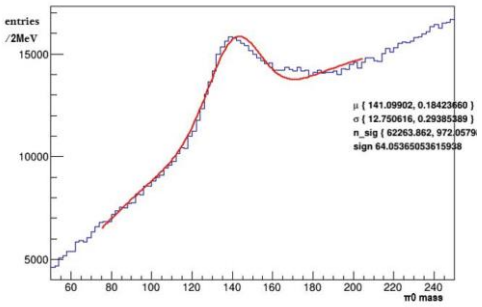
- For Run3 data taking, LHCb will use a fully software trigger
- Mission: develop and maintain the real-time processing of LHCb data for Run 3 and beyond

π^0 Energy Calibration and Monitoring Development

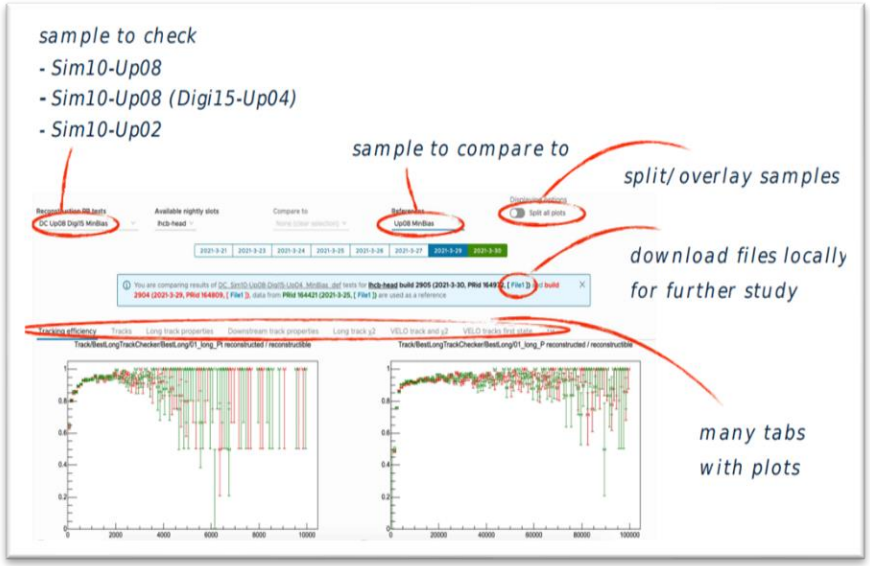
- A new π^0 energy calibration program as part of the monitoring and calibration system







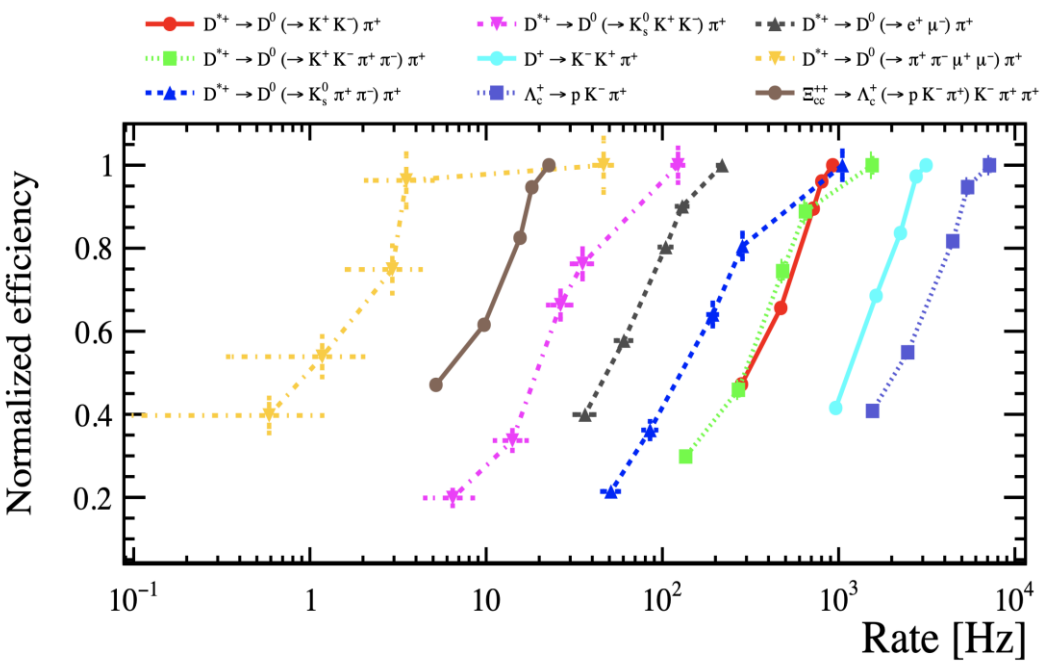
- An integrated rapid response test framework to monitor performance of high-level quantities
  - ✓ Automatic check of differences for selected Merge Requests
  - ✓ Accessing and visualizing counters



Development of Data Persistency

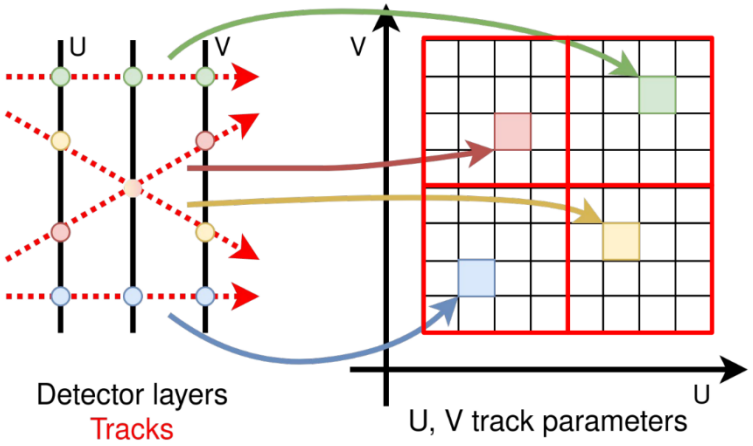
- Selected trigger objects need to be compressed and serialised into binary data suitable for transfer online
- **Rewrite** Gaudi algorithm for serialisation to accommodate requirements of parallel processing; **Add** serialisation functionality of selecting trigger objects to be persisted with the new algorithm

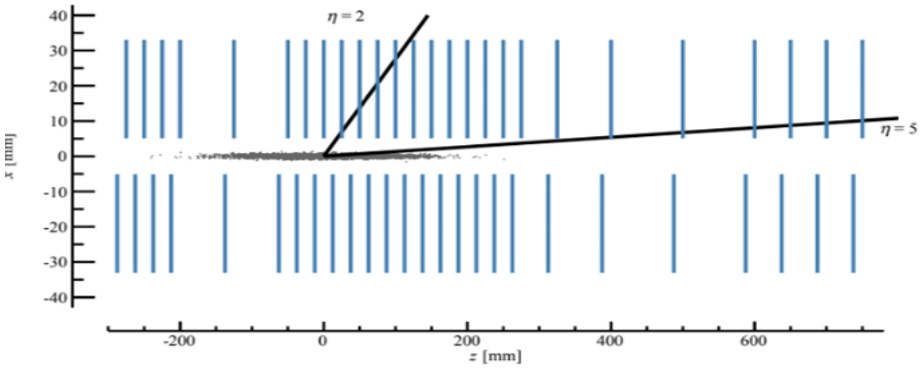
- Physics performance of the RTA model is tested with charm benchmark channels
- Signal efficiency is studied as a function of trigger output rate
  - Provide guidance for tuning of selection within the bandwidth limit



VELO Tracking with FPGAs

- Need to move more complex event reconstruction at the earliest stage of the trigger
- Tracking: large combinatorial problem → calls for high parallelization → can be moved on FPGAs using the “artificial retina architecture”
- Prototype system: reconstruction of tracks in the LHCb vertex detector
  - Composed of 52 silicon pixel modules, 38 in the forward region
  - Relatively compact FPGA system
  - Good first test-case for future and larger-scale applications

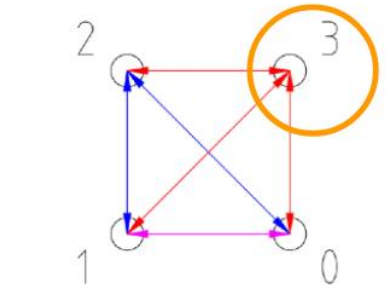




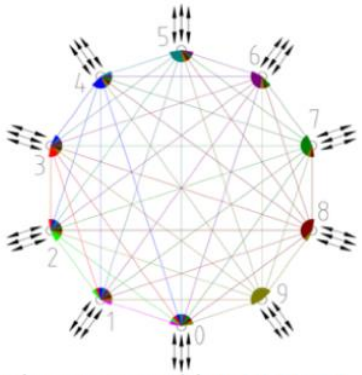
PoS Vertex2019 (2020) 047
EPJ Web. Conf. 245, 10001 (2020)

VELO Tracking with FPGAs

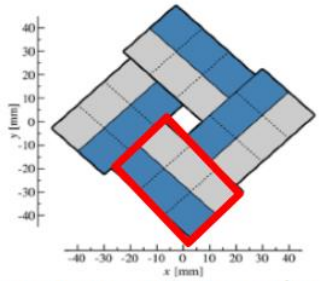
- Demonstrated, in simulation, feasibility using a network of 40 FPGAs
  - 4-ring*10 node full-mesh, each ring has enough power to process ¼ of VELO
- **Prove operation of 1 ring of 8 FPGA in Run 3 real DAQ demonstrates the technology**



4 interconnected networks

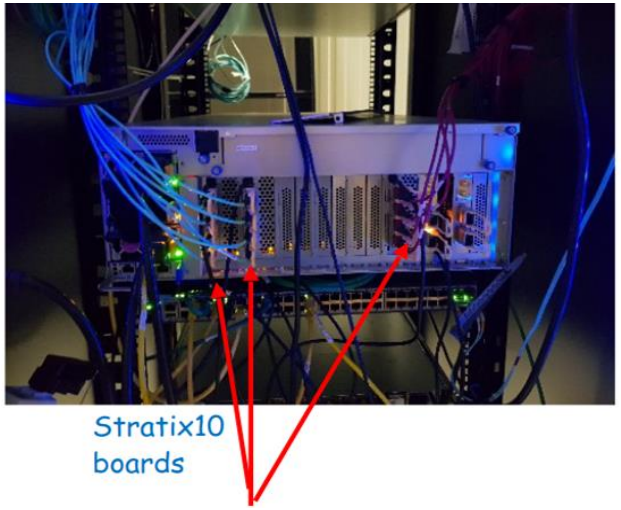


each composed by 10 FPGA

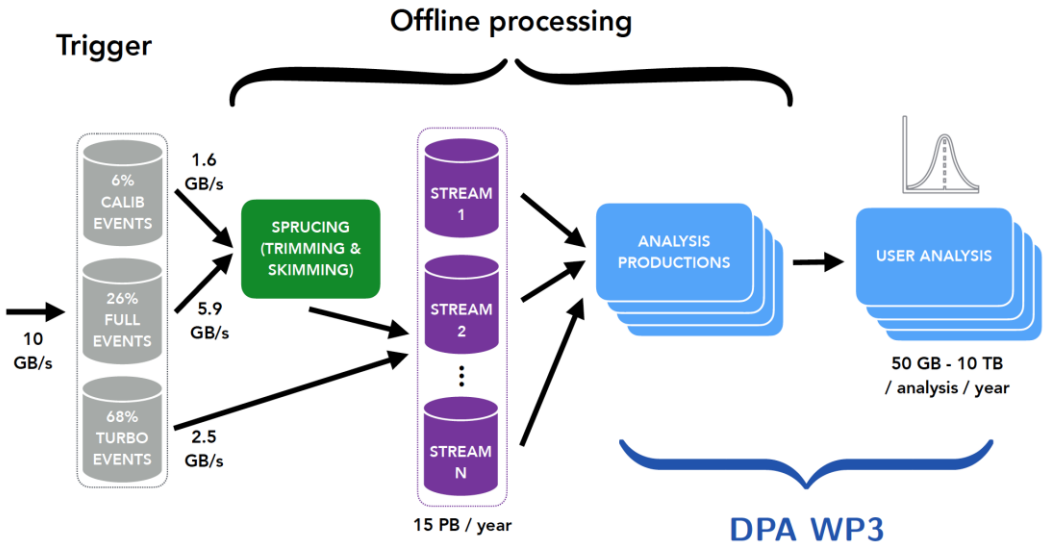


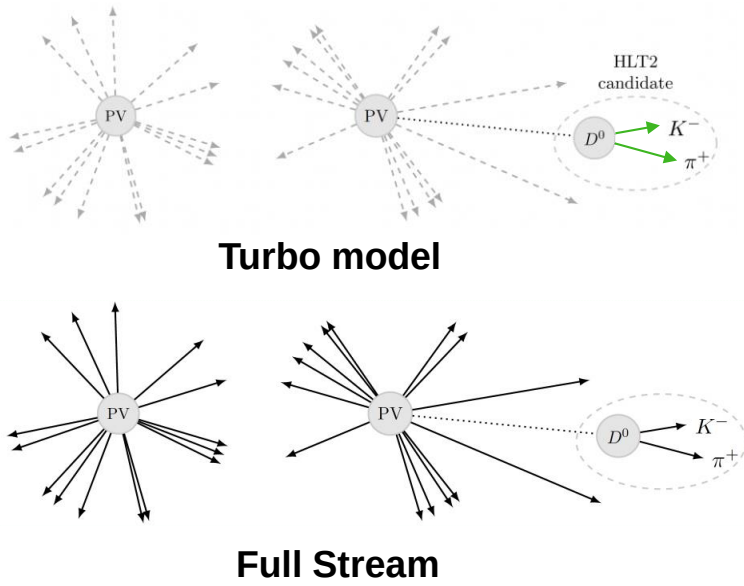
that cover a VELO quadrant

- Currently testing FPGA cards, and communication between FPGAs and DAQ boards at LHCb coprocessor testbed



Data Processing & Analysis





DPA project created to coordinate offline data processing activities. Main contributions (China):

- Sprucing (reduction of the data from the trigger) development. Sprucing Campaign Manager (2022+)
- Several offline analysis tools' development & maintenance

SciFi Activity Overview

- SciFi : 524,000 SiPM Channels
- SciFi readout ASIC: PACIFIC – 64 channel SiPM readout

LHCb SciFi China Group:

- **Co-design the PACIFIC Frontend Board (with Heidelberg)**
- **Manufacture all 2,528 PACIFIC Boards**
- **(100% produced & delivered to CERN)**
- **Test 1/2 of PACIFIC Boards (another ½ @Valencia, 100% finished)**

- Quality Assurance System for PACIFIC chip & boards (11 setups @Tsinghua , Valencia, Barcelona and Heidelberg)

- Software: Build new sequence for SciFi specific processing of Testbeam data.

LHCb SciFi - Current Status

6 SciFi C-Frames on the C-Side behind the LHC beampipe. Photo by S. Jakobsen.

	C-side						A-side					
Workpack.	**C1**	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**C11**	**C12**
Mechanics	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	Ok	ok
Cabling	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	Ok	ok
Services:												
Water	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok		
NOVEC/vacuum	ok	ok	ok	ok	ok	ok	ok	ok	++			
Dry-gas	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok		
Modules	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok		
Heating	ok	ok	ok	ok	ok	ok	ok	ok	ok	++		
Electronics	ok	ok	ok	ok	ok	ok	ok	ok				
Optical fibres	ok	ok	ok	ok	ok	ok	++	ok				
Commissioning	ok	ok	ok	ok	ok	ok		++				

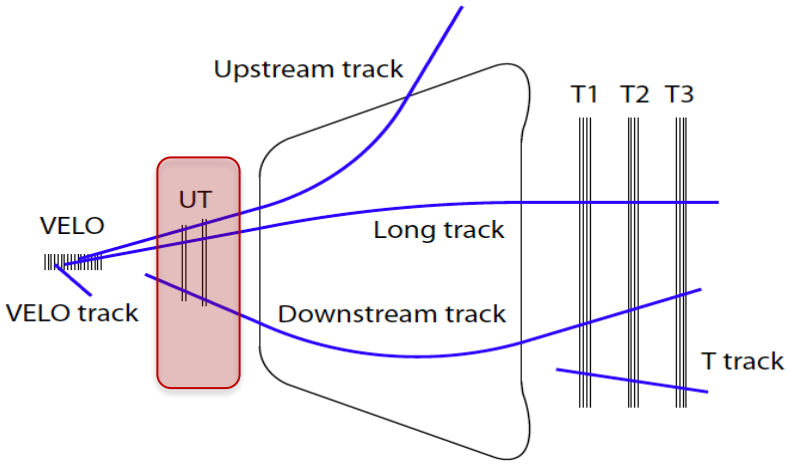
++ means just ongoing

256 Front-end Boxes needed for the SciFi

type of status of the FEBs	number
FEBs on Cframes	176
FEBs used on mezzanine floor test setup	2
FEBs ready to be install on Cframe	2
FEBs passed QA , waiting for optical inspection	22
FEBs needs to be repaired	76
Total number of FEBs assembled	278

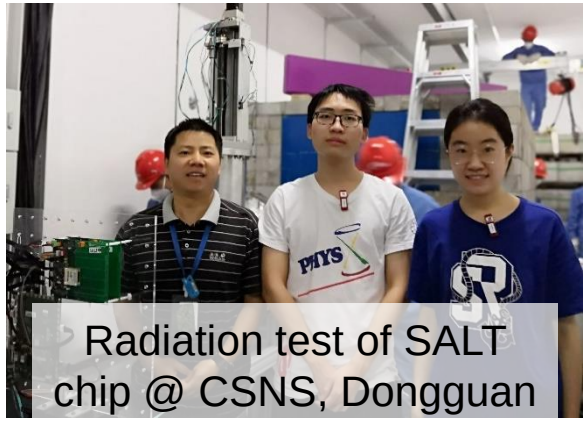
Upstream Tracker (UT)

- UT is silicon strip detector located upstream of the magnet, key for
  - Fast tracking and trigger decision
  - Reduction of ghost rate
  - Efficient reconstruction of long-lived particles
- Chinese groups are core members in system design, test and integration




Slice test of UT stave @ CERN

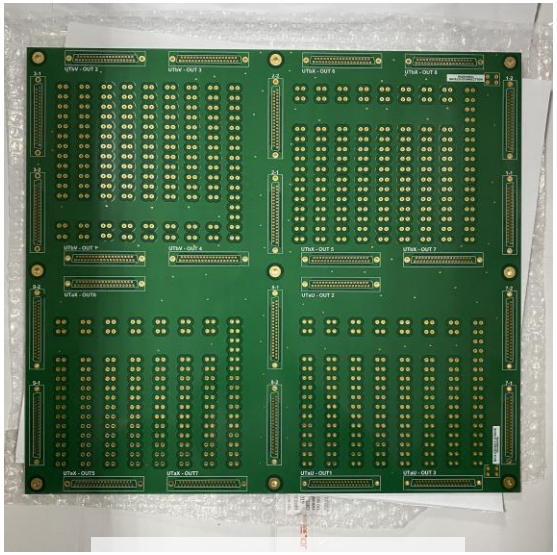

Radiation test of SALT chip @ CIAE, Beijing


Radiation test of SALT chip @ CSNS, Dongguan

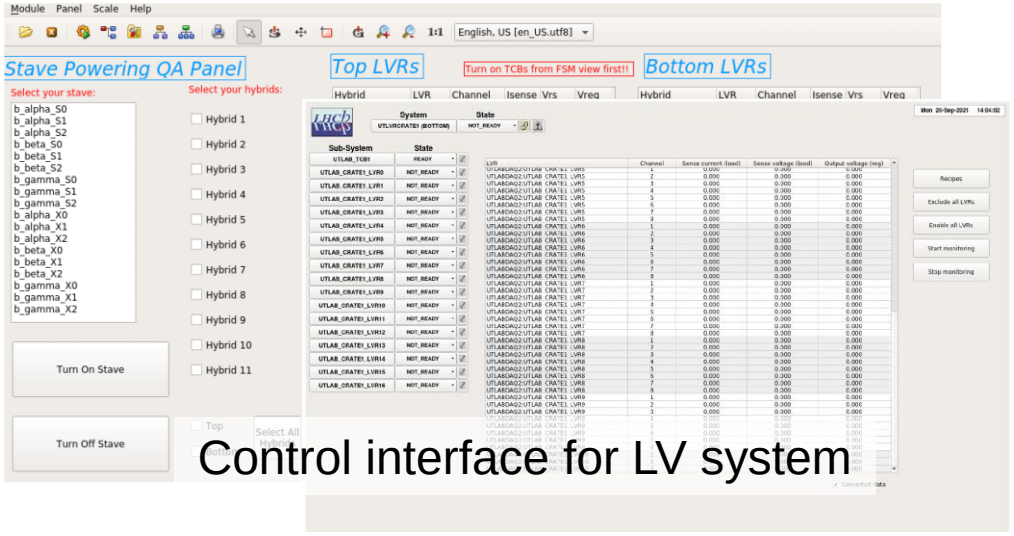
See talk by Quan Zou "LHCb UT upgrade status"

UT System Integration

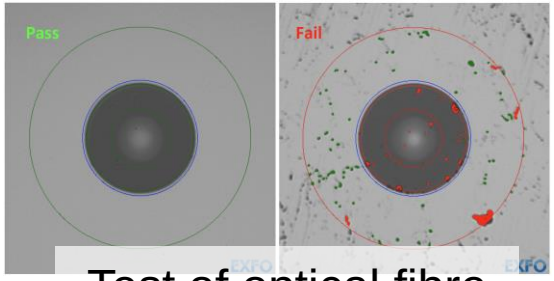
- Preparation for installation:
  - patch panel design / cabling / optical fibre test / mechanical test / …
- Design of control and safety software for test and commissioning



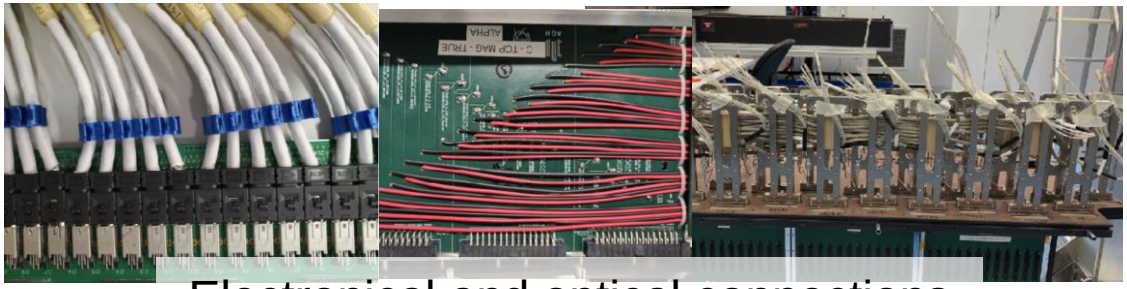
HV patch panel



Control interface for LV system



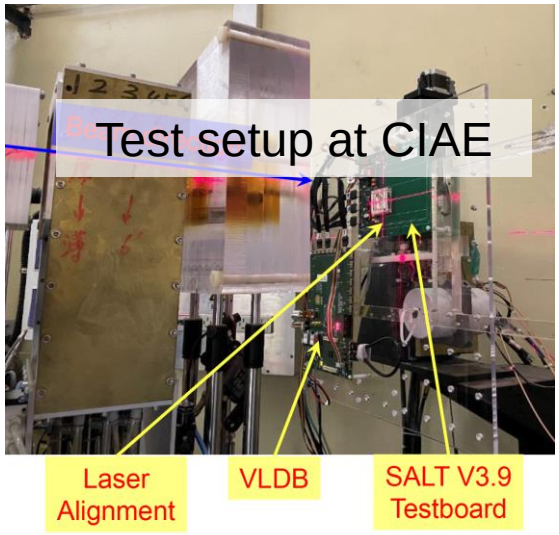
Test of optical fibre

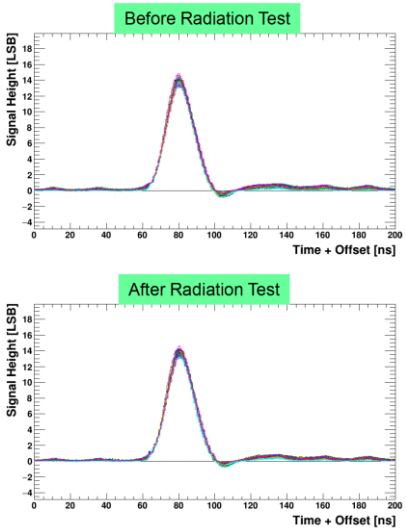


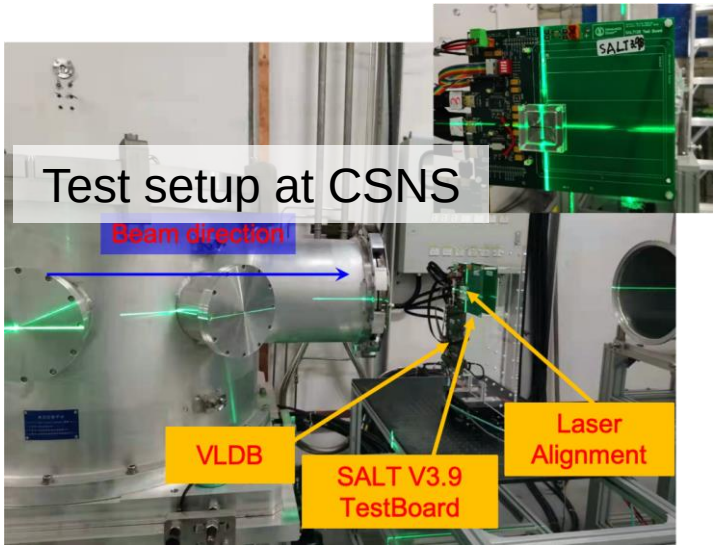
Electronical and optical connections

Radiation test for SALT

- FE chip SALT for UT was modified in 2020 for better radiation hardness, in urgent need of validation given Run3 schedule
- Despite difficult in available facility and travel globally, IHEP team carried two radiation tests using Chinese facilities
  - Dec 2020: 120MeV *p* beam at CIAE, Beijing → demonstrated new SALT chip has significantly improved against Single Event Upset (SEU)
  - Oct 2021: 80 MeV *p* beam at CSNS, Dongguan → analysis ongoing, estimating the rate of SEU for whole UT at operation





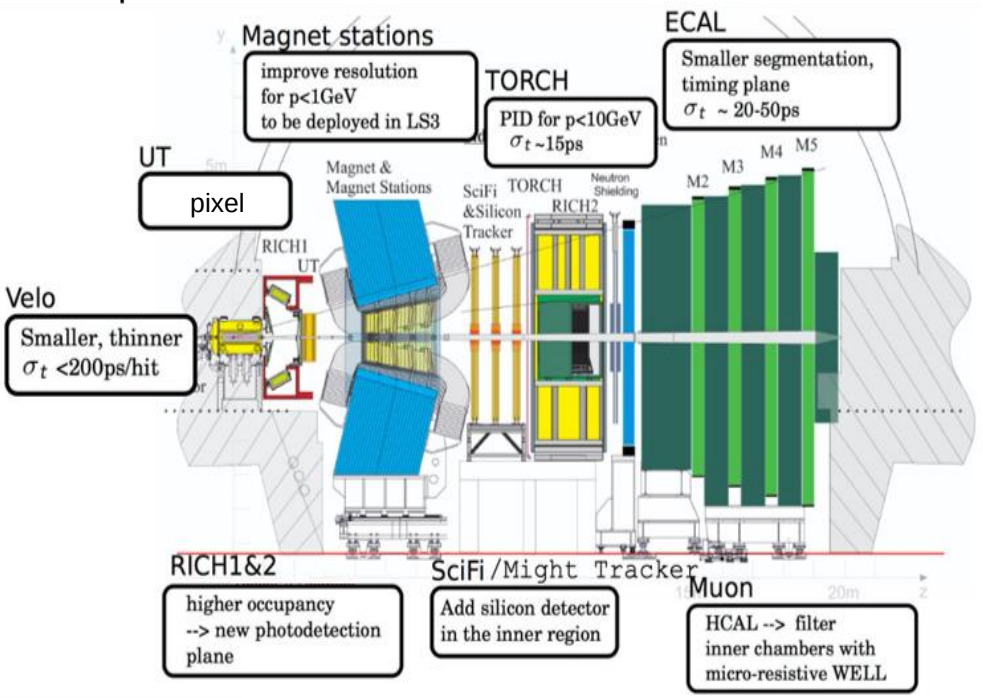


See talk by Shuaiyi Liu "Radiation Study of the LHCb UT Readout ASIC"

Upgrade II

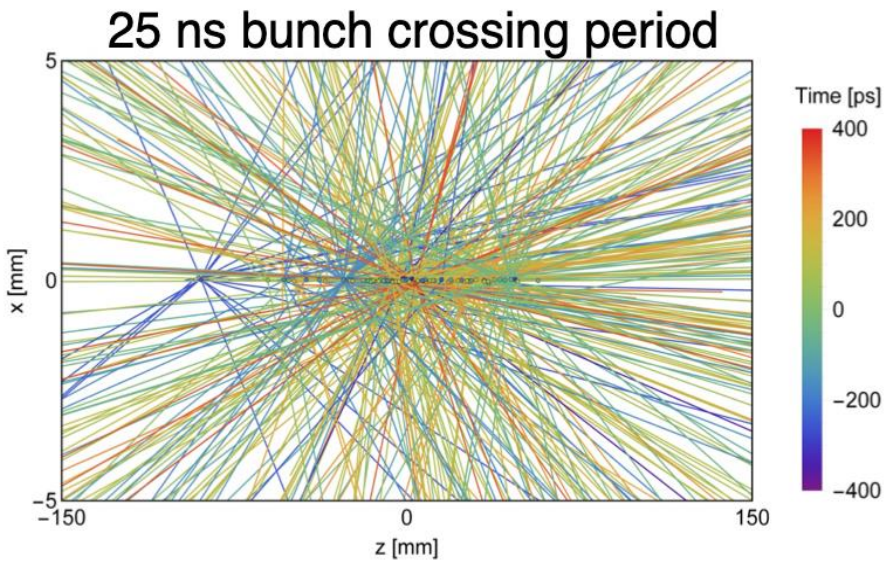
- Factor >5 increase in particle multiplicity (compared to Run 3)
  ~40 interactions per crossing; $L \sim 10^{34}\mathrm{cm}^{-2} \cdot \mathrm{s}^{-1}$; $\int L \sim 300\mathrm{fb}^{-1}$
- Aim at retaining or improving the Run 3 detector performances but in a more difficult environment
  - More channels:
    Increase the granularity of the detectors
    Add timing information to use the fact that PVs are spread in time at the interaction over ~100 ps
  - Detectors more resistent to radiation effects:
    Electronics with <65 nm silicon technologies for chips
    Large power and cooling requirements

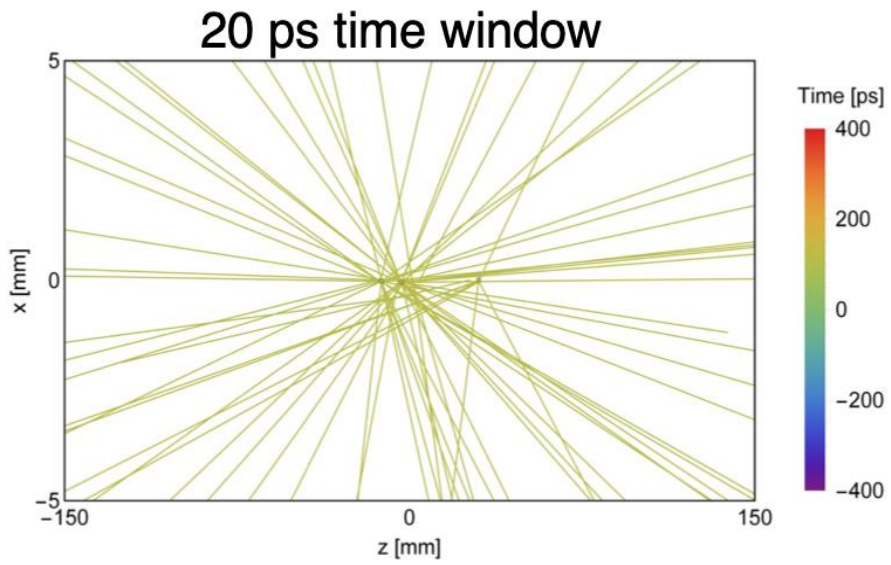
- Changes to all parts:
  - Remove HCAL (replace by iron shield before muon detectors
  - Add tracking stations inside the magnet
  - Add TORCH detector in front of RICH2
  - All other detectors replaced by new versions



Timing Information

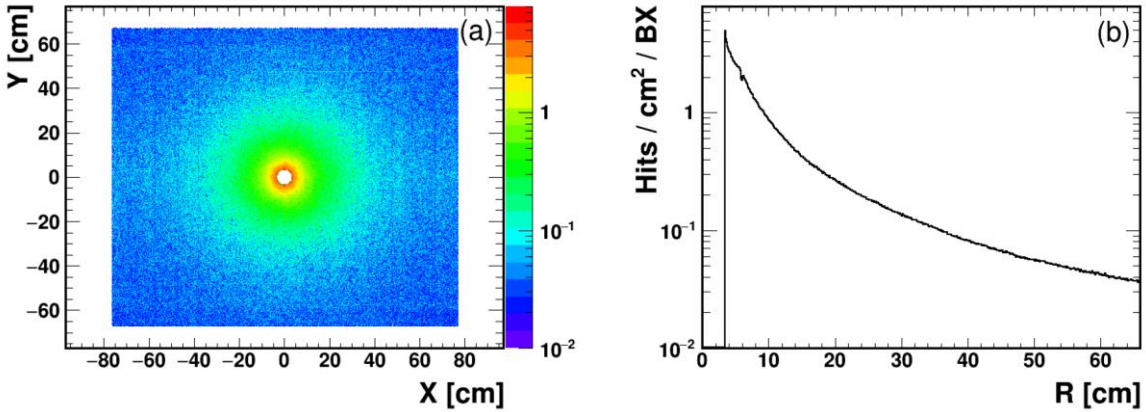
- Measurement of time of individual particles, with ~10 ps resolution, will allow tracks and clusters to be associated with the correct interaction
- Usage of timing foreseen in VELO, RICH, ECAL and TORCH
  - Information on timing needs to be exchanged between subdetectors: for example for data suppression in software trigger
  - Resolution of 10ps is challenging for the detectors' electronics: R&D needed for new sensor and Front-End ASIC technologies





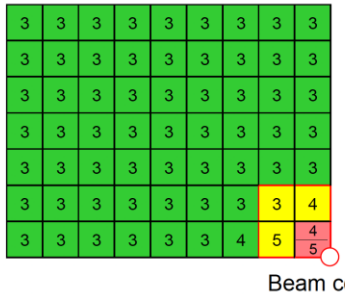
UT for Upgrade II

- Studies led by Chinese groups started on upgrade of UT at Upgrade II luminosity (2e33 $cm^{-2}s^{-1}$ → 1.5e34 $cm^{-2}s^{-1}$). Simulation studies shows UT has to be upgraded with higher granularity for UII
  - The occupancy (max ~10%) will compromise the performance
  - The data rate would be too high

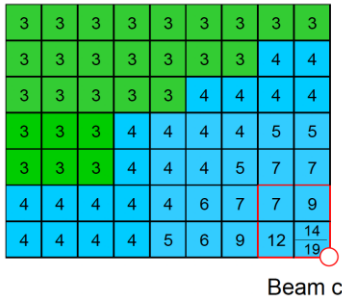


Current UT UT @ UII

The colors are for different sensors (with different pitches)



Data links / ASIC



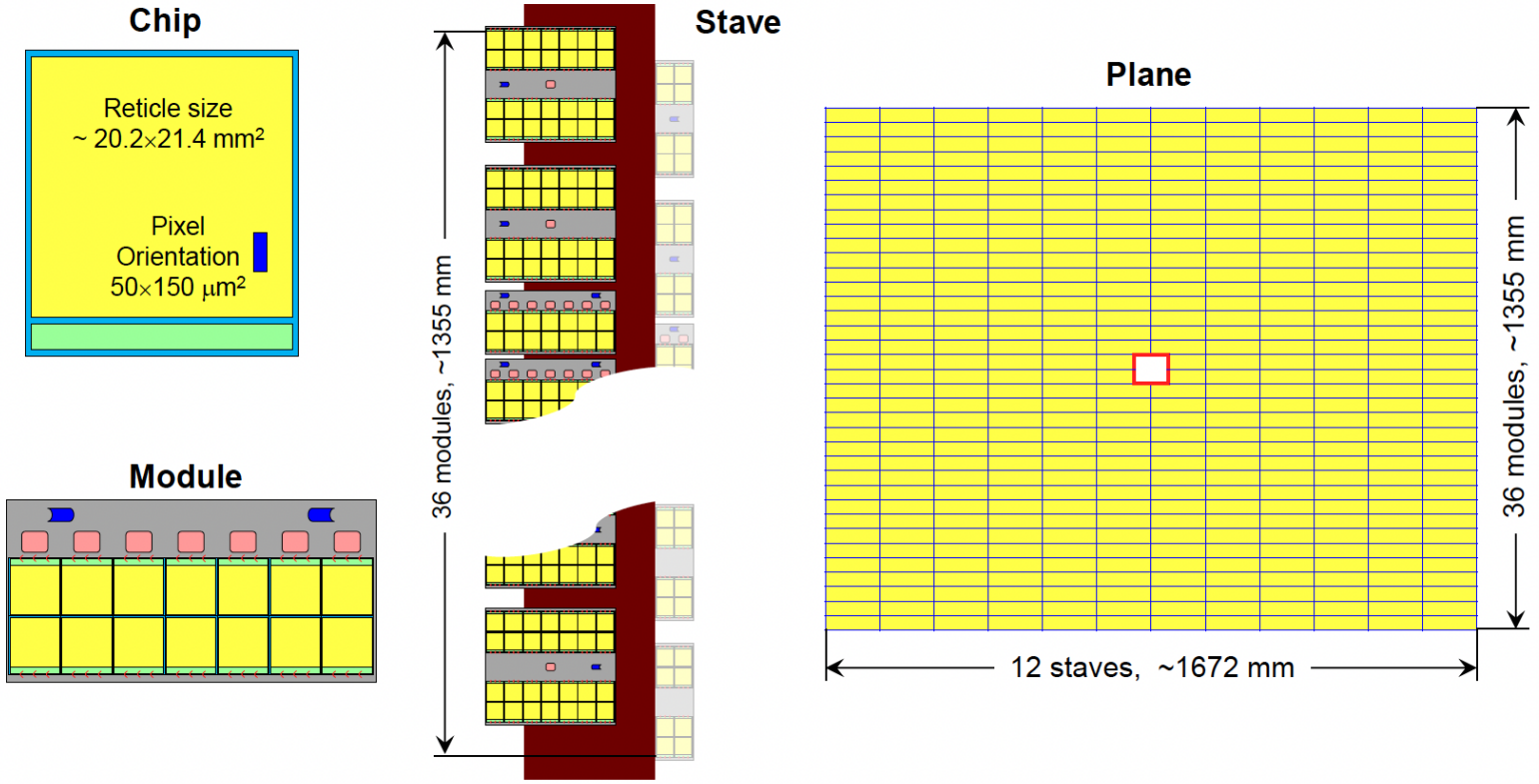
Blue color means the e-links will be not enough with current UT granularity

Beam center Beam center

Occupancy and data rate of UT with simulation study

UT for Upgrade II

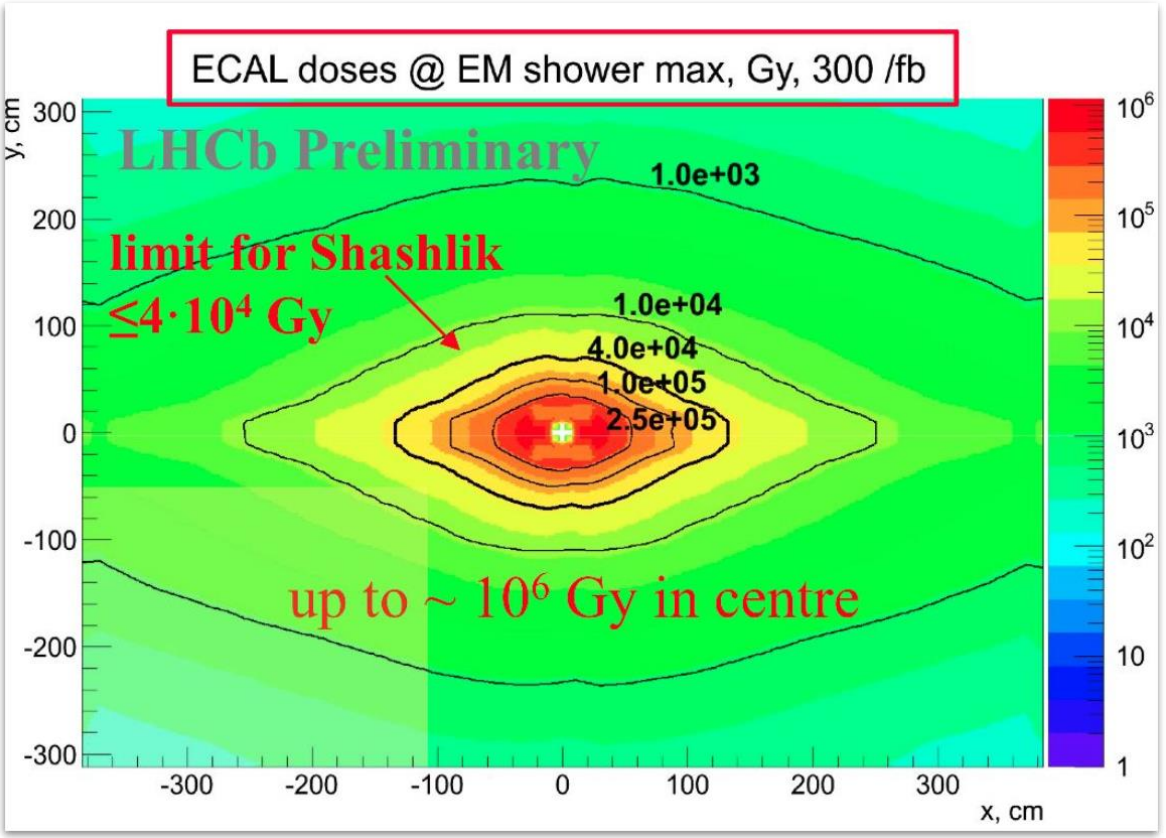
- Possible CMOS technologies including LV-CMOS and HV-CMOS; IHEP has started R&D in available HV-CMOS prototype
- UT Framework TDR under LHCC review



Upgrade II Challenges to ECAL

Challenge points:

- Fine granularity to reduce occupancy
- Good time resolution to deal with pile-up
- Radiation hardness to operate at high radiation exposure



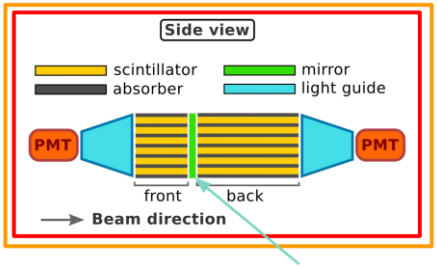
Benefits from ECAL upgrade

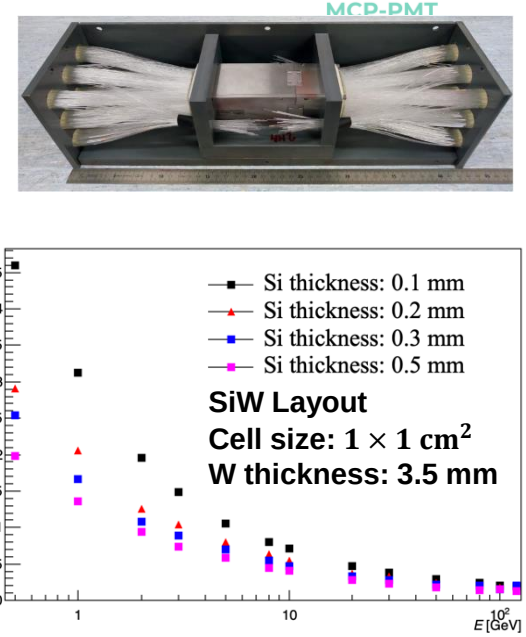
- **An ECAL with good γ/e detection and γ/π^0 separation**
  - Important to improve sensitivities of many key measurements
  - Largely expand the physics that can be explored by LHCb

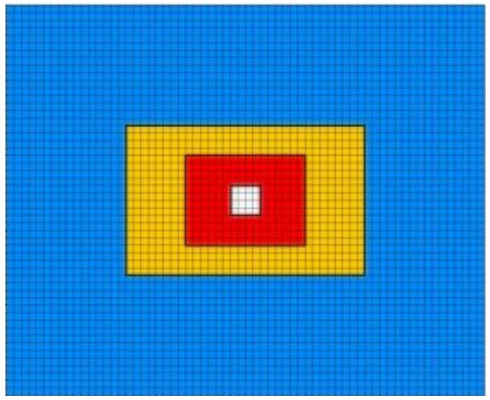
- **Main physics cases:**
  - Lepton-universality violation, e.g. $B^0 \to K^* e^+ e^-$, $b \to c l^- \bar{\nu}_l$
  - Photon polarisation , e.g. $B_s^0 \to \phi\gamma$, $\Lambda_b^0 \to \Lambda\gamma$
  - CP violation, $B_{(s)}^0 \to J/\psi\pi^0$
  - CKM γ measurement with $B \to D^* X$
  - Radiative decays and baryon magnetic moments, e.g. $\Lambda_b^0 \to J/\psi p K^- \gamma$

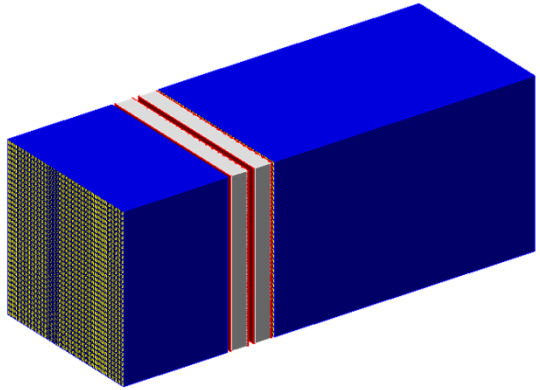
Simulation Studies of ECAL

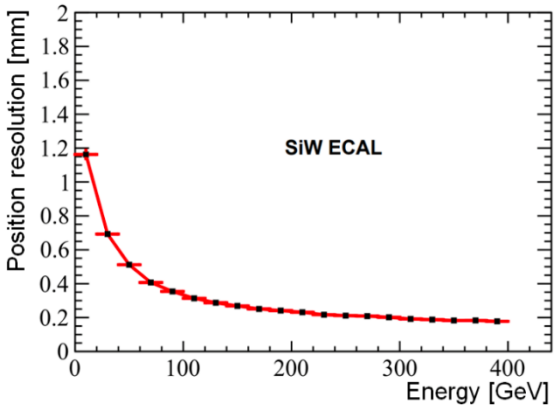
- Pure SPACAL（CERN）, SiW（China）and SPACAL+Si mixture（China）, three layouts are proposed
  - Energy resolution, time resolution , position resolution, and physics performance under study

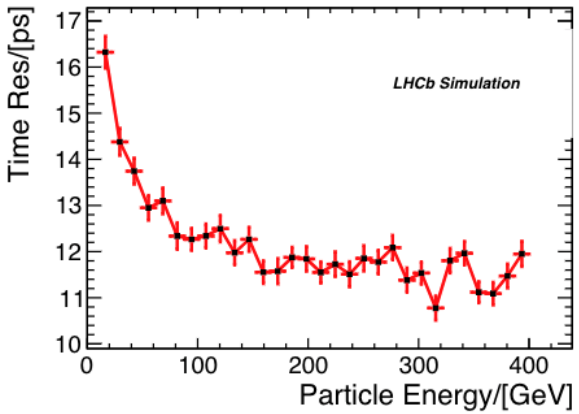








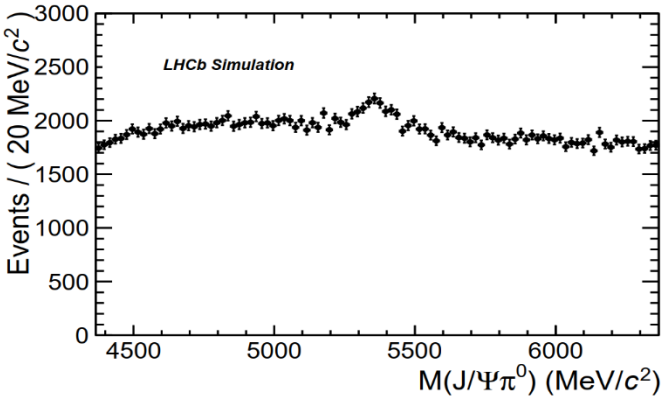


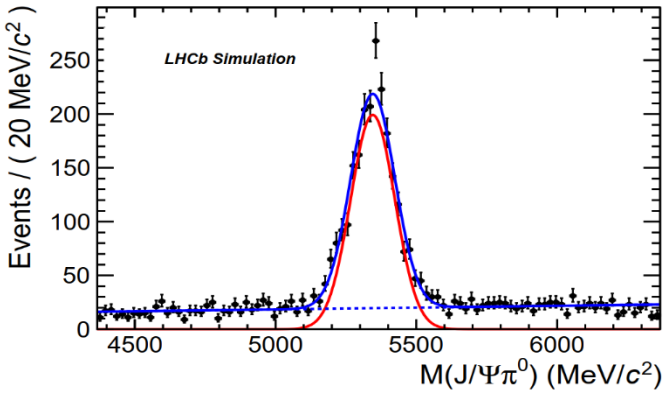


See talk by Jiale Fei “Electromagnetic calorimeter simulation for the LHCb Upgrade II”

Performance Check: SiW Layout

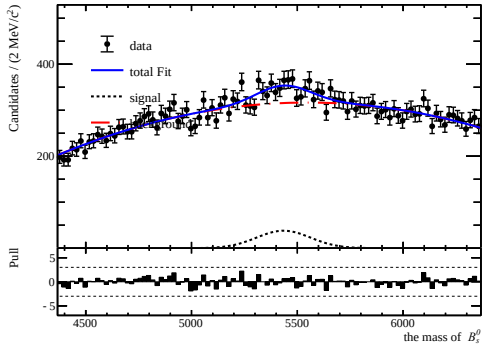
- $1.5 \times 10^{34} cm^{-2}$, $B_s^0 \to J/\psi\pi^0$

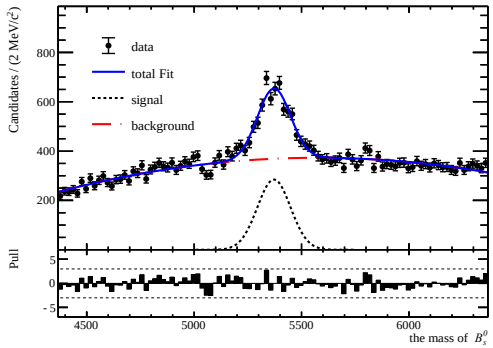




Left: no time matching; right: with time matching of two gammas when reconstruct $\pi 0$; $\pi 0$ time matching to the J/ψ vertex when reconstruct $Bs0$.

- Current cell size also doesn't work well in high luminosity.





Both: time window applied; Left: current cell size; right: small cell size

Performance Check: Mixture Layout

- Layout setup:

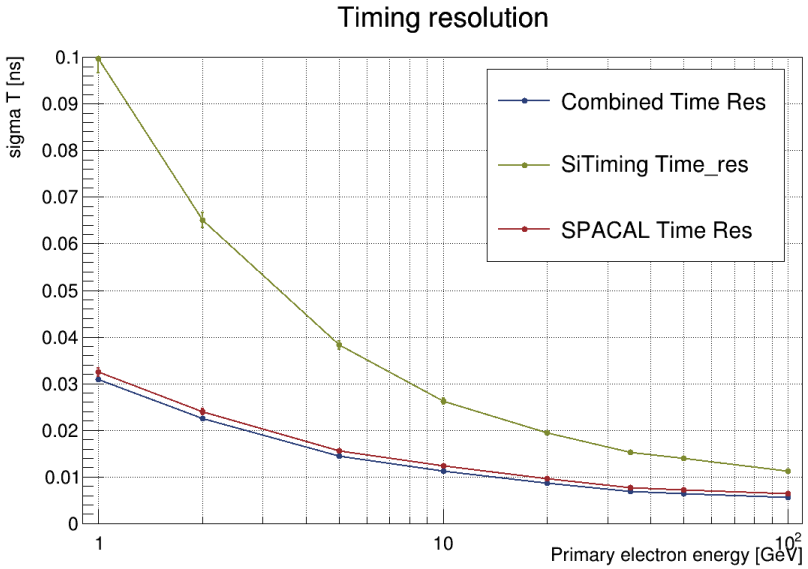
  Crystal Material : GFAG

  Absorber Material : Tungsten

  SPACAL Cell size : 1.5 cm^2

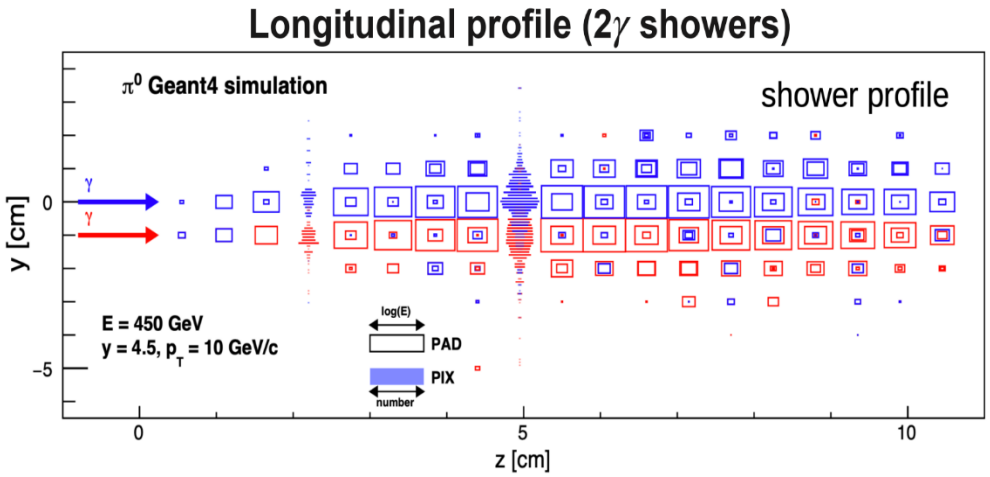
  Silicon Cell size : 1 cm^2

  Silicon thickness : 0.5 mm



- Main advantages of this layout:

  - have good energy resolution and timing resolution
  - can also have good spatial resolution: e.g. using MAPS (~30×30 μm2) for the silicon layers
  - benefit into π0 reconstruction



ALICE: New Forward Calorimeter

Summary and Outlook

- LHCb Upgrade I installation is ongoing; the Upgrade II framework TDR is submitted, with first ideas on the possible design choices

  - Chinese cluster have made and are making very important contributions to several projects
    - ➤ RTA, DPA, FPGA-tracking, SciFi, UT (I)
    - ➤ UT, ECAL (II)

- The ultimate goal is to build a detector to make best use of the HL-LHC phase for flavour physics and more.
  - high resolution timing information is an important idea
  - mixturing of different detector techniques seems quite promising