ATLAS Detector Upgrade

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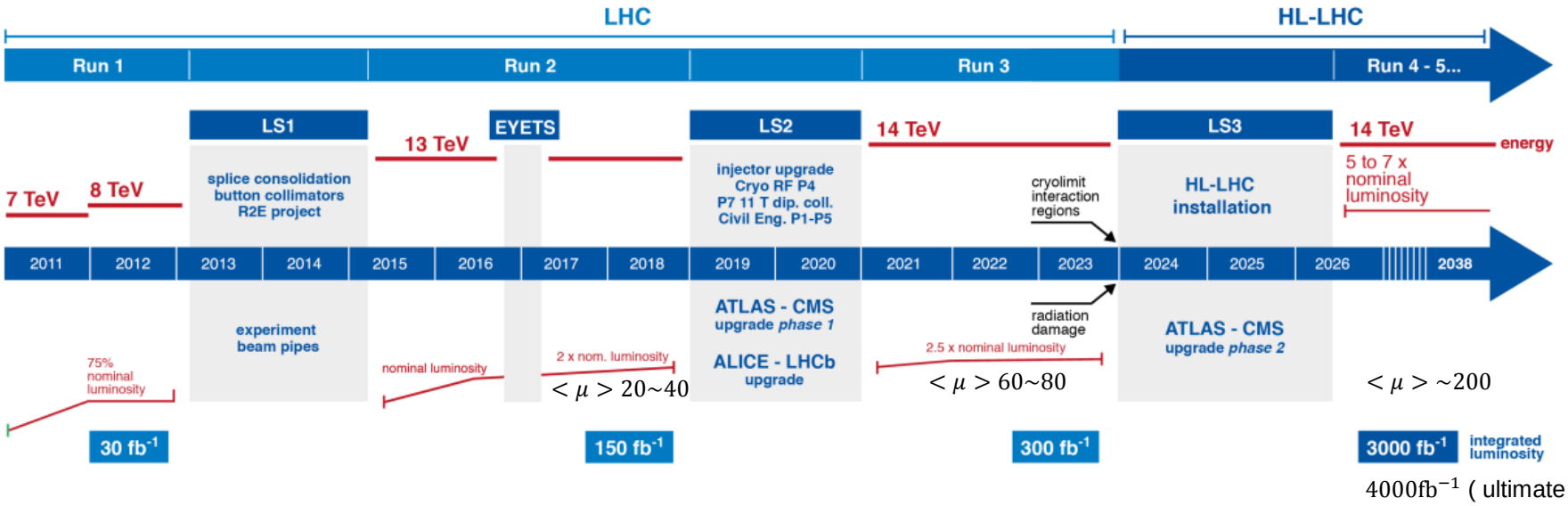
On behalf of the ATLAS Chinese Clusters

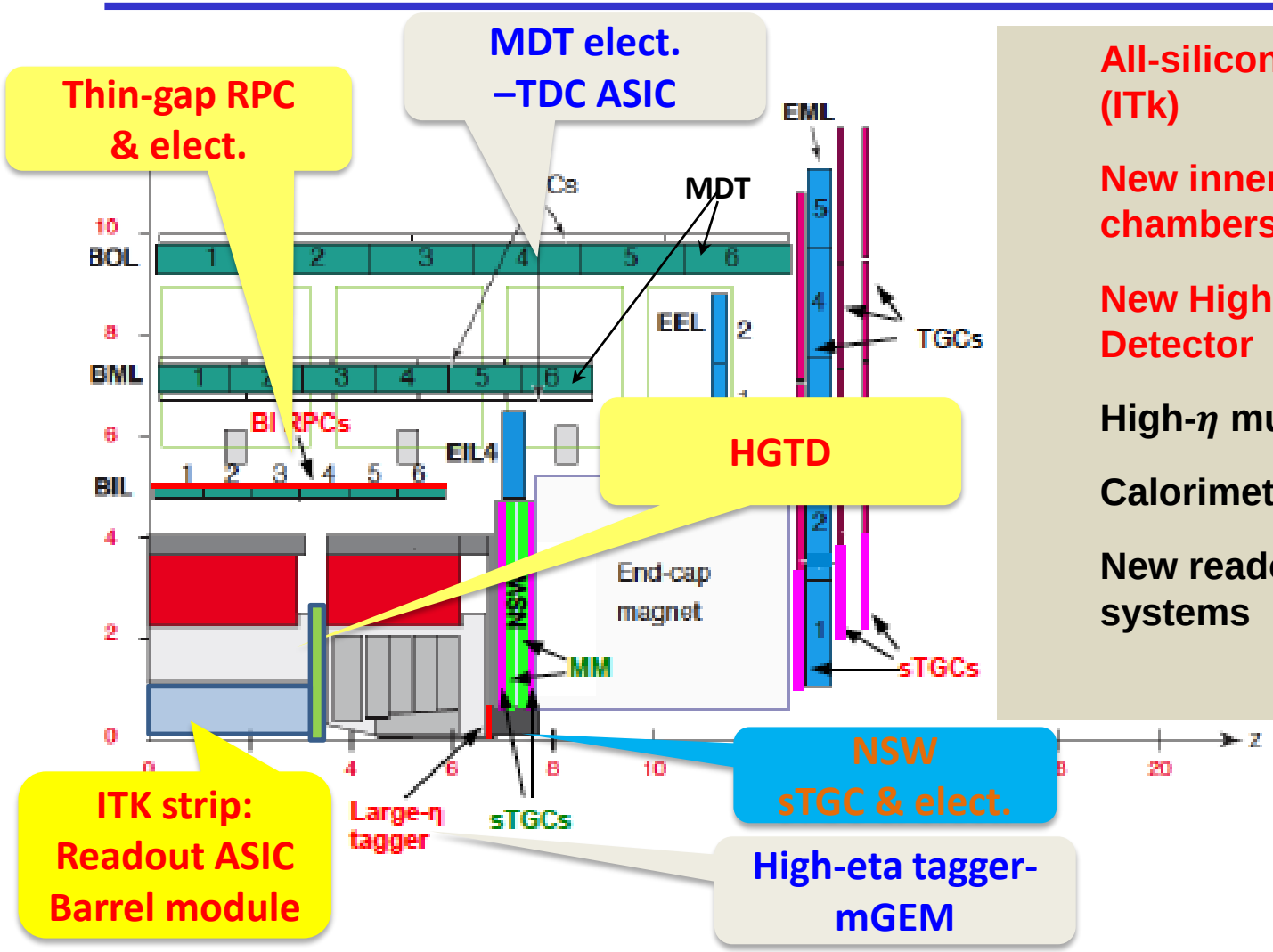
The 7th CLHCP workshop (Nanjing), 28 Nov 2020, Zoom

Roadmap to HL-LHC



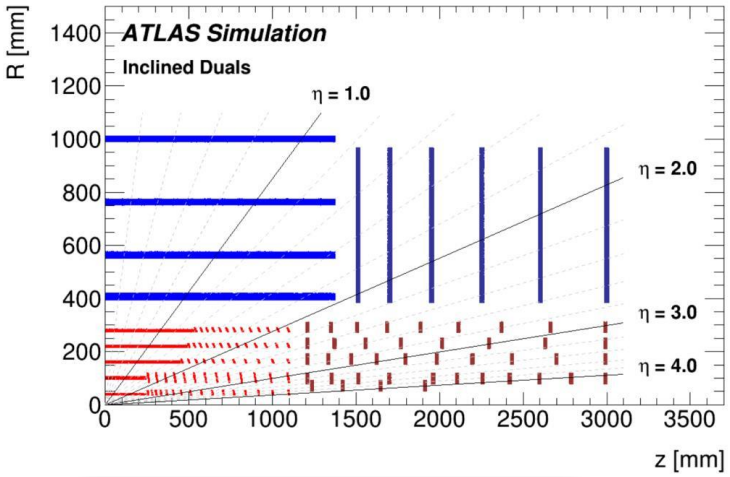
- The high-luminosity LHC (HL-LHC) is intended to provide $300\ \mathrm{fb}^{-1}$ of data each year
  - An instantaneous luminosity of $\mathcal{L}\sim 7.5\times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - pile-up, $<\mu>=200$
- The ATLAS detector would be upgraded to cope with the increased occupancies and data rates.

The Upgrades of ATLAS Detector

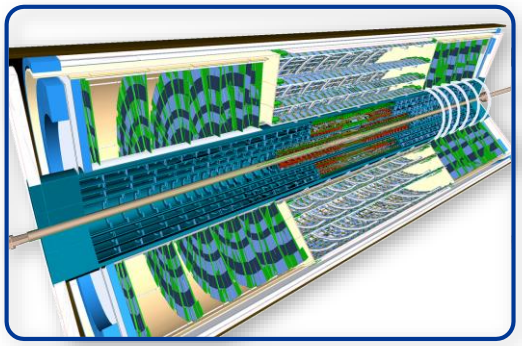


- All-silicon new Inner Tracker (ITk)
- New inner Muon barrel trigger chambers
- New High-Granularity Timing Detector
- High-η muon tagger
- Calorimeters (only TDAQ)
- New readout electronics for all systems

Inner Tracker Strip Detector



- All-silicon Inner Tracker (ITk) with extended coverage ($|\eta|<4$) to improved the tracking performance
- IHEP and THU committed to **deliver 1000 strip** barrel modules (10m^2 of sensor surface)
- 10% of total strip barrel modules (US 50% + UK 40%)
- Additional contributions to strip barrel system **integration, installation and commissioning**

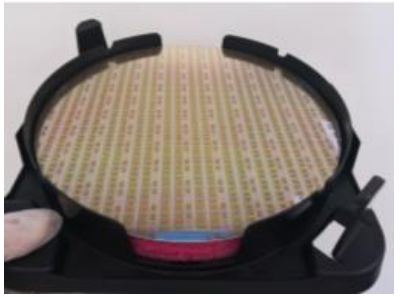


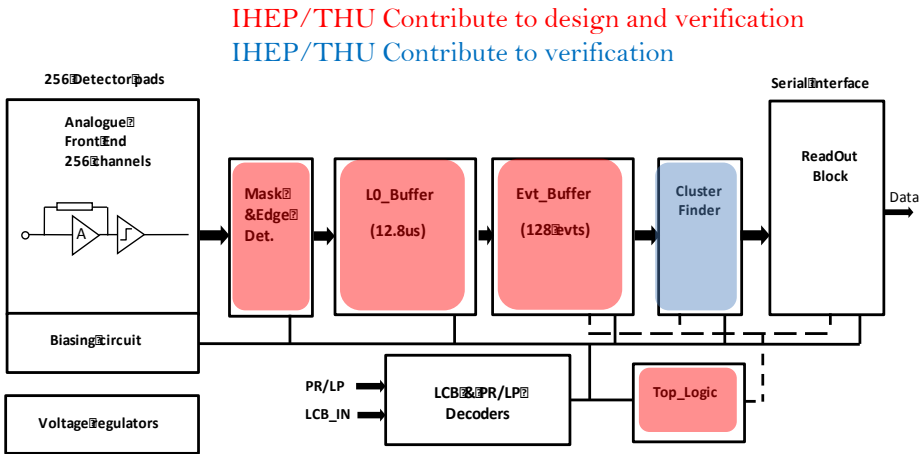
Objectives

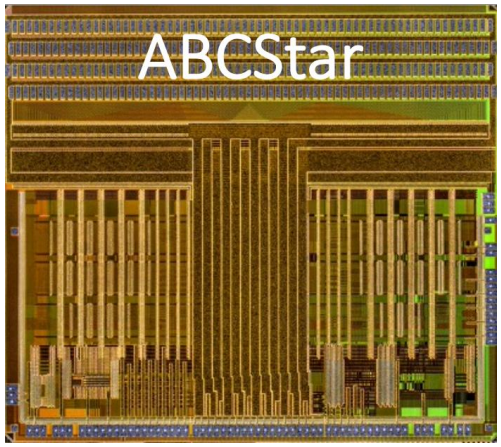
- Radiation hard readout ASIC **design and study**
- High performance Strip detector **module production**
- Complex silicon detector **system integration**

Radiation Hard FE ASICs

- ABC-STAR chips with readout architecture redesigned to **cope with the increased trigger rate**
- Significant contributions to design and verification of digital blocks
- Passed Production Readiness Review (PRR) on **Oct 2021**
  Ready to launch production of ABCStarv1



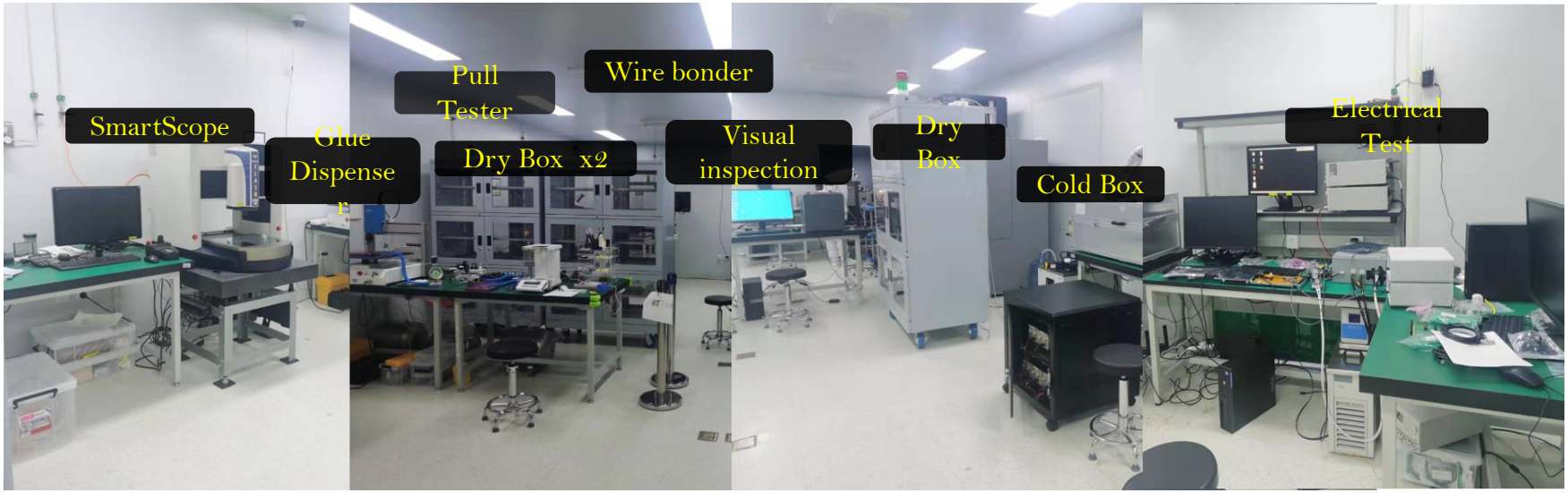




Export license available for shipment of chips from CERN to IHEP

Infrastructure Readiness

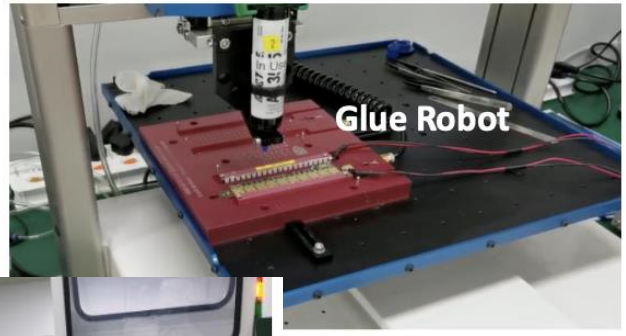
- Constructed ISO Class 7 clean room at IHEP
- Most of the instruments required for module production in place
- Production Site Qualification **in progress**



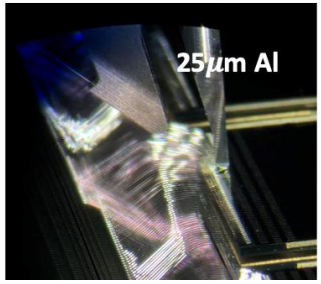
Module Prototyping

- Producing module prototypes exactly following the Quality Control steps
- Produced fully functional electrical modules

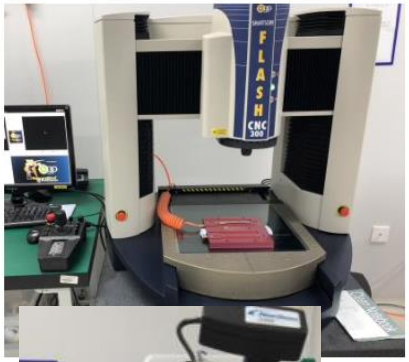
Calibration of glue amount

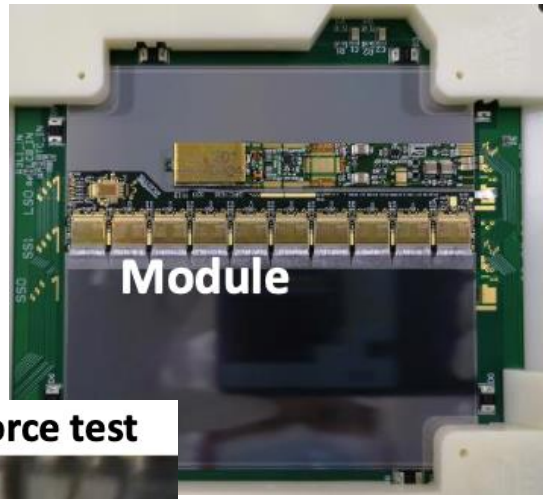


Wire bonding

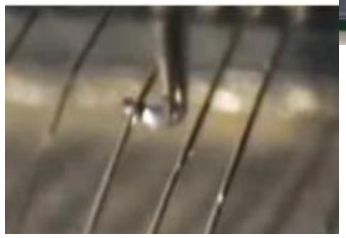


Metrology of glue thickness



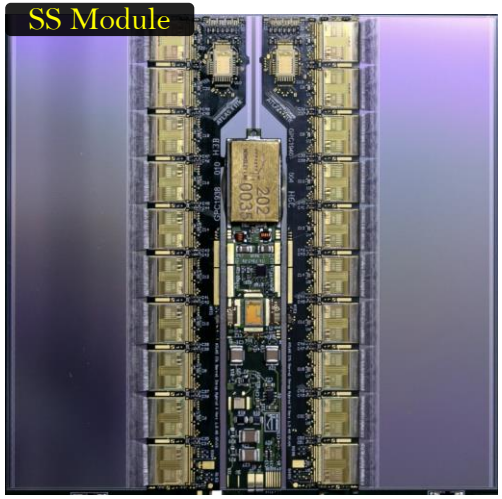


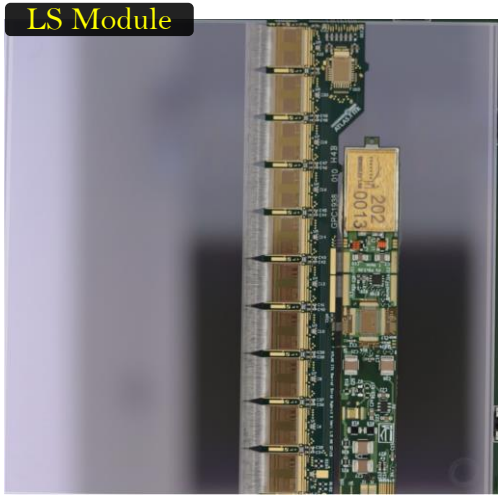
Pull force test

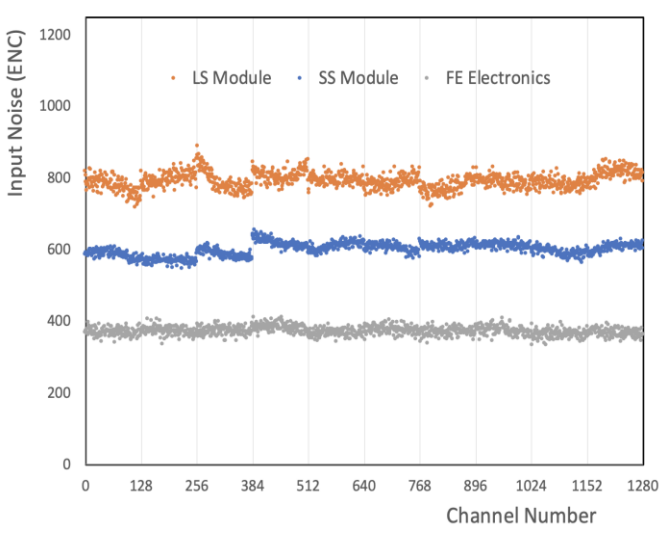


Produced Modules in IHEP

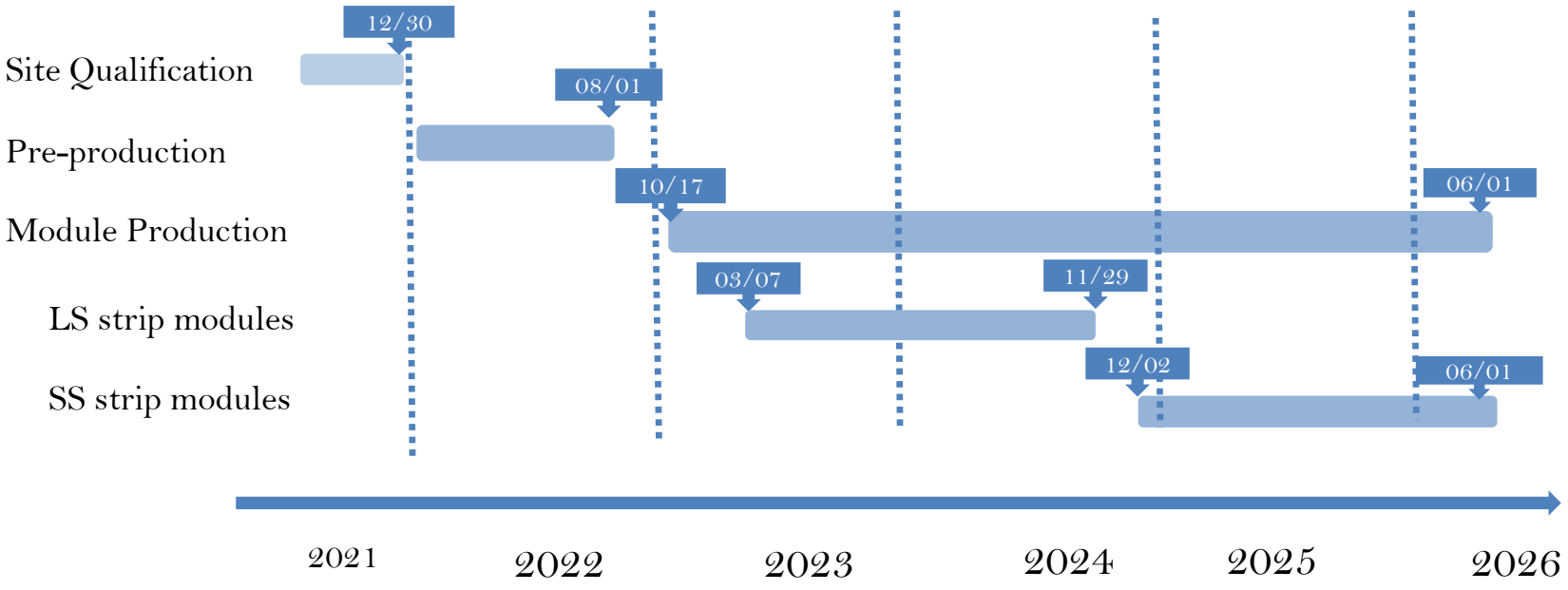
- 5 LS Modules + 3 SS Modules
  - 2 prototype LS Modules
  - Passed electrical tests with expected noise level
  - SS modules have been sent to UK for stave construction







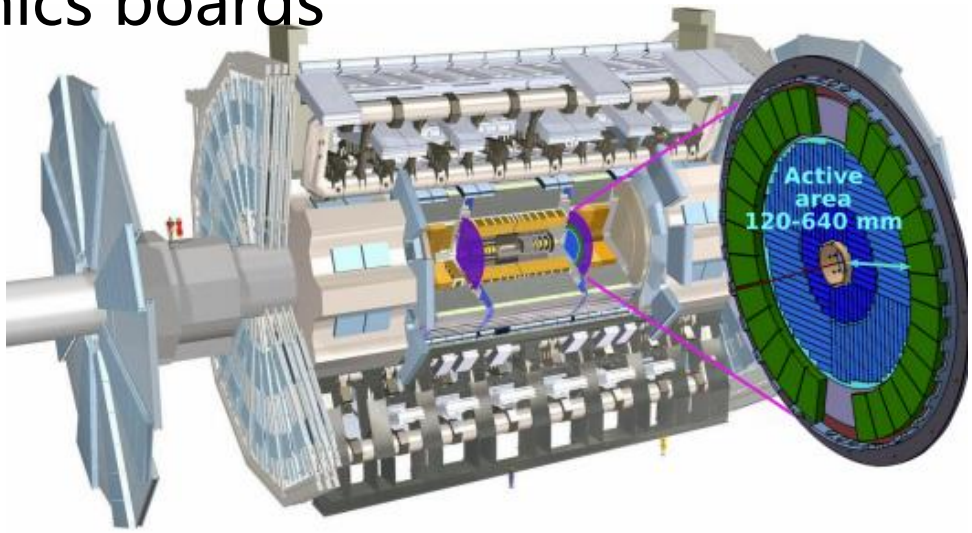
Module production schedule



High granularity timing detector (HGTD)

ATLAS High Granularity Timing Detector (HGTD)

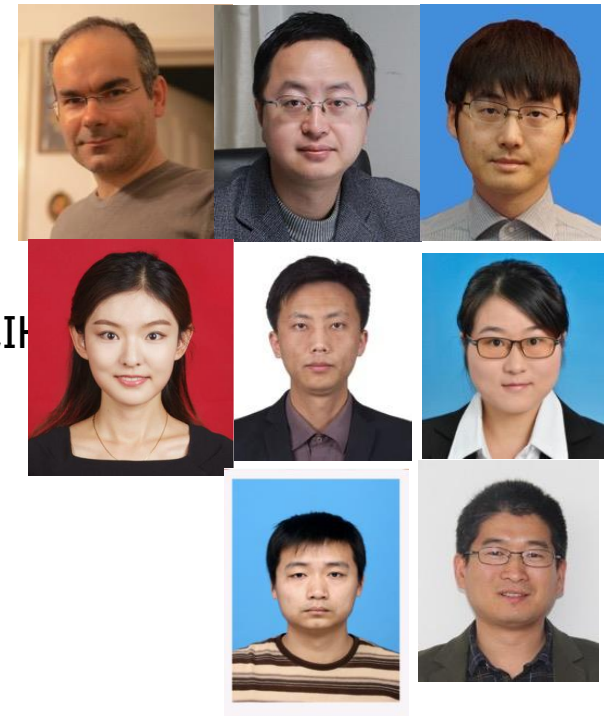
- Goal: Timing measurement to reduce pileup in HL-LHC
  - **MIP timing measurement (30-50ps)**
  - **6.4m² area silicon detector**
  - **Granularity: ~1mm²**
  - **Radiation hardness : > 2.5x10¹⁵ N_{eq} /cm² and 2MGy**
- China group is making leading contributions in HGTD
  - 100% Peripheral electronics boards
  - >33% LGAD sensor
  - 45% module assembly
  - 50% ASIC testing
  - >16% HV system

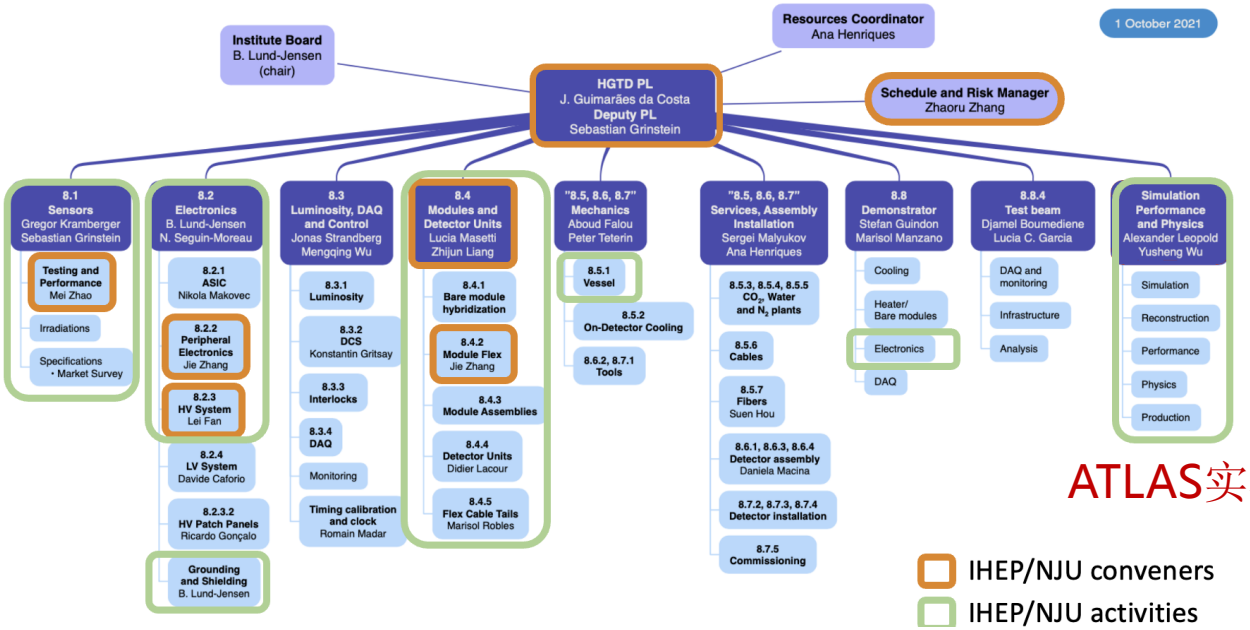


***z* position: ± 3.5 m**

ATLAS HGTD project – Leadership

- ATLAS China is leading HGTD project, taking important management role
- 1st time, China took project leader on ATLAS subdetector
  - Project leader (Joao Guimaraes da Costa，IHEP)
  - Detector Module Level-2 convener（Zhijun Liang,IHEP)
  - Simulation group Level-2 convener （YuSheng，USTC）
  - Risk manager （Zhaoru Zhang，IHEP)
  - Peripheral board and module flex L3 convener（Jie Zhang,IH
  - Sensor testing Level-3 convener （Mei Zhao，IHEP）
  - HV system Level-3 convener (Lei Fan, IHEP)
  - HGTD Speaker committee （Yanwen Liu，USTC）



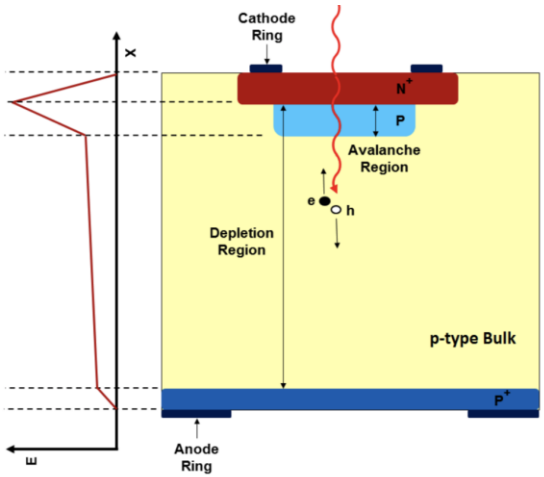


ATLAS实验HGTD项目管理层架构

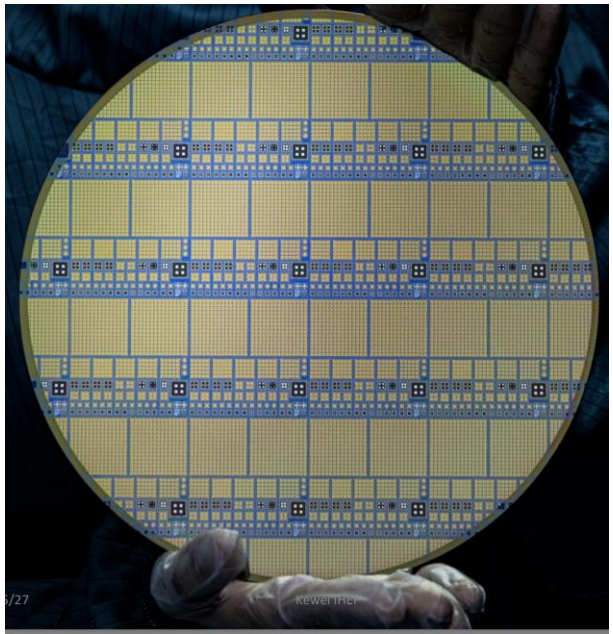
Ultra-fast timing silicon sensor R & D

- Ultra-fast sensor based on Low-Gain Avalanche Diode (LGAD)
- IHEP developed full-size LGAD sensor (15*15 channels)
  - IHEP team design and testing, IME CAS engineering run
  - Single pad yield 99.3%, good uniformity
  - Aim to provide >7000 sensors to ATLAS (>33%)

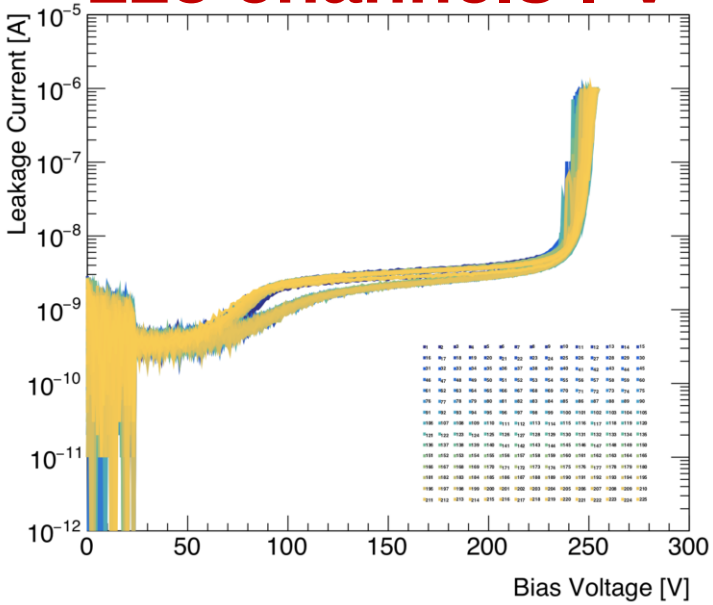
LGAD



IHEP-IME LGAD 8-inch wafer



Good uniformity 225 channels I-V



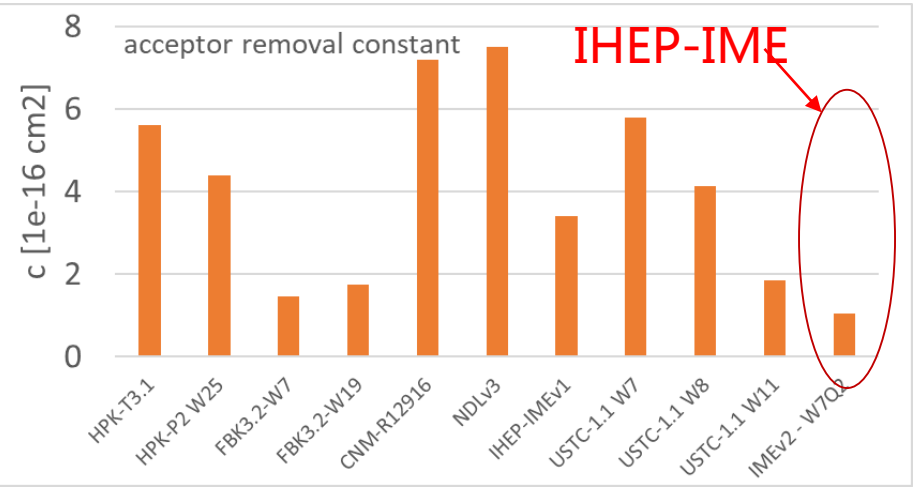
Radiation-hard LGAD sensor

- Challenge at HGTD:
  - Single event burn-out after irradiation at HV (>600V)
- IHEP-IME explored radiation-hard LGAD
  - Optimized carbon doping
  - Got the most radiation hard LGAD
  - Lowest acceptor removal rate

Single event burn-out

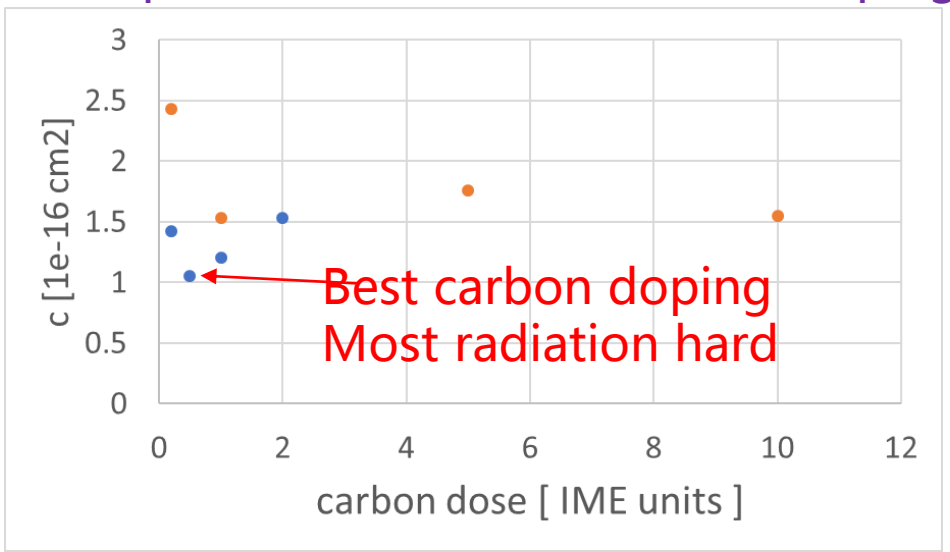
The most radiation hard LGAD: IHEP-IME

Acceptor removal for different LGADs



IHEP team optimized carbon doping

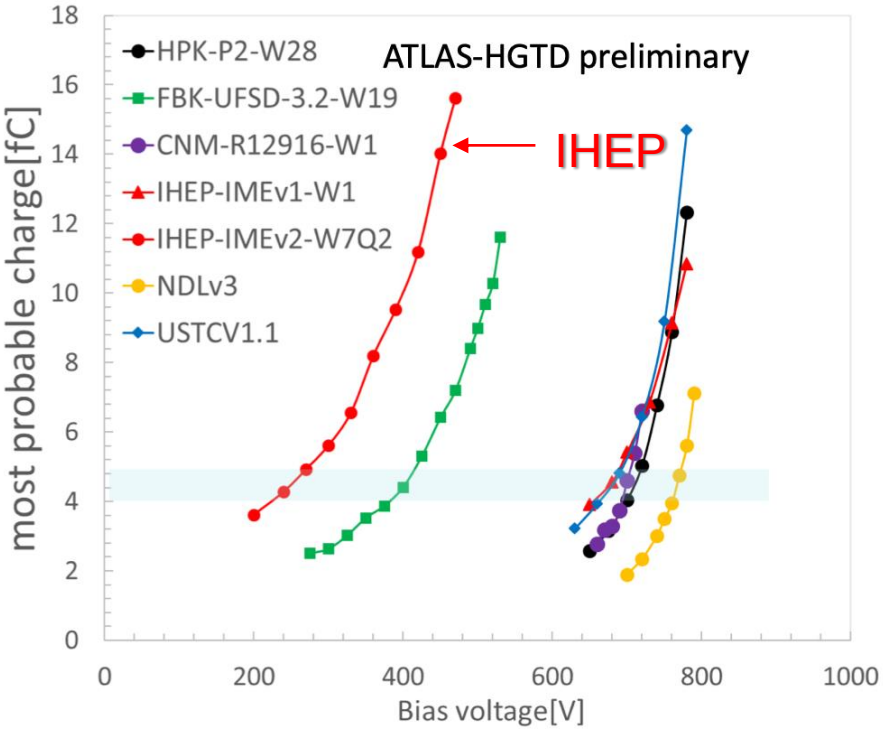
acceptor removal rate vs carbon doping



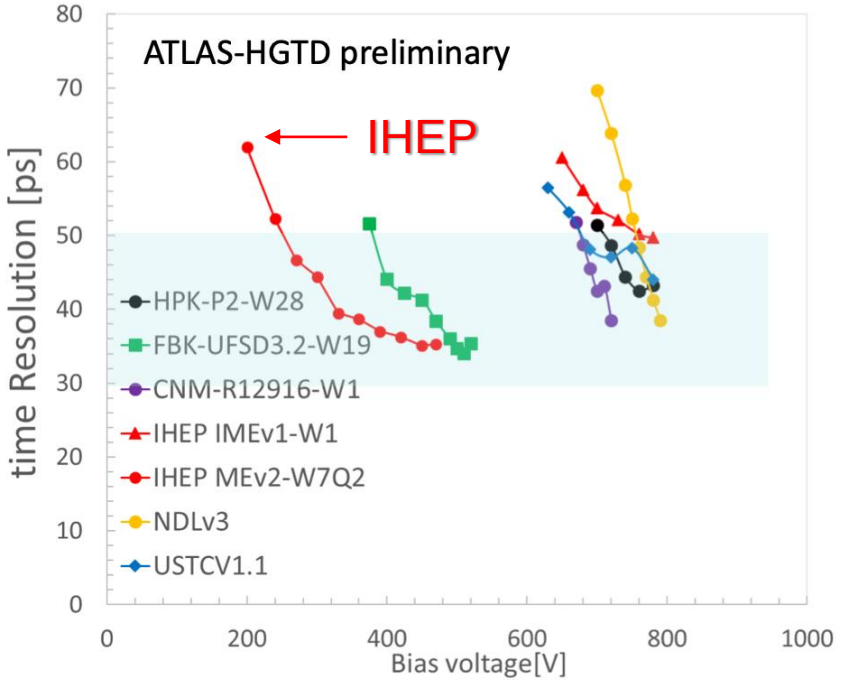
Radiation-hard LGAD sensor

- IHEP developed the most radiation-hard LGAD sensor
  - Time resolution can reach 35ps even after irradiation
  - High charge collection at low bias voltage (300V)
  - Low bias voltage to avoid single event burn-out
  - No LGAD burn-out at CERN high intensive beam

Charge collection after irradiation from different foundries



Time resolution after irradiation from different foundries

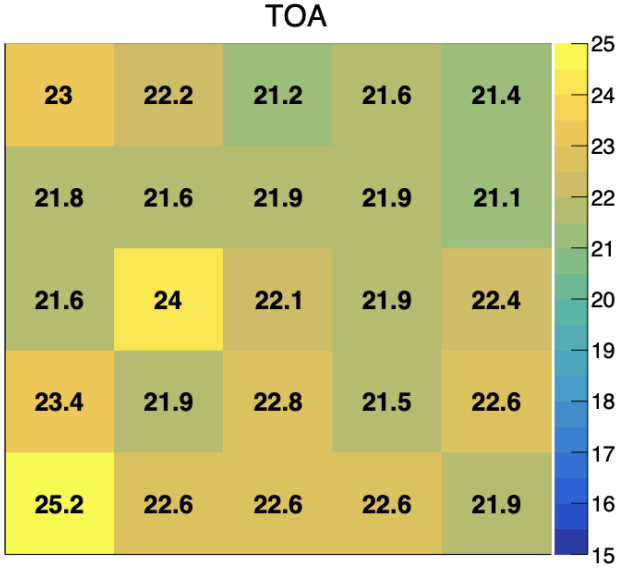


more on IMEv2 run at RD50 workshop

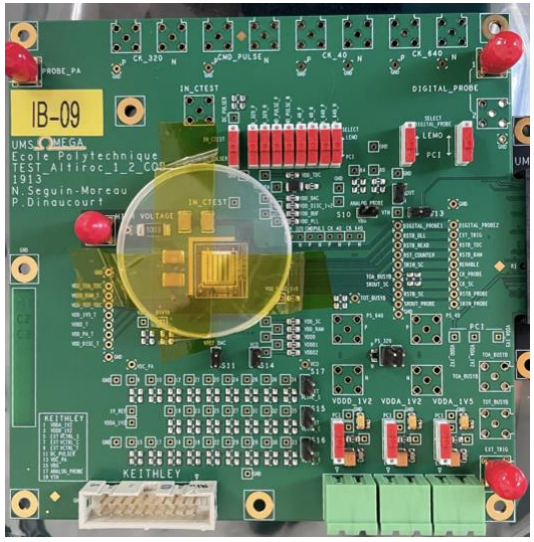
Fast ASIC readout chip : ALTIROC

- ALTIROC: Radiation-hard fast TDC with 10ps resolution
- China is responsible for 50% of ASIC wafer testing
  - IHEP tested small ASIC prototype ALTIROC1
  - Start testing ALTIROC2 (full-size chip in 8-inch wafer)

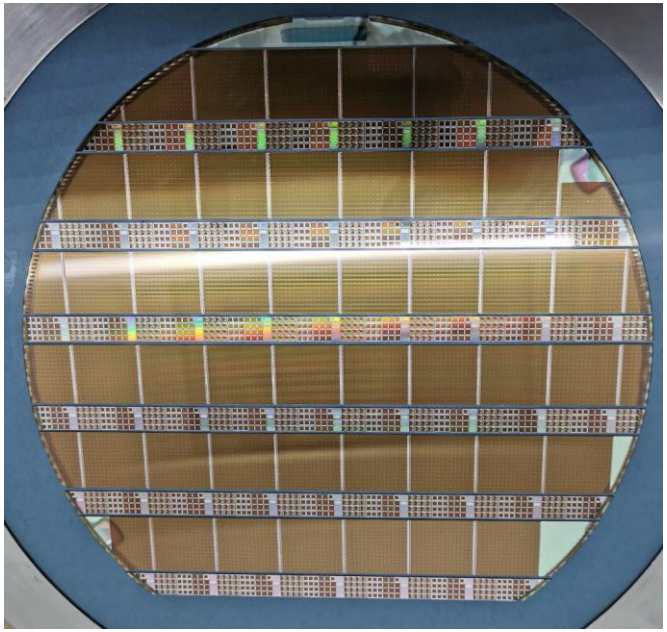
Good timing uniformity
25 channels



ALTIROC1 ASIC test

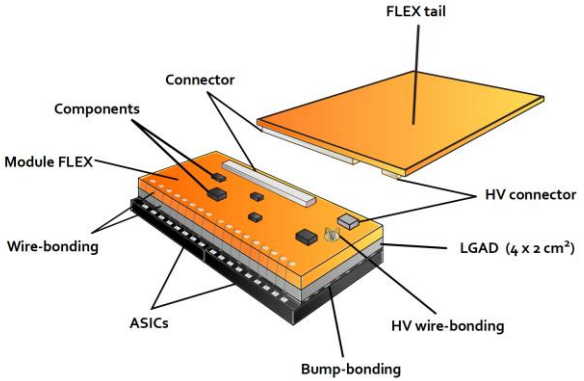


ALTIROC2 8-inch wafer



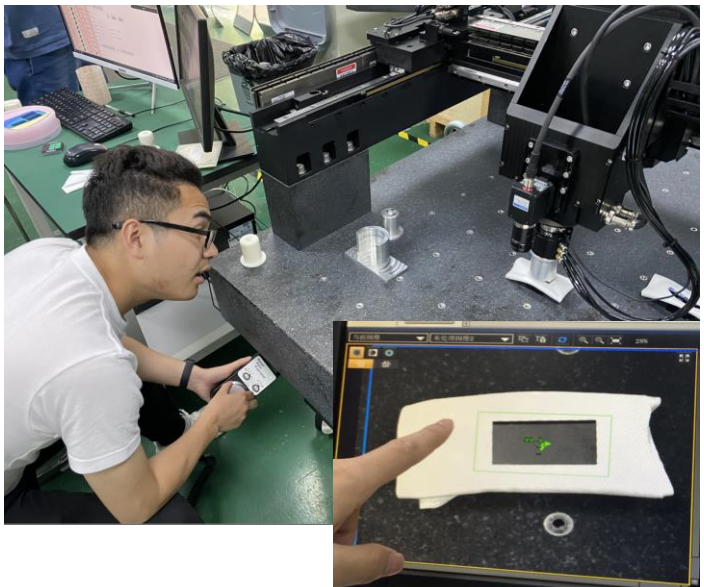
HGTD detector modules

- China will assembly more than 4000 modules (~45%)
- IHEP is leading module assembly R & D and production
  - Design the flexible PCB for module
  - Bump bonding (ASIC + sensor)
- IHEP developed domestic gantry system
  - Automatic module assembly
  - Aim to build 10 modules per day

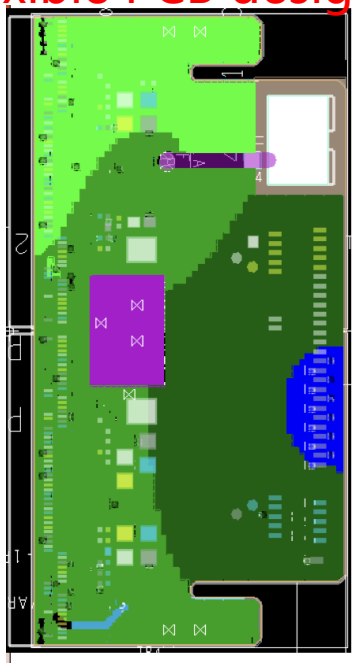


IHEP mini-module in beam test

Gantry automatic assembly

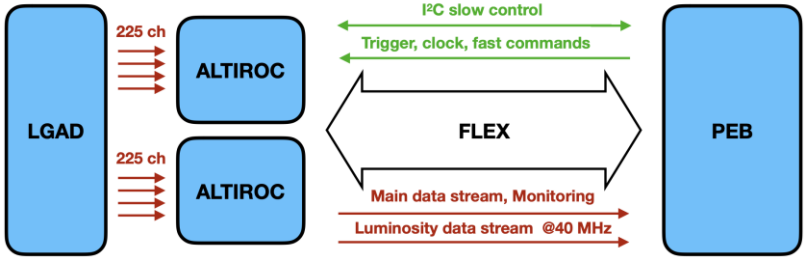


flexible PCB design

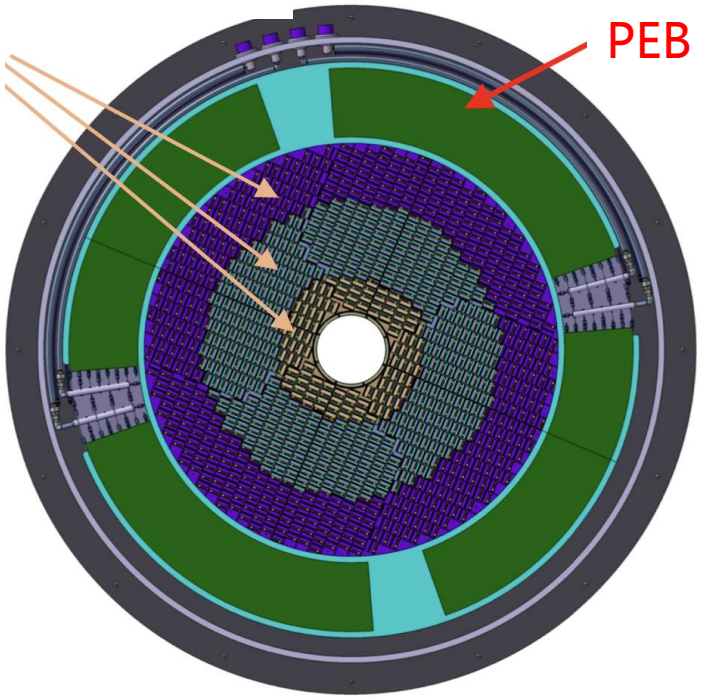


Peripheral electronics boards (PEB)

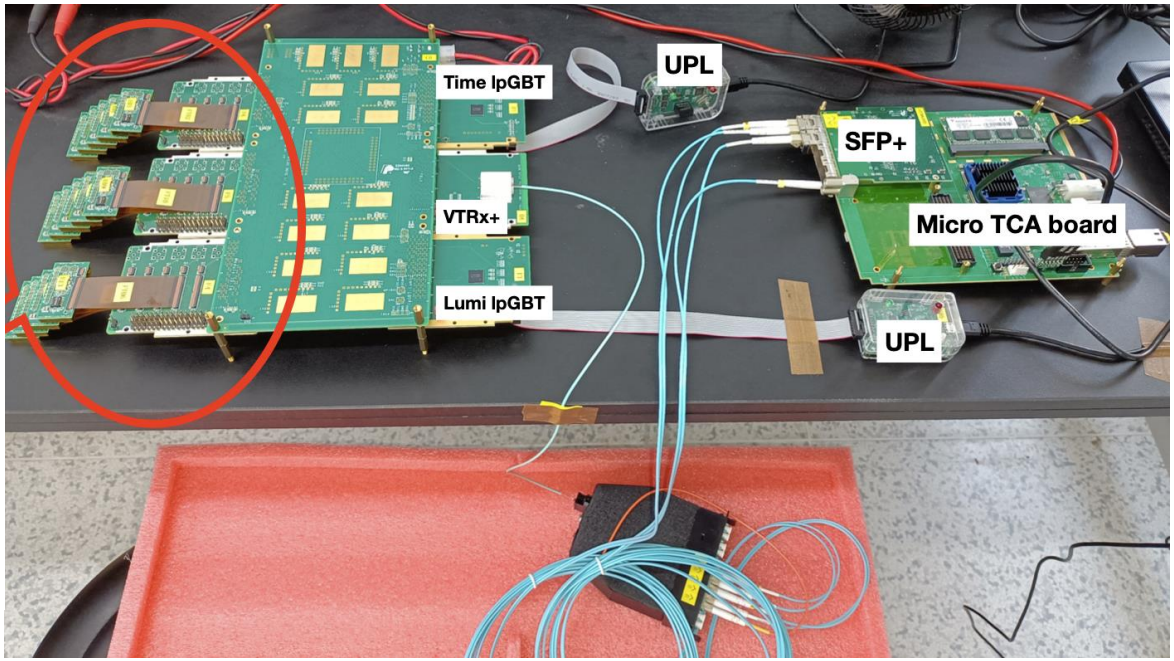
- China contributed 100% of Peripheral electronics boards
- IHEP/NJU leading PEB design and prototyping
  - DAQ demonstrator prototype
  - read 14 modules @320Mbps



modules



DAQ demonstrator



USTC activities on HGTD

- **Sensor design and production**: USTC-IME-v2 and v2.1 LGAD show promising performance in tests [See Xiao Yang's talk at this WS]

- **Measurements of large-array sensors with probe card** [See Xiangxuan Zheng and Jiajin Ge's talks at this WS]

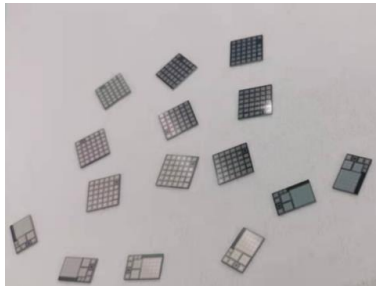
- **ASIC chip testing: tested ALTIROC1_v2 and v3,** prepared to test ALTIROC2 [See Yongkang Cai's talk at this WS]

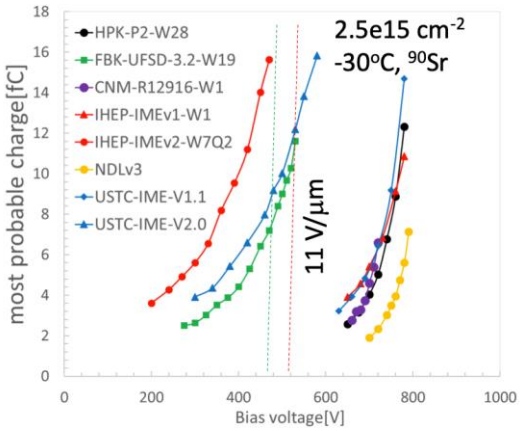
- **Assembly**: bare-module hybridization at SINANO

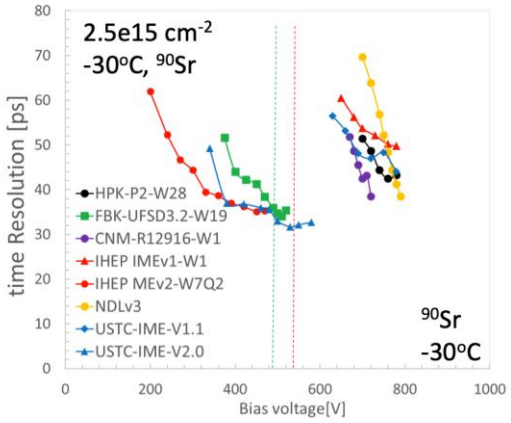
Sensor design and production

- USTC-2.0 and USTC-2.1 sensors are fabricated at IME (produced five 8” wafers for each version).
- USTC-2.0 are irradiated with reactor neutrons at JSI and with 450 GeV protons at CERN SPS
- Preliminary results show promising performances

Diced sensors

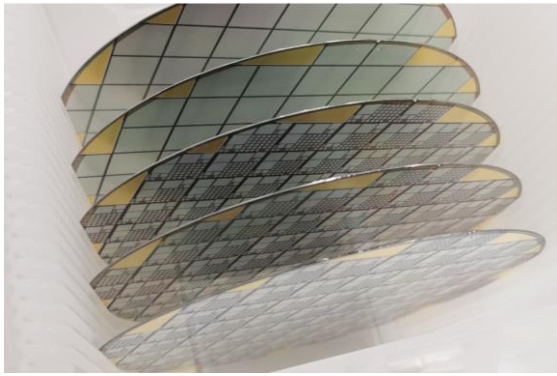






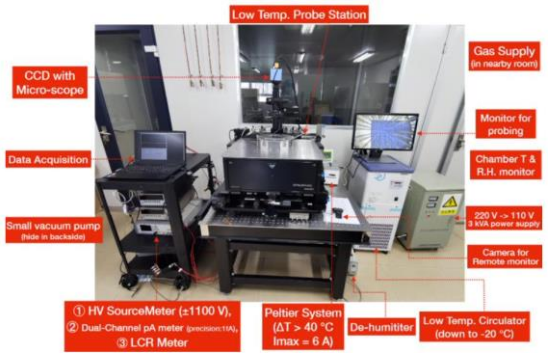
Plots shown by Gregor Kramberger at HGTD mini-week in 2021/11

Sensor wafers after UBM

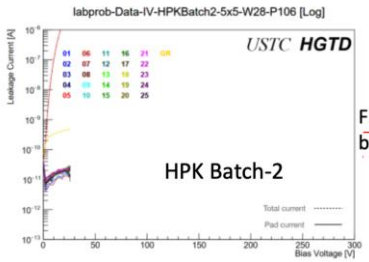


Measurement of large-array sensors

- USTC study the impact of a bad pad inside a large LGAD sensor (pads of 15x15 array)
- Very systematic and conclusive studies done with probe card
- Brief conclusion: large currents of a bad pads collected by the grounded guard-ring or other pads nearby via punch-through

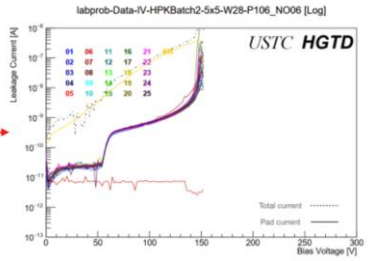


15x15 probe card and digital switcher



1 HPK 5x5 sensor with 1 bad pad:
all pads and GR grounded

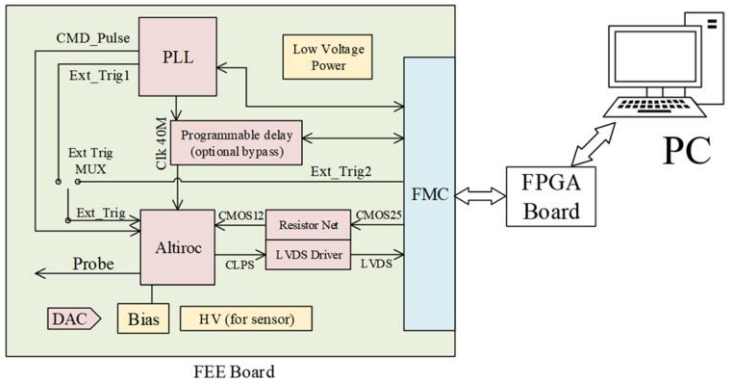
Floating bad pad



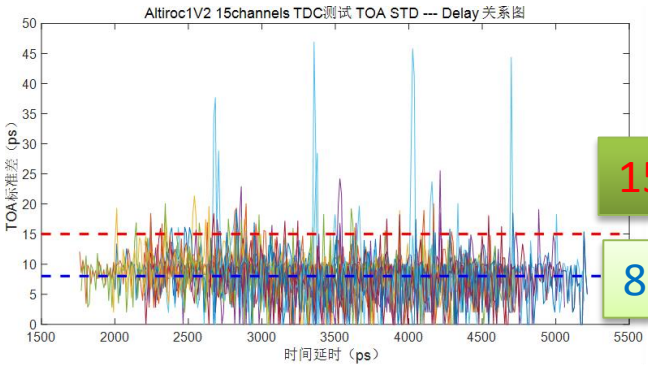
1 HPK 5x5 sensor with 1 bad pad:
Bad pad floating, others grounded.

ALTIROC1 ASIC chip measurements

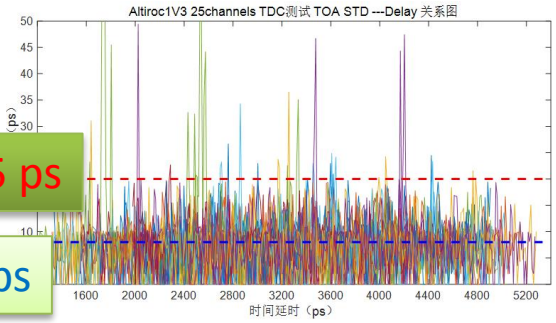
- USTC designed a system to test the ALTIROC1 ASIC chips.
- Tested v2 and v3 chips: see TOA RMS vs. delay below, problematic channels seen.
- Prepared to test the ALTIROC2 chips



ALTIROC1_v2

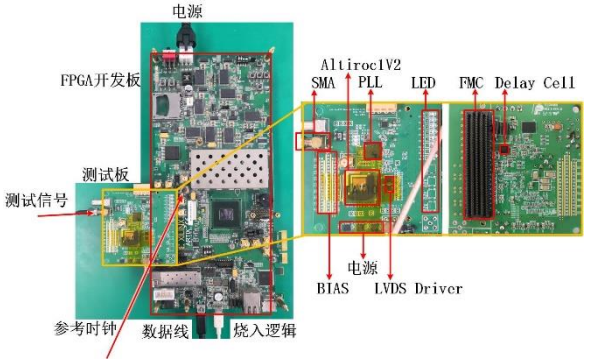


ALTIROC1_v3



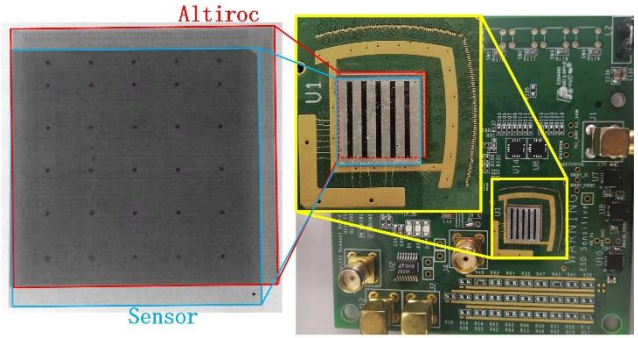
15 ps

8ps

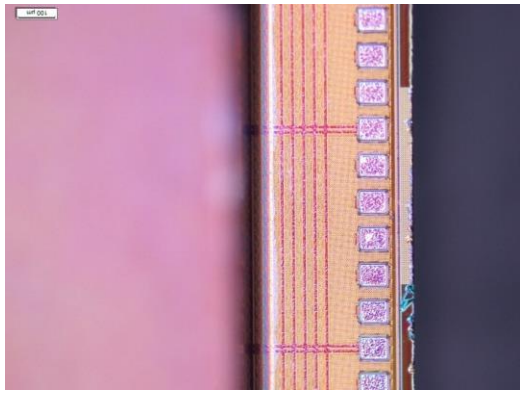


Progress on the module assembly

- USTC is setting up a production site, expected to be ready in 2022
- SINANO has been studying the bare-module hybridization process
  - First attempt was not successful: shorts between sensor and ASIC chip
  - Second prototype will be ready by end of November and will be tested at USTC(test system is ready)



Module test system

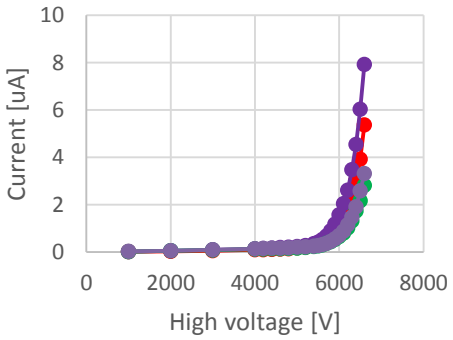


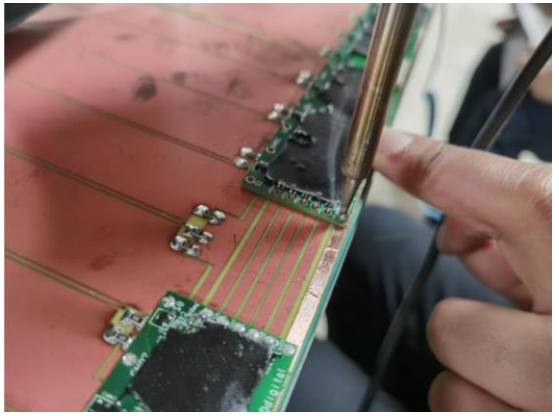
Optical inspection of the pads on ASIC after bump-bonding

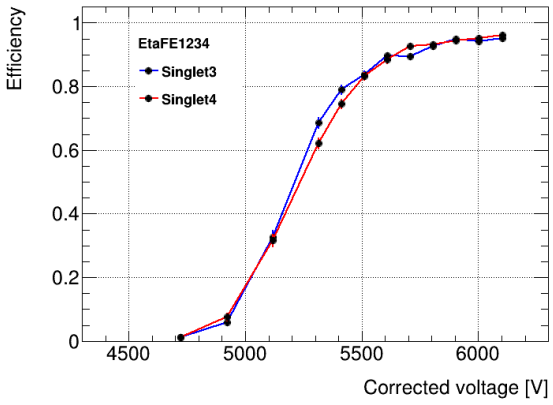
Phase-II RPC upgrade

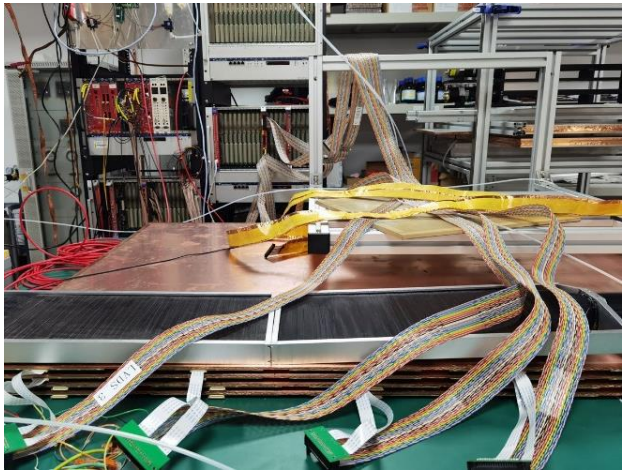
Full size RPC singlets assembly and test

- Assembly procedures
  - Gas gap training & test
  - FE board soldering & connectivity test
  - Resistors soldering
  - Singlet assembly
  - Assembly speed: ~ 2 days / singlet
- Test
  - Efficiency curves: reach up to 95%
  - Cluster size: ~2
  - Time resolution: better than $1\ ns$



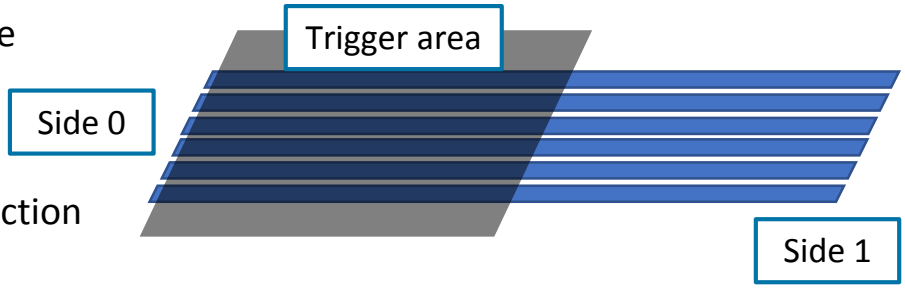




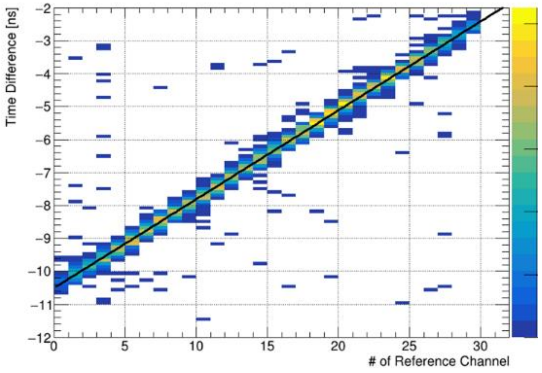


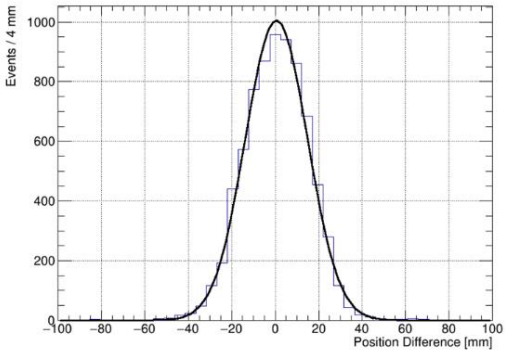
Double-end readout test with chip-based FEE

- Motivation
  - To check if FEE works properly in double-end scheme
  - To check the space resolution performance
- Experiment setup
  - FEE board: chip-based, the same with Phase-I production
  - 32 BIS7s RPC gives reference position
  - TDC: V1190 (100 ps resolution)



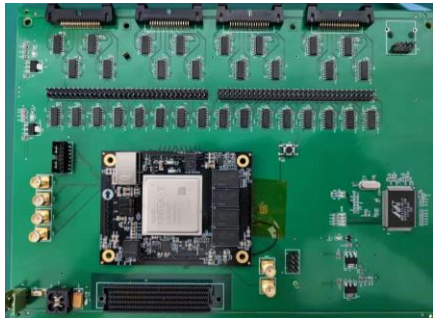
- Reconstruction
  - Get $\Delta t - x$ relationship
  - Reconstruction position and compare with real position
- Results:
  - Double-end efficiency up to 91%
  - Space resolution $\sim 12\ mm$

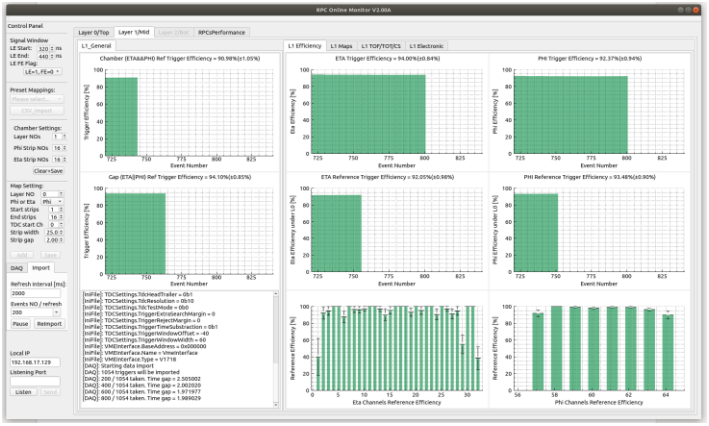




Procedures and facilities for the mass production

- Prepare for the coming mass production: ~ 300 RPC singlets
- Basic production procedures and facilities have been established
  - The manuals of manufacturing processes
  - The QA&QC system
  - The online monitor for the qualification test
  - A large cosmic ray trigger system: 1.3 x 2 m^2
  - A FPGA based TDC system: 128ch/board
  - The flatness check for the honeycomb panels



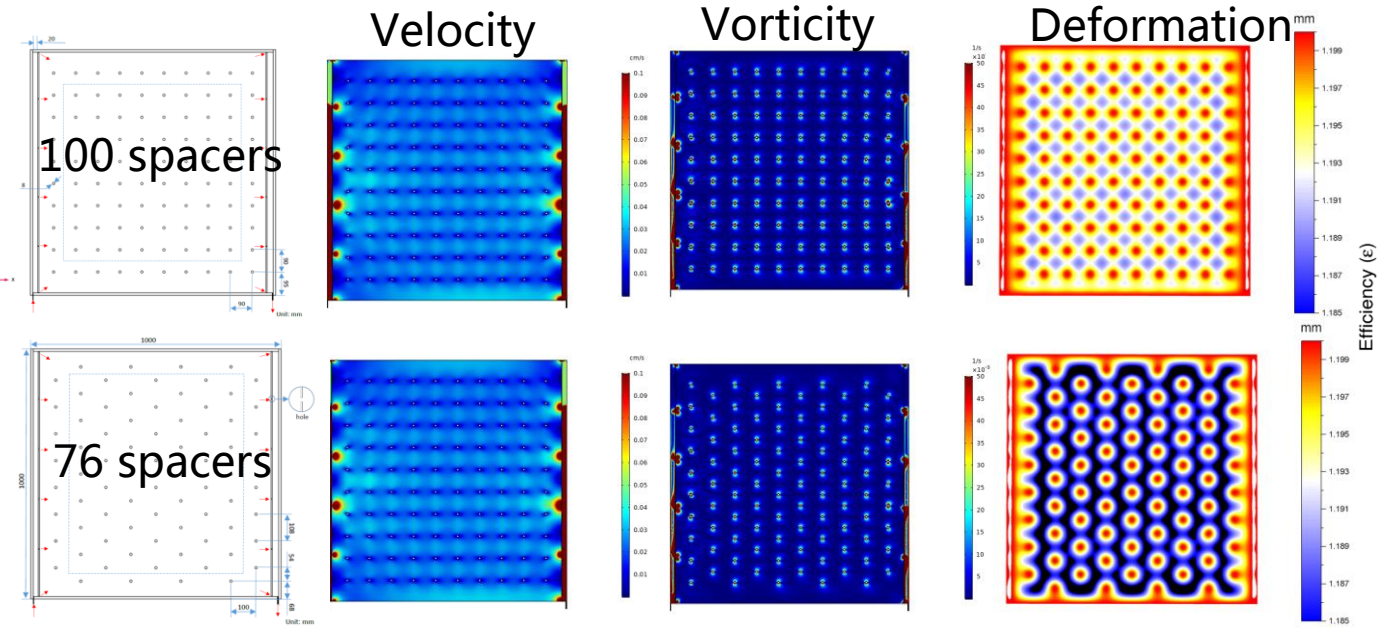


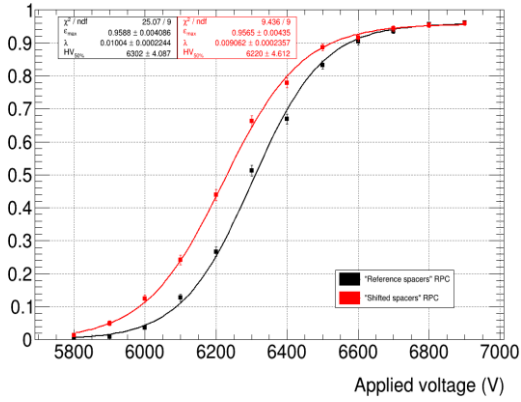
RPC gas flow simulation and cosmic results @SJTU

- Gas flow and electric-field has been simulated

  → New chamber design with **24% less spacer** has been built
  - Easier to build
  - Less dead zones

- 1mx1m chambers with “Shifted spacers” has been built and test with cosmic ray.





Submitted to JINST (https://arxiv.org/abs/2108.12843)

Summary

- Many activities in several main upgrade projects have been carried out in both Chinese clusters.
  - The inner tracker strip detector production site qualification in progress
  - RPC production procedures and facilities have been established
  - HGTD sensors of both Chinese cluster showing promising performance, the chip testing system developed.

Thank you!