ATLAS High Granularity Timing Detector Activity at IHEP/NJU

Jie Zhang (张杰)
on behalf of the IHEP/NJU HGTD collaboration

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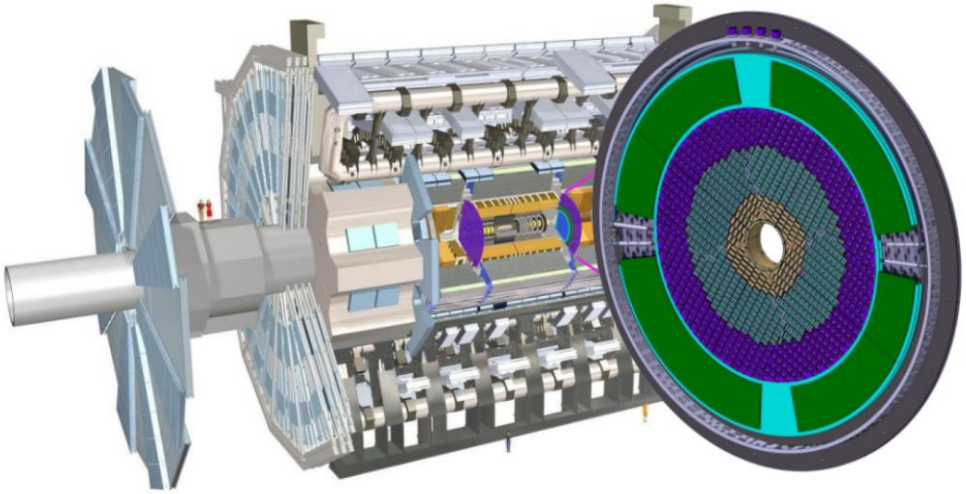
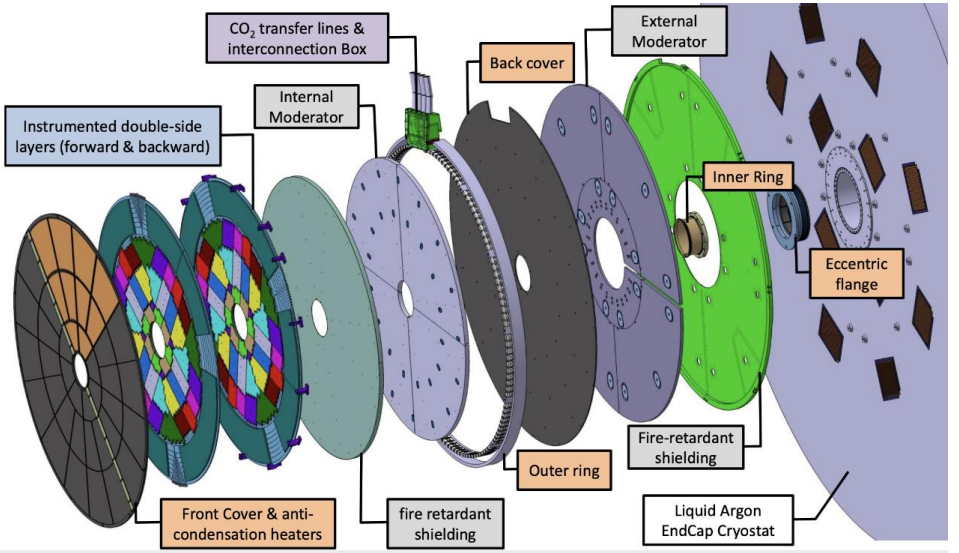
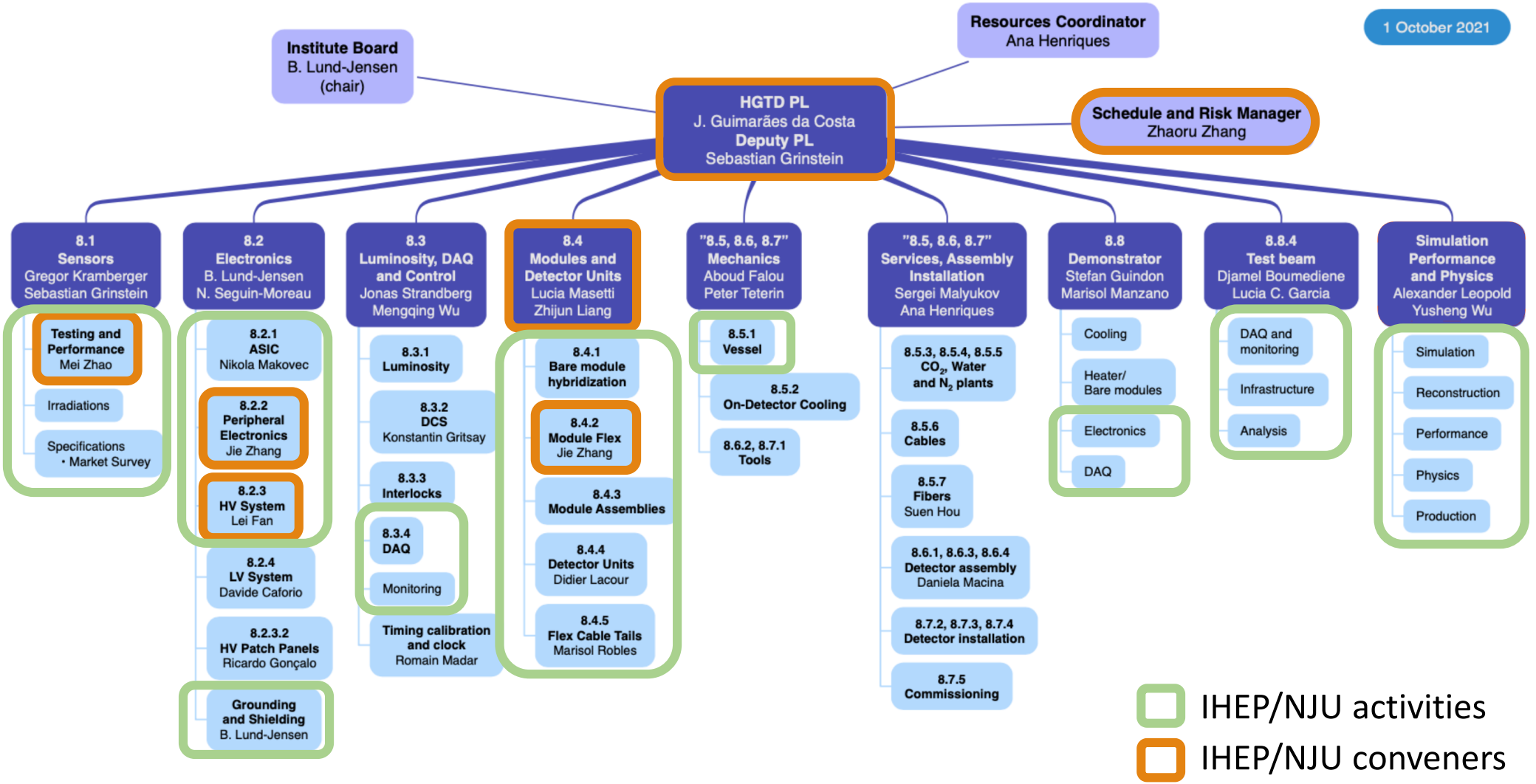
High Granularity Timing Detector (HGTD)

- High precision timing (per-track resolution of **35-50ps** up to 4000 fb-1) to mitigate pileup effects and improve the ATLAS performance in the forward region (**2.4 ≤ |η| < 4.0**)
- Provide online and offline luminosity measurements by transmitting N_{Hits} per ASIC at 40MHz in outer region
- 2 disks (one per endcap) outside of ITk volume, upstream of the fwd. calorimeters, consisting of **2 double-sided layers** each
- Very limited space in z-direction ↠ overall thickness of 12.5 cm for each disk
- Max expected fluence in “3-ring layout” is **2.5e15 neq/cm²** and sets the radiation hardness requirements for the sensors and electronics

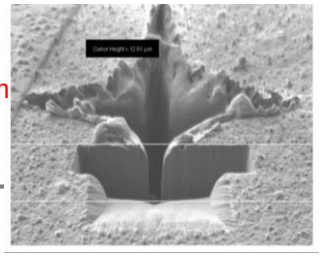




Organization Structure

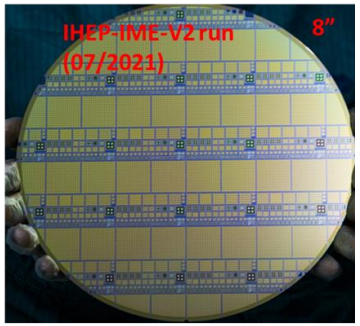


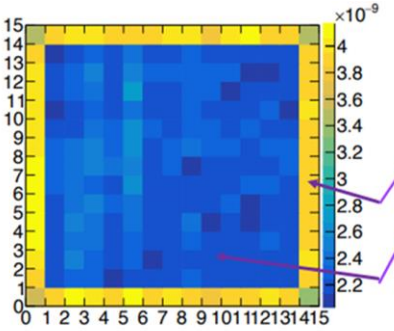
Sensor:
LGAD(Low-Gain Avalanche Detectors)

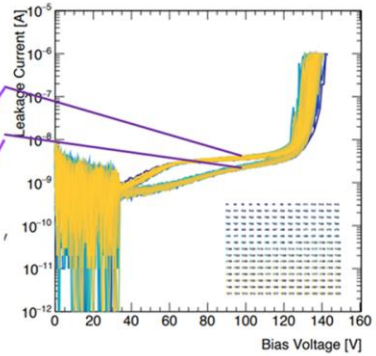


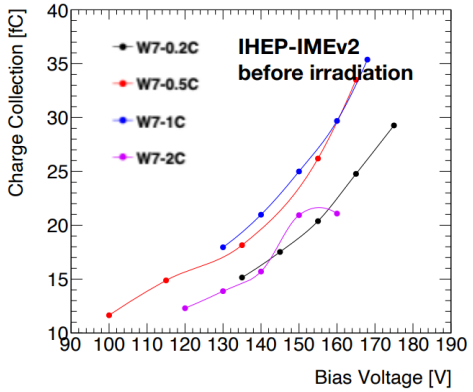
burn mark in the CNM sensor after ATLAS TB in 2018 after the test beam –dimensions are few tens mm (crater photo taken by CNM)

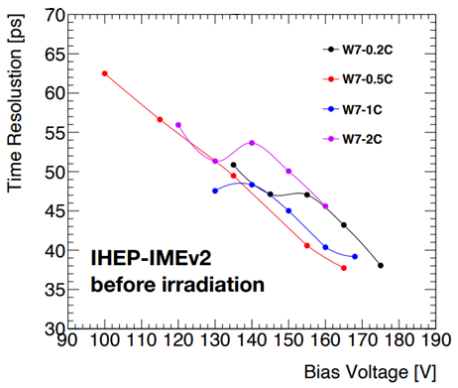
- "Single event burnout" effects observed in LGADs irradiated to the highest fluences
- Concentrated on studies of sensors with carbon enriched gain layers -> can be operated at lower bias voltages
  - Two version of IHEP-IME sensors have been fabricated
  - IHEP-IMEv2 good uniformity
    - BV Spread over 15x15 sensor < 4%
    - Leakage current Spread < 3%
  - IHEP-IMEv2 yield
    - Pad yield ~99.3%
    - 15x15 sensors ~50%

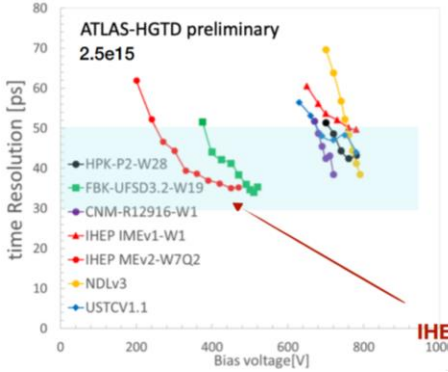


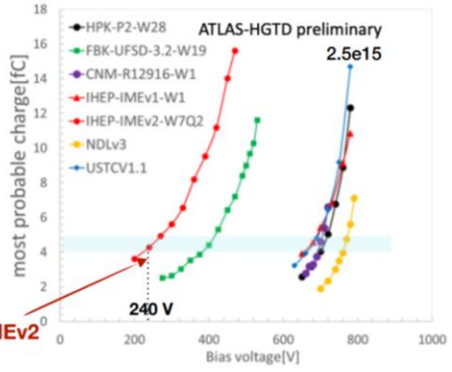








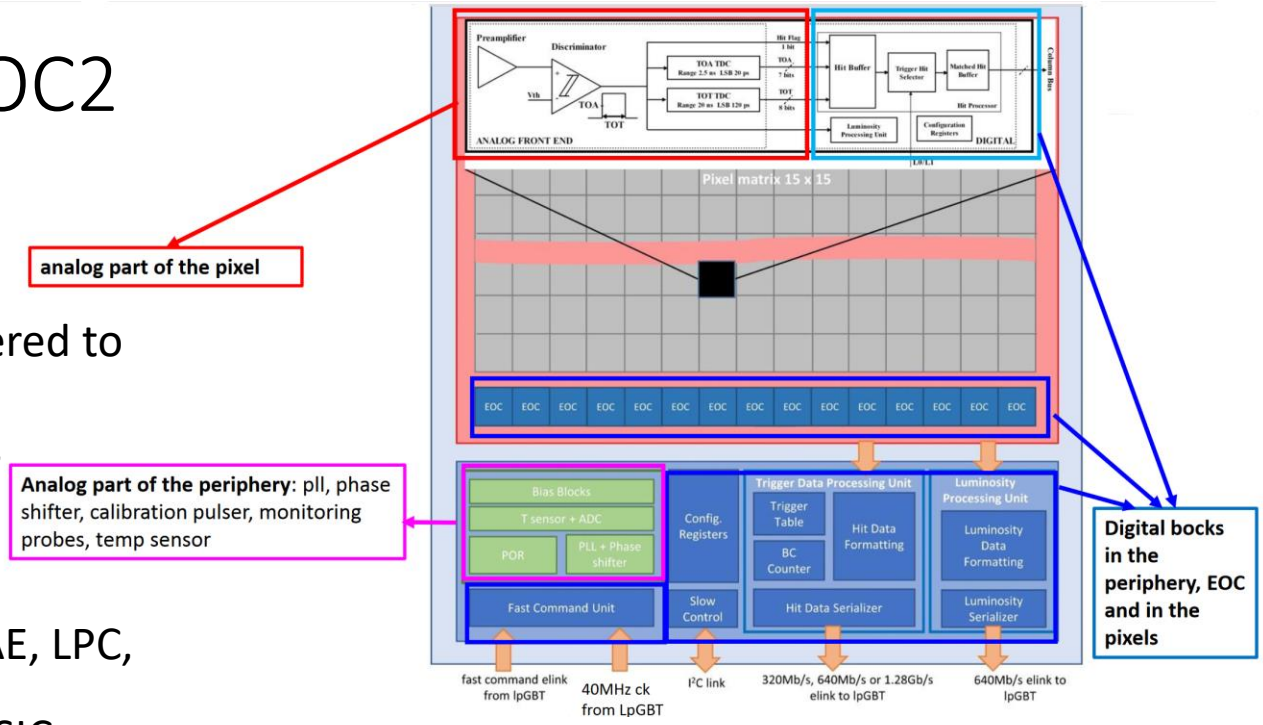


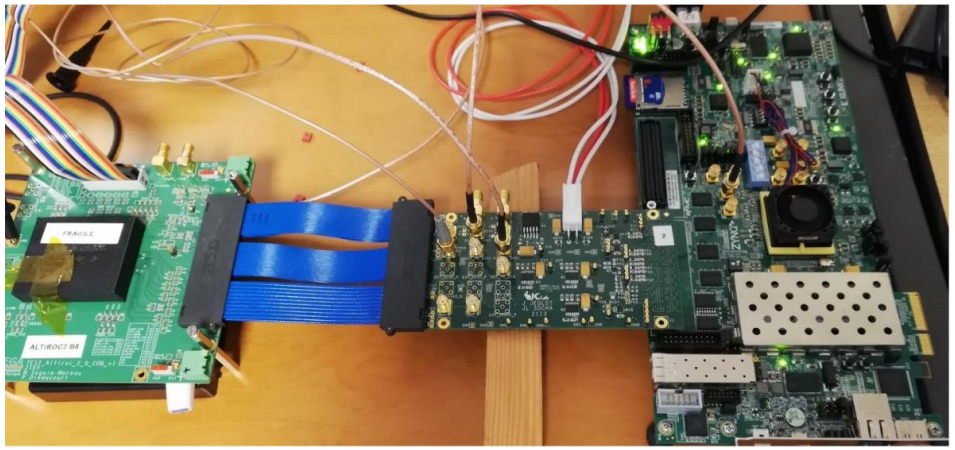


- Before-irradiation performance
  - Collected charge > 30fC
  - Time resolution < 40ps
- Post-irradiation performance
  - Voltage for 4fC < 400V
  - Time resolution < 50ps

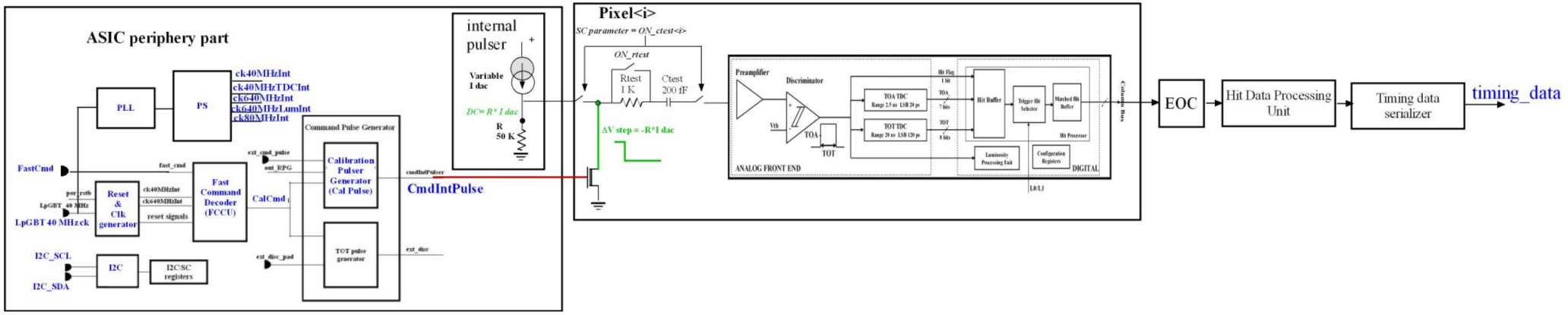
Electronics - ALTIROC2

- ALTIROC2 is the full size ASIC (15x15 pixel matrix)
  - Submitted in May 2021, delivered to CERN in Sept. 2021
  - Debug tests started Oct. 2021, dedicated testbench setup developed (HW/FW/SW)
  - Setups available at different institutes (OMEGA, IJCLAB, IFAE, LPC, IHEP,
    USTC), will perform tests on ASIC and ASIC + Sensor
    ⇒ So far all blocks functional, a few small issues to be understood and solved in ALTIROC3 (no showstoppers so far)
  - First measurements on power consumption, I2C communication & configuration, internal bias voltages, DAC linearity, clocks,...

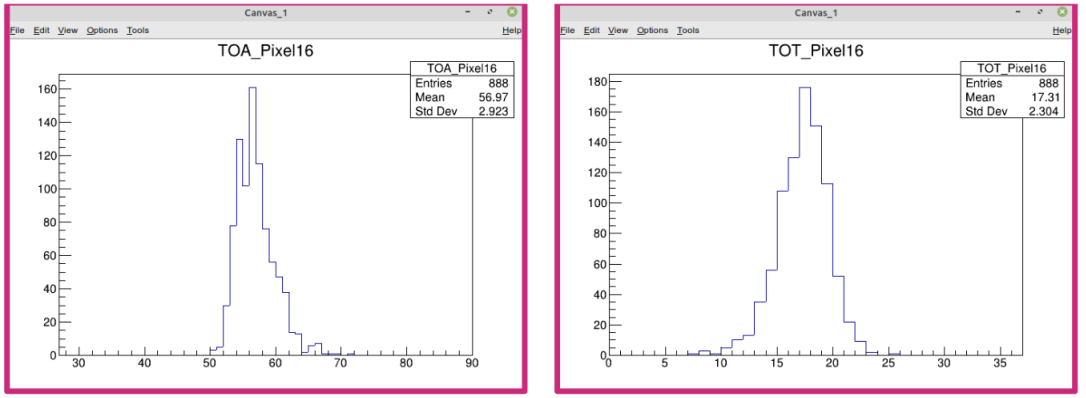




TOA and TOT measurements



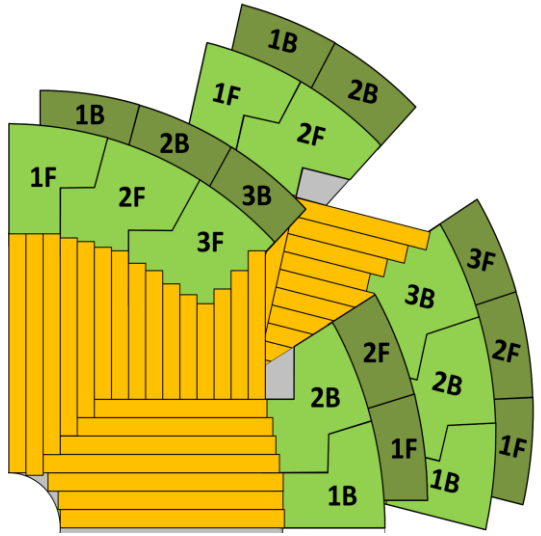
- Measurement (TOA and TOT histograms) using the full chain
  - Using calibration path, CalCmd fast command
  - ↠ Decoded by the fast command decoder ↠ activates the internal pulser ↠ signal through the preamplifier, the discriminator ↠ signal digitised in the 2 TDC ↠ stored in circular SRAM and passes the logic that follows the SRAM (Trigger Hit Selector and Matched Hit Buffer)
  - ↠ The timing data is encoded (8b10b) and sent to the "DAQ" through the serializer



TOA and TOT data for one pixel

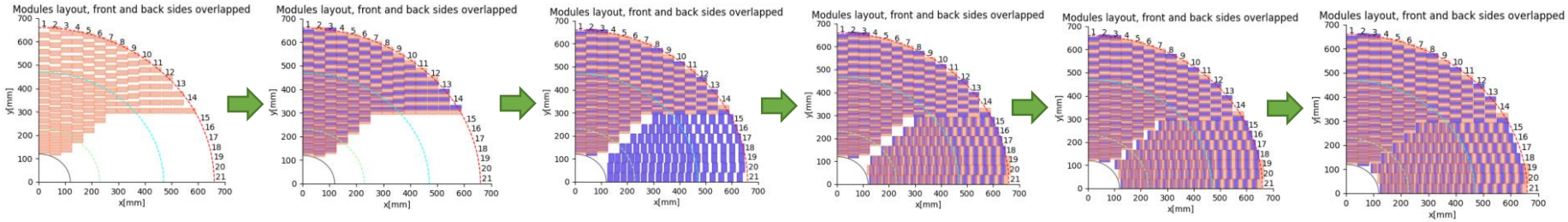
Module Layout Adjustment

- To reduce PEB types from 10 to 6
  - 1F, 2F, 2B and 1B are re-used at both side
  - Reduce the risk of the new design
    - The PCB placement and routing of 1F and 1B, 2F and 2B, have something in common, but readout speed of modules near boundaries are different. This need new channel arrangement for lpGBT
  - Save costs
    - The PCB NRE (Non Recurring Engineering) Cost for rigid-flex is 8~10 times to the price per unit
  - Reduce the risk on the project schedule
    - Design, production and testing
    - Each type of PEB will have different testing setup and software



One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

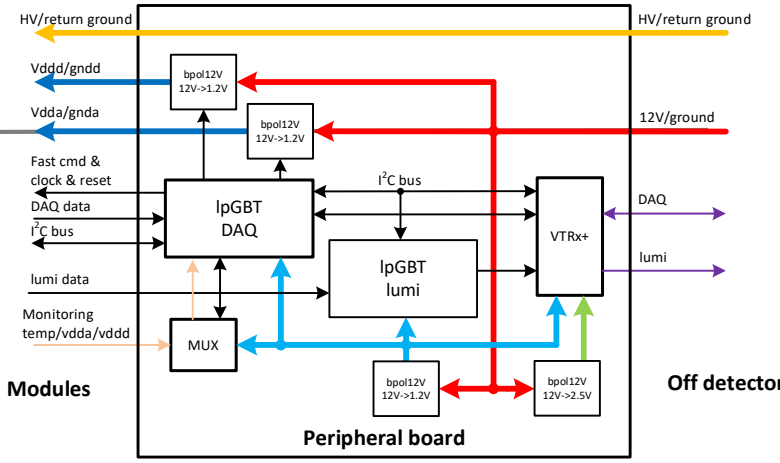
- Mirror Structure
  - Python3 script is developed according to the constraints from TDR
  - Workflow - 6 steps to generate module layout

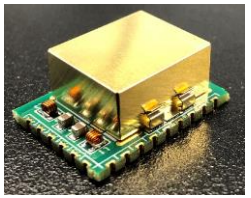


- The new layout is being evaluated by mechanical design and physical simulation

Electronics – PEB

- Peripheral electronics boards, connect FE to the DAQ system, provide LV&HV to the modules
- Work on the characterization of all individual components, prototypes under production:
  - Detailed testing of the DC/DC converter (bPOL12V), different options under consideration ↠ need to fulfil space constraints, power efficiency measured
  - Started tests on lpGBT with evaluation board
  - VTRX+: successfully tested 2.56G/10.24G communication, bit error rate (<10e-12/<10e-13), passed eye diagram test
  - MUX64: analogue multiplexer (for monitoring of ASIC power supply and temperature) ↠ basic functionality confirmed, On-resistance is larger than expected (further investigations necessary)
- SPR: “Peripheral electronics board ” passed ✓

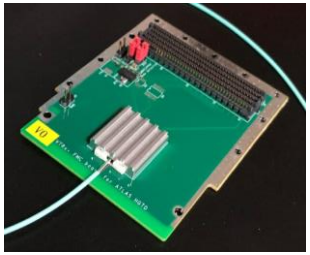




DC/DC converter

USB lpGBT programmer

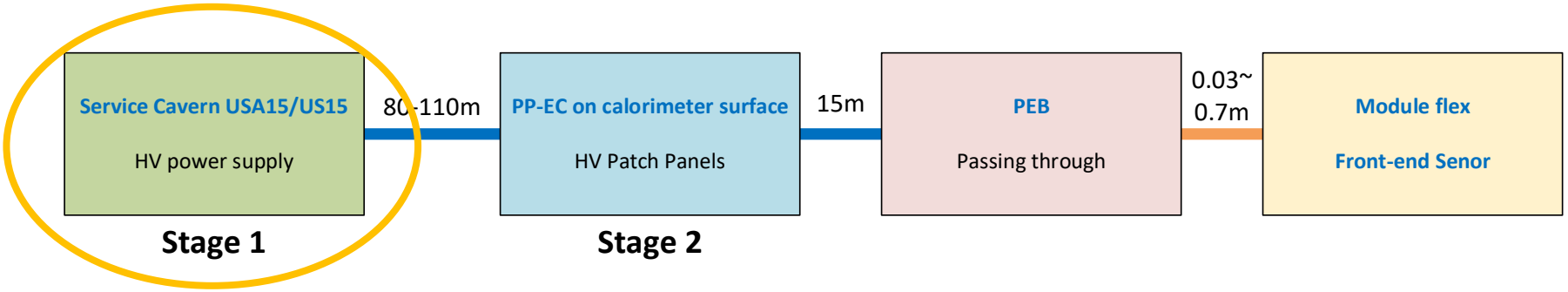
lpGBT eval. board



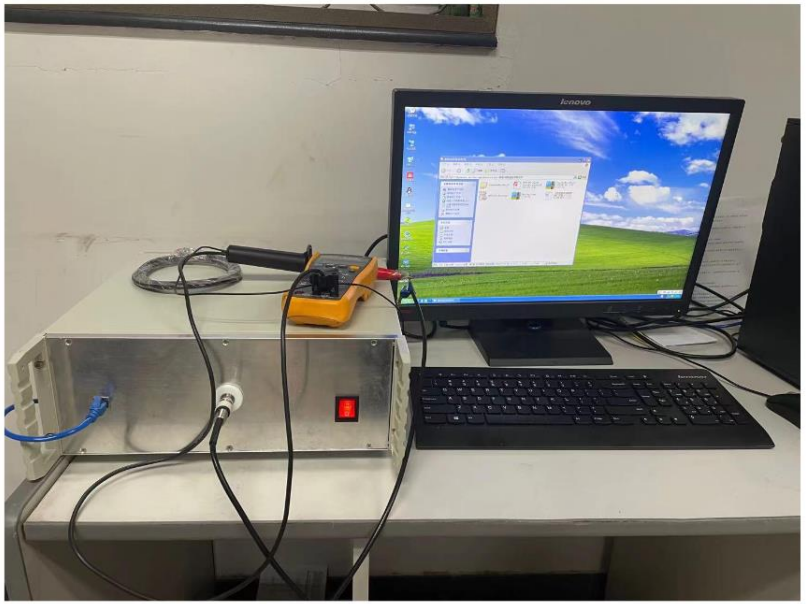
VTRx+ eval. board

MUX64 in QFN88

Electronics - HV System Stage 1



- Investigate the power supply manufacturers in China
- Customize a single-channel prototype
  - Remote controlled by Ethernet
  - Under electrical performance test and joint test with sensors

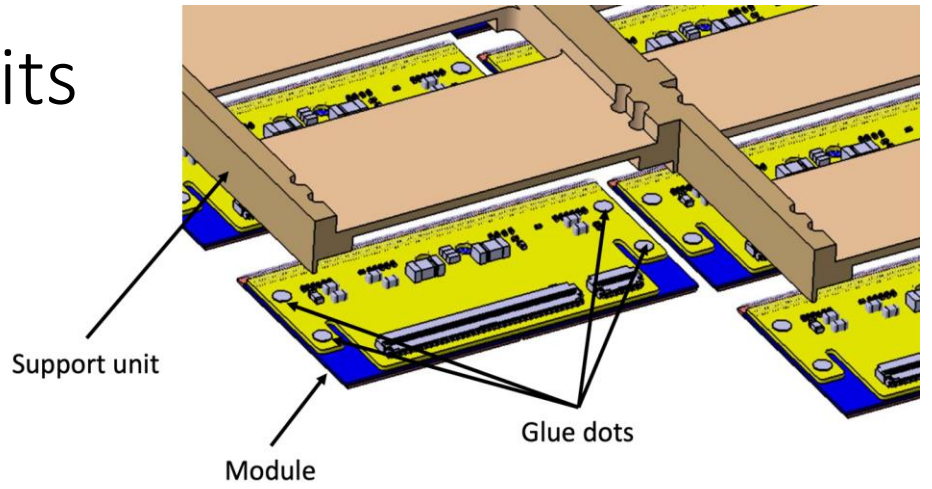


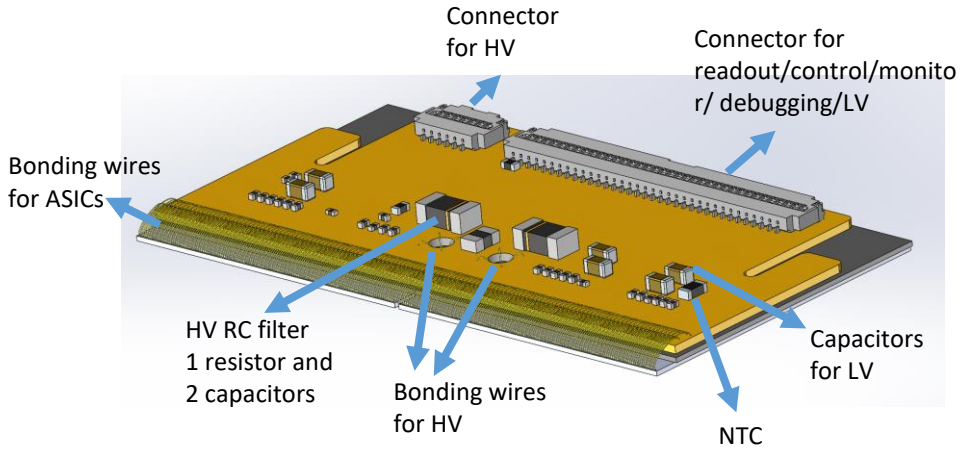
Single-channel prototype

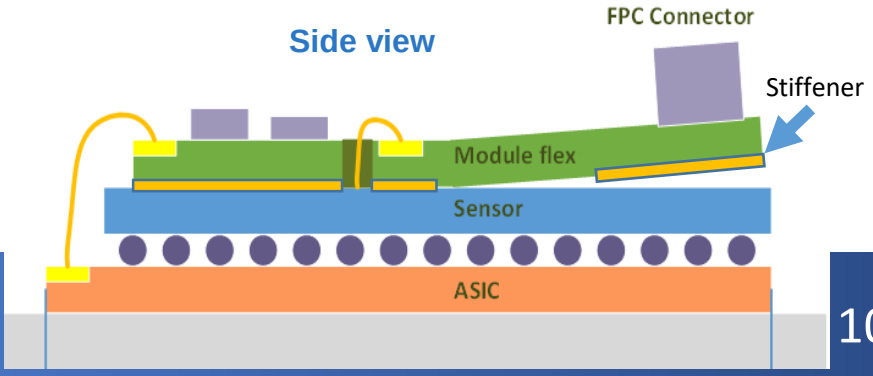
Modules and Detector Units

- Module contains 2 ASICs, 2 Sensors & module flex
  - Focus on first full size hybrids (LGAD sensors (HPK, FBK, IHEP-IME) with 15x15 pixel matrix bump bonded to ALTIROC2 chip)
  - Hybridization procedure is tested at different companies (IFAE, AEMtek, NCAP/IHEP), ASICs were shipped to the sites producing hybrids on schedule, ready for testing soon
  - Design of the “module flex” advanced (flexible PCB glued to sensor), 3 design options of PCB stack with different grounding schemes considered and already in production
- SPR: “Modules, Detector Units, Module flex, Flex tails” on Nov. 22rd, 2021

Loading modules on support units

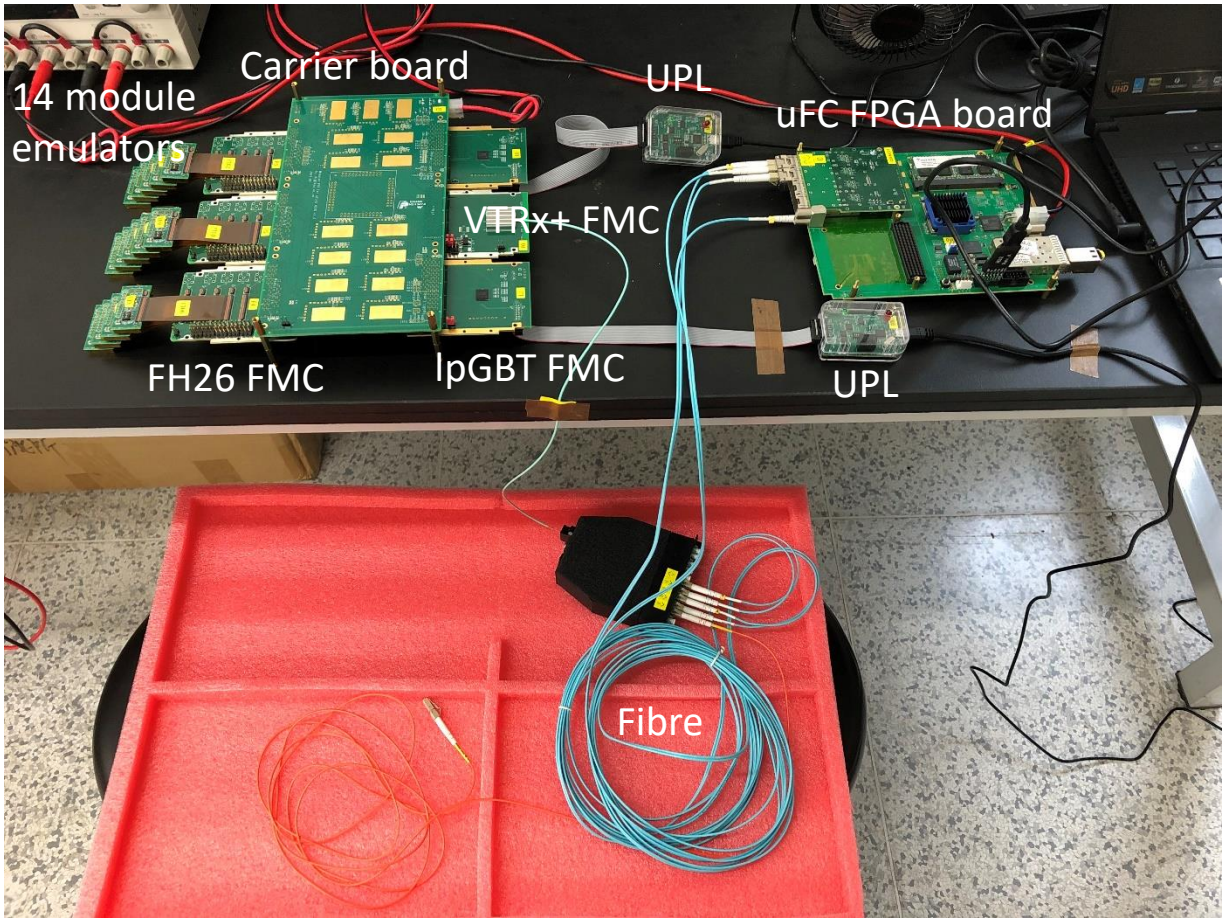






Demonstrator

- Modular PEB demonstrator
  - Minimum system for full chain readout, from module/ module emulators to FELIX board
- Support up to 14 modules with two lpGBTs and one VTRx+
  - Timing
    - Up to 3 modules @ 1.28Gbps
    - Up to 7 modules @ 640Mbps
    - Up to 14 modules @ 320Mbps
  - Luminosity
    - 7 modules @ 640Mbps
- Integration testing in progress
  - Will send the first set to CERN soon



Summary

- LGAD Sensor
  - Clear progress in the last year towards an LGAD design fulfilling the radiation hardness requirements for HGTD
- Electronics
  - ALTIROC 2 (full size ASIC) on schedule, currently under detailed test, so far all blocks are functional
  - Discrete implementation/evaluation of PEB components are almost done, then start the prototype design
  - Customized single-channel HV prototype is under test
- Modules and Detector Units
  - First full size hybrids are in production and expected soon
  - Module flex PCB is under production
- Demonstrator
  - Minimum system for full chain readout, from modules/module emulators to FELIX board
- Activities are ramping up, still a lot of work ahead