山东大学（青岛）
SHANDONG UNIVERSITY, QINGDAO

哈尔滨工业大学（威海）
HARBIN INSTITUTE OF TECHNOLOGY, WEIHAI

# 面向高能物理实验的高速高精度SAR ADC


**张亮**

Email: zhang.l@sdu.edu.cn



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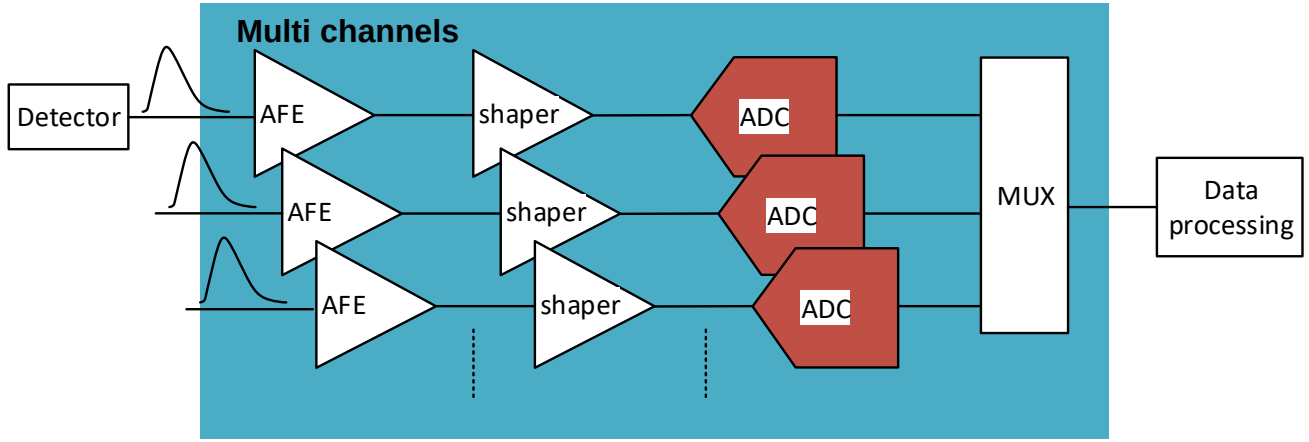
# Outline

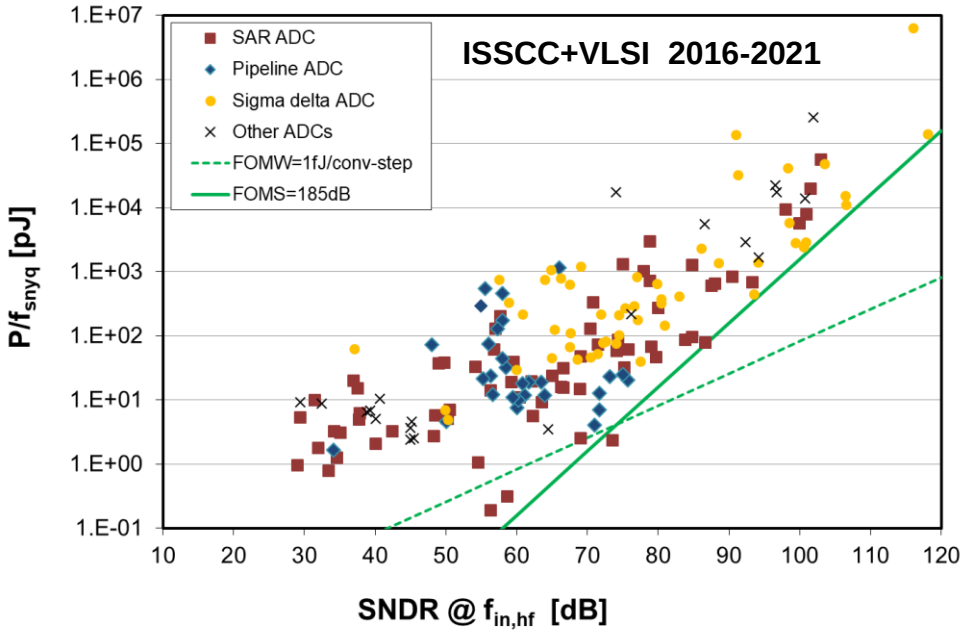
- Introduction
- Development of 10bit 100MHz SAR ADC
  - Architecture
  - Measurement results
- Development of 10bit 160MHz and 12bit 100MHz SAR ADC
- Summary

# Introduction

- Readout electronics in high energy experiments
  - High-speed high-resolution ADC for digitalization
  - Large amount of channels
    - High integration → ASIC
  - Low power small area




Signal chain in readout electronics

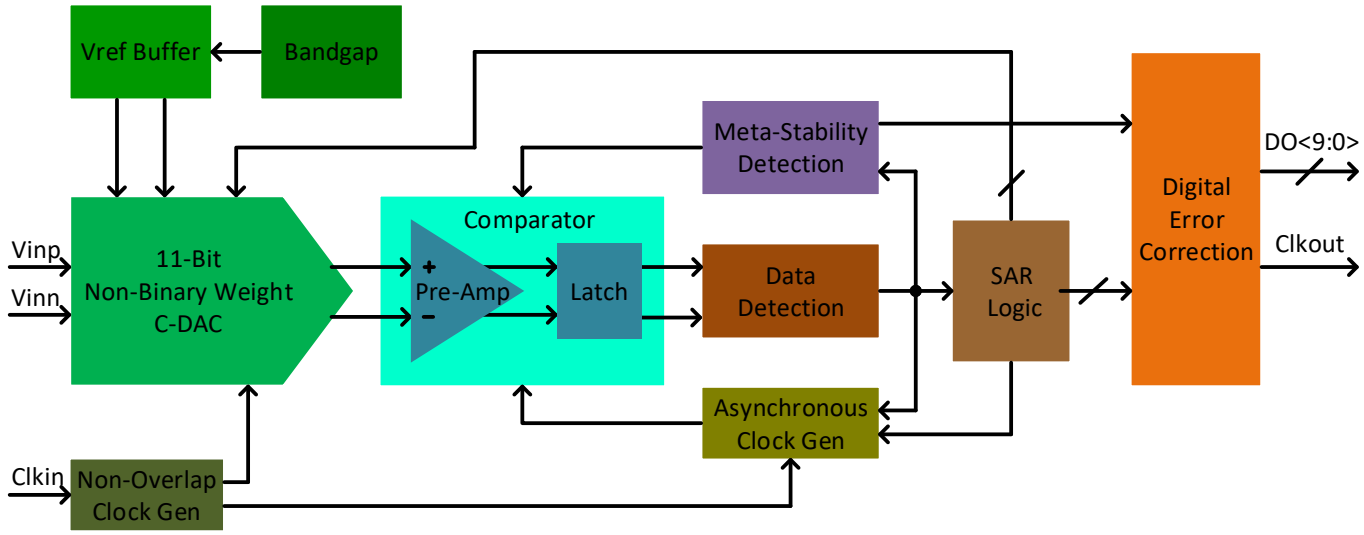



ADC's power efficiency versus SNDR

(Modified from B. Murmann "ADC Performance Survey" [Online] http://web.stanford.edu/~murmann/adcsurvey.html)

# 10bit 100MHz SAR ADC

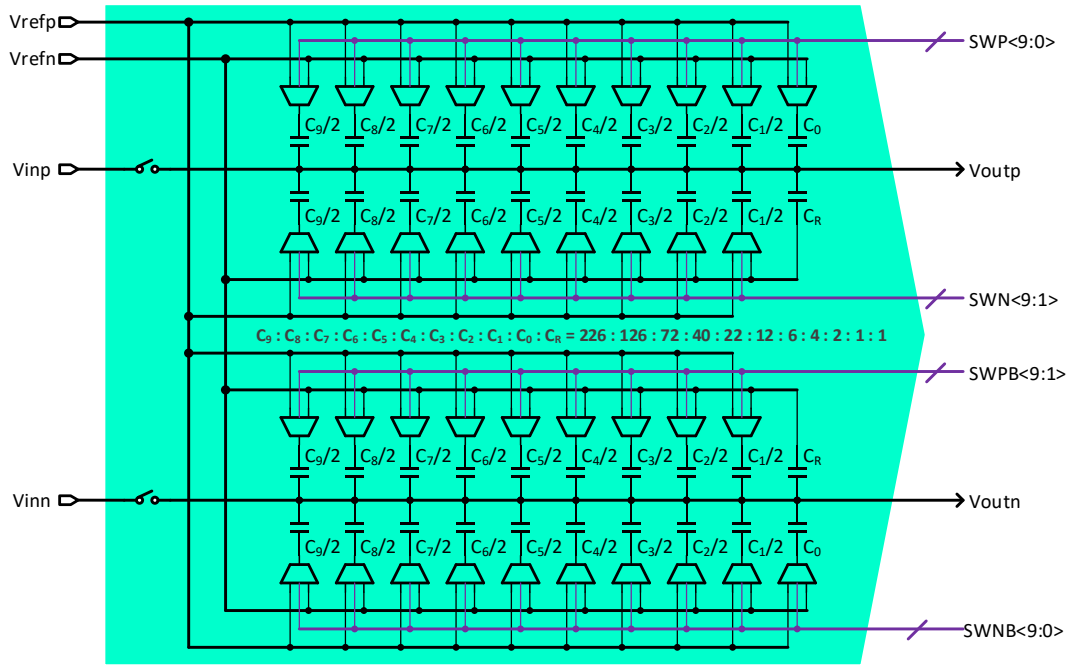
- Architecture and building blocks
  - Internal bandgap
  - High bandwidth reference buffer
  - Non-binary weight capacitor digital-to-analog converter (C-DAC)
  - Non-overlap clock generator
  - High-speed comparator
  - High speed asynchronous SAR logic
  - Full custom logic cells
    - Without floating nets
      - → improve radiation hardness
  - Metastability elimination circuit
  - Digital error correction




Architecture of proposed SAR ADC

# 10bit 100MHz SAR ADC

- Non-binary weighted C-DAC
  - Top-plate direct sampling technique
    - Remove capacitor of MSB
      - → reduce area
  - Hybrid capacitor switching procedure
    - $C_9$ to $C_1$ employ interpolated VCM-based switching
      - → only switch Vrefp and Vrefn
      - → remove VCM buffer, saving power & area
    - $C_0$ employs a monotonic switching
  - Non-binary weight algorithm
    - Decreases the settling time
      - → improve speed

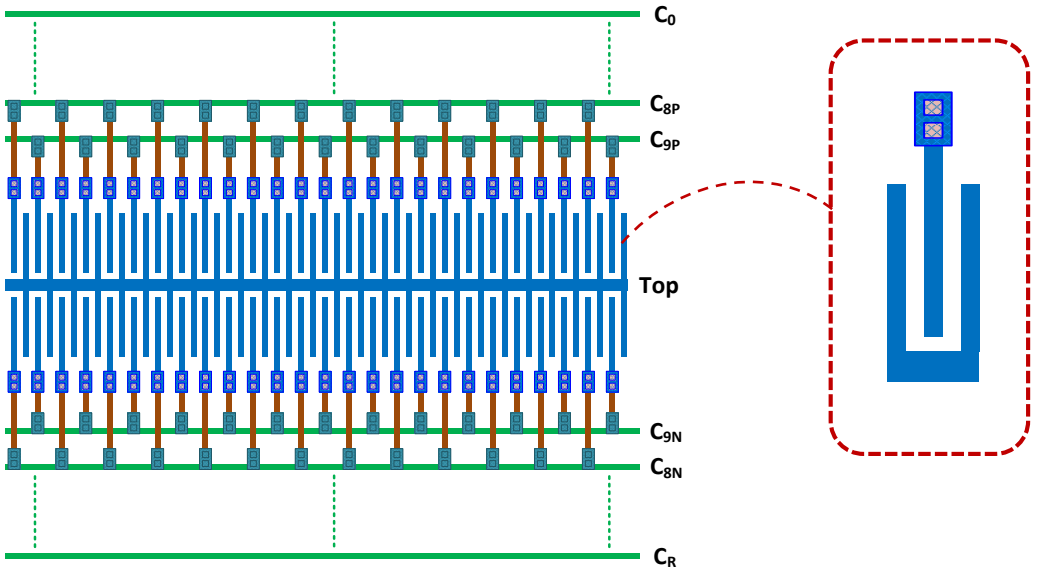



| Bit | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | $C_R$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Weight | 226 | 126 | 72 | 40 | 22 | 12 | 6 | 4 | 2 | 1 | 1 |
| $C_{P<9:0>}$, $C_R$ | 113 | 63 | 36 | 20 | 11 | 6 | 3 | 2 | 1 | 1 | - |
| $C_{P<N:0>}$, $C_R$ | 113 | 63 | 36 | 20 | 11 | 6 | 3 | 2 | 1 | - | 1 |

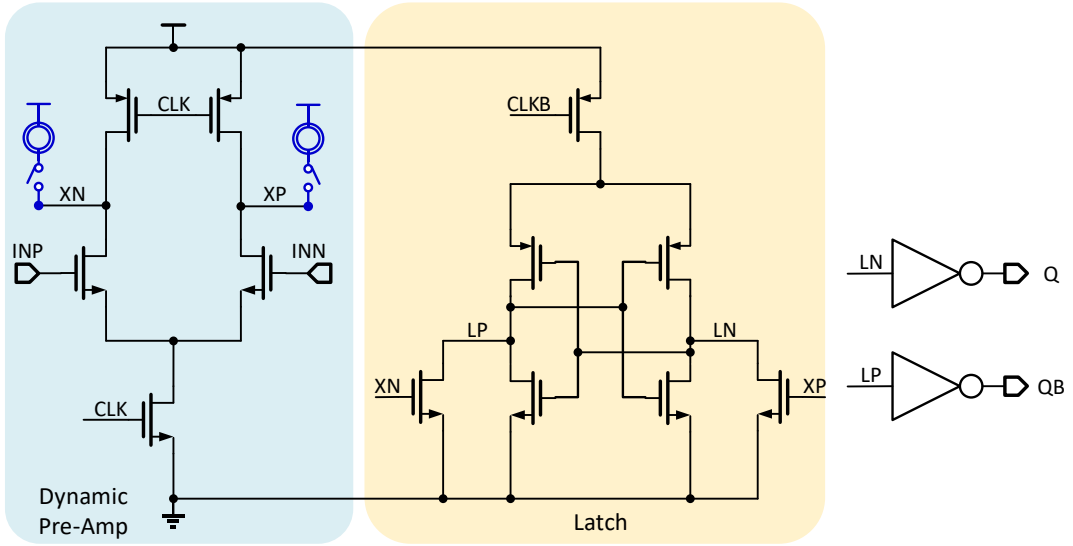
Capacitor value

# 10bit 100MHz SAR ADC

- Non-binary weighted C-DAC
  - MOM capacitor
    - Low parasitic capacitor to the substrate
  - Fishbone shape
    - Improve matching
    - Reduce DNL and INL
  - Unit capacitor is 2.5 fF, 2.56 pF in total

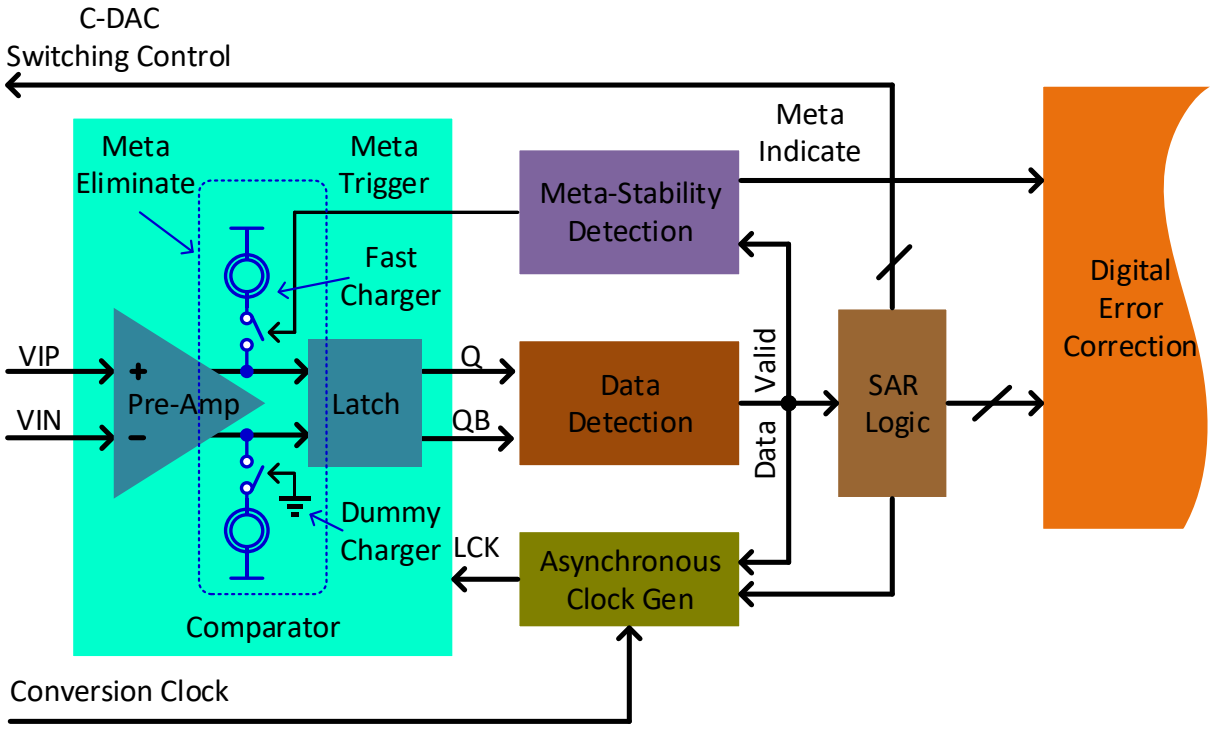


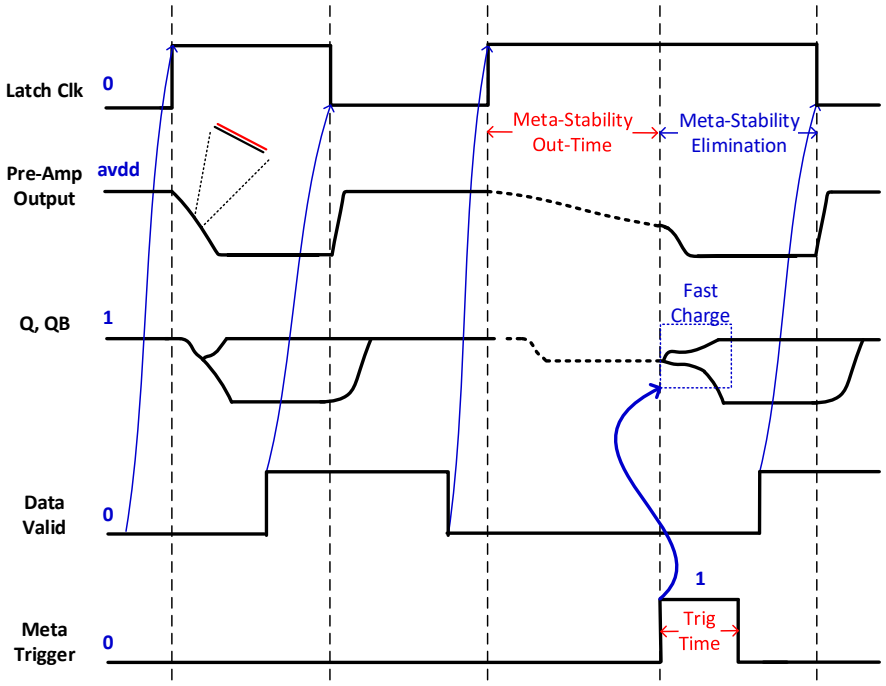

- Dynamic comparator
  - Dynamic pre-amplifier
    - Reduce equivalent noise of the latch
    - Low power



# 10bit 100MHz SAR ADC

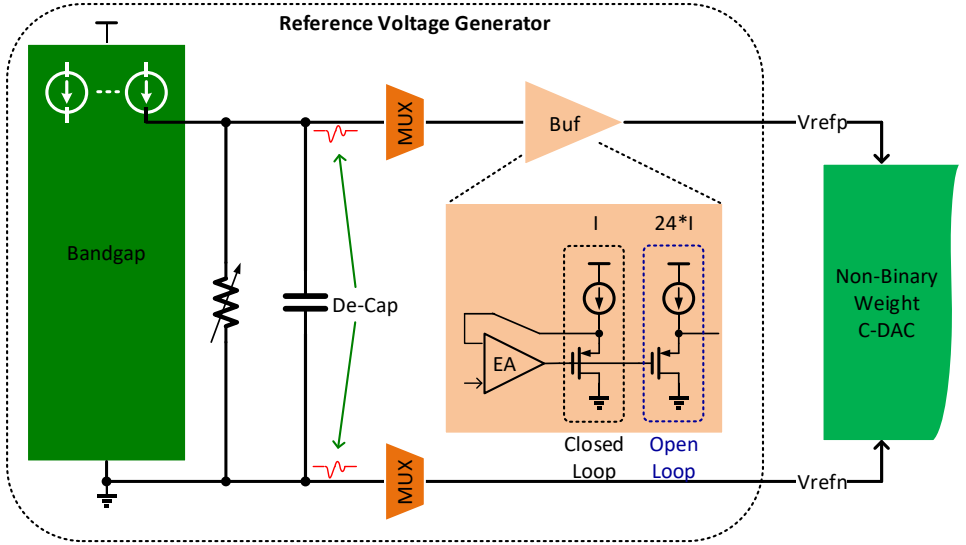
- Metastability elimination
  - Employ a metastability detection
  - Fast charger and dummy charger @ pre-amp output
  - Generate a trigger to the input @ latch
    - break down the metastability



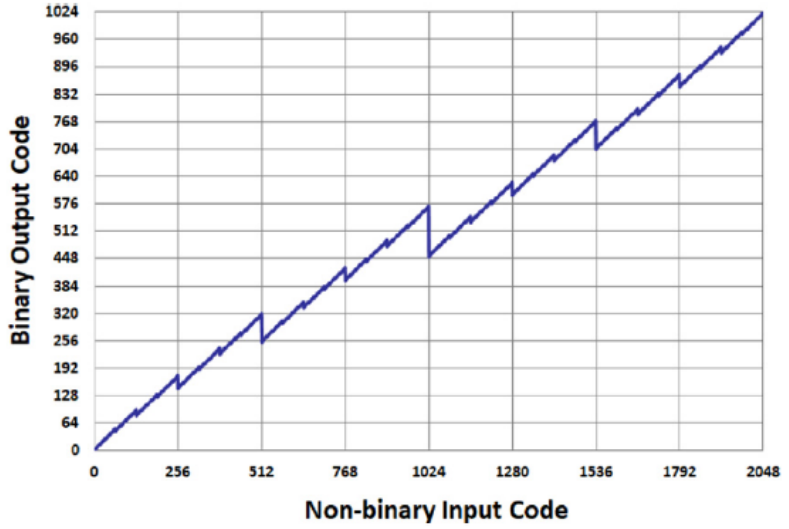
# 10bit 100MHz SAR ADC

- Reference voltage generator
  - Full integration
    - Fully functional chip
    - Relax test board
  - Current mode bandgap
  - Programmable resistor
  - Voltage selection multiplexer
  - Wide bandwidth reference buffer



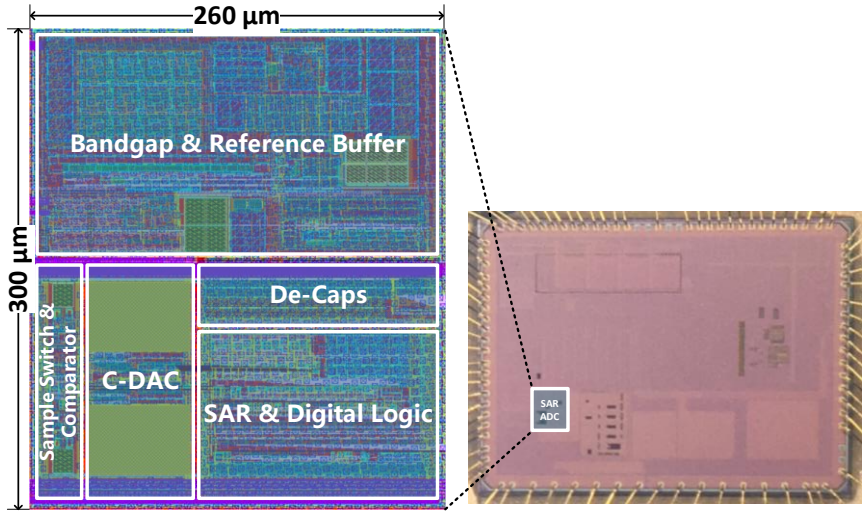

- Digital error correction
  - Convert 11-bit to 10-bit
    - Implemented with adder, D flip-flop

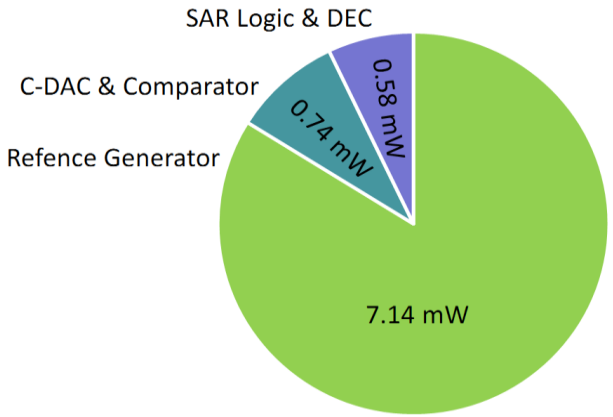
$$D_{OUT} = 512 + (2\cdot B_{10}-1)\cdot 226 + (2\cdot B_9-1)\cdot 126 + (2\cdot B_8-1)\cdot 72 + (2\cdot B_7-1)\cdot 40 + (2\cdot B_6-1)\cdot 22 + (2\cdot B_5-1)\cdot 12 + (2\cdot B_4-1)\cdot 6 + (2\cdot B_3-1)\cdot 4 + (2\cdot B_2-1)\cdot 2 + (2\cdot B_1-1)\cdot 1 + (B_0-1)\cdot 1 \quad (2)$$

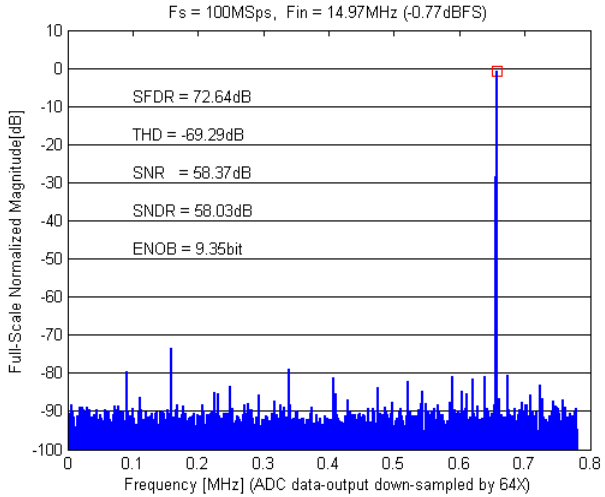


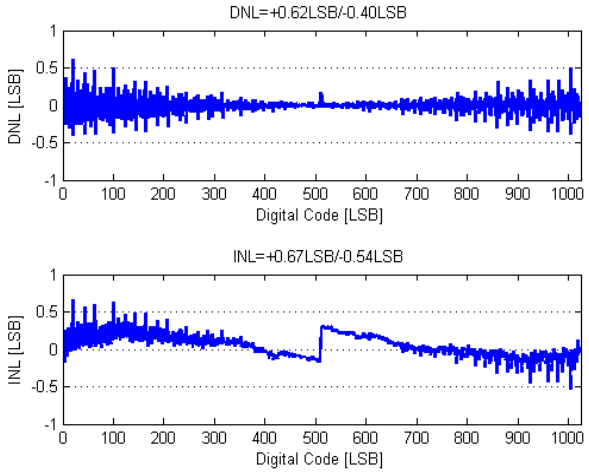
# 10bit 100MHz SAR ADC

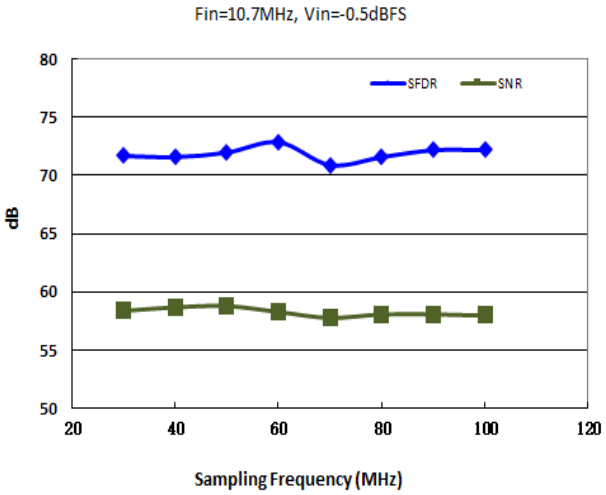
- Measurement results
  - Designed and fabricated in 40nm CMOS process
  - total area: 0.078 $mm^2$
    - core area: 0.037 $mm^2$
  - total power consumption: 8.5 mW
    - core power: 1.32 mW
  - FOM: 130 fJ/conversion-step
  - SFDR: 72.6 dB, THD: -69.2 dB, SNDR: 58.0 dB
  - DNL: +0.62/-0.4 LSB, INL: +0.67/-0.54 LSB



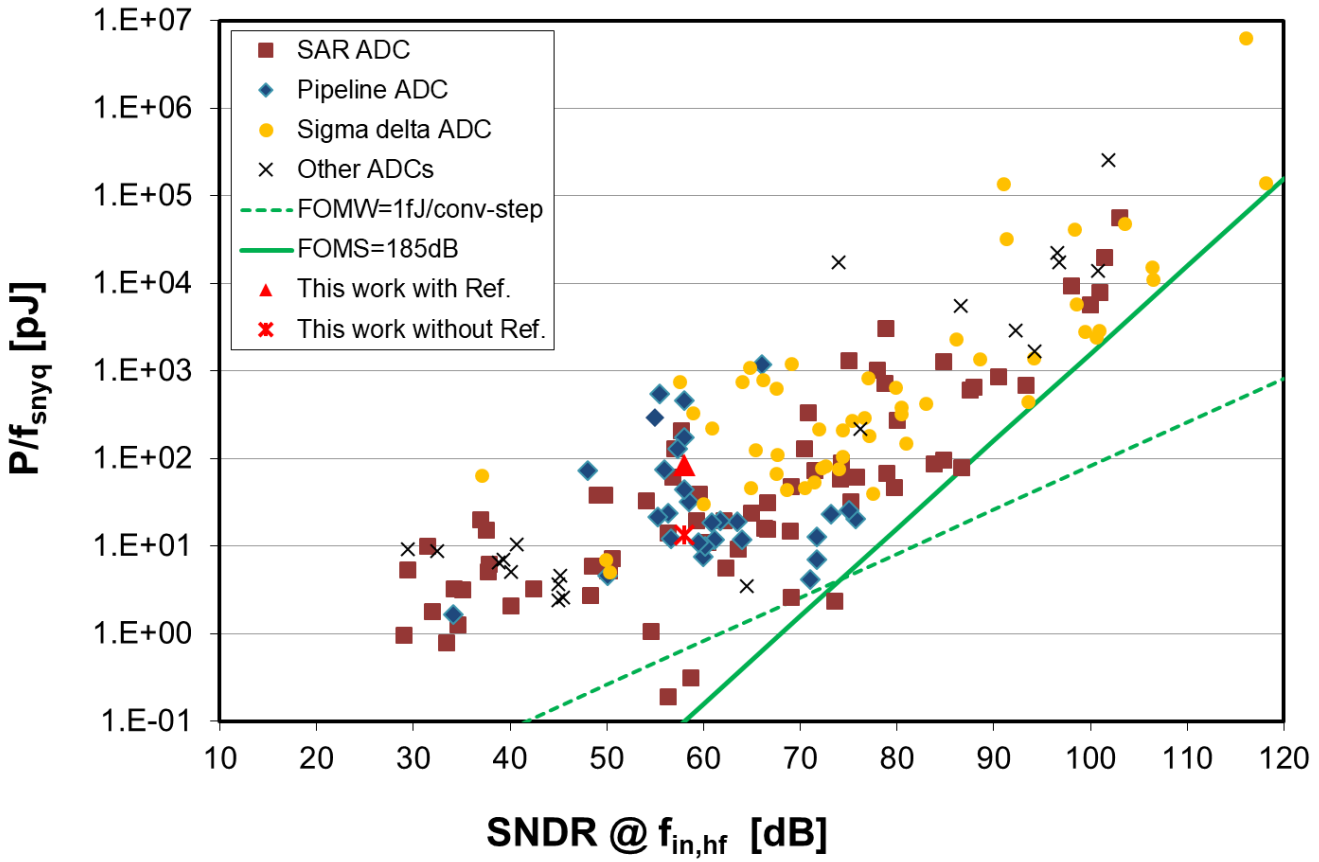



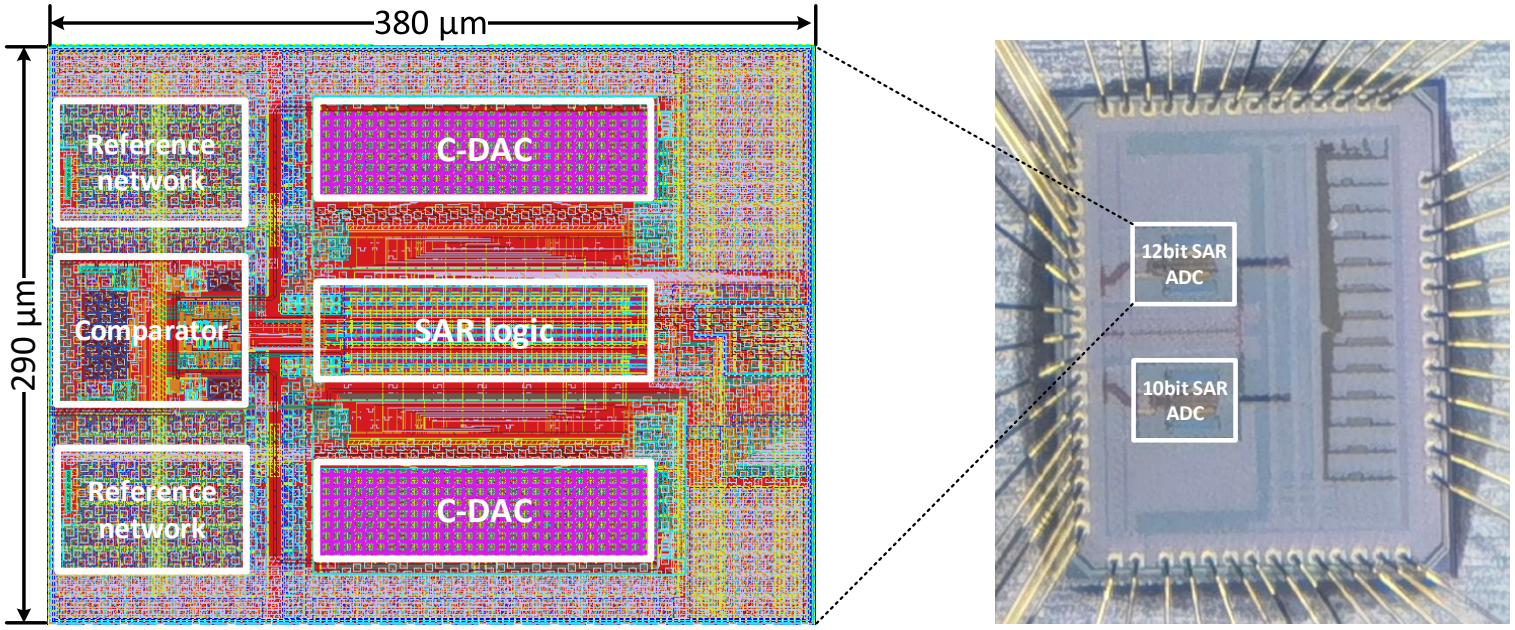



# 10bit 100MHz SAR ADC



# 10bit 160MHz and 12bit 100MHz SAR ADC

- 10bit 160MHz and 12bit 100MHz SAR ADC
  - Optimization
    - Asynchronous logic
    - Remove voltage generator
    - High speed comparator
  - Same architecture
  - Total area: 0.11 $mm^2$
  - Total power consumption
    - 10bit 160MHz: 2.72 mW
    - 12bit 100MHz: 1.84 mW
  - Package in QFN48
  - Both ADCs are under test
    - Send samples if someone are interested, including documents as a commercial IP has.



# Summary

- High speed high resolution ADC has a great requirement in readout electronics of high energy experiments.
- Three high speed high resolution SAR ADC prototypes have been developed, which have low power and small area.
- 10bit 160MHz and 12bit 100MHz SAR ADCs are developed as a standard IP, that samples can be delivered in the future.

**Thank you!**