Prototype Characterization of a Charge-integration Pixel Detector Readout Chip with In-pixel A/D Conversion

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Outline

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  - Charge-integration Readout Chip
- The Chip Design
- Measurement results
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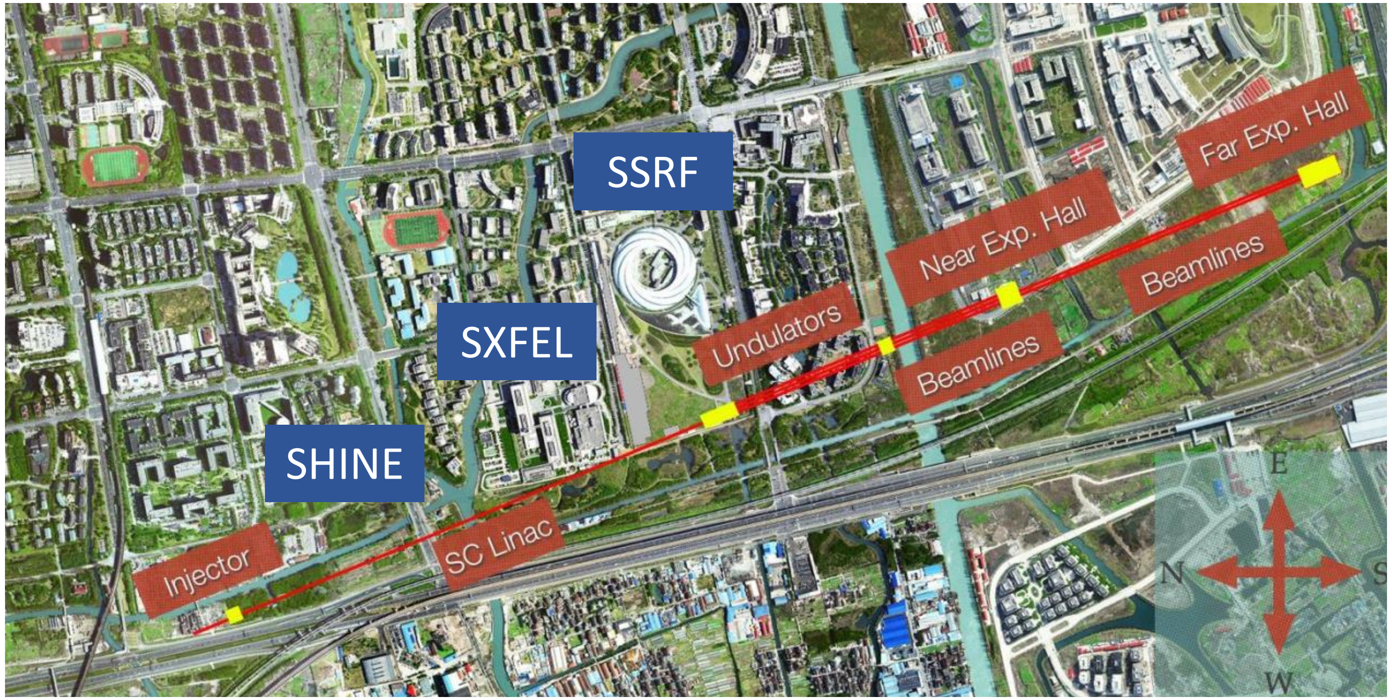
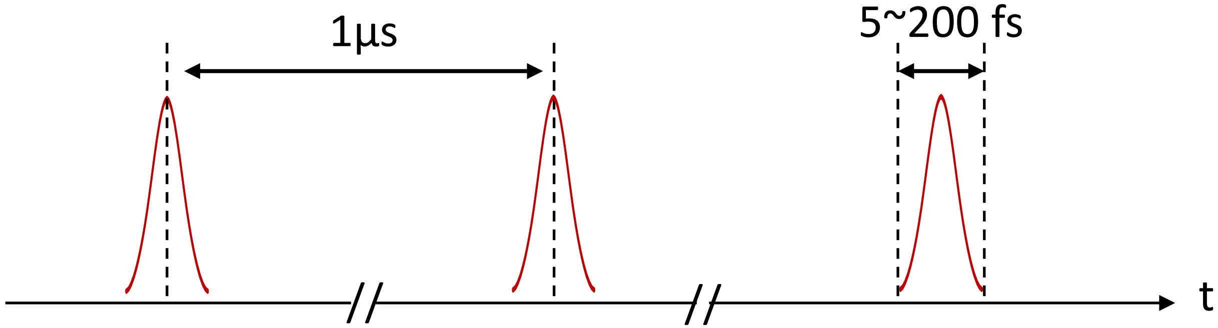
SHINE

Shanghai HIgh repetition rate XFEL aNd Extreme light facility

- 3 FEL beamlines: FEL-I, FEL-II, FEL-III
- Photon Energy: 0.4~25 keV
  - FEL-I: 3~15 keV
  - FEL-II: 0.4~3 keV
  - FEL-III: 10~25 keV
- Pulse Duration: 20~50 fs (5~200 fs)
- Repetition Frequency: 10kHz (1MHz)
- Peak Brightness: 10^{32} ~10^{33} photons/μm²/rad²/s/0.1%BW





Counting VS Integrating

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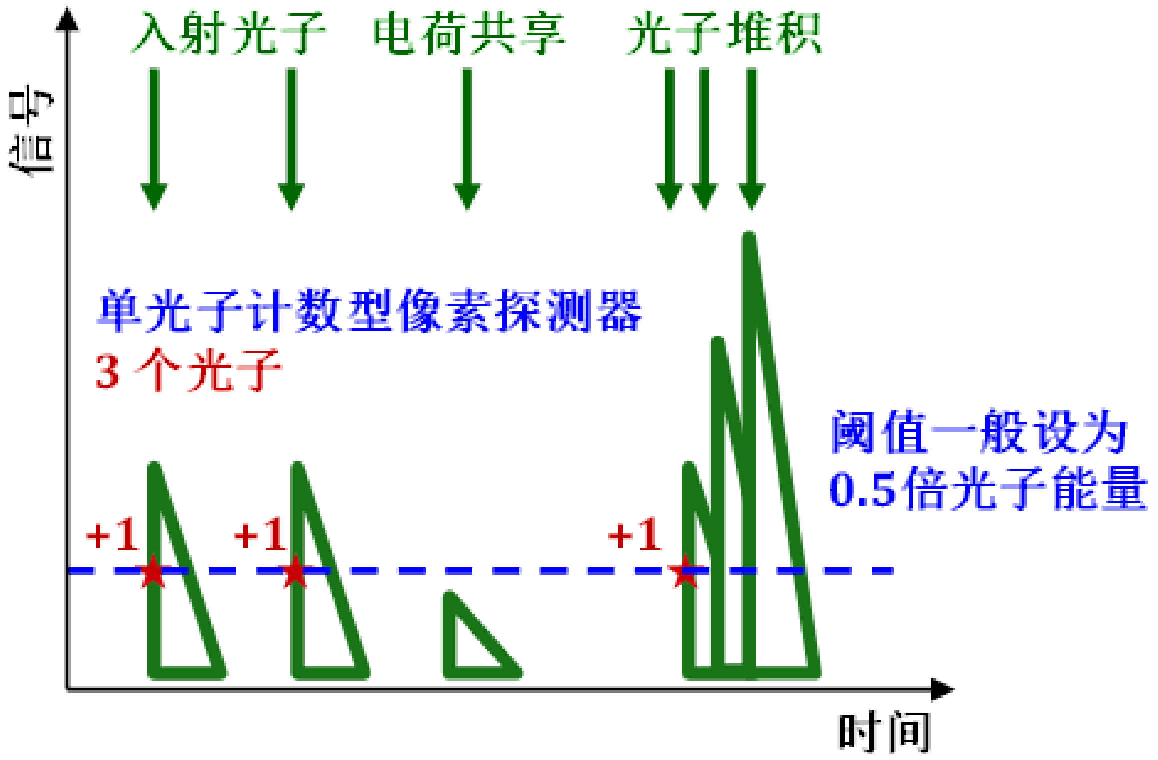

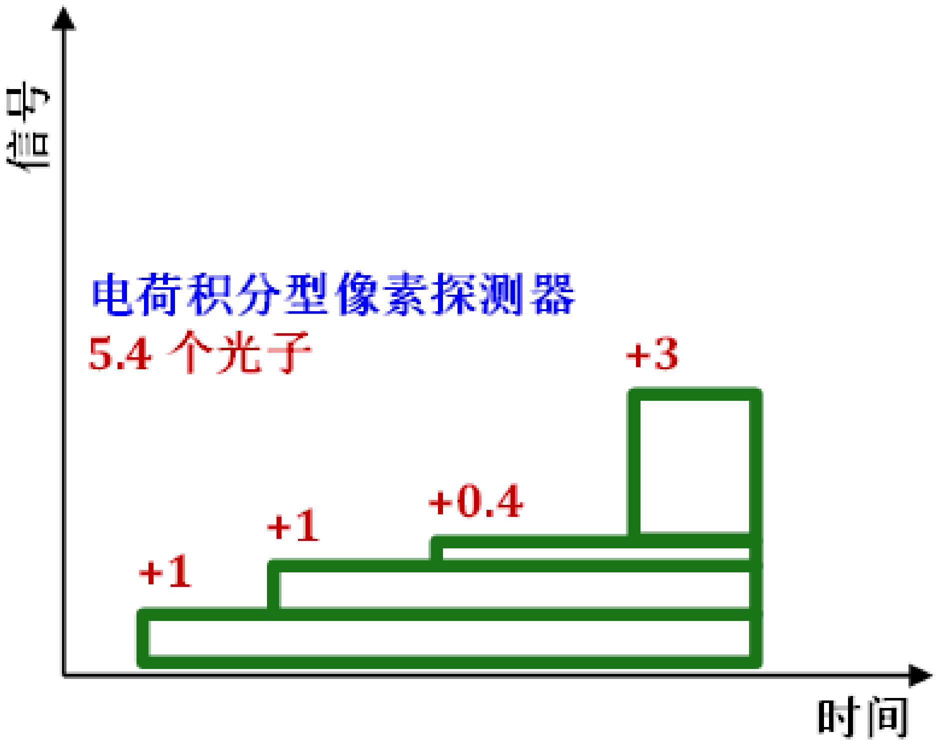

- "Zero Noise" but photons are piled up.
- All of the Charges are integrated including noise.

Hybrid Structure

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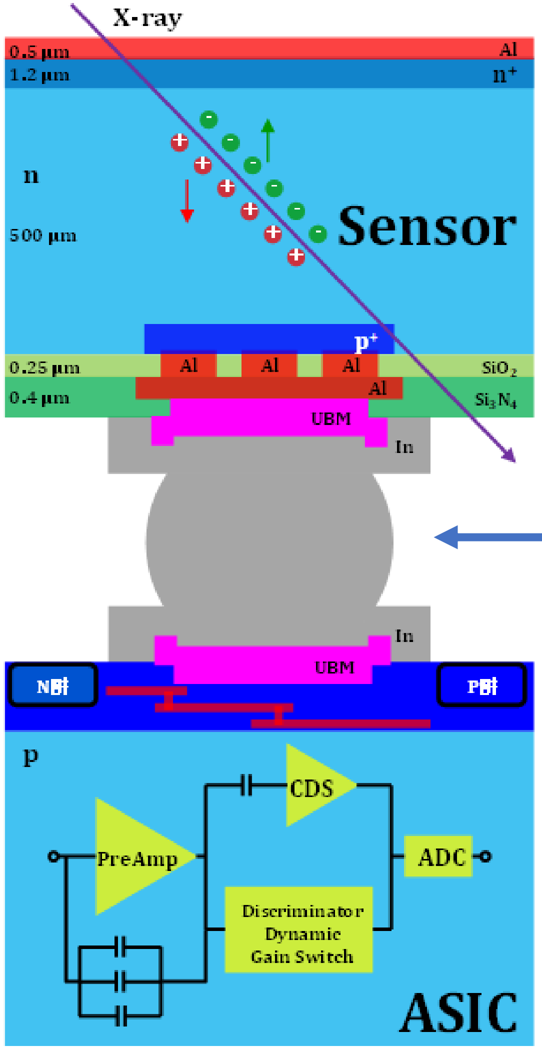
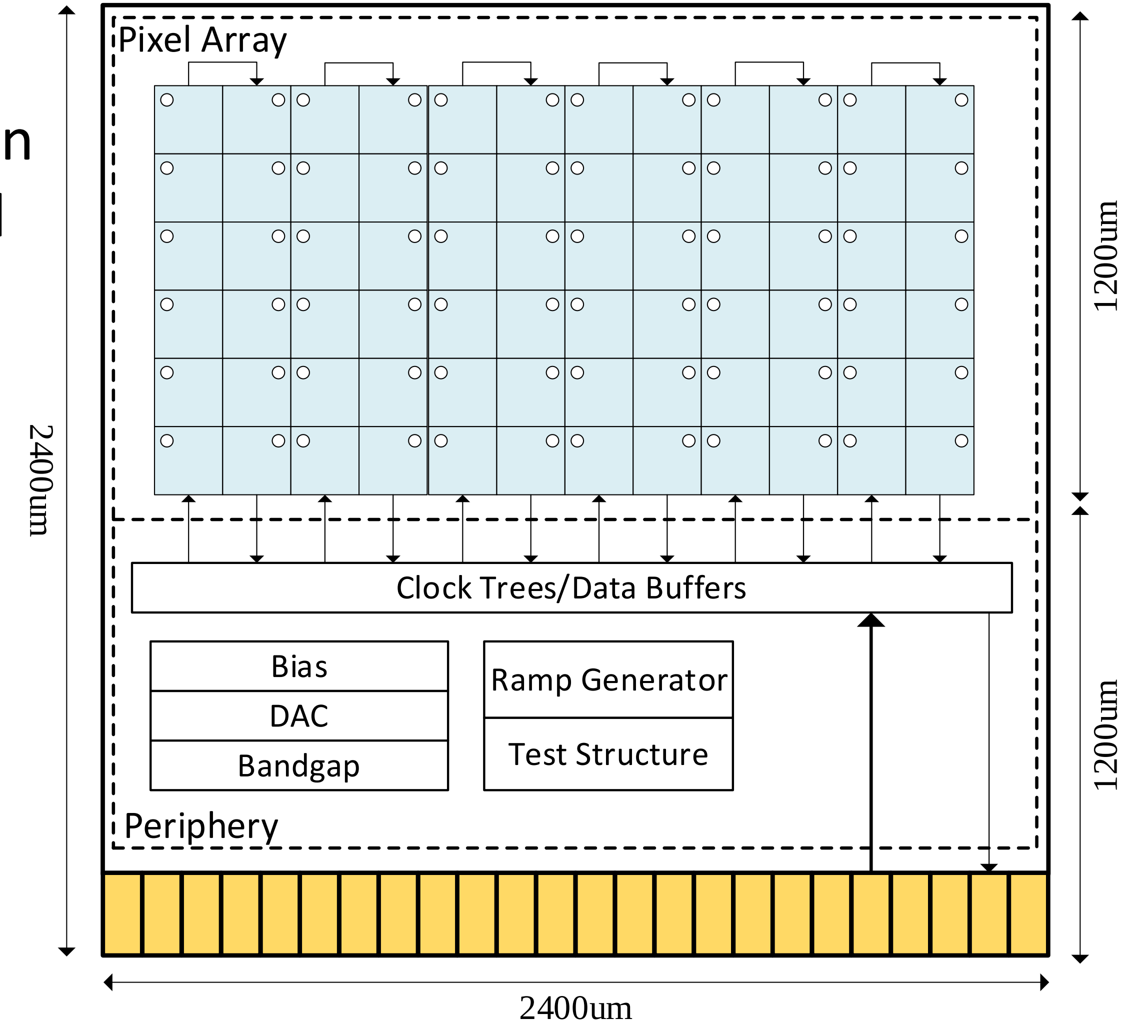
- PIN Sensor
- Bump Bonding
- Readout ASIC



HYLITE

HYLITE (High dYmamic range free electron Laser Imaging deTEctor) is a charge-integration pixel detector readout chip, which is designed for SHINE and other advanced light sources.

- Technology: 130 nm 1P8M CMOS
- Pixel Pitch: 200 μm (100 μm)
- Frame Rate: 10 kHz (continuously read out)
- Dynamic Range: 1~10000 photons @12 keV
- HYLITE 0.1: the first verification chip
  - Chip Size: 2400 μm * 2400 μm
  - Array Size: 6*12



Pixel Architecture of HYLITE

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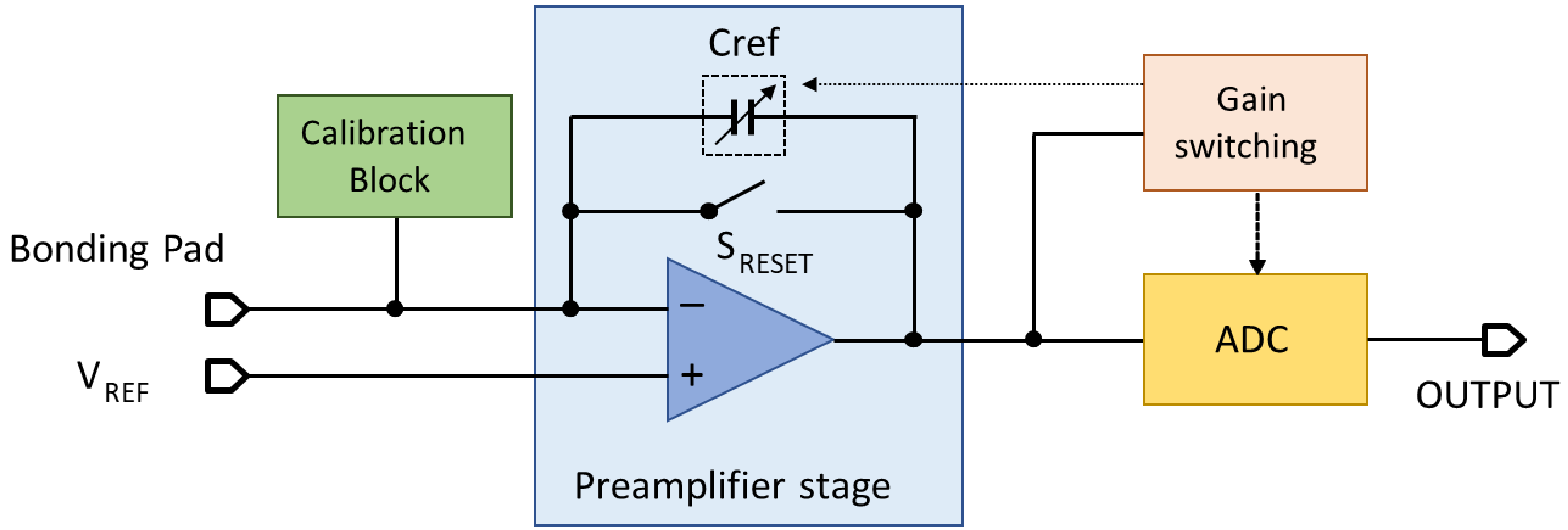

- Auto Gain Switching
- Total Power: 34 μW/pixel

Work Timing

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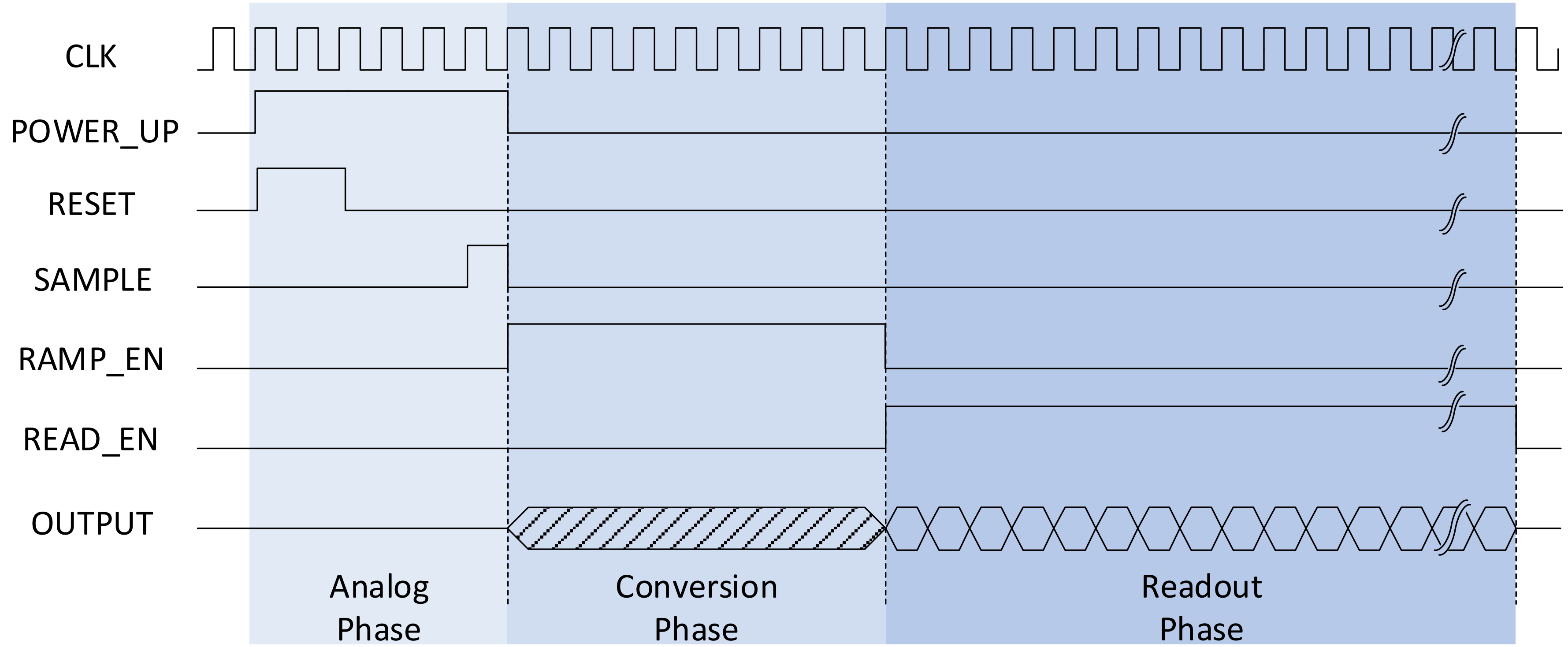

- **Three Working Phases**
  - Analog Phase (less than 1 μs)
  - Conversion Phase (20 μs)
  - Readout Phase (~70 μs in full size chip)

Global Simulation

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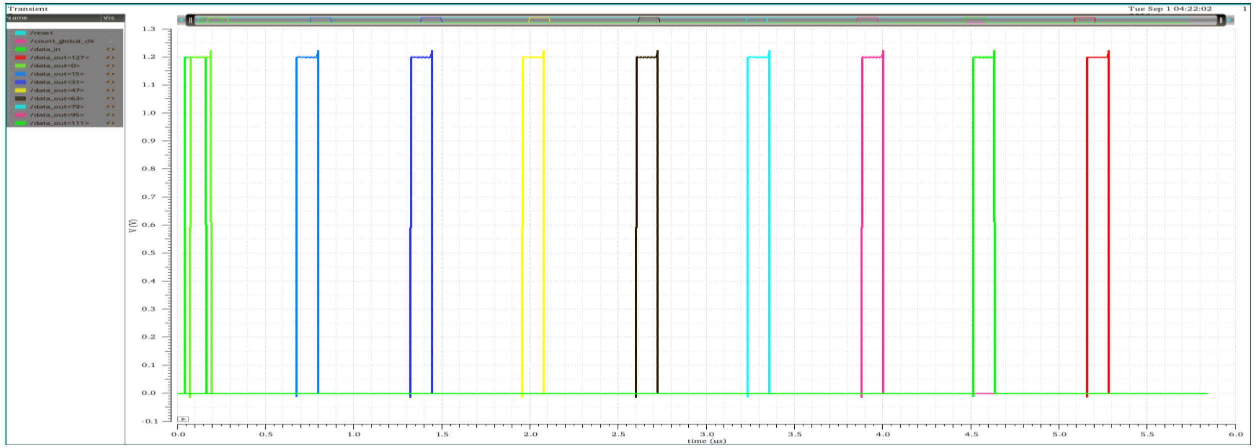
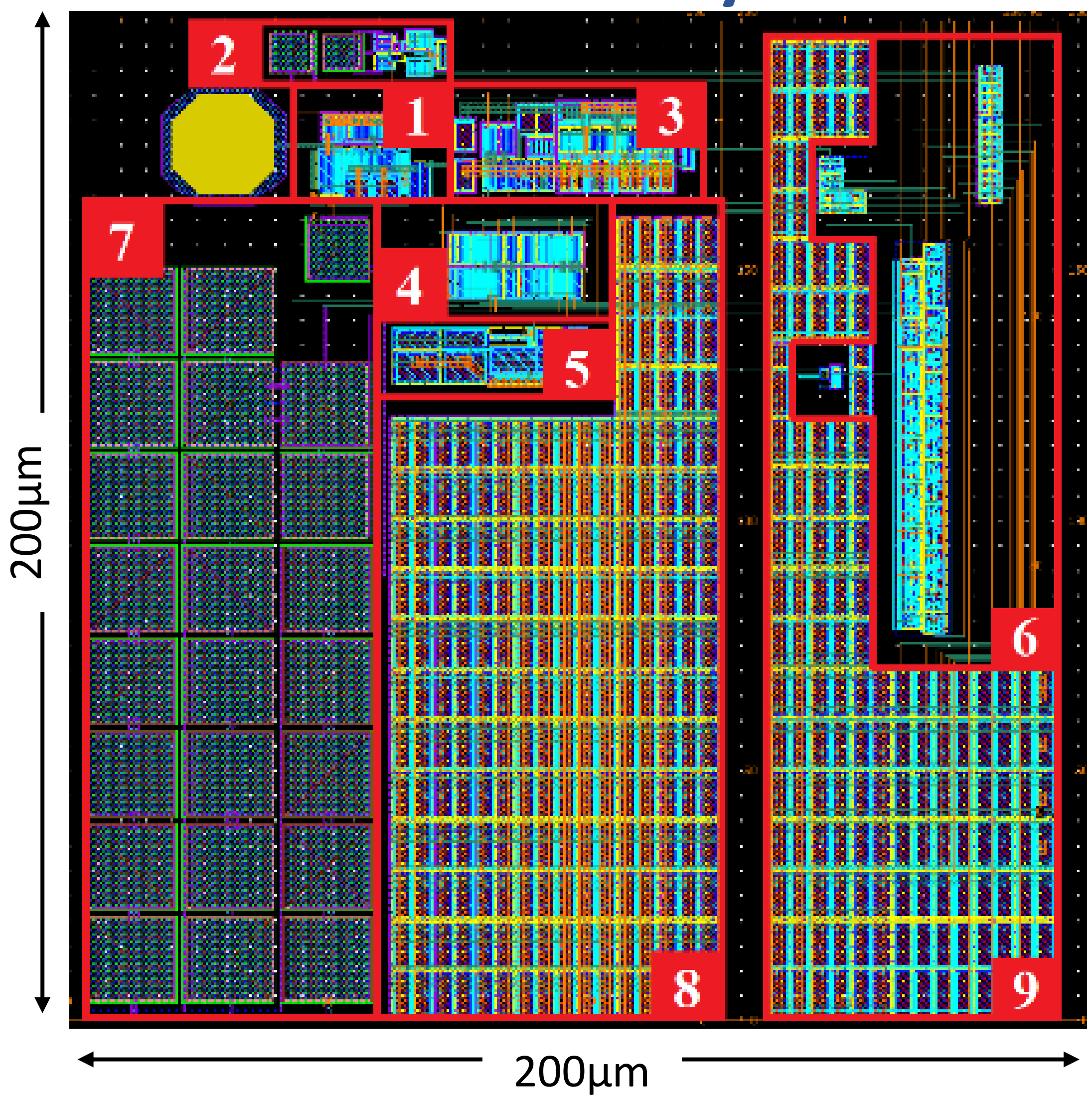


- Careful simulations before the tape out, including:
  - Verifying the Correctness of behavior
  - Power integrity
  - Timing integrity
  - ……

HYLITE 0.1 Layout



- 1: Preamplifier
- 2: Calibration Block
- 3: Gain Switching Circuits
- 4: Switches
- 5: Comparator of WADC
- 6: Digital Logic
- 7: Integrating Capacitors
- 8: Decoupling Capacitors of Analog Power
- 9: Decoupling Capacitors of Digital Power

Measurement System

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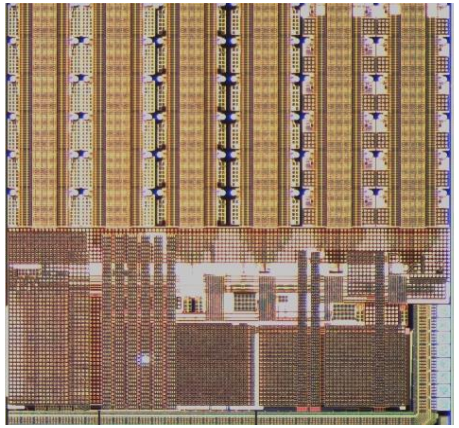
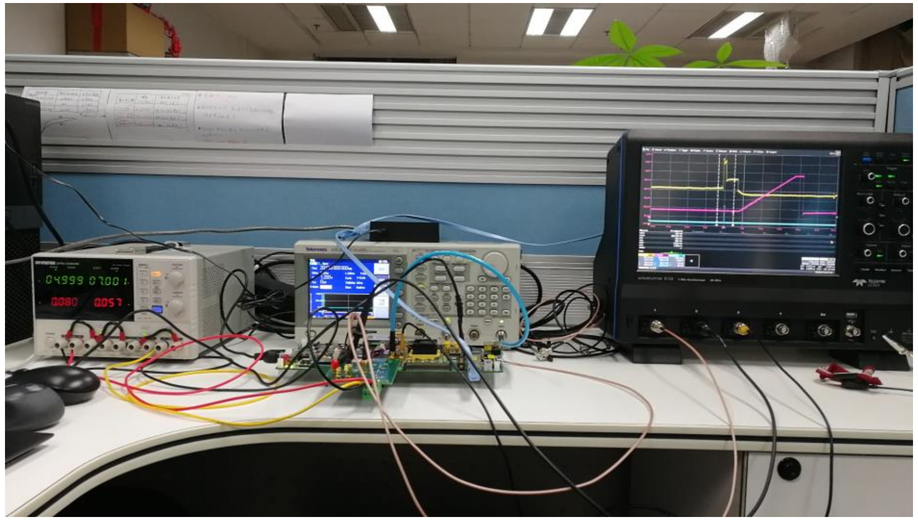
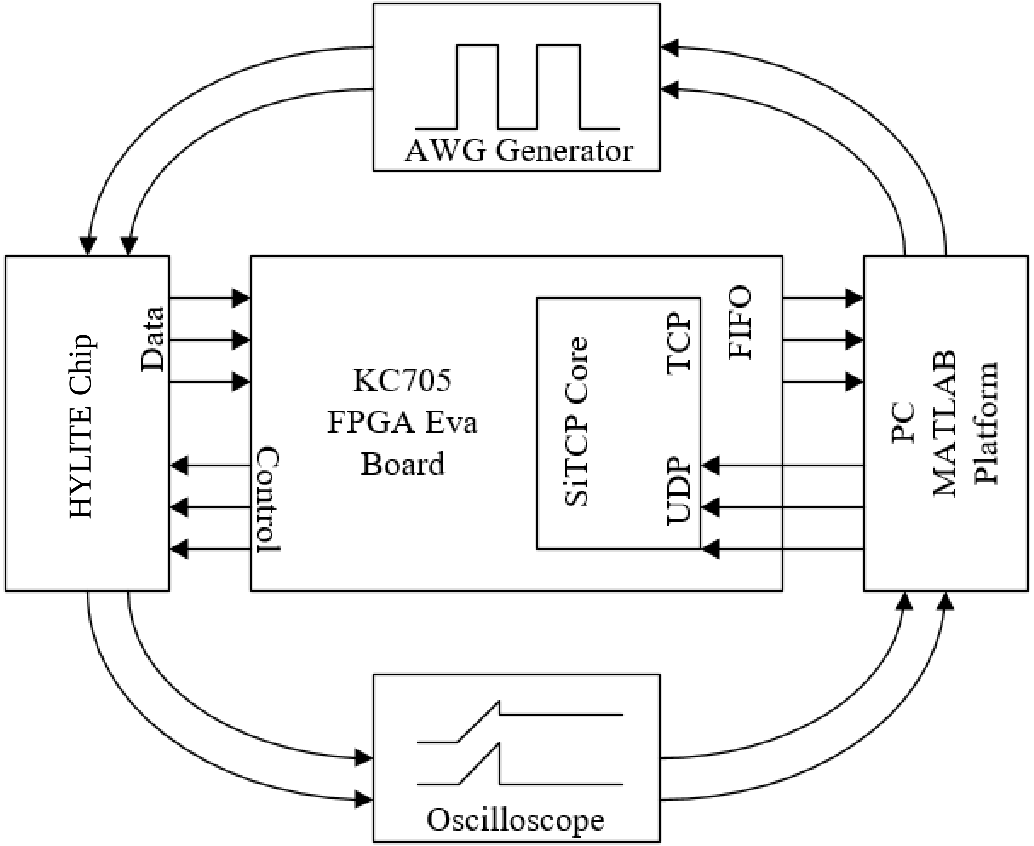


HYLITE0.1 Die

Chip Test PCB

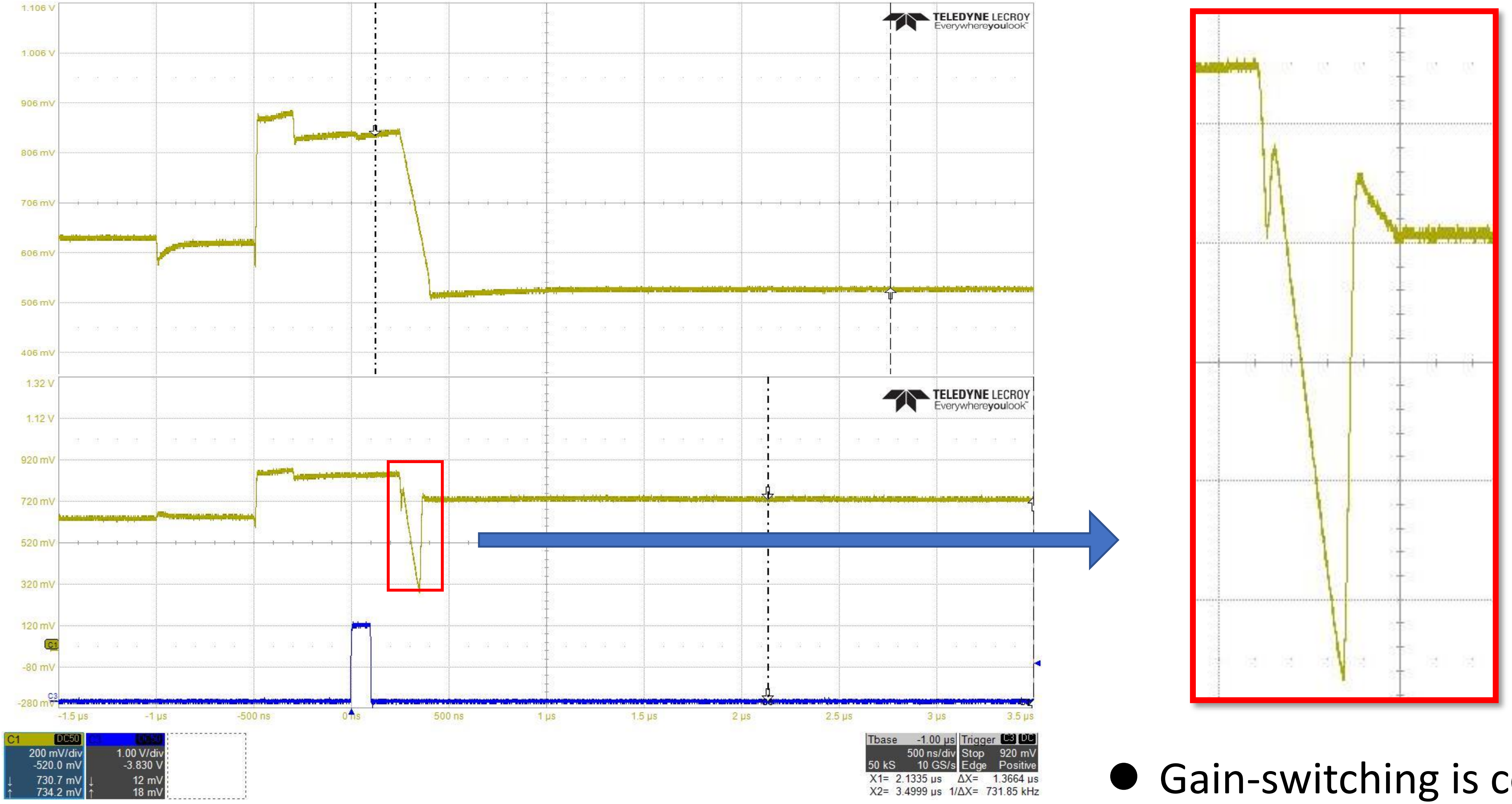


Measurement Environment



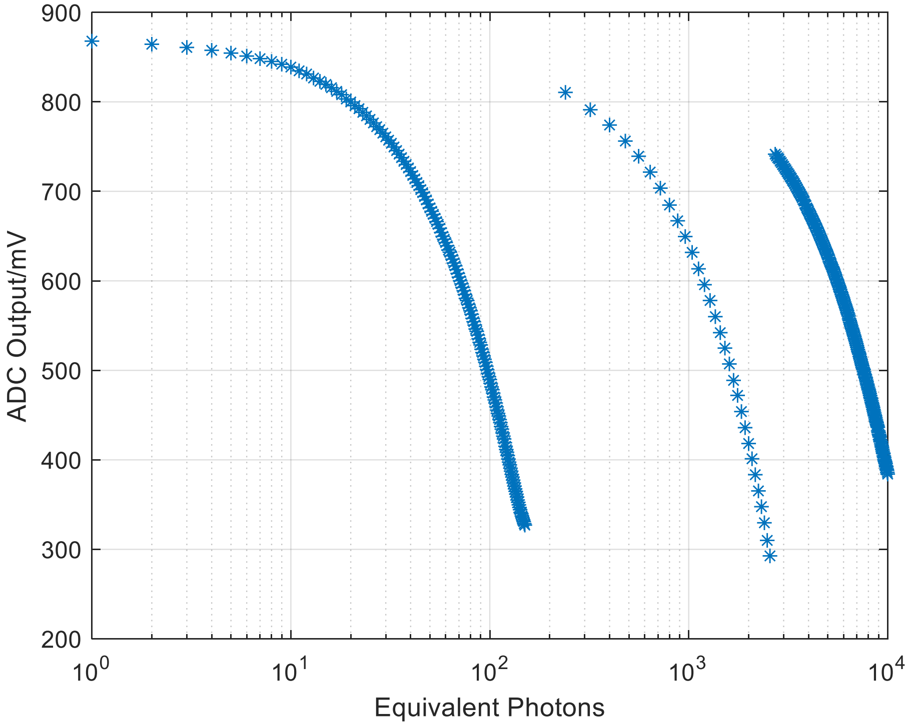
Block Diagram of Measurement System

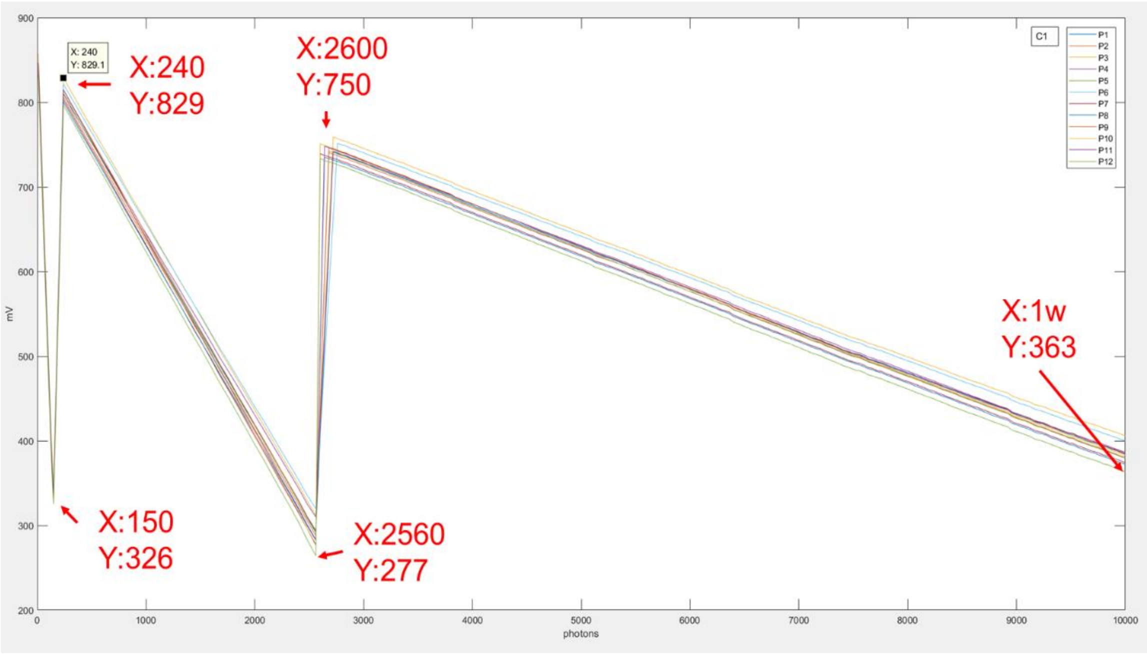
Analog Outputs



- Gain-switching is correct.

Dynamic Range

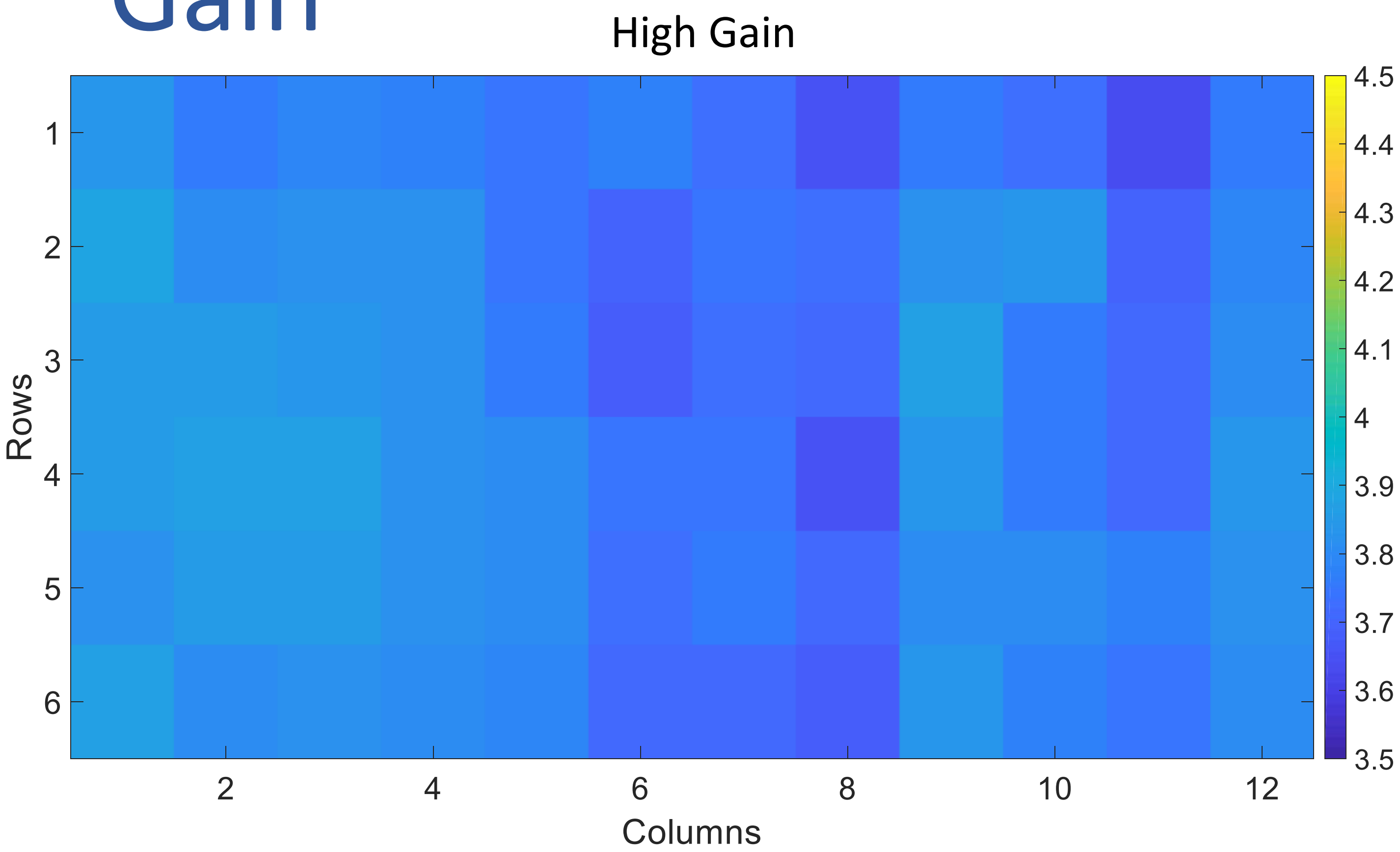




- A dynamic range of 10^4 photons is achieved.

High Gain /12keV photons	Med Gain /12keV photons	Low Gain /12keV photons
1~160	160~2600	2600~10000

Gain



High Gain /(mV/Photon)	Med Gain /(mV/Photon)	Low Gain /(mV/Photon)
3.82	0.23	0.050

- High Gain: G_{MIN}/G_{MAX}=93.6%
- The discrepancy will be corrected by the calibration system in the future.

Noise

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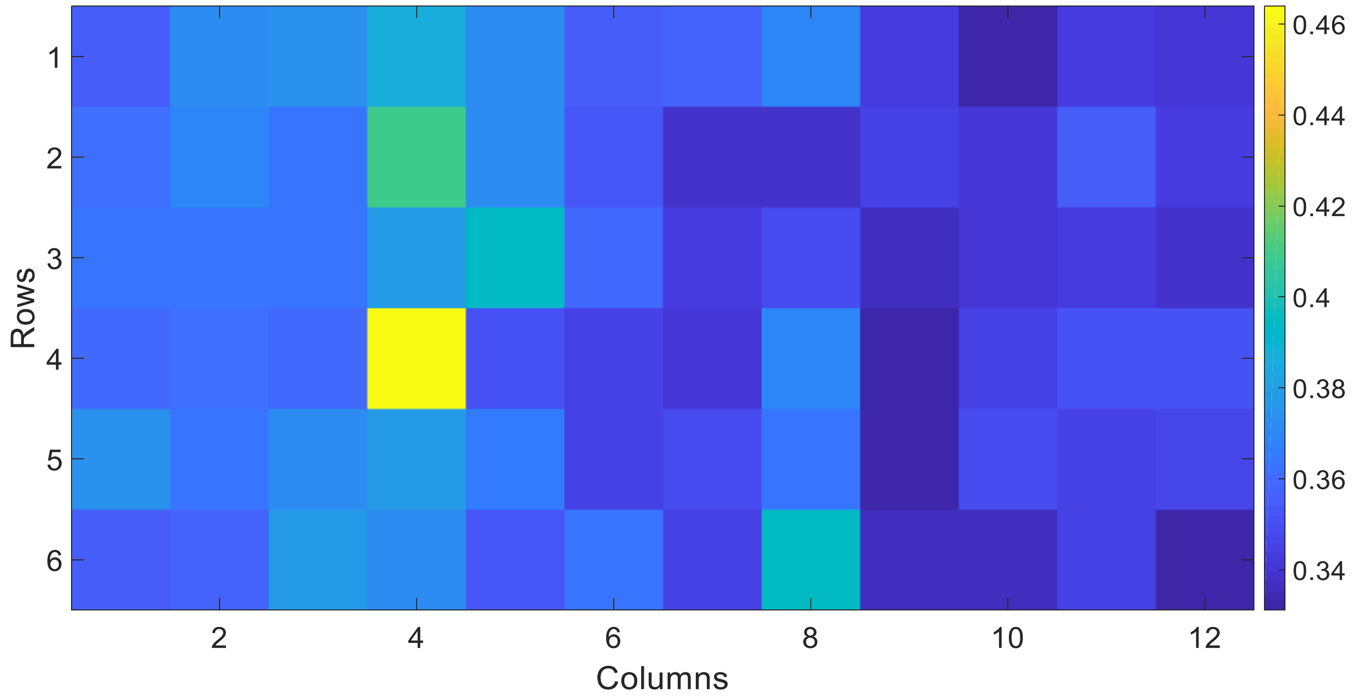

High Gain /12keV γs	Med Gain /12keV γs	Low Gain /12keV γs
0.38	5.1 (12.6)	12.7 (60.0)

- The equivalent input noise is calculated on the number of 12keV photons.
- The noise performance in high gain mode can be improved further by increasing gain.
- Noise in medium and low gain mode is much lower than the minimum Poisson fluctuation in corresponding range.

Non-Linearity

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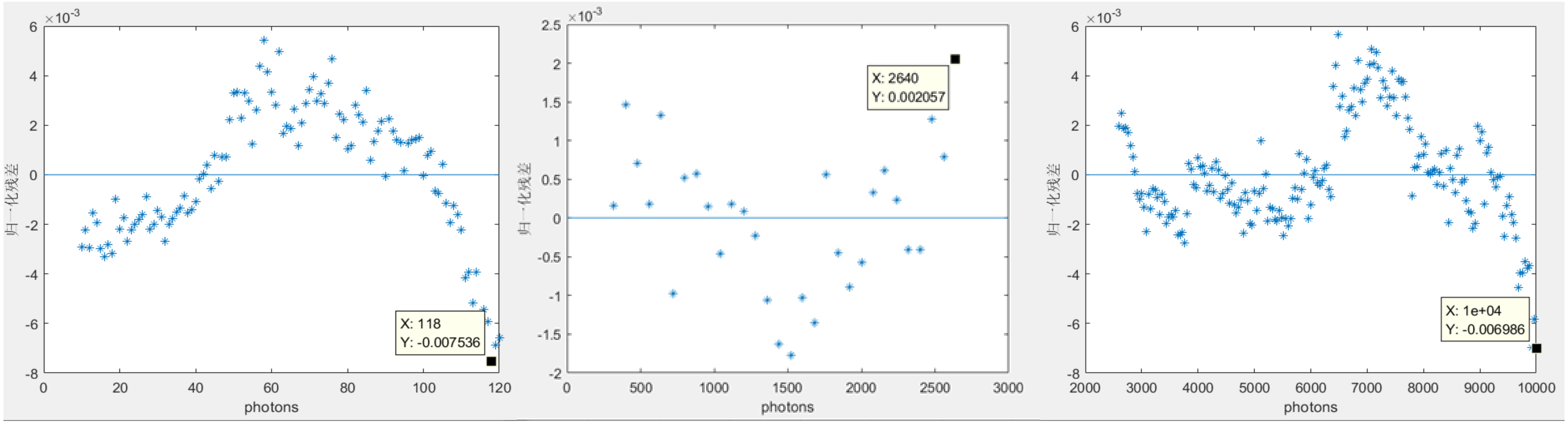
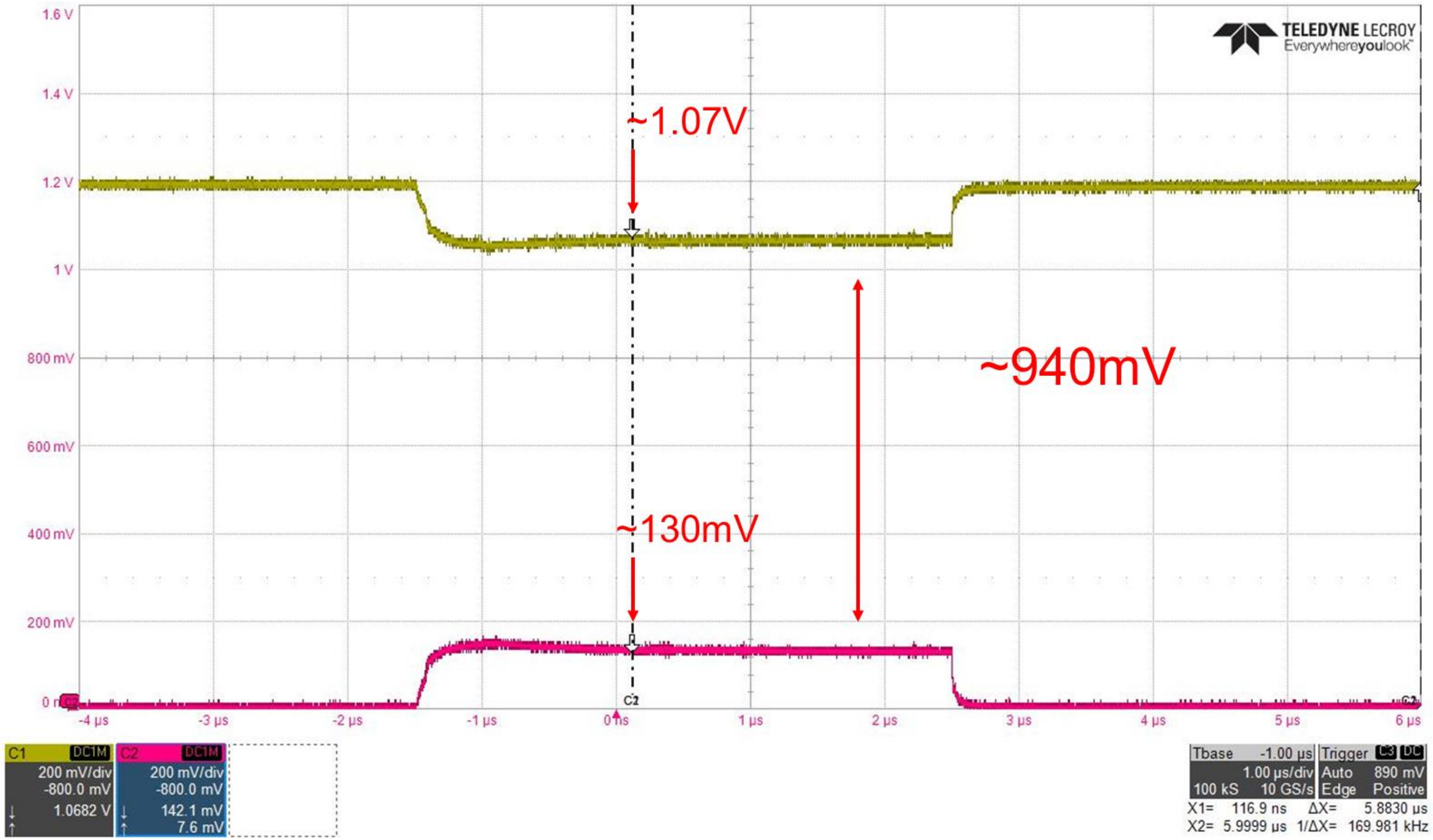


High Gain	Med Gain	Low Gain
0.75%	0.21%	0.70%

- Non-Linearity is less than 1%.

IR Drop



- A test structure was achieved to measure the IR Drop.
- Results show that the simulation is accurate, and attentions must be paid to the power system when it comes to the full-size chip.

Conclusions

- Measurement results show that the pixel works correctly.
- The In-pixel ADC scheme is proved.
- Noise performance could be improved further.
- The full-size chip is under developing.

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