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硅阵列探测器前端变增益宽动态读出 ASIC 初步设计

Summary

Si 探测器输出脉冲电流信号响应动态范围较宽，其动态范围在 fC~pC，可能跨越 3~5 个量级，因此，开展宽动态、高集成度前端读出电路研究是必要的。在这篇文章中，采用 0.18μm 工艺，单通道芯片面积 0.23mm×0.15mm，通过设计三级增益调节电路以满足探测器输出信号的宽动态范围。为对整个电路提供稳定的直流电流偏置，设计了基准电流源电路。仿真结果表明读出电路性能基本符合预期。基于模拟结果，分析了影响电路信噪比主要因素，探讨了减小前端 ASIC 噪声主要技术途径。

The output pulse current signal of Si detector has a wide response dynamic range, and its dynamic range is fC~pC, which may span 3~5 orders of magnitude. Therefore, it is necessary to carry out wide dynamic and high integration front-end readout circuit research. In this paper, a 0.18μm process is used, and a single channel chip area is 0.23mm×0.15mm. A three-stage gain adjustment circuit is designed to meet the wide dynamic range of the detector output signal. In order to provide a stable DC current bias for the circuit, a reference current source circuit is designed. The simulation results show that the performance of the readout circuit basically meets expectations. Based on the simulation results, the main factors affecting the signal-to-noise ratio of the circuit are analyzed, and the main technical ways to reduce the front-end ASIC noise are discussed.

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