ARCADIA

Status Report

CEPC Physics and Detector Meeting
June 2nd, 2021
Remote Connection

Istituto Nazionale di Fisica Nucleare

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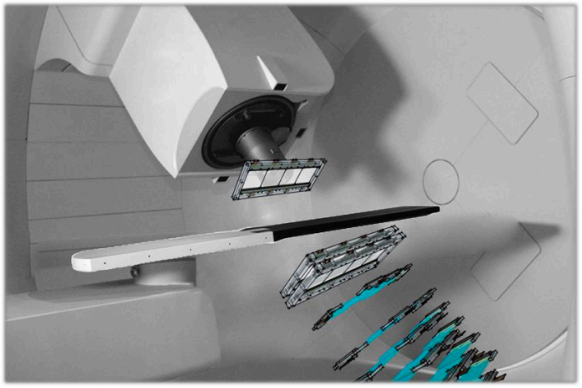
on behalf of the ARCADIA Collaboration

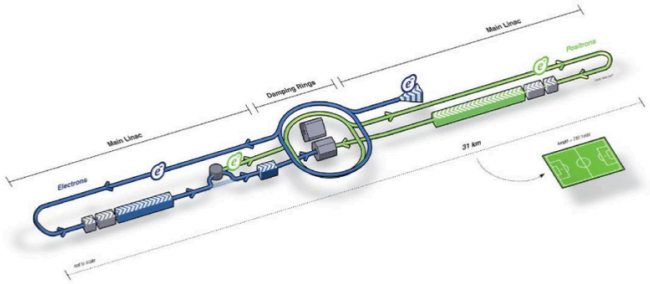
ARCADIA: CMOS DMAPS platform at INFN

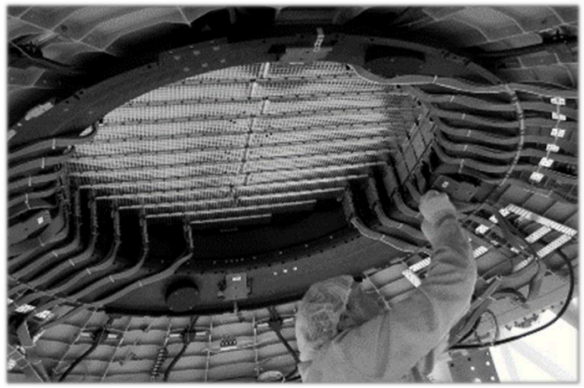
What do we want: to develop a design and fabrication platform for large-area fully-depleted CMOS sensors, at the moment targeting space, medical and future HEP infrastructures (thin sensors) and X-ray detectors (thicker sensors)

What do we need from the silicon foundry:

- access to an engineered CMOS process (developed in collaboration with LFoundry) and custom starting substrates
- access to future SPW runs for dedicated reticle size (next 3 years) and larger-than-reticle (from 2023) designs





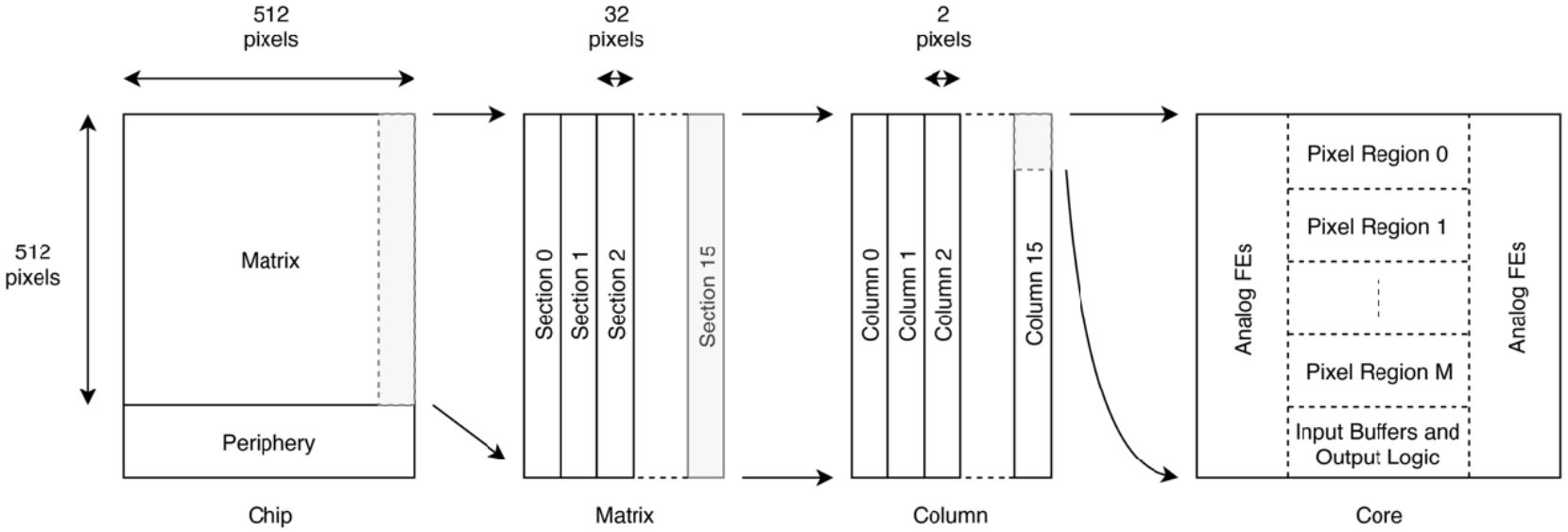


Medical
- Low power (≤ 40 mW/cm²)
- Medium rate ≈ 10 MHz – 100 MHz/cm²
- Ultra low material budget (low energy)
- Very large area (≥ 16 cm²)
- 3-side buttable design
- Low to medium rad-tolerance ≈ 10 kGy

e⁺e⁻
- Low power (≤ 40 mW/cm²)
- Medium rate ≈ 10 MHz – 100 MHz / cm²
- Very low material budget
- Large area (≥ 6 cm²)
- 3-side buttable design
- Low to medium rad-tolerance ≈ 10 kGy

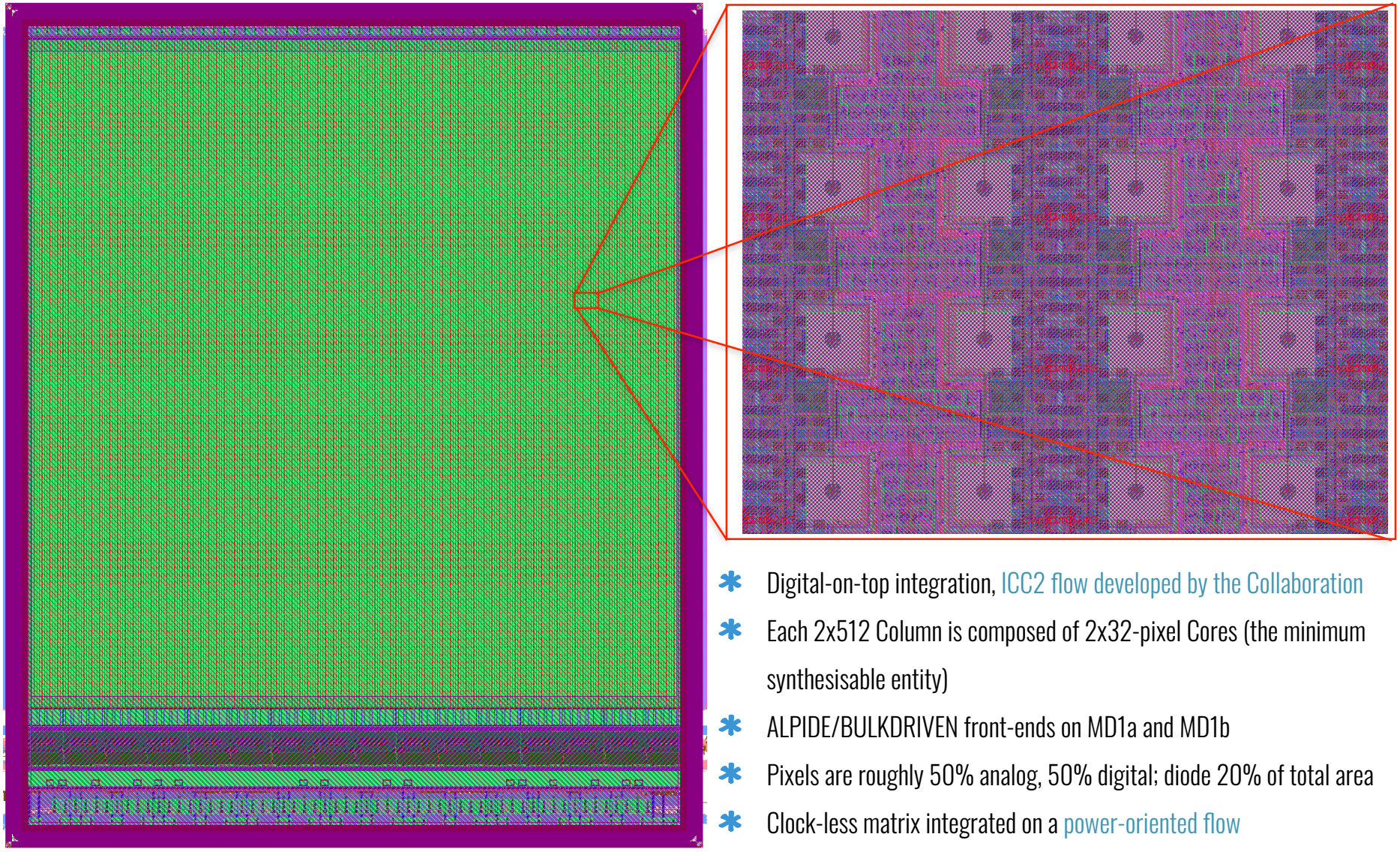
Space
- Ultra low power (≤ 10 mW/cm²)
- Very low rate ≈ kHz/cm²
- Low material budget
- Large area (≥ 6 cm²)
- 3-side buttable
- Low rad-tolerance ≈ 1 kGy

ARCADIA-MD1: Main Demonstrator Chip



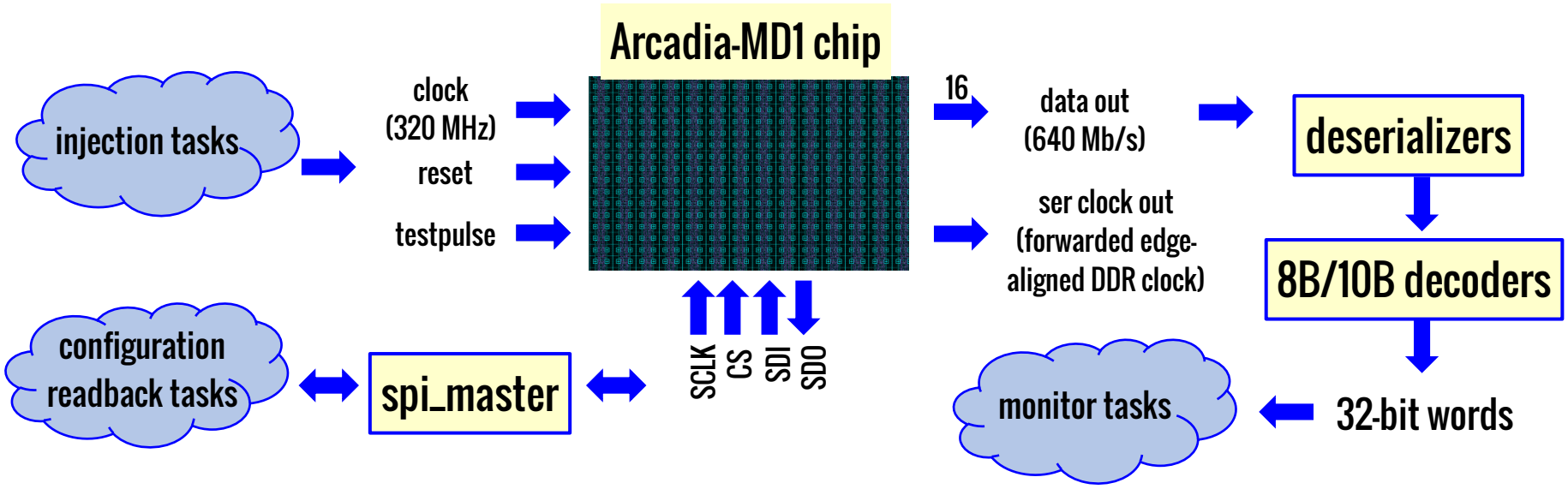
- Pixel size 25 µm x 25 µm: process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam).
- Matrix core 512 x 512, "side-abuttable" to accomodate a 1024 x 512 silicon active area (2.56 x 1.28 cm^2). Matrix and EoC architecture, data links and payload ID: scalable to 2048 x 2048*
- Triggerless binary data readout, event rate up to 100 MHz/cm^2
- First Engineering Run (SPW) with ARCADIA-MD1 by 11/2020, 2nd full CMOS maskset mid-2021 (higher data throughput, SEU protection, on-chip data compression), 3rd SPW mid-2022 with design fixes, explorative sensor and CMOS designs

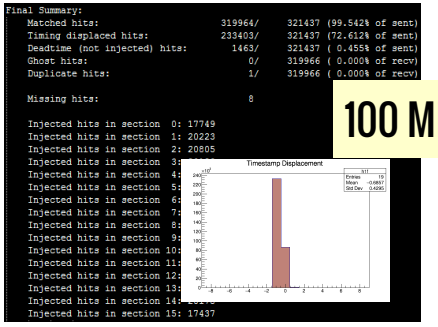
ARCADIA - Main Demonstrator Chip



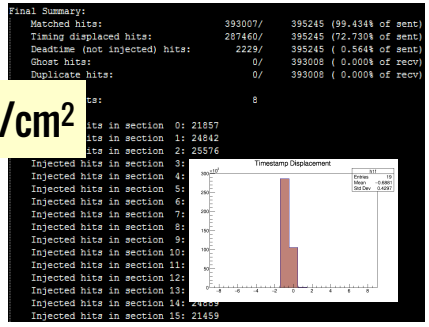
- Digital-on-top integration, ICC2 flow developed by the Collaboration
- Each 2x512 Column is composed of 2x32-pixel Cores (the minimum synthesisable entity)
- ALPIDE/BULKDRIVEN front-ends on MD1a and MD1b
- Pixels are roughly 50% analog, 50% digital; diode 20% of total area
- Clock-less matrix integrated on a power-oriented flow

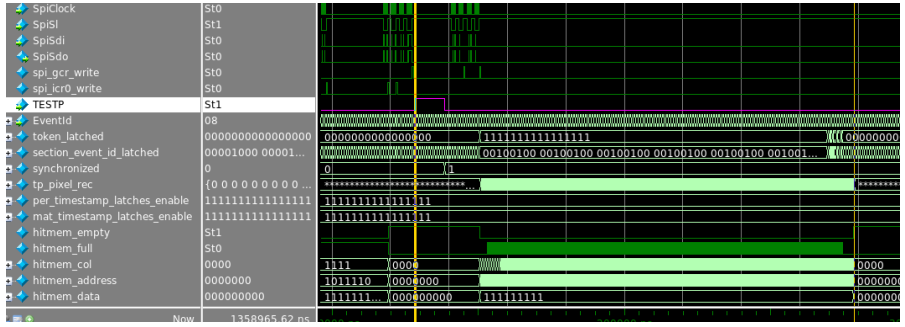
ARCADIA-MD1 Verification Framework





100 MHz/cm^2





dEdx9.2_thetamax0_thickness100_posMED_100MHz_50mmColl_uniform

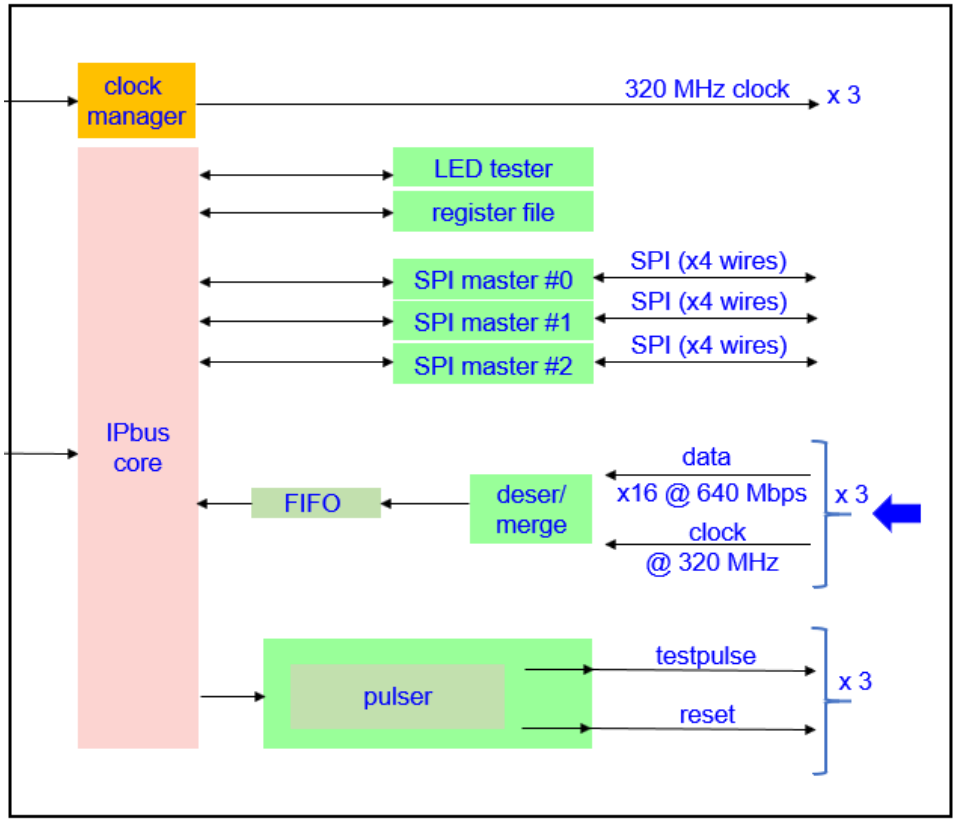
dEdx23_thetamax4_thickness100_posMED_100MHz_50mmColl_uniform

ARCADIA DAQ Firmware

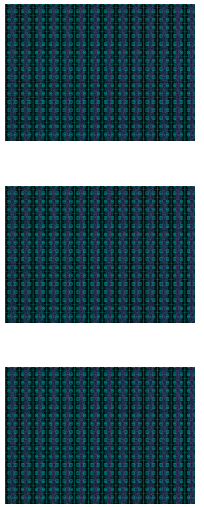
- The DAQ firmware blocks have also been inserted into the same simulation framework used for the ARCADIA-MD1 chip verification;
- We currently have a **universal simulation framework** in which the **ARCADIA-MD1 chip is configured and readout** via IPbus atomic operations **through the DAQ blocks**. This list of atomic operations is also being translated into the software running on the PC, which is being designed.

IPbus tasks:

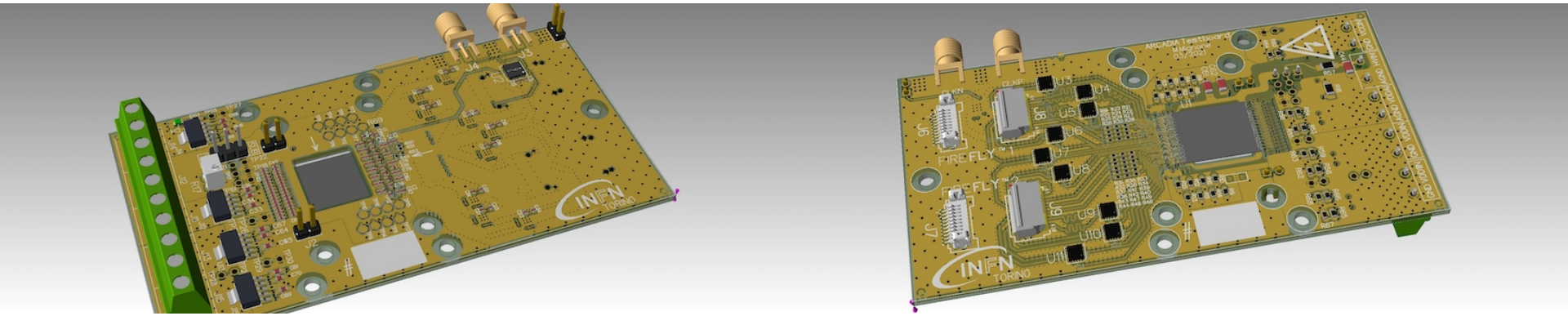
IPbus write
IPbus read
IPbus read_block



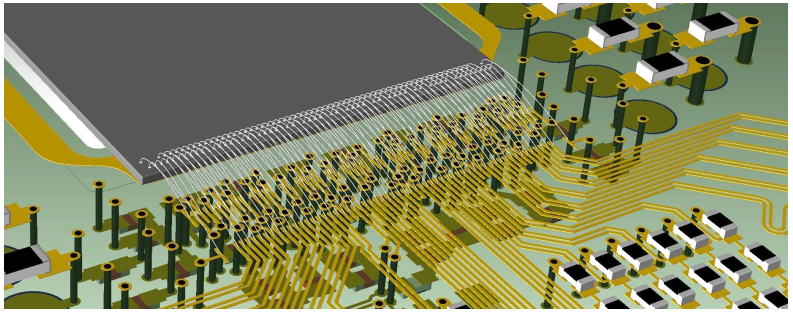
ARCADIA- MD1
(3 chips)



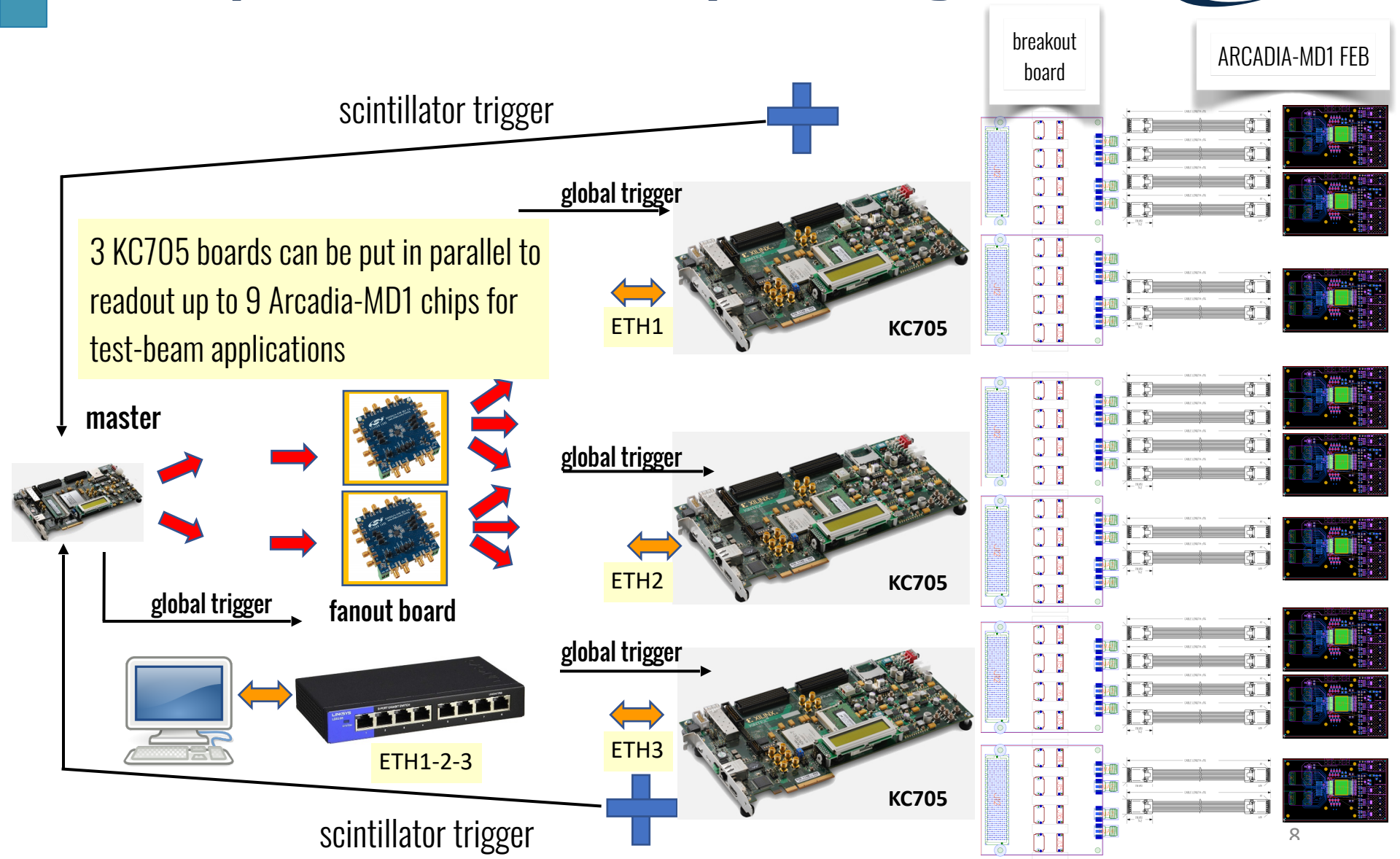
ARCADIA-MD1 Front-End Board



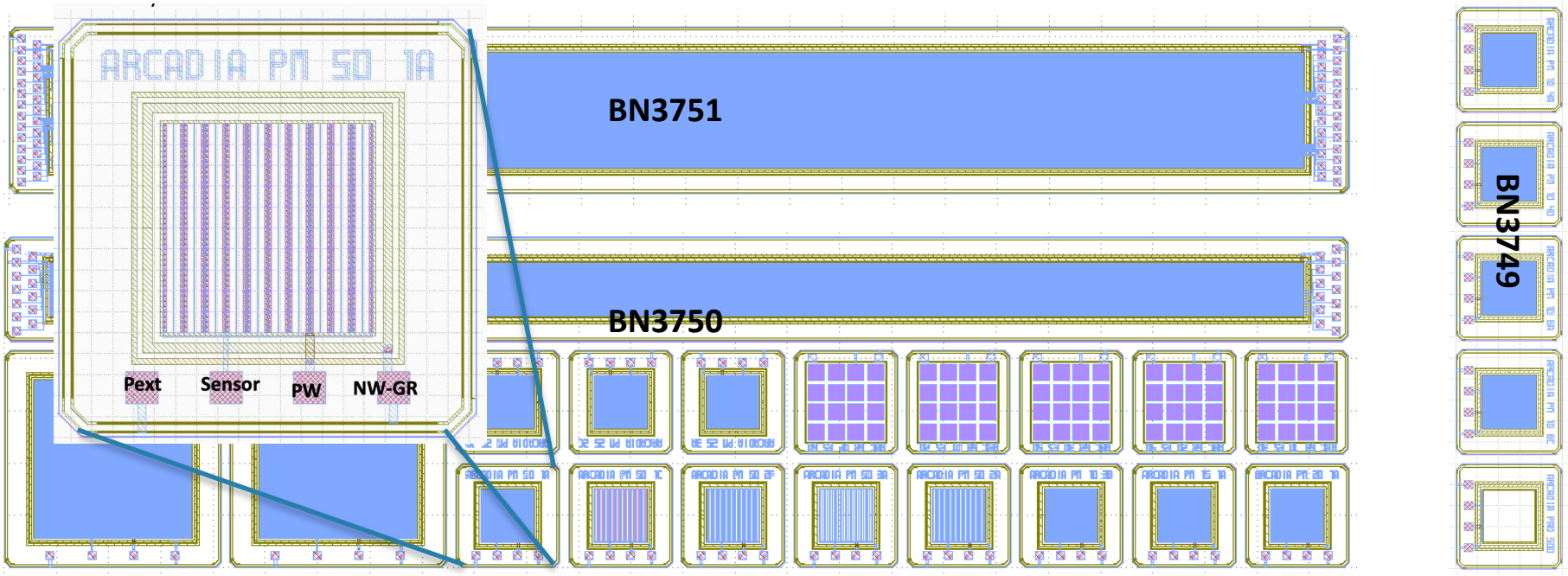
- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Possibility to use both an external low jitter Clock (via SMA connectors) or the clock provided by the FPGA
- Possibility to connect the high voltage on the DMAPS substrate or via the (wire bonded) pads on top
- Independent voltage regulators for the regional domains on-chip (IO Buffers, Analog Core, Digital Core)
- Extensive lab tests for the C-LVDS links
- PCB through-hole for matrix BSI
- production finished, in transit



Multi-plane MD1 Telescope Configuration



Pixel/Strip Test Structures



* **strips come in different flavours:**
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

* **and pixels as well:**
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - **10 μm (6 variants)**

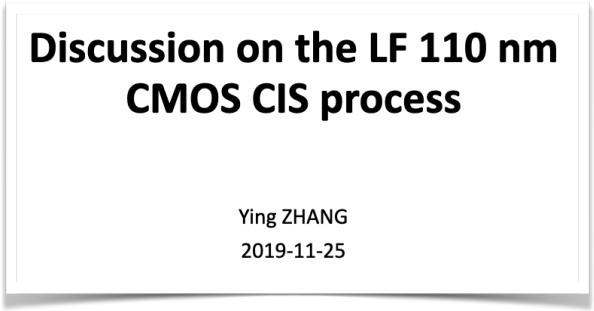
Getting ready for silicon: priorities

- **Measurements on bonded test structures (first non-irradiated and then irradiated with x-rays and neutrons), front-side and back side**
  - IV curves with temperature, extraction of depletion, punch-through voltages, dark current and capacitance
  - Charge collection with focused pulsed laser (back-side). On pixels: only signal evolution with time and position of the laser spot. On strips: charge sharing is also possible.
  - Lab. sources. (top-side and back-side)

- **Characterisation of the ARCADIA-MD1**
  - functional and electrical characterisation (basic functionalities with on-chip test pulse and hit injection, s-curves, threshold calibration, rate assessment)
  - laser scans with red and IR light (CCE vs bias voltage, uniformity, clustering and resolution)
  - tests with x-ray and radioactive sources (55Fe, 241Am, 90Sr)
  - cosmic ray stand (sync and event building, efficiency, resolution) and beam tests with MD1 telescopes

Platform for sensor design and fabrication

- Discussion on the use of SEED/ARCADIA for the R&D towards CEPC started in 2019.



中国科学院高能物理研究所
Institute of High Energy Physics
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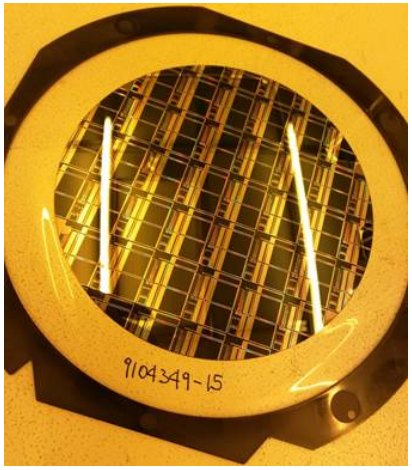
- **The access to LFoundry Process Design Kit (PDK) and Synopsys PyCells for CMOS LF11is is active at IHEP since January 2020.**
  - ☑ INFN and IHEP can share CMOS design databases and program shared tapeouts to foundry
- **Discussion started on design and fabrication flow towards a Joint IHEP-INFN MAPS:**
  - INFN provides IHEP with a signal sample database and a simplified sensor geometry
  - IHEP designs (in-house or in cooperation with INFN) a CMOS MAPS using LFoundry LF11is
  - INFN cares the final DRC on IHEP's gds2, validation of the design and production

ARCADIA: status and plans in a nutshell

- **ARCADIA** has now secured a total budget of 1.4 M€ with several groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space Instruments

- **Schedule for 2021-2022**
  - all hardware and firmware ready for testing, first silicon just delivered
  - 1st SPW run included 800 mm2 of innovative DMAPS, sensor and CMOS technology (first tests on sensors are ok, wafers currently being diced)
  - 2nd run mid-2021: in preparation, 3rd run planned for mid-2022;



Thank you for listening!