Status of TaichuPix chips

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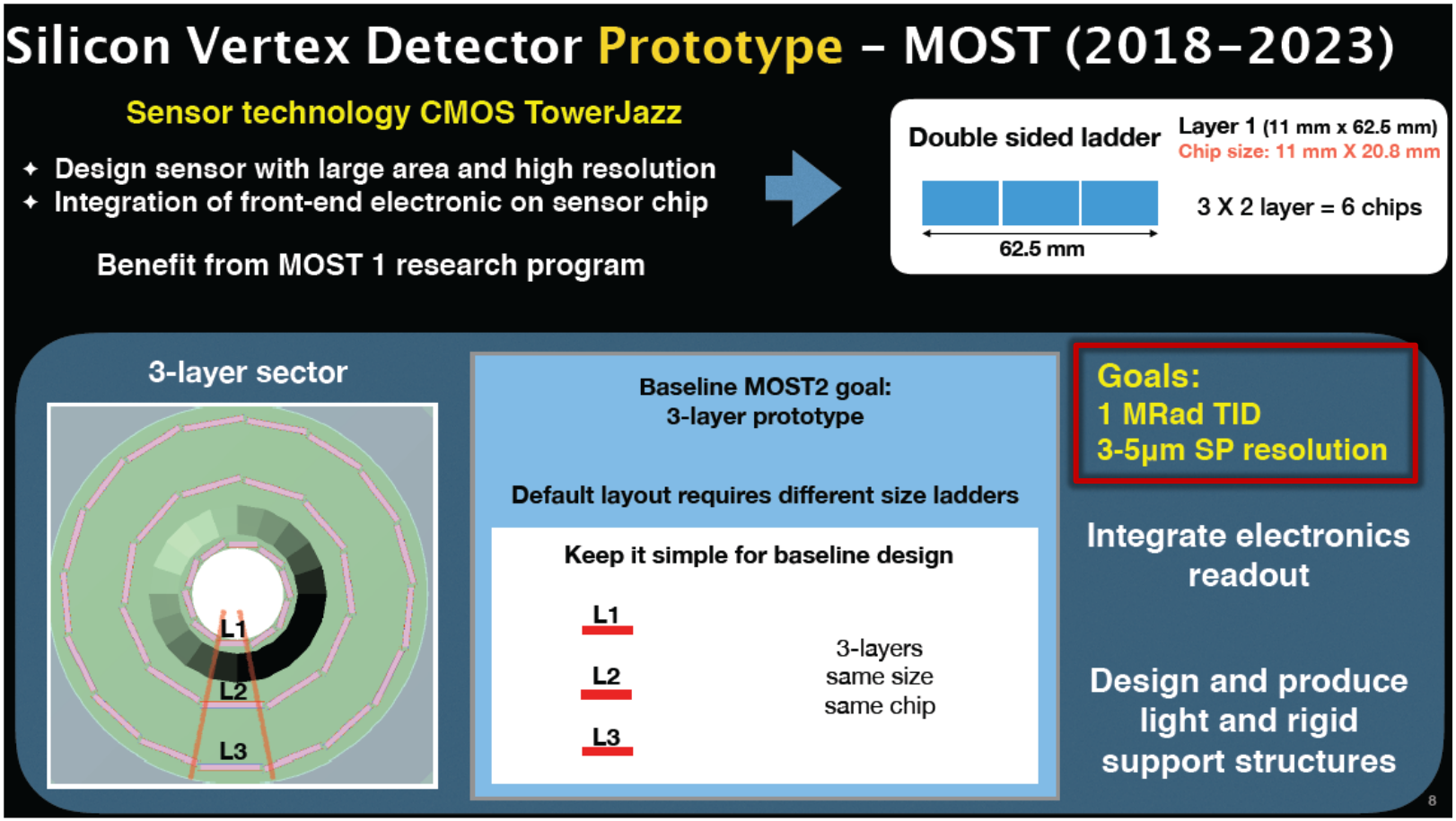
On behalf of the CEPC MOST2 Vertex detector design team

2021-6-25

Outline

- **Status review**
- **Updates on test result**
- **Full size chip design**

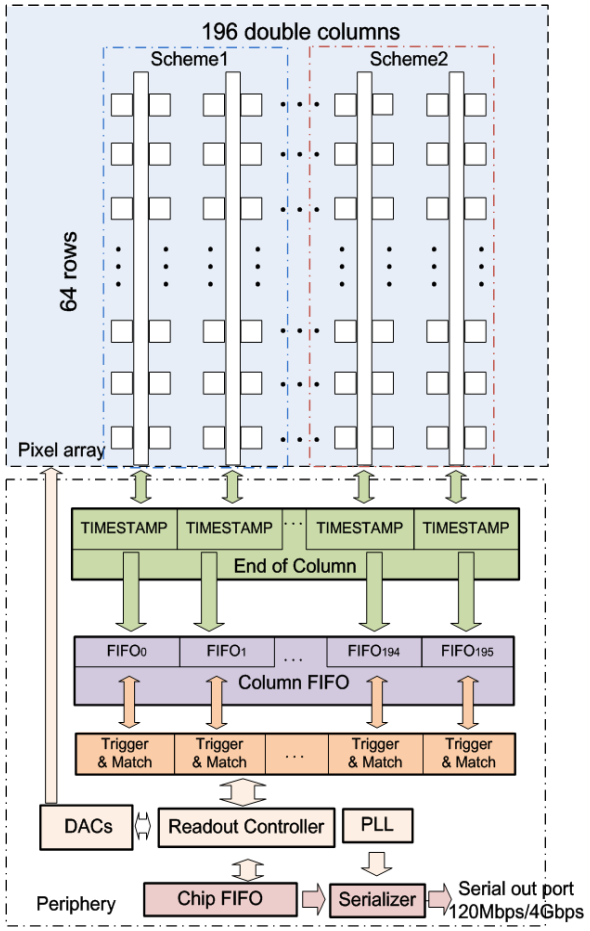
MOST2 project requirements on pixel chip



- **Motivation for TaichuPix chip design**
  - Large-scale & full functionality pixel chip
  - Fit to be assembled on ladders with backend Elec. & DAQ

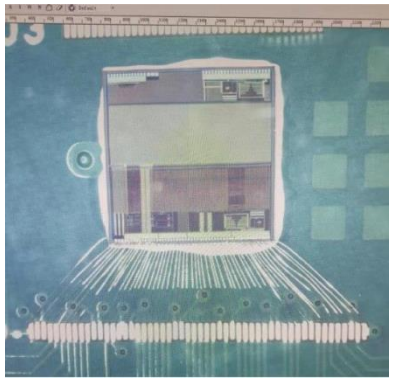
Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

TaichuPix architecture

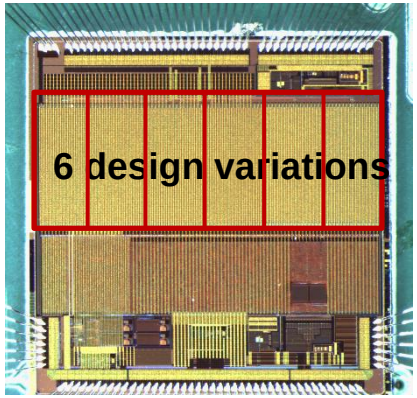


- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - Priority based data driven readout, zero-suppression intrinsically
  - Modification: time stamp is added at EOC whenever a new fast-or busy signal is received
  - Dead time: 2 clk for each pixel (50 ns @40MHz clk)
- **Two parallel pixel digital schemes**
  - ALPIDE-like: Readout speed was enhanced for 40MHz BX
  - FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area
- **2-level FIFO architecture**
  - L1 FIFO: In column level, to de-randomize the injecting charge
  - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
  - Make the data rate in a reasonable range
  - Data coincidence by time stamp, only matched event will be readout

TaichuPix small prototypes overview



TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm



TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

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Chip to chip uniformity of threshold and noise

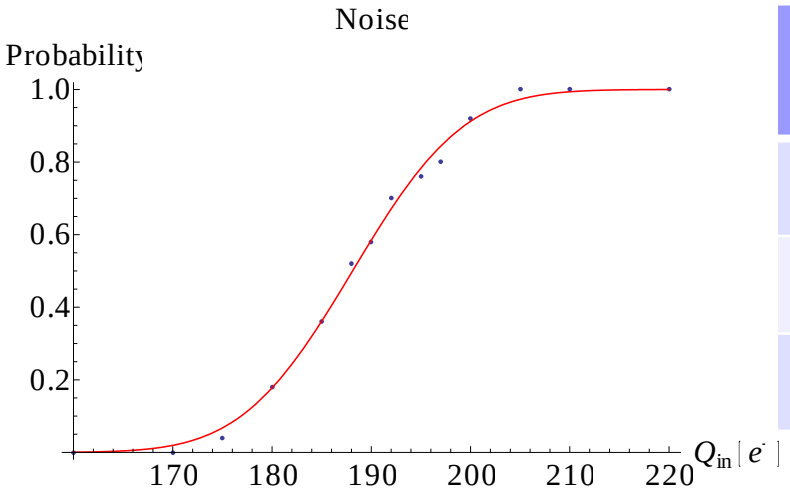
- **Bias setting: ITHR = 6.2 nA, VSUB = 0 V**
  - Converting the noise/threshold voltage to electrons by 0.91 mV/e-
    - Charge injection capacitance in each pixel is 0.177 fF extracted from layout

Chip4	Threshold Mean (e-)	Threshold rms (e-)	Temporal noise (e-)	Total equivalent noise (e-)
S1	272.9	50.9	30.0	59.1
S2	299.9	55.7	27.5	62.1
S3	393.4	59.7	24.9	64.7
S4	421.0	57.8	27.0	63.8

Chip7	Threshold Mean (e-)	Threshold rms (e-)	Temporal noise (e-)	Total equivalent noise (e-)
S1	308.2	54.9	31.5	63.3
S2	320.5	56.0	28.1	62.6
S3	456.6	65.8	24.1	70.0
S4	471.5	65.4	28.5	71.3

Simulated threshold and temporal noise

- **Transient noise simulation with extracted layout of FE for different input charge → s-curve of one pixel ➔ mean threshold and temporal noise**
- **Nominal design: Cd = 2.5 fF, AVDD = 1.8 V, ITHR = 4.5 nA**

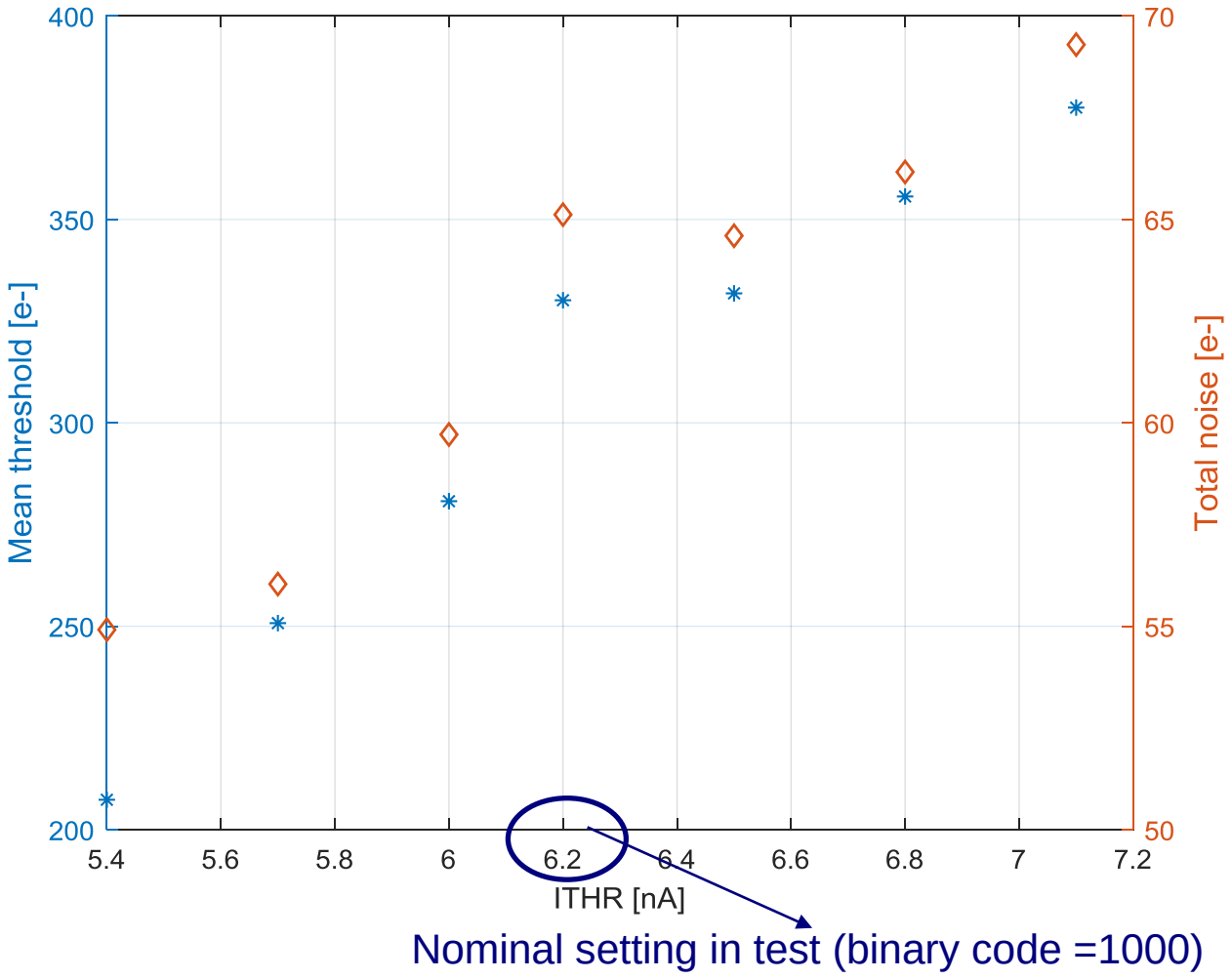


	Threshold Mean	Threshold rms (e-)	Temporal noise	Total equivalent noise (e-)
Cd= 2.5 fF AVDD =1.8 V	188.1 e-	4.7 e-	8.8 e-	10 e-
Cd= 5 fF AVDD =1.8 V	296.8 e-	7.5 e-	10.0 e-	12.5 e-
Cd= 5 fF AVDD =1.745 V	297.6 e-	7.5 e	10.0 e-	12.5 e-

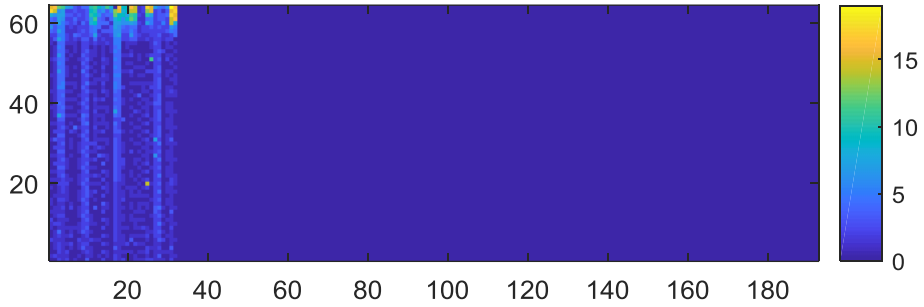
- **Sensor capacitance Cd has a direct effect on the threshold and noise level**
  - Cd is strongly dependent on the substrate biasing
    - Cd =2.5 fF @ -6V SUB; Cd = 5fF @ VSUB = 0 V tested by CERN
  - The tested threshold 276 e^- agreed well with simulated 297 e^- at Cd= 5fF@ 0V SUB
    - Proves the pixel design, and the Cinj calibration gain
  - The limit to further push down the threshold is that ITHR cannot be set smaller because of the leakage current from DAC

Working range of threshold and noise

- **Measuring s-curve of one Db-col of S1 on Chip7 with different ITHR (current biasing)**



Fake hit rate test at chip level



Hitmap for 2 hours(only S1 is enabled)

ITHR code	Fakehit	Total time (s)	Fakehit rate
3'b010	3238	7200	5.5e-12
3'b100	1/0/543	300	4.1e-14 /2.2e-11

Nominal setting in test (binary code =1000)

Table 1
Sensor requirements for the ALICE ITS Upgrade for Inner Barrel (IB) and Outer Barrel (OB) [1].

Parameter	IB	OB
Sensor thickness (μm)	50	50
Spatial resolution (μm)	5	10
Dimensions (mm^2)	15 × 30	15 × 30
Power density ($mW\,cm^{-2}$)	300	100
Time resolution (μs)	30	30
Detection efficiency (%)	99	99
Fake hit rate[a]	10^{-5}	10^{-5}
TID radiation hardness[b] (krad)	2700	100
NIEL radiation hardness[b] (1 MeVn_{eq}/cm^2)	1.7×10^{13}	10^{12}

[a] Per pixel and readout.
[b] Including a safety factor of 10, revised numbers w.r.t. TDR.

- **Fake hit definition:**
  - $R_{fh} = \frac{N_{fh}}{N_{pix}N}$
  - N_{fh}: fake hit counts
  - N_{pix}: total pixels for test
  - N: sampled frame counts
    - =total time/25ns
- **Compared with ALPIDE fake hit rate of 10^{-5}, with a readout time (frame time) of 500 ns, the tested fake hit rate is low**
  - Frame rate is much higher
  - Threshold is set at relatively high level and cannot be pushed down further
- **The test environment also suffers from EMC in the space with a sudden flash on image**
  - can be improved with proper shielding for even lower fake hit rate

Summary of the test of TaichuPix-2

- **Major functionality fully verified**
- **Detected bugs/problems – solutions for the engineering run**
  - Pixel matrix
    - ALPIDE-like approach not functioned
      - Not integrated in the full size chip
    - Tested noise/threshold higher than simulation, while the pixel design is the same
      - Mainly due to the increased Cd from 2.5fF to 5fF, while SUB was only biased at 0V
        - ➔ Tested threshold at 0V SUB biasing agreed well with simulation
      - Threshold setting (ITHR) by DAC has to be pushed down, to have reasonable detection efficiency and spatial resolution for MIPs
      - Cinj can not be effectively calibrated
    - Kept unchanged for conservative consideration
  - DAC
    - Large leakage current: threshold can not be set to the current as low as expected
      - New block designed specifically for low current path, bypass-able with the former design
    - Found non-linearity region in the transfer curve for all the DACs
      - Not critical for the biasing
  - LDO not well functioned
    - Will only be involved as a test block (black box) in the engineering run
    - The full size chip has to be power supplied by independent powers

Outline

- Status review
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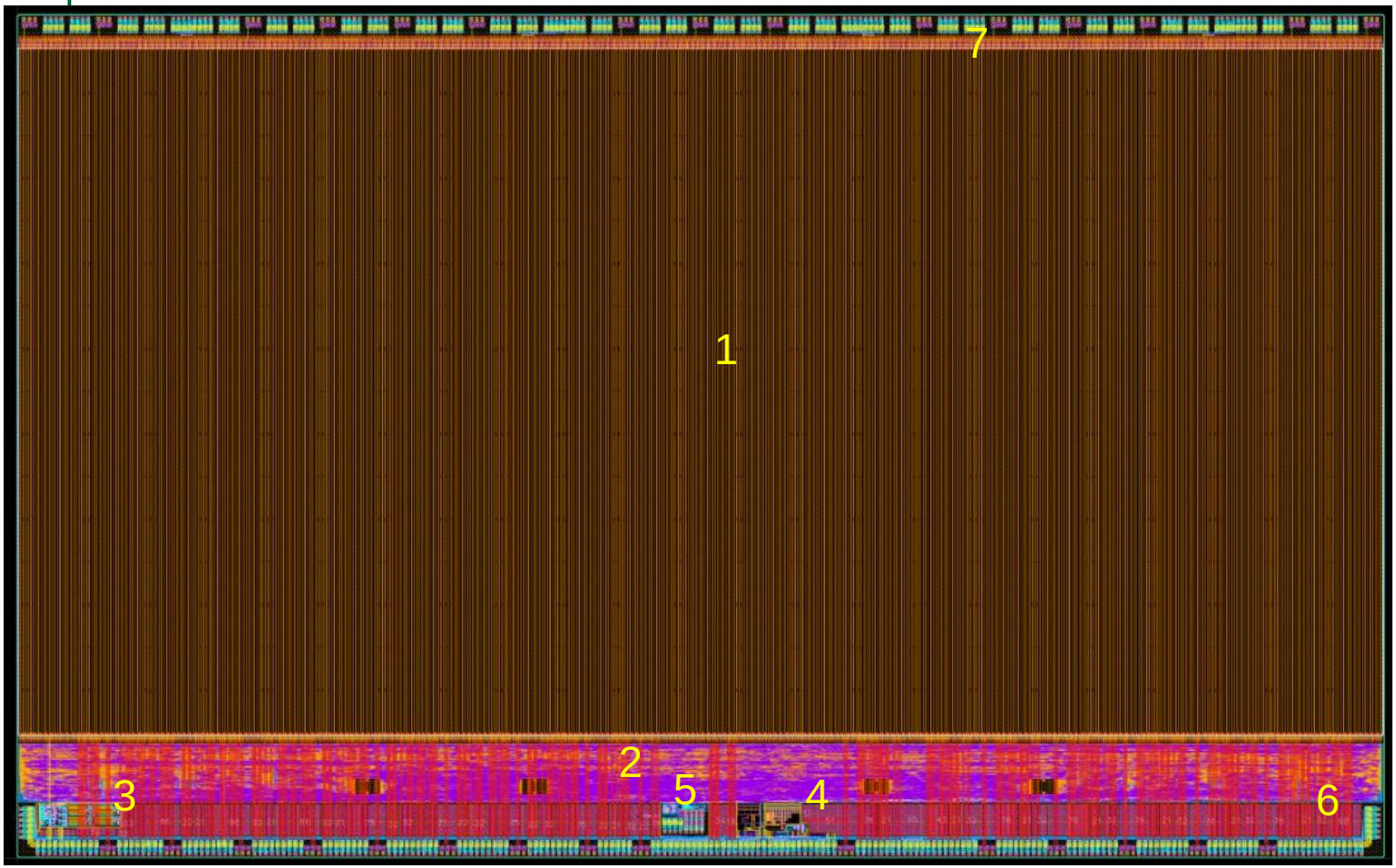
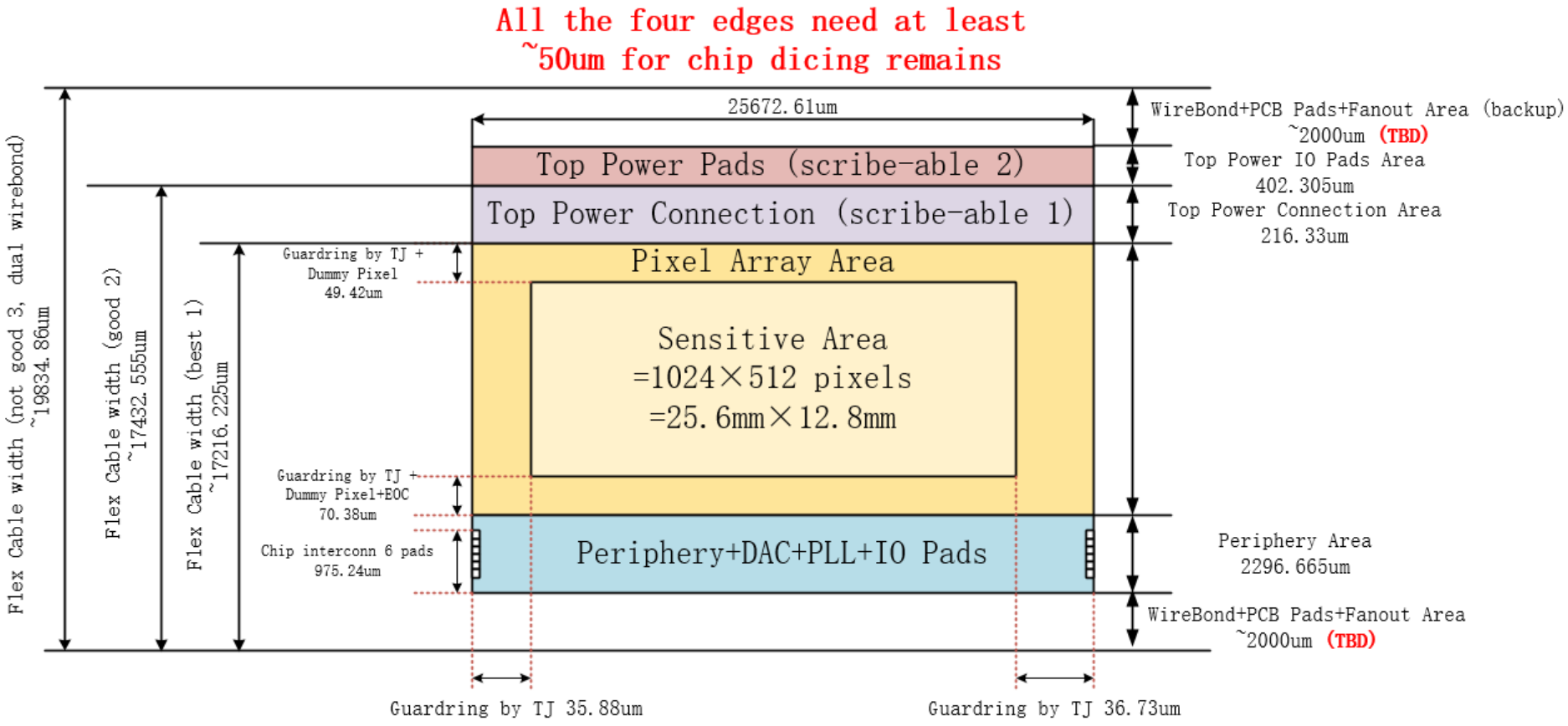
Overview of the full size engineering run



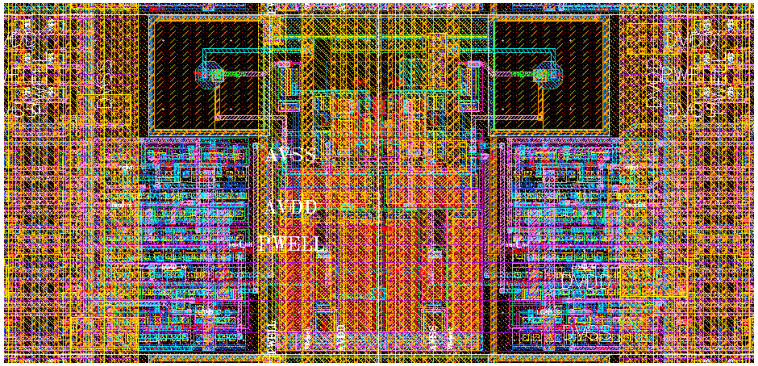
1. Pixel array 1024*512
2. Periphery
3. DAC & Bias generation
4. Data interface
5. LDO (test blocks)
6. Chip inter-connection features
7. Scribe-able top power connection features

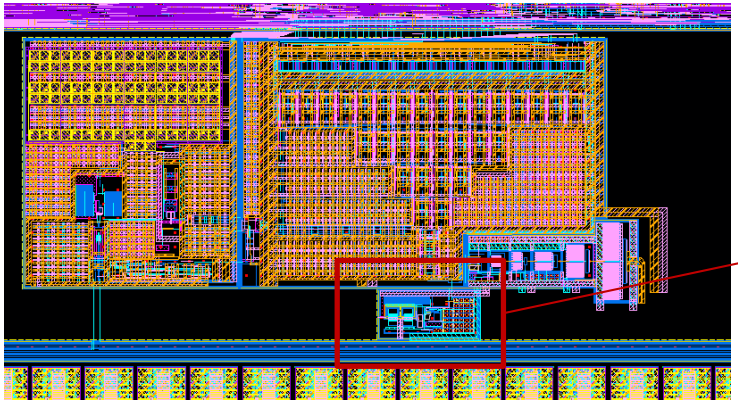
- Process: TowerJazz 180 nm 7M2L (2 Top Metal)
- Pixel cell copied exactly from MPW + scaled logic with new layout Periphery + debugged/improved blocks + enhanced power network

Full size chip dimension



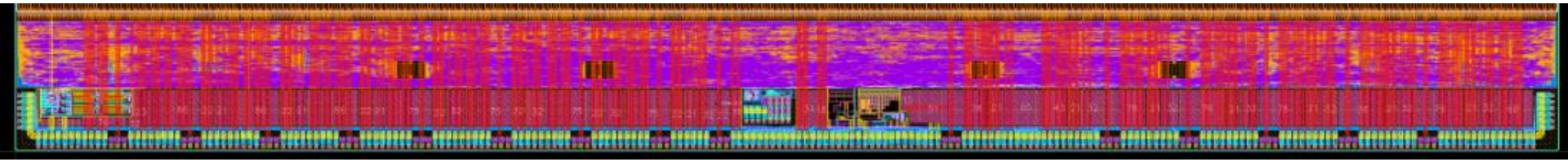
Design improvement for the full size chip



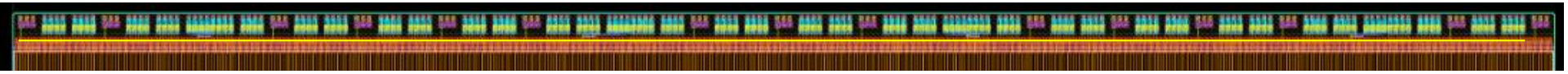


- **Process improved for better power supply: 6 Metals to 7M with 2 Top metal**
  - Will help for the full size chip power integrity
- **25 μm×25 μm pixel, unique design (S1)**
- **A 1024×512 Pixel array**
- **Periphery logics**
  - Unique design for FE-I3 like readout
- **High speed data interface**
  - Optimized for trigger mode and low power: optional low power LVDS port added
- **On-chip bias generation**
  - Bugs detected & solved from the Tcpx2 test
- **IO placement in the final ladder manner**
  - chip interconnection bus features included for ladder
- **LDO will be independently tested as a test block due to the remain issues**

Power net arrangement in IO



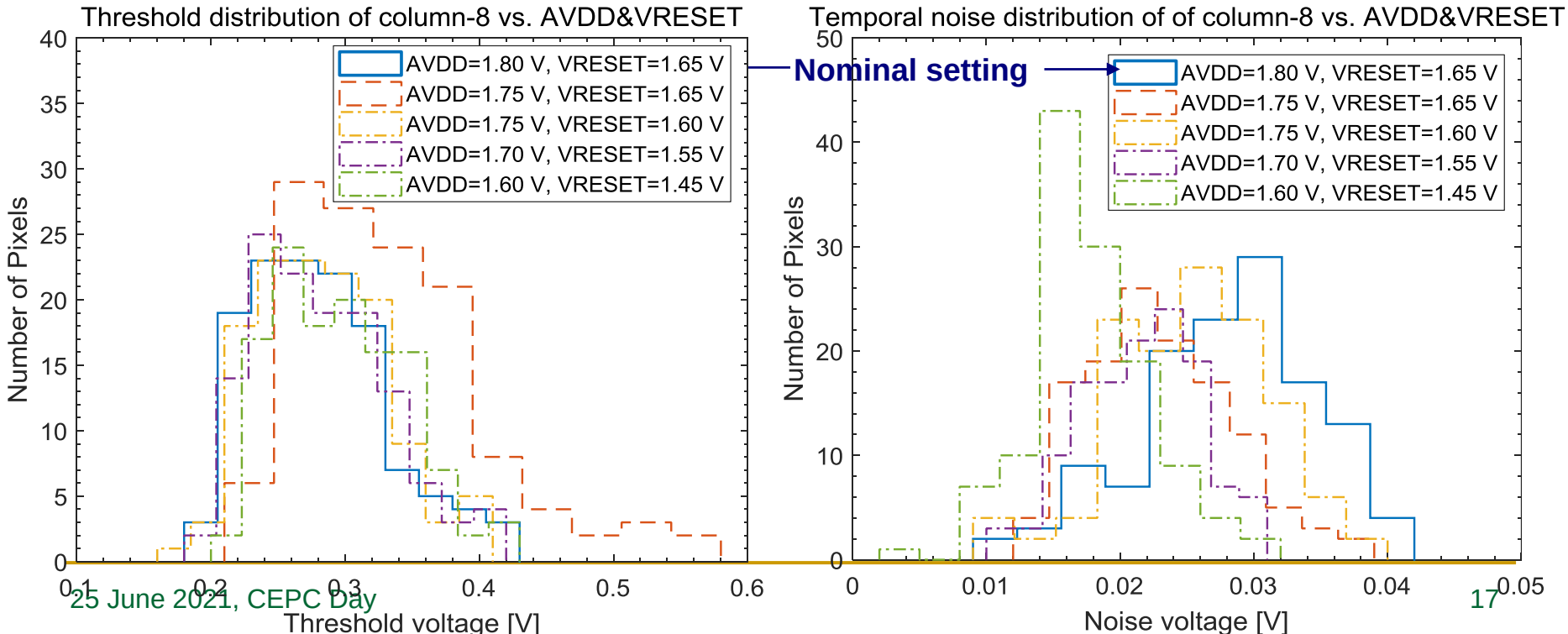
- **227 IOs at the bottom**
  - 37 signal pads, 190 power pads
- **Power interface ports to the matrix**
  - Analog: 18, furthest 2420um, longest supply path 48 column
  - Digital : 16, furthest 3300um, longest supply path 132 columns
  - Periphery: 15, furthest 3400um, longest supply path 1700um



- **Power Pads and power/bias rails at the top to help ease the IR Drop**
  - 2 levels dice-able for complete power study
    - top IO+ power rails: full testability at the test board
    - Only with power rails:
      - extra power path; extra bias connection make the resistance half
      - Only 200um dead zone added, with noticeable improvement
    - Can be fully diced, left as a real chip for ladder

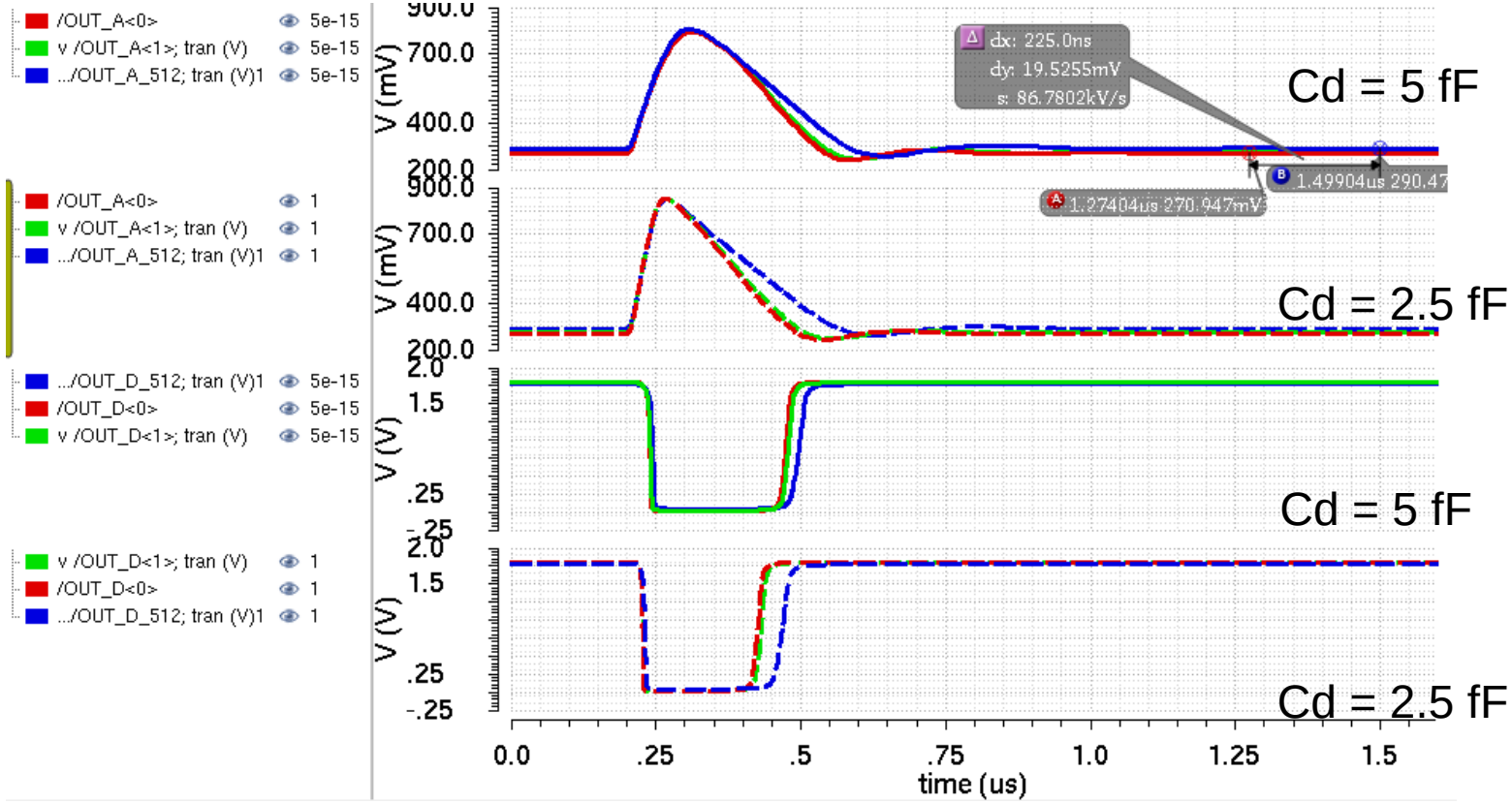
Functionality vs imperfect power supplies

- **Measured s-curves of one double column of S1 on chip 7**
  - Lower power leads to obvious threshold shift and larger dispersion
    - Difference in AVDD changes the working point of FE
  - **Decreasing AVDD and VRESET with same level results in slight changes in threshold distribution**, but lower average temporal noise due to the fact that temporal noise decreases with VRESET
- **Conclusion: chip can work at least 1.7V with VRESET tuned at the same level; requiring VRESET independently supplied to each chip on ladder**



Transient response with IR drop in both directions

OUT_A<0> with ideal power supply, OUT_A<1> is the pixel with IR-drop in horizontal dire., OUT_A_512 is the pixel with IR-drop in both dire.



- **IR drop in the vertical direc. shows larger effect than the horizontal direc.**
- **Cd with diff substrate voltage (5fF@0V/ 2.5fF@-6V) was considered, in normal condition, Cd is not at the minimum level**
- **Even in the worst case, analog output shows normal functionality and similar shape, the deviation on OUTA baseline will introduce an FPN of ~3.3 mV on the pixel threshold**

FPN induced by IR-drop of power line

- **In the worst power case, the deviation on OUTA baseline will introduce an FPN_{power} of ~3.3 mV on the pixel threshold**

	Threshold Mean (mV)	Threshold rms (mV)	Temporal noise (mV)	Total equivalent noise (mV)
S1	248.3	46.3	27.3	53.75

- Total equivalent noise = $\sqrt{(\text{Threshold rms}^2 + \text{Threshold noise}^2 + FPN_{power}{}^2)}$

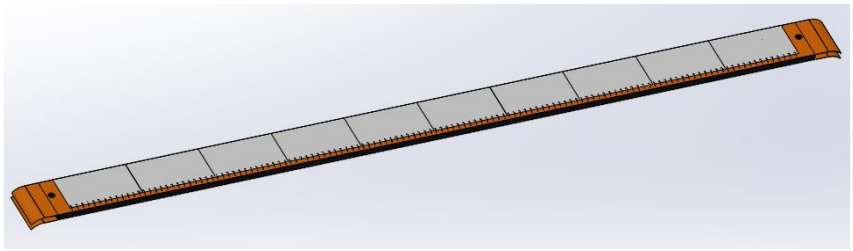
  = 53.85 mV

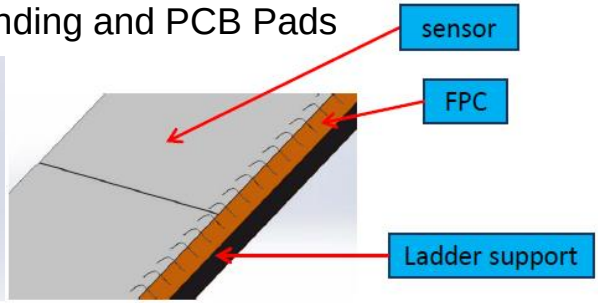
FPN due to the power supply IR-drop increases the total equivalent noise by 1.9%

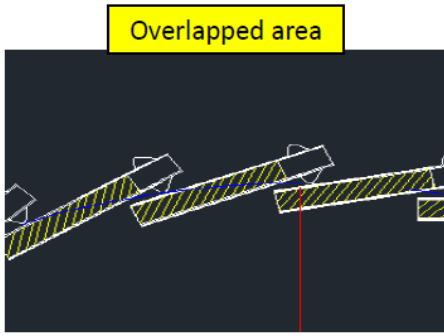
The effect of power IR-drop on the noise of pixel is acceptable.

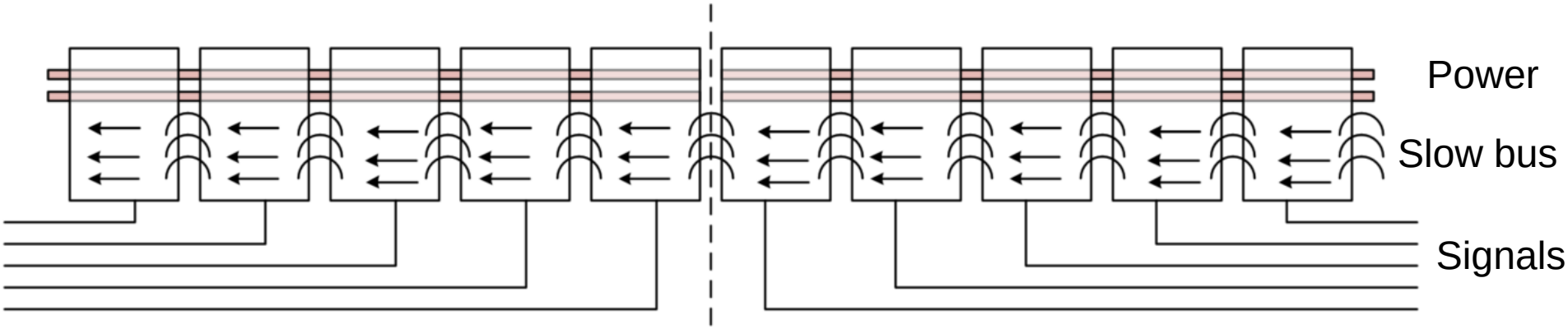
Flex cable design consideration

2mm margin for wire bonding and PCB Pads







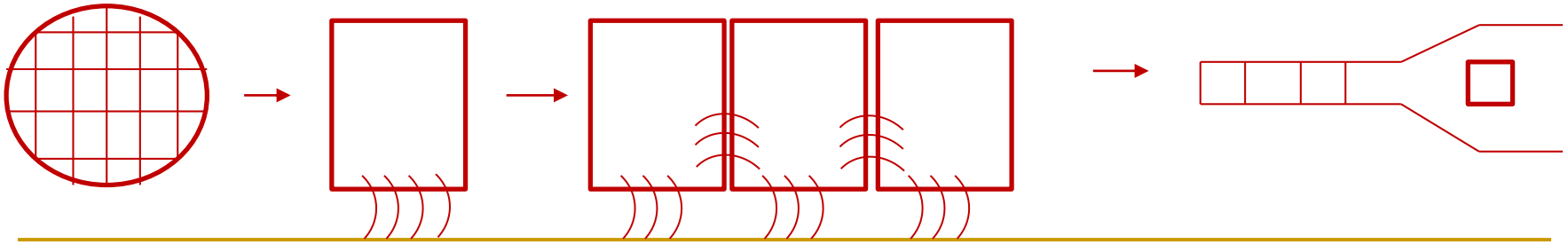


- **Design goals & considerations for the Flex PCB**
  - Minimum material budget
    - Minimum dead zone extension, limited height of PCB
      - Minimum set of signals on Flex
      - Slow buses to go on chip area by chip interconnection buses
    - Robust power supply
  - Manufacturability

Testability design & test plan consideration

- **All test features reserved, while the connected IOs will decrease at diff stages depending on chip test & study results**
  - Analog probe signals at the top part, accessible from the top pads
  - When mounted on ladder, only minimum self test possibilities can be reserved

1. **Probe Card design for the wafer test**
   - For all the pads at both sides
2. **Single chip test board design**
   - Designed with all the test features for the chip functional study
3. **Multiple chip test board for the ladder debugging**
   - Designed following the same manner as the ladder but on PCB
   - Signals and power supplies will be limited just with the ladder's dimension
   - Extra test signals can be connected to the extended area, to help debugging
4. **The real flex cable design for the ladder**
   - Core design and lessons will be exported from 3



Summary & recent plan

- **TaichuPix small prototypes were fully verified and preparing to submit the full size tapeout**
  - Full signal chain & functionality verified with both electrical & radioactive test
  - TID performance satisfied with CEPC's requirement with a large headroom
  - Design review finished
- **Recent plan**
  - Design will be submitted for the engineering run after budget approval
  - Full chip simulation and verification till the real submission
  - Wafer probe card design
    - June ~ August
  - Single chip study board design
    - June ~ August
  - Multiple chip study board design
    - June ~ August
  - Flex cable design
    - April ~ ?

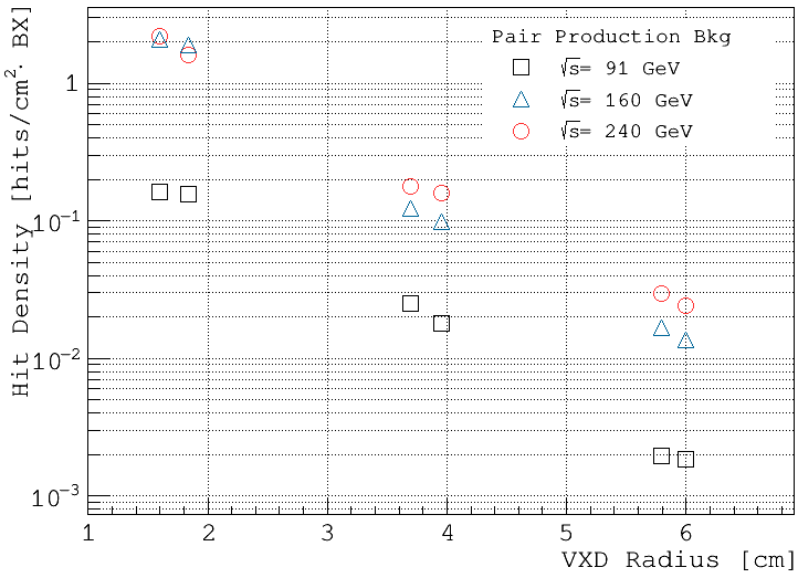
Thank you for your attention!

Backup

Main specs of the full size chip for high rate vertex detector

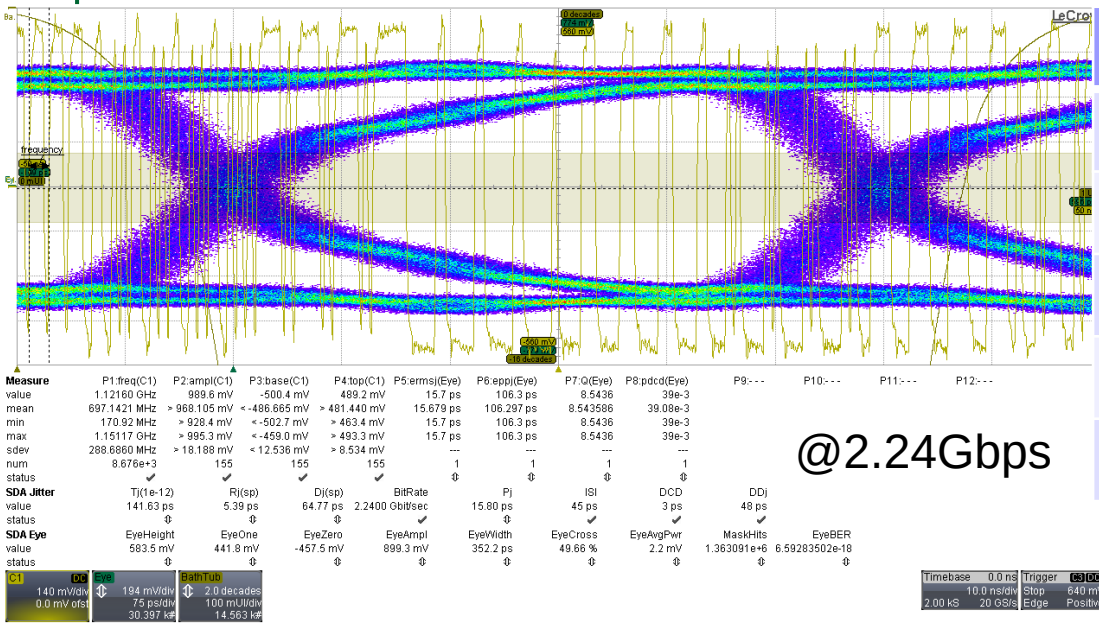
- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: 25 ns
  - Meaning 40M/s bunches (same as the ATLAS Vertex)
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: 3pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm

From the CDR of CEPC

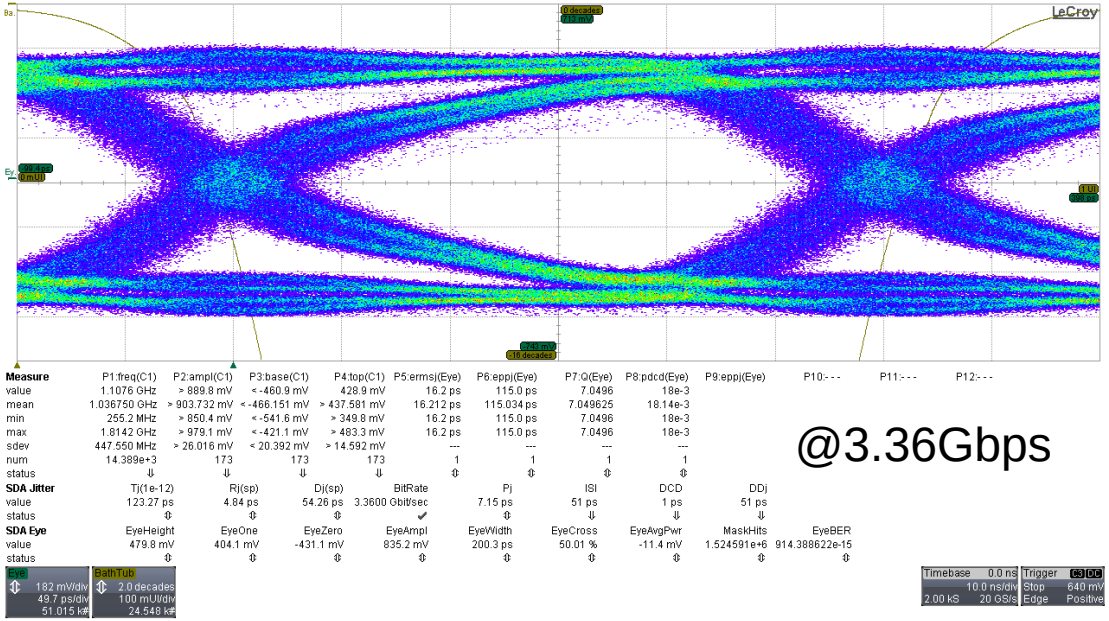


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Date rate	3.84 Gbps --triggerless ~110 Mbps --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	<500 ns --for 98% efficiency	Chip size	~1.4 cm×2.56 cm

Test of the data interface



@2.24Gbps



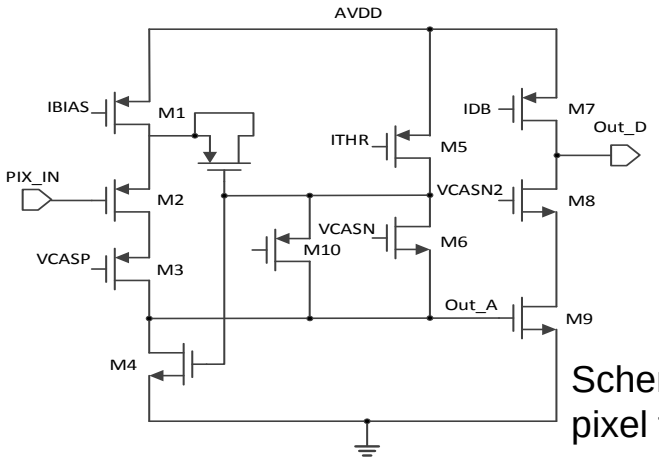
@3.36Gbps

Bit rate	2.24Gbps	3.36Gbps	4.48Gbps
Clk freq	1.12GHz	1.68GHz	2.24GHz
BER	6.59e-18	9.14e-13	3.23e-5
Tj@e-12	141.63ps	123.27ps	147.14ps
Rj	5.39ps	4.84ps	5.35ps
Dj	64.77ps	54.26ps	70.90ps

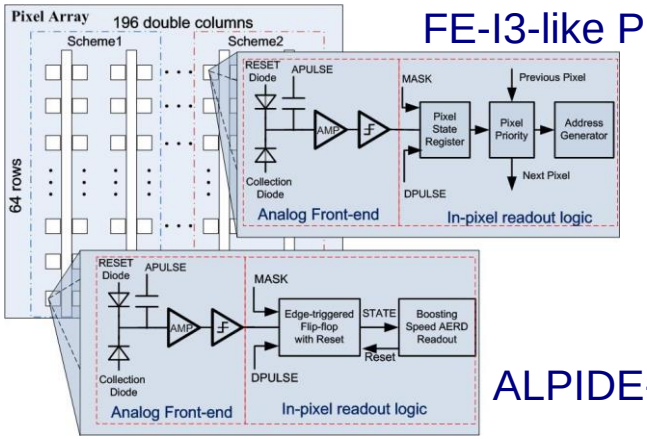
- **Data readout in DDR mode**
- **Data interface was tested by the on chip PRBS source, a high speed oscilloscope (@16Gsps), and code stream verified in FPGA**
- **BER qualified till 3.36 Gbps, failed at 4.48 Gbps**
- **Concerning the highest data rate for triggerless at 4Gbps, at least 2 SER interface ports needed**
- **Thus bit rate @2.24Gbps is safe and power optimized**

Design variations of pixel array in TaichuPix-2

Sector	Pixel front-end	Pixel digital	Pixel size
S1	Same as S1 of TC1, reference design	FEI3-like	25 μm × 25 μm
S2	M6 with guard-ring, PMOS in independent nwell	FEI3-like	25 μm × 25 μm
S3	M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 μm × 24 μm
S4	Increasing M3, M4, M9. M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 μm × 25 μm
S5	Same FE as S2, with smaller sensor	ALPIDE-like	25 μm × 25 μm
S6	Same FE as S1	ALPIDE-like	25 μm × 25 μm



Schematic of in-pixel front-end

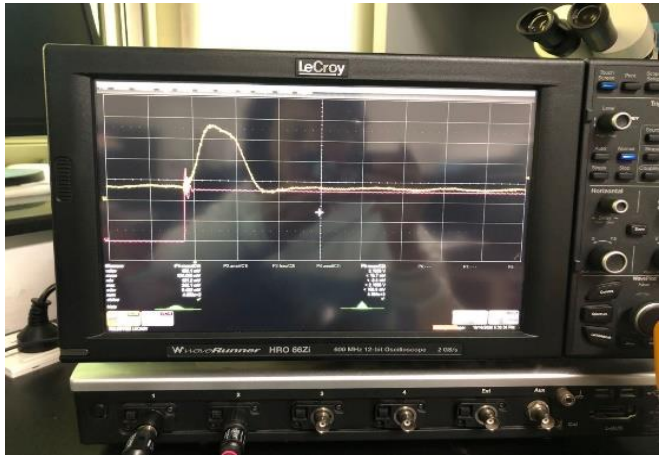


FE-I3-like Pixel

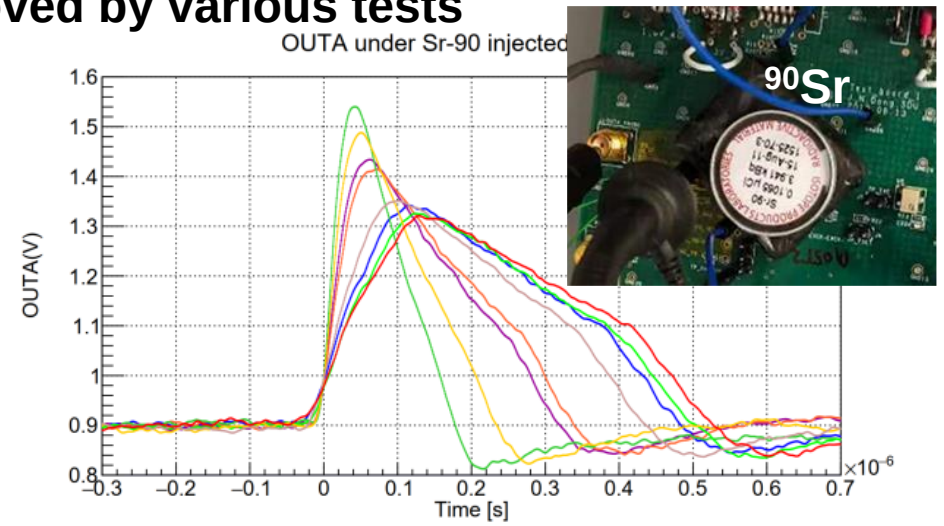
ALPIDE-like Pixel

Overview of previous test results

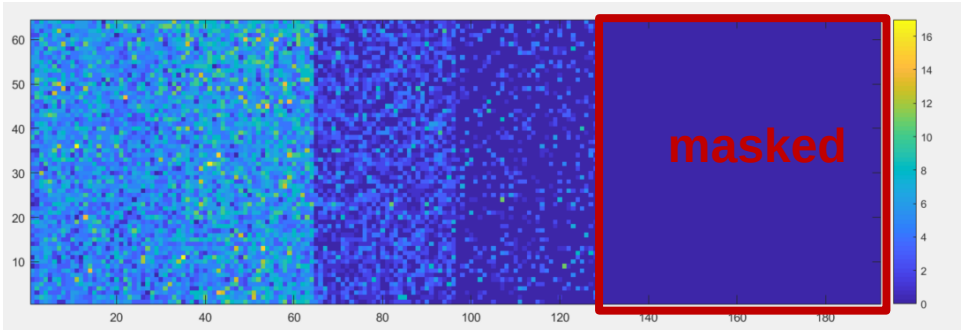
- **Functionality of TaichuPix1&2 proved by various tests**



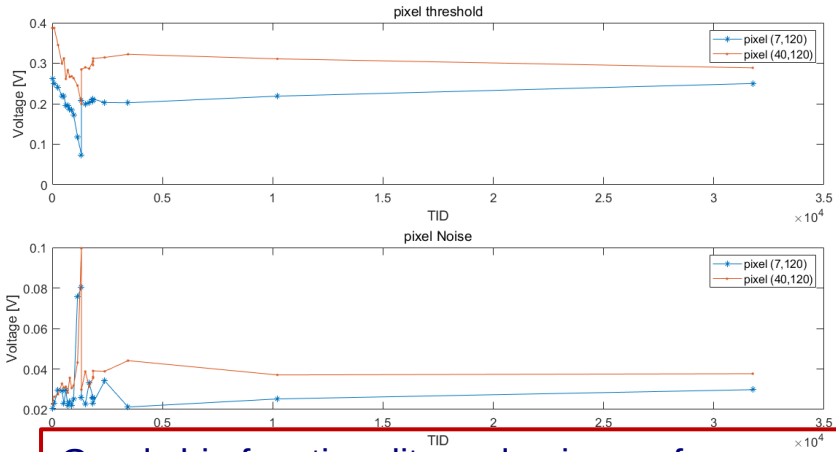
Analog output of a pixel with a **voltage input**



Analog output with ^{90}**Sr** exposure



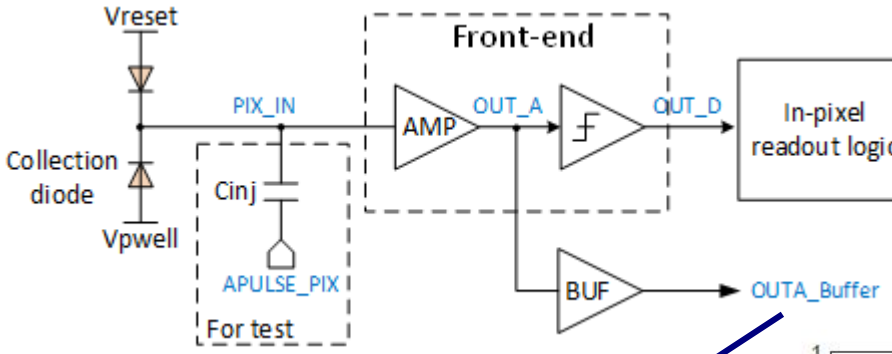
X-ray imaging with 5 min exposure @ 8 kV X-ray tube



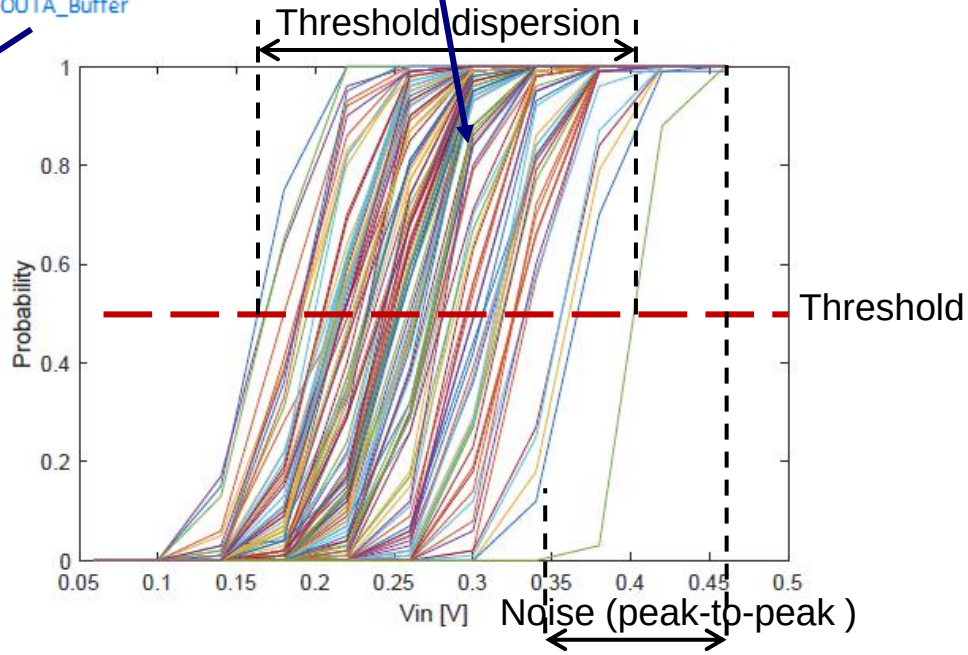
Good chip functionality and noise performance proved up to **30 Mrad TID**

Electrical test

- **Electrical performance verified by injecting external voltage pulses into pixel front-end**



Analog output of a pixel @ Vin = 0.9 V



Measured “S-curve” for 128 pixels