Progress of the CMOS pixel sensor JadePix-3

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On behalf of the **JadePix-3 study group**

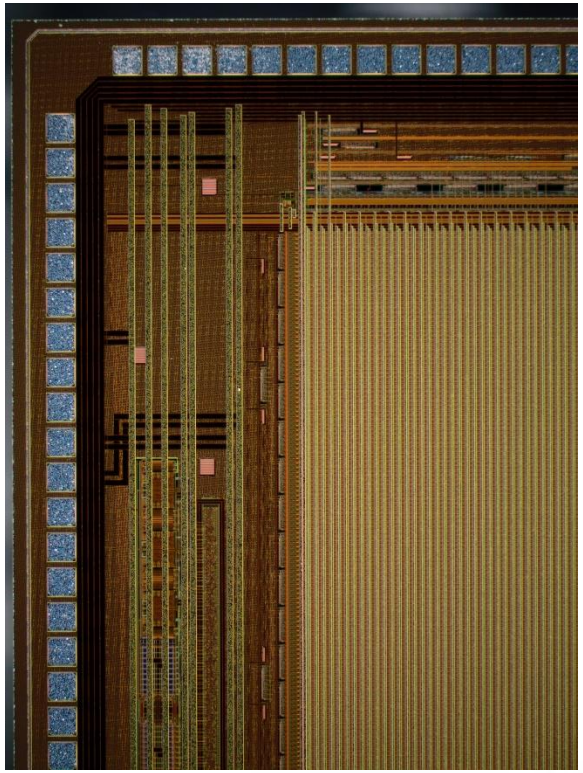
CEPC Day

June 24, 2021

Outline

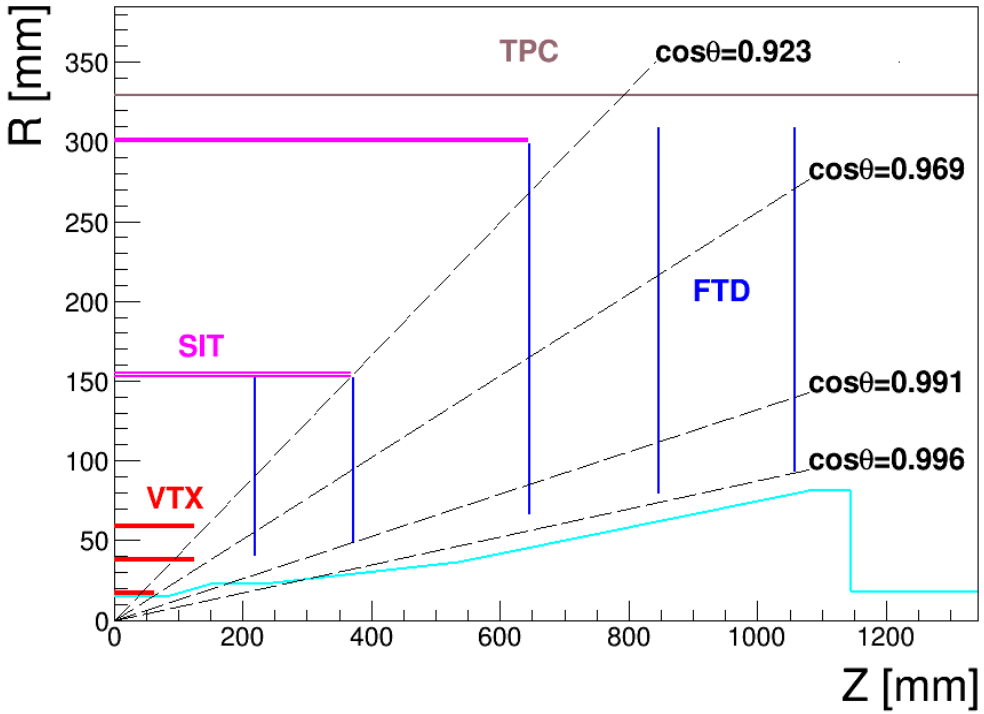
- Motivation
  - Requirements of baseline scheme in the CDR
- Revisit the JadePix-3 design
- Progress of test and measurement
  - Basic characterization
  - Highlights of performance
- Summary and outlook

Microscopic view of JadePix-3
(Top-left corner)



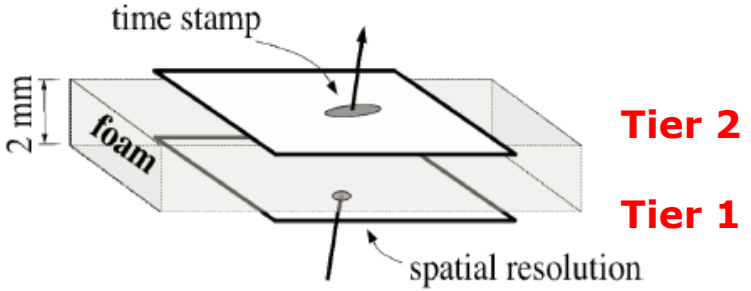
Baseline scheme in the CDR

Silicon tracking system



- SIT: Silicon Internal Tracker
- FTD: Forward Tracking Detector
- SET: Silicon External Tracker
- ETD: End-cap Tracking Detector

- VTX:
  - 3 (mechanical) double-sided layers
  - σ_{SP} = **2.8 μm** in Tier 1
  - Total number of pixels: 690M



Concept of a double-sided **layer**

Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Tier 1	16	62.5	2.8	0.15%/X_0
Tier 2	18	62.5	6	0.15%/X_0
Tier 3	37	125.0	4	0.15%/X_0
Tier 4	39	125.0	4	0.15%/X_0
Tier 5	58	125.0	4	0.15%/X_0
Tier 6	60	125.0	4	0.15%/X_0

A complementary design to meet the specs

- Tier 1: high resolution, low power and modest readout speed
  - JadePix-3 targeting on: **3 μm**, 50~100 mW/cm^2, 100 μs
- Tier 2: Fast readout speed, low power and relaxed constraint of resolution
  - 4~6 μm, 50 mW/cm^2, **1 μs** is foreseen
- Radiation tolerance is a common requirement to Tier 1 and 2

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs

$\sigma_{s.p.}$ ~ 2.8um

Material budget ~ 0.15% X_0/layer

r of Inner most layer ~ 16mm

Pixel sensor specs

Tier 1

Small pixel ~ 16um

Thinning to ~ 50um

low power ~ 50mW/cm^2

fast readout ~ 1us

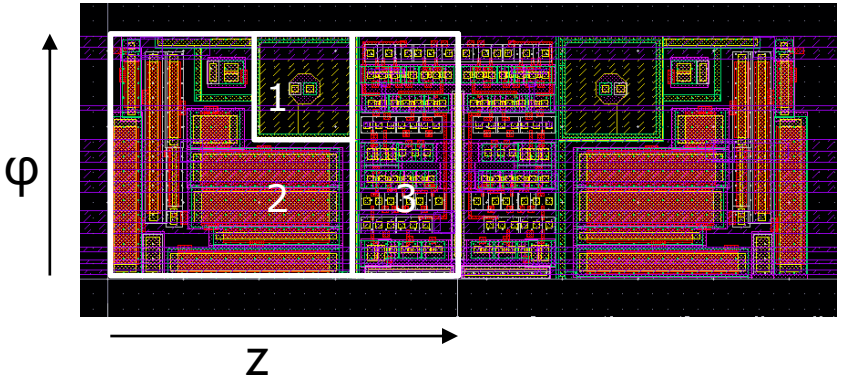
Tier 2

radiation tolerance ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\ year)$

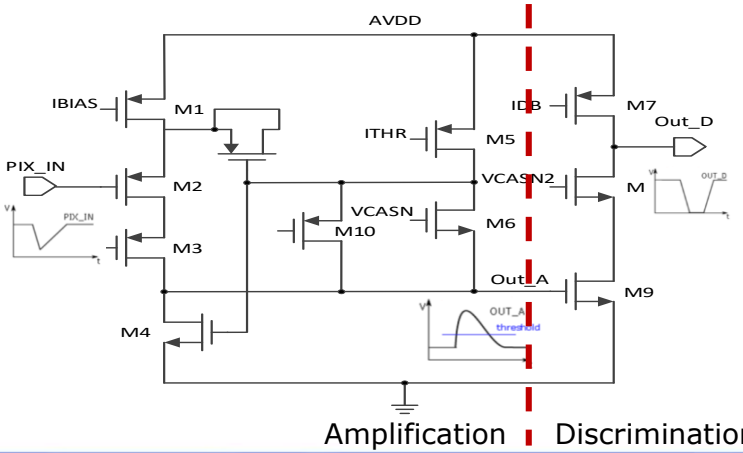
Small pixel implemented in the JadePix-3



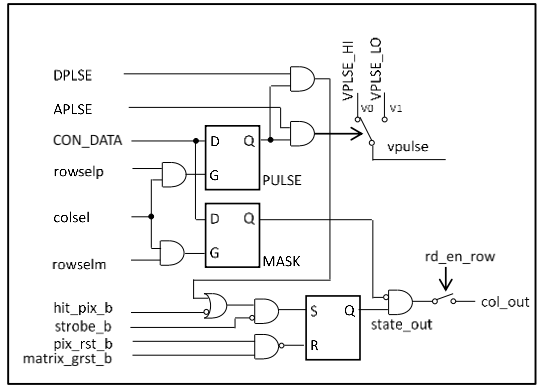
Pixel footprint:
1: Sensing diode
2: Analog frontend
3: digital frontend

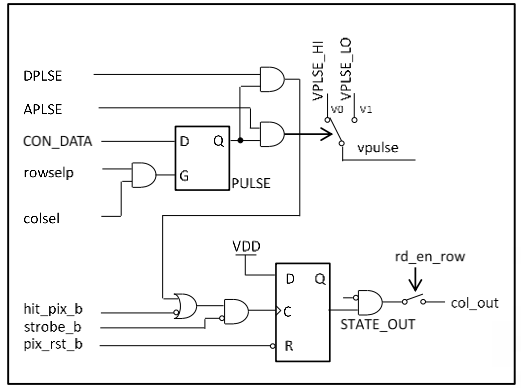
- Fix φ direction to **16 µm** and allow z to vary
  - Sensing diode of minimized geometry verified on JadePix1
  - Analog part with **tradeoff** between layout area and FPN
  - 3 variants of digital part (D-FlipFlop vs RS-latch)
- Mirrored layout to share bias lines between two columns

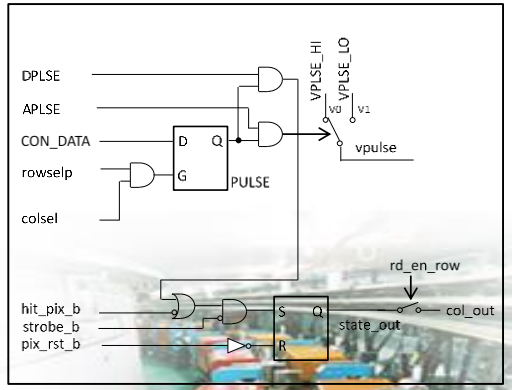
Frontend / analog part



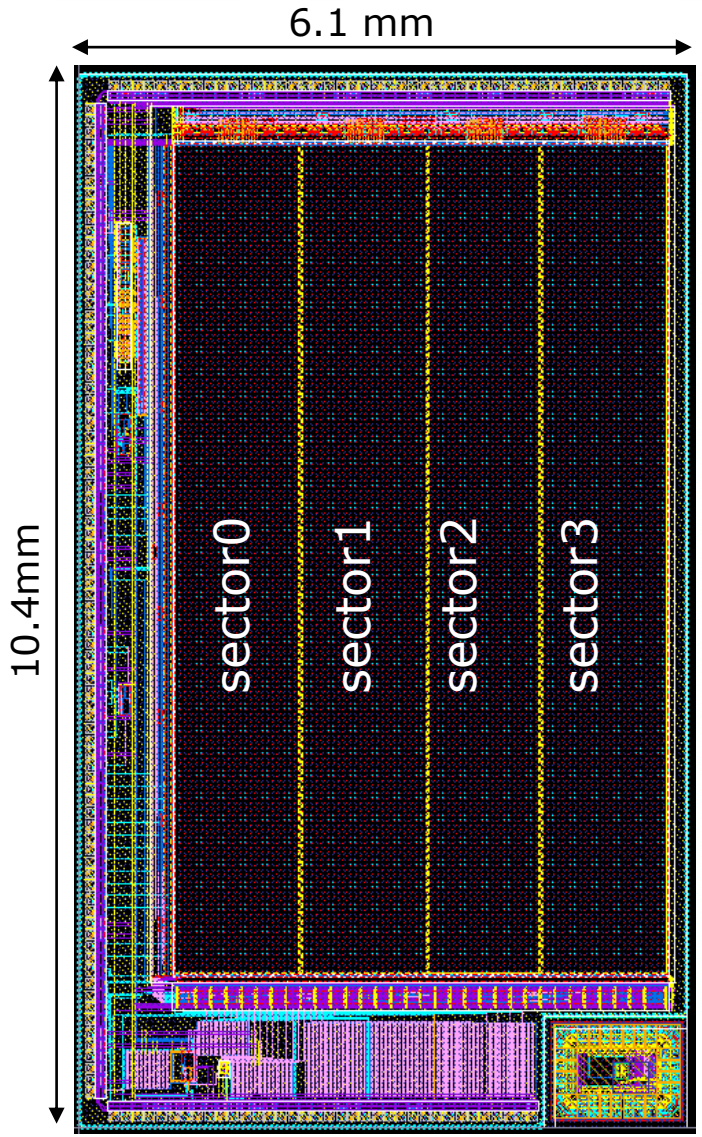
3 variants of digital part







Implementation of the pixel array

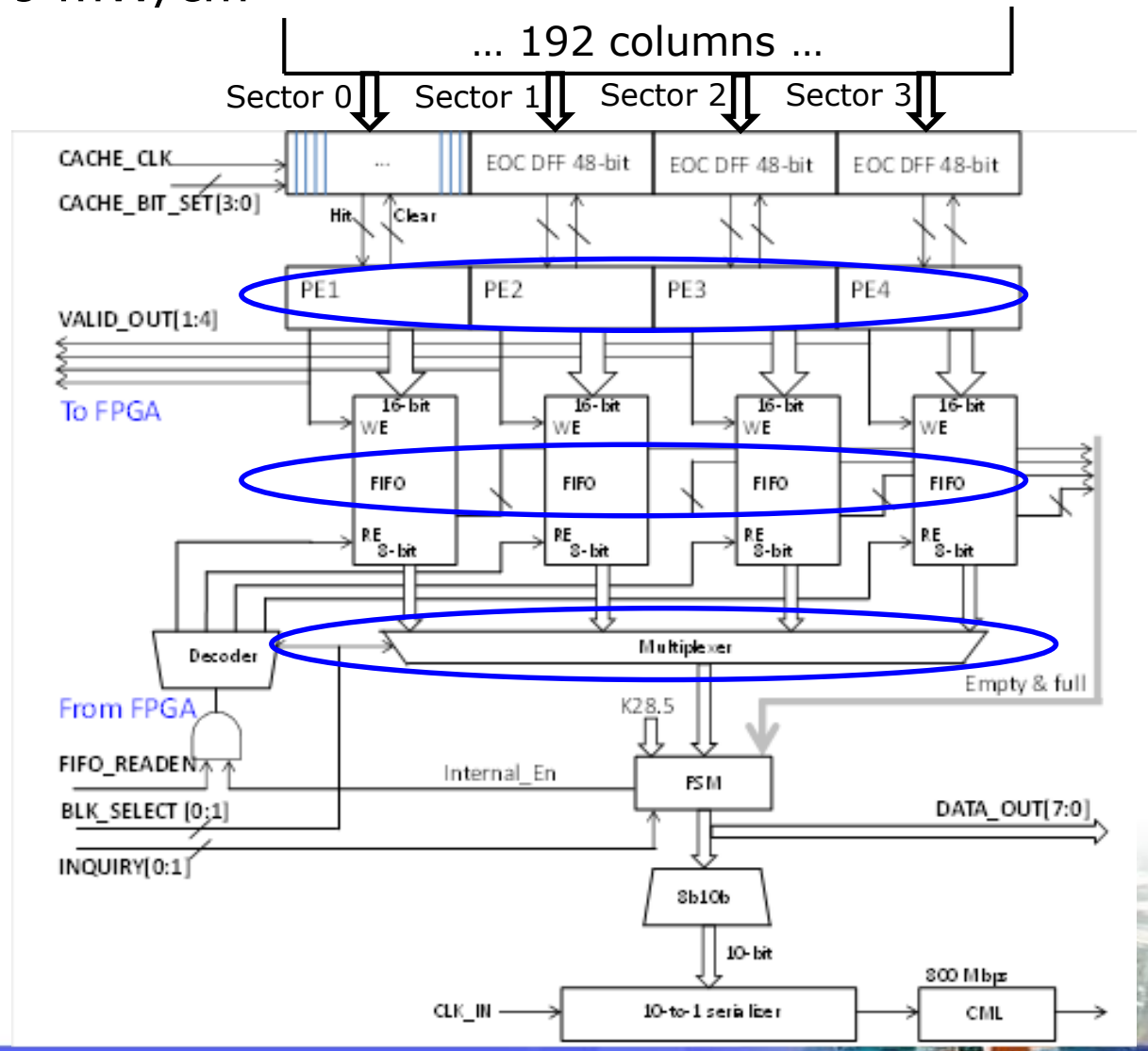


- **Full-sized** in the φ direction
  - Matrix coverage: 16 μm × 512 rows = 8.2 mm
- **Rolling shutter** to avoid heavy logic and routing in the column-wise
  - Minimum pixel size: **16 μm × 23.11 μm**
  - Matrix readout time: 512 rows × 192ns/row = **98.3 μs/frame**
- 4 parallel sectors, **scalable**
  - 48 columns/sectors × 4 = 192 columns

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

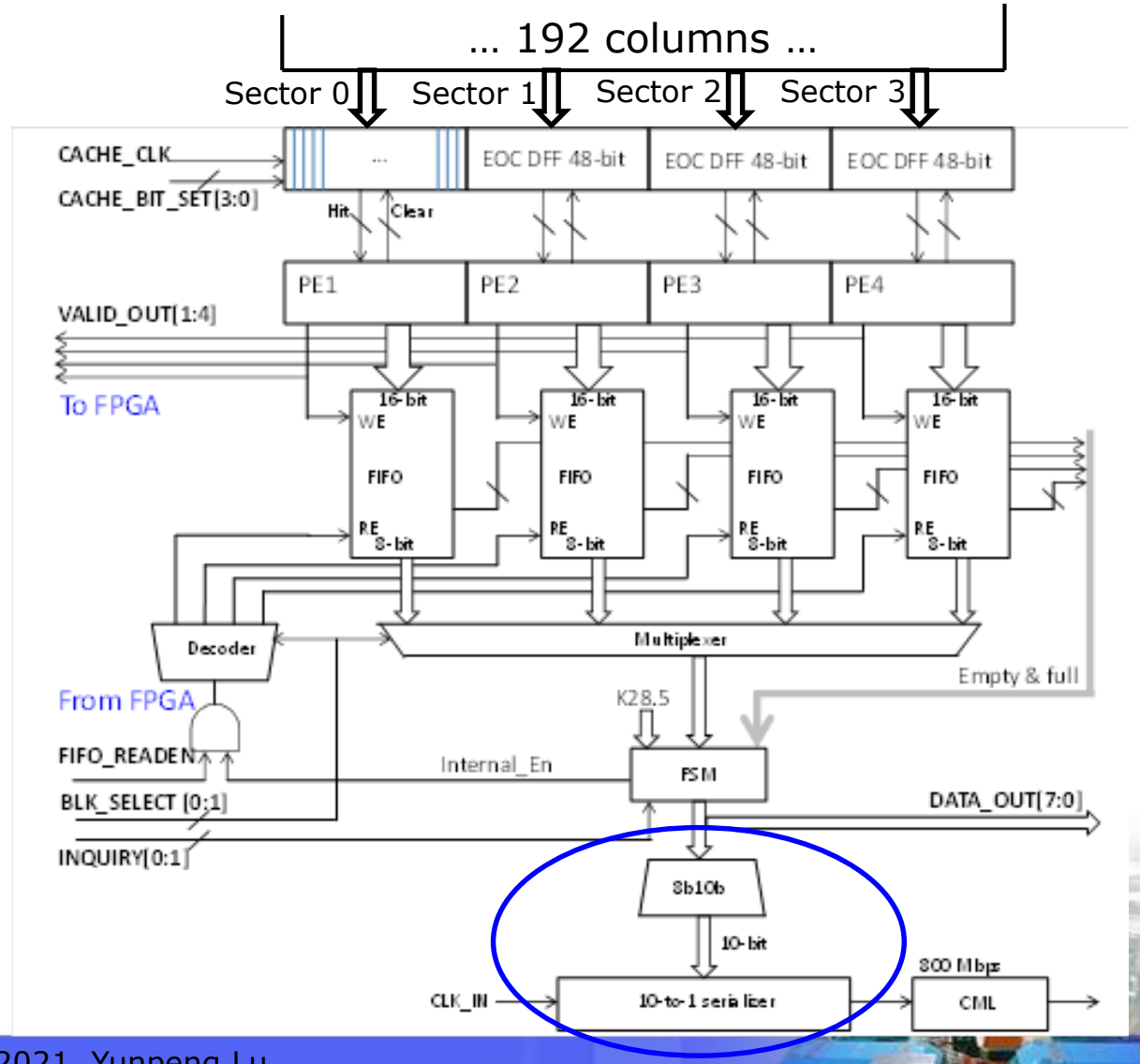
Lower power design

- A low power frontend of **20 nA**, equivalent to 9 mW/cm^2
  - Except for the sector 3, where 60 nA used for the comparison of radiation tolerance
- Zero suppression at the end of column
  - HIT address extracted by Priority Encoder **(PE)**
  - Compress the bit flow dramatically
- Flexible readout strategy allowed
  - 4 parallel **FIFO**s * 48 depth
  - **Multiplexer** steered by FPGA
- Scalable along with the pixel sectors



Engineering consideration

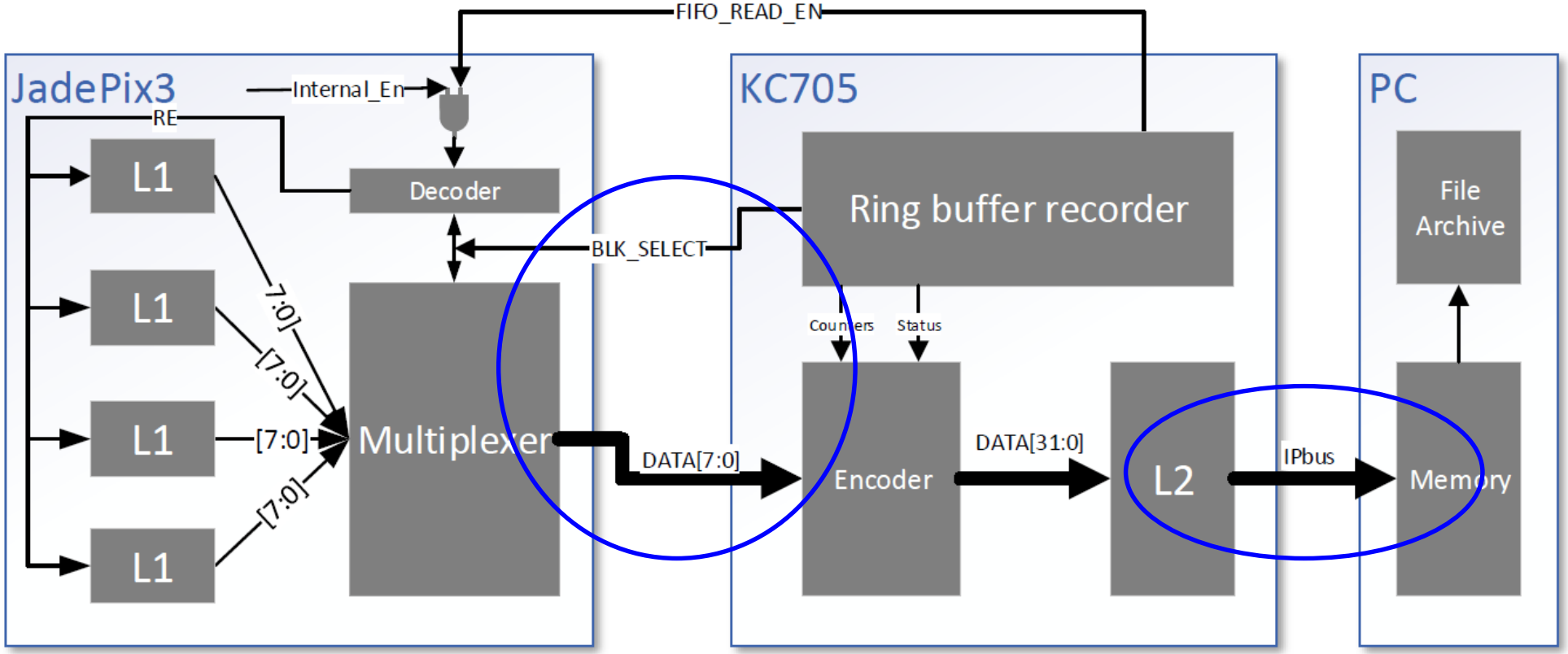
- High speed data transmission modules
  - 8b10b **Encoder**
  - 10-to-1 **Serializer**
  - **PLL**-based clock module
- **DACs** for the analog biasing
  - 10-bit voltage DAC × 6 channels
  - 8-bit current DAC × 6 channels
- Adjustable **Bandgap** module
- Serial Program Interface (**SPI**)
- Low power differential transceiver
  - **RSDS** (Reduced Swing Differential Signal)



Test system

Sheng DONG, Hulin WANG, Yunpeng LU

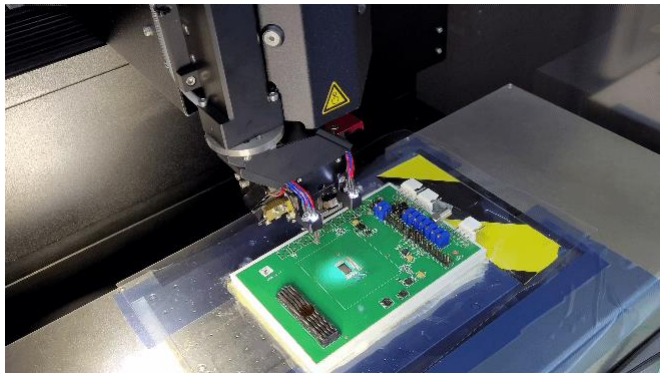
- General-purpose FPGA platform, KC705
  - Well-defined **FPGA firmware**
  - Debugged **Interactively** with the JadePix3 chips
- Two test setup deployed in IHEP and CCNU
- IPBUS protocol
  - Reliable high-performance **control link** for particle physics electronics
  - **JUMBO PACKAGE feature** developed and integrated to the latest release



Chip-board assembly

Daming SUN, Yunpeng LU

- 7 chips assembled with the test board
  - **All passed functional tests**
  - ESD counter-measures proved effective
- Good **uniformity** observed
  - Power supply current
  - Bandgap output
  - Analog waveform of frontend
  - Threshold and noise



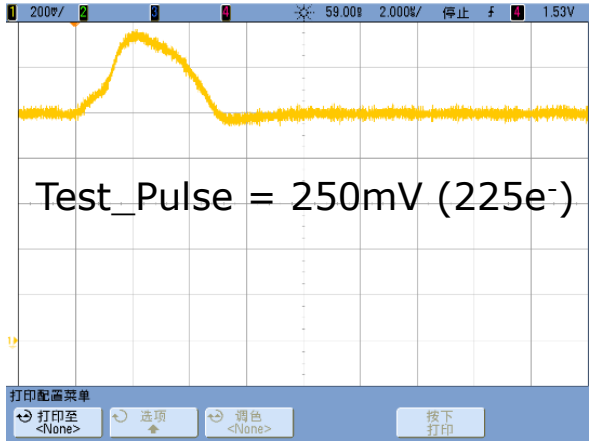
Wire bonding on the JadePix-3 chip

Functional verification

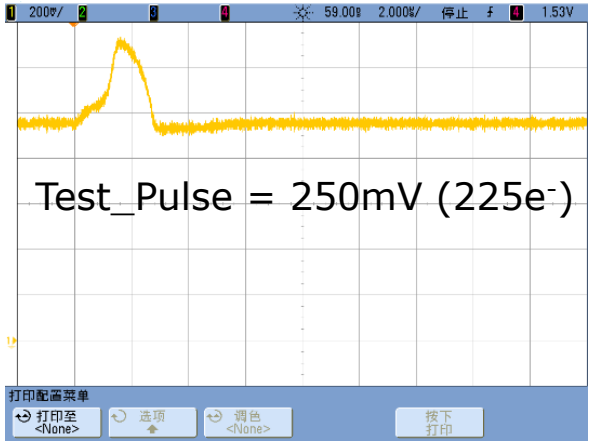
Sheng DONG, Yang ZHOU, Ying ZHANG, Zhan SHI, Yunpeng LU

- **All module** functions verified
  - Configuration of matrix registers
  - Configuration of DAC
  - Pulse test
  - Analog output waveform
  - Data readout
  - PLL clock
  - Serializer output pattern
- Response to the radiation verified
  - Radiative source ^{55}Fe
  - Cosmic ray
  - **Pulsed laser beam**

Frontend output @ Sector 1



Frontend output @ Sector 3

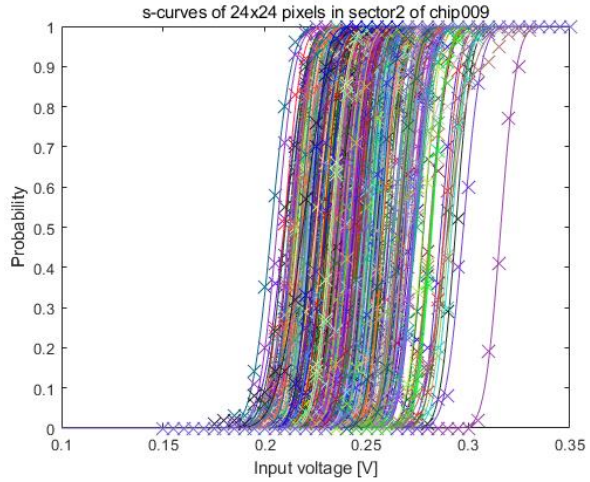


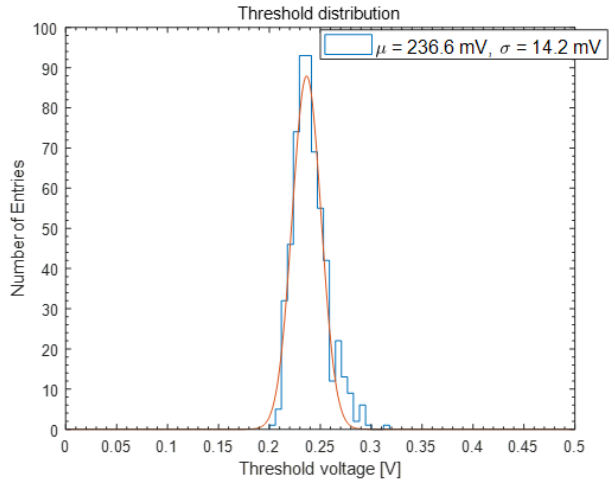
Output pattern of serializer @ 1Gbps

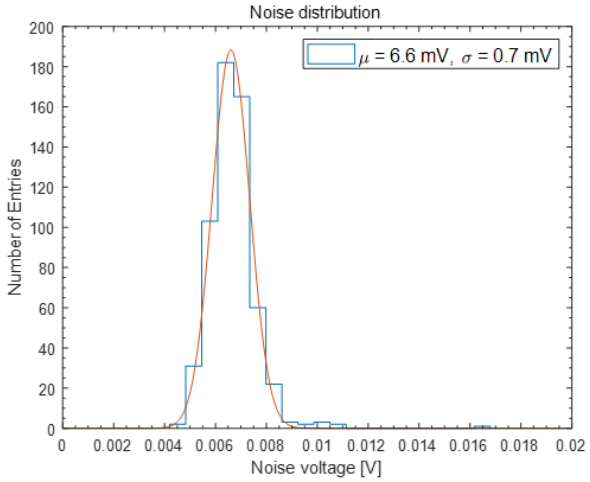
Threshold and Noise

Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

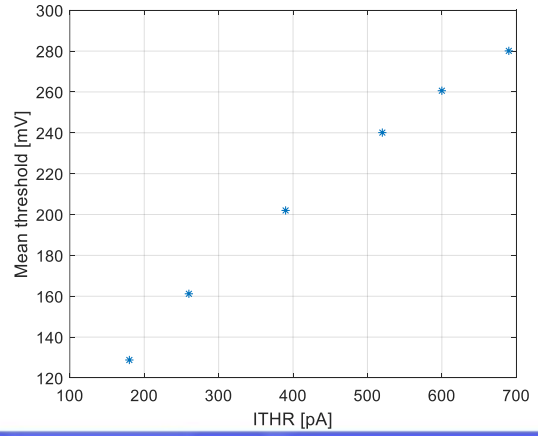
- Pulse amplitude scan and **S-curve** fit (1 mV ~ 0.9 e$^-$)

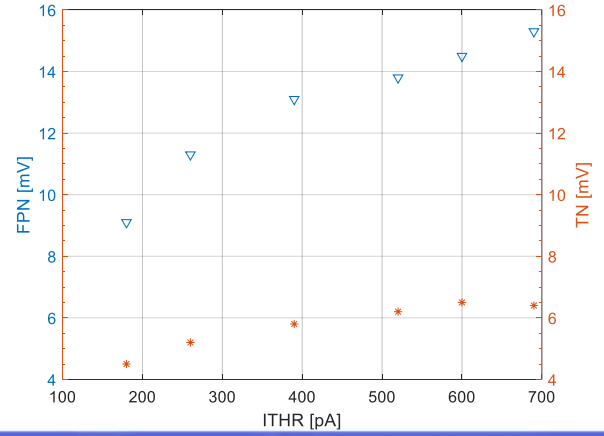


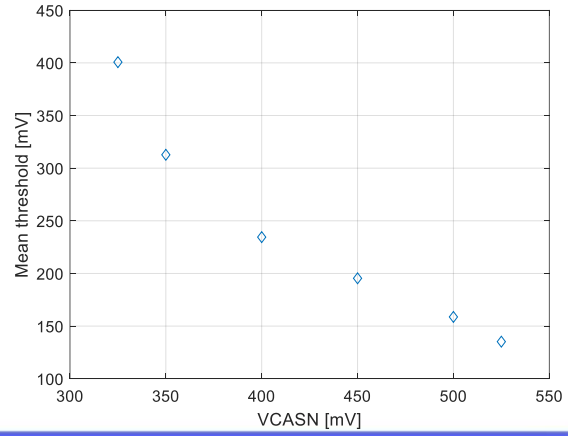


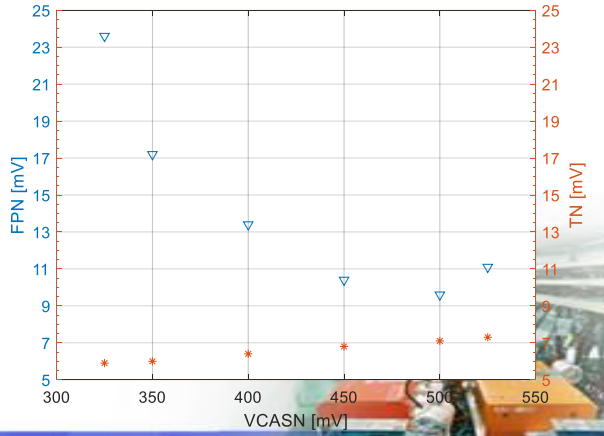


- Parameter scan @ sector 2
  - Threshold = 220e$^-$ @ nominal I_{THR} = 0.5 nA, V_{CASN}= 400 mV





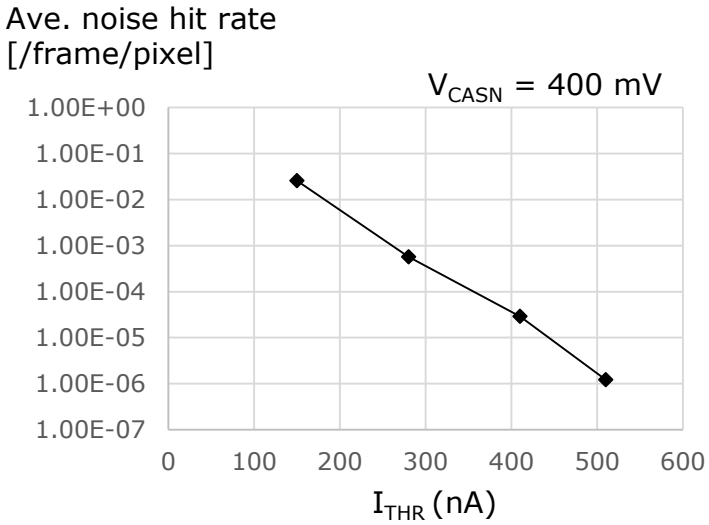


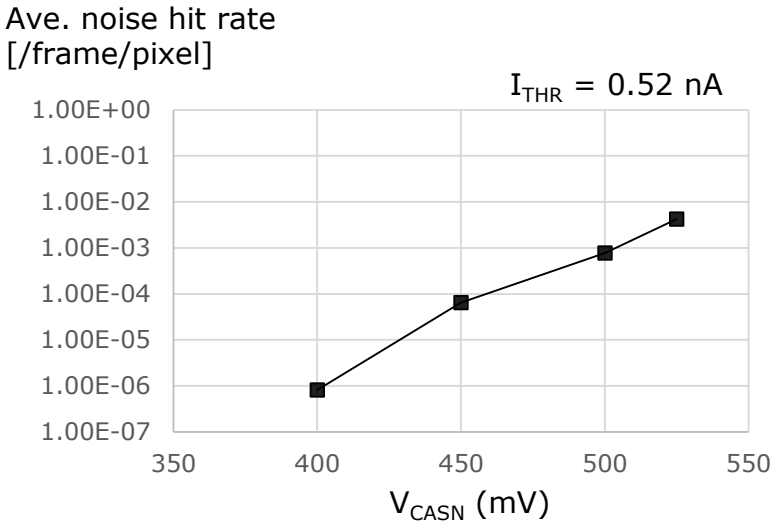


Noise hit rate

Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

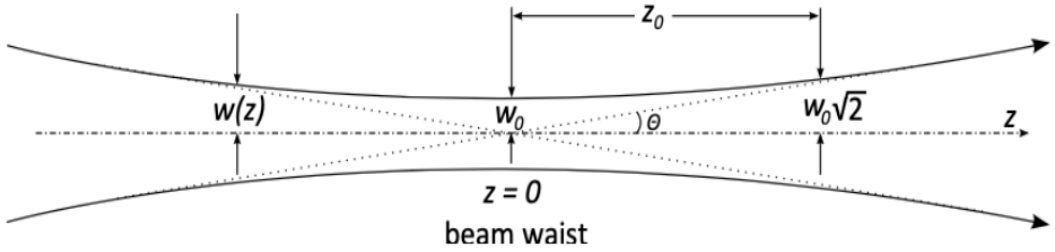
- Average noise hit rate @ Sector 2
  - Noise hit rate ~10^{-6} /frame/pixel

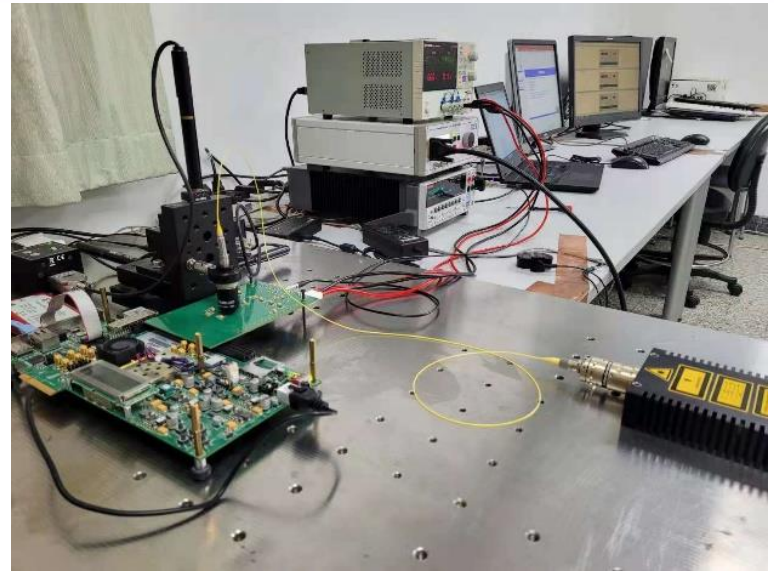




Pulsed laser test

Hulin WANG, Shen DONG, Yunpeng LU



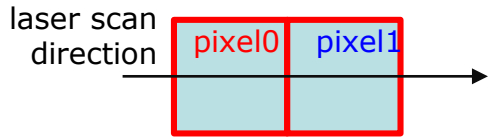


- Laser beam characterization
  - Wavelength: 1064 nm
  - Beam waist ω_0 ~ **1.7 μm**
  - Rayleigh range z_0 ~ 8.5 μm
  - Divergence Angle **θ = ~ 11°**
  - Laser pulse duration ~100 ps
- Laser power tune
  - 0% : maximum power; 100% : minimum power
  - For final results, use 92.7%, 92.9%, 93.3%, 93.5%, 93.7%
  - 92.7% ~ 880e^-
  - 93.7% ~ 440e^-
- **Calibrated** with the threshold setting to 220 e-

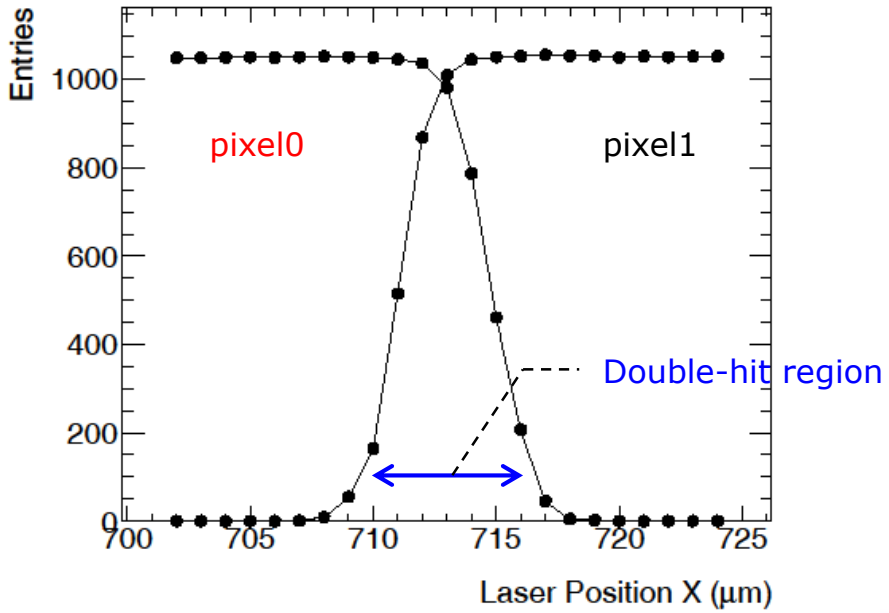
Measurement of position residual

Hulin WANG, Shen DONG, Yunpeng LU

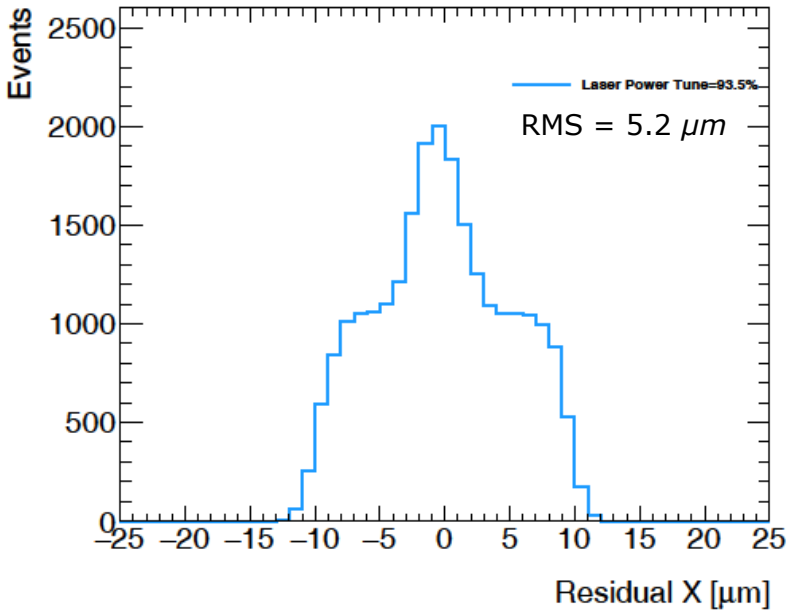
- 1-D scan of laser position
  - Step = 1 *μm* and repeat 1000 at each step
  - Laser power tune = 93.5% (~520 e^-)
- Distribution of position residual
  - Reference position: motion stage
  - Measured position: weight center of hit pixels
- RMS taken as the 1-D spatial resolution



1-D scan of laser position



Residual distribution



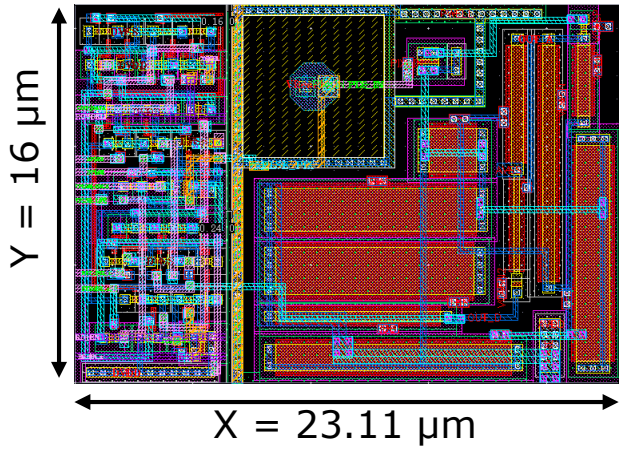
Impact of the Signal / threshold ratio

Hulin WANG, Shen DONG, Yunpeng LU

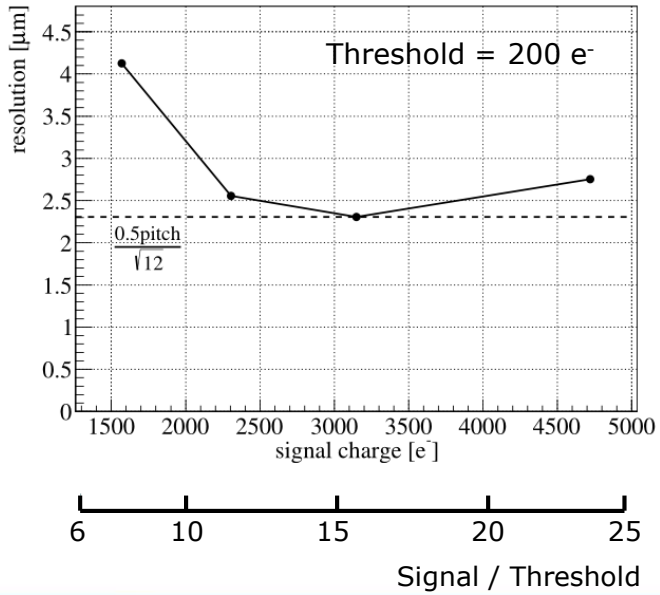
- Double-hit region varied with the sig. / thr. ratio
  - Threshold set to 220 e-
  - Laser power carefully tuned from 92.7% to 93.7%
- 1-D spatial resolution on X and Y
  - **Minimum 3.4 µm and 2.7 µm** respectively
- Compared to the CPV-2 (SOI) results
  - 0.5 pitch / √12 achievable on both
  - More charge sharing

  (diffusion vs drift)

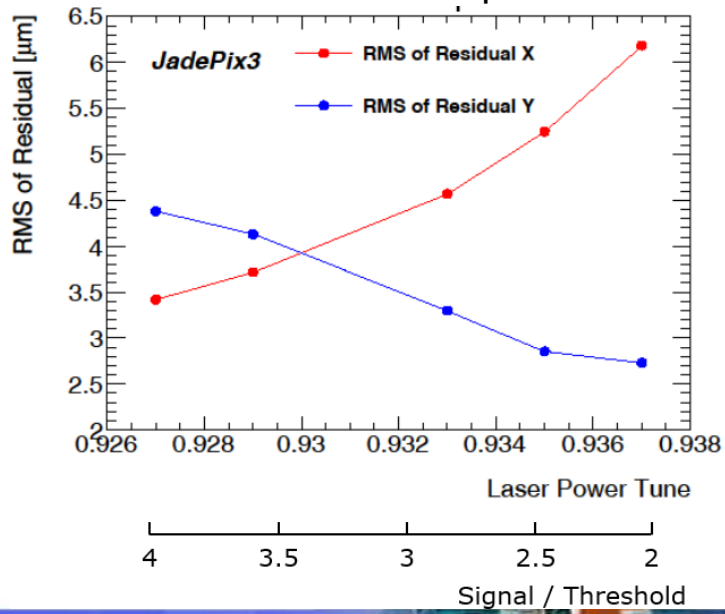
Layout of pixel undertest



RMS of residual on CPV-2

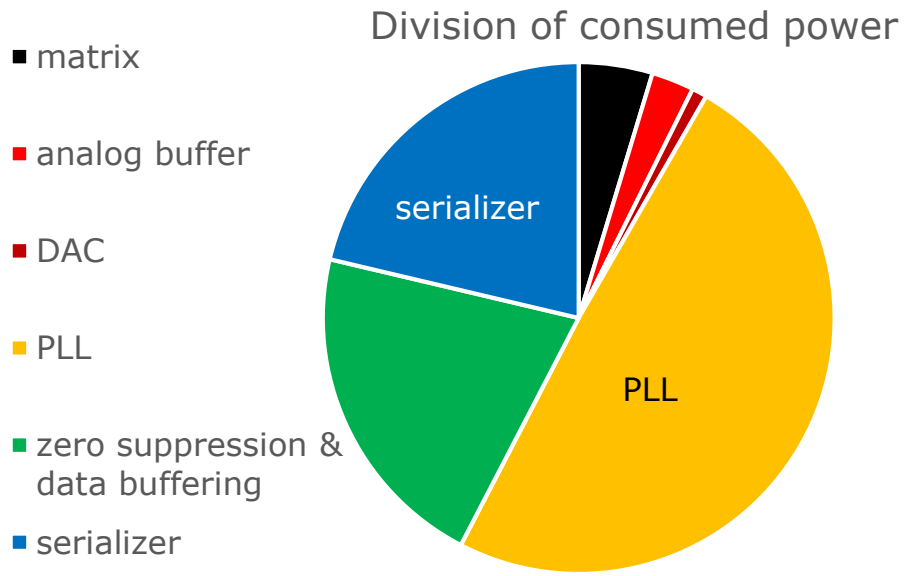


RMS of residual vs Laser power tune



Power consumption

- Average power consumption **46.9 mW/cm²**
  - PLL and Serializer not included (single chip readout)
- Extrapolated to a full size chip of 1 cm × 2.56 cm
  - Average power **91.44 mW/cm²**
  - PLL and Serializer included (multiple chip readout)
- Need to optimize further on
  - Zero suppression (51%)
  - PLL and Serializer (26%)
  - Test function (9%)



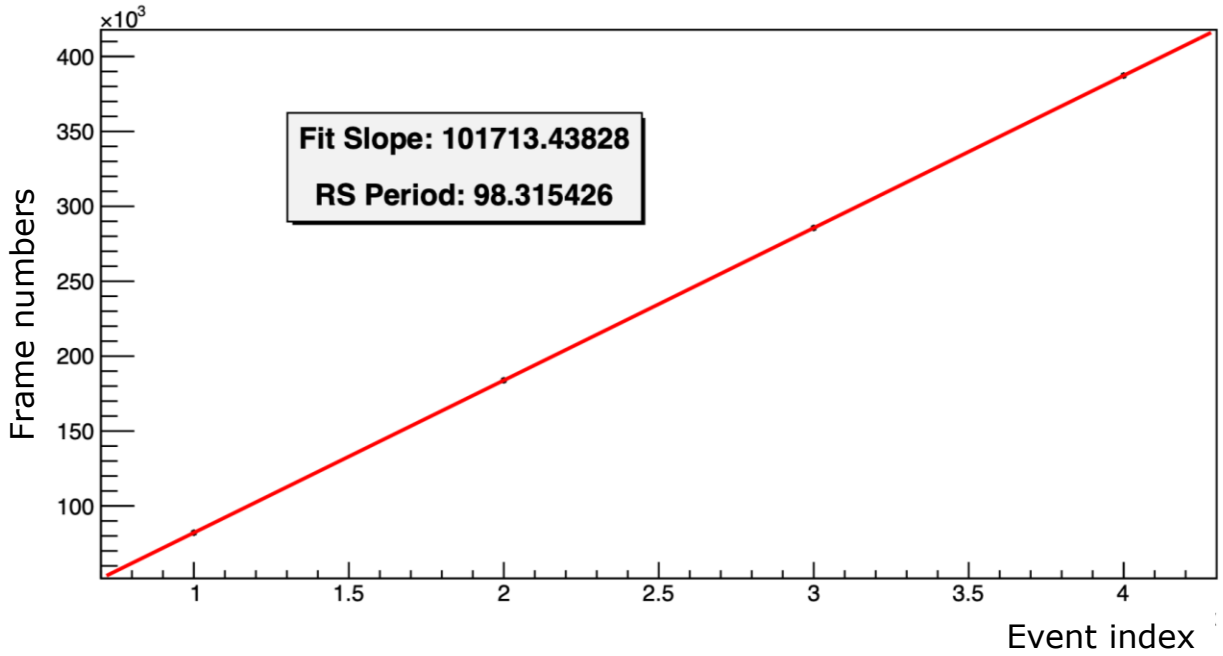
Extrapolation of average power consumption

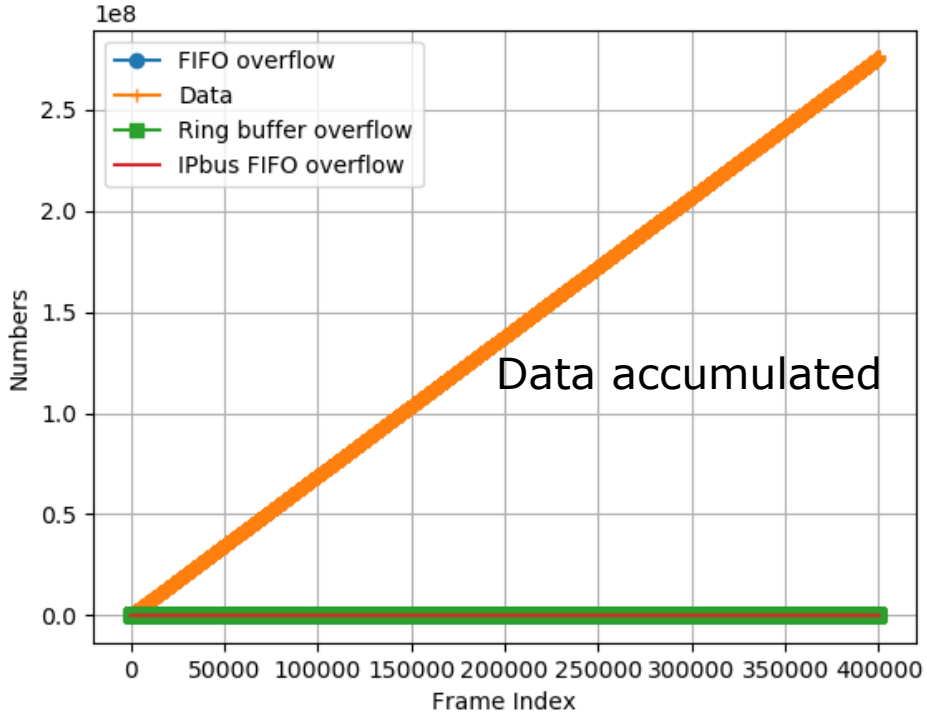
	512 × 192 (JadePix-3)	512 × 1024 (Full-sized chip)
Matrix	3.15 mA	16.79 mA
Zero suppression and data buffering	12.47 mA	66.47 mA
Other modules	46.82 mA	46.82 mA
Sum	62.44 mA	130.08 mA

Rolling Shutter Readout

Sheng DONG, Hulin WANG, Yunpeng LU

- Frame period (**Integration time**)
  - Count the frame numbers in an interval
  - 10 s was set by two external events
  - Measured **98.315 μs / frame**
- Stability test
  - Hit number per event: 2048
  - Event interval: 110 μs
  - Data throughout: **595.8 Mbps * 39.3 s**





Summary

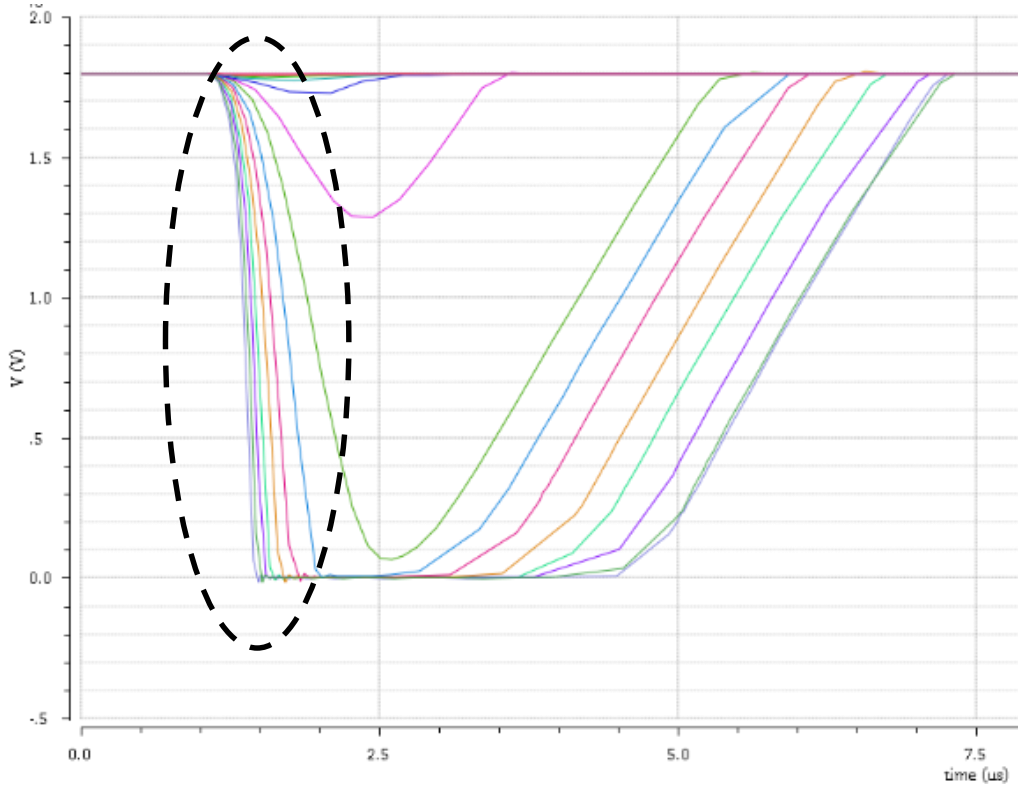
- JadePix3 is designed for the baseline scheme of **double-sided** structure
  - Optimized for high resolution, low power and modest readout speed
- Portable and reliable **test systems** developed and deployed in IHEP and CCNU
- Performance **consistent with the design** targets
  - Low threshold and noise
  - Single point resolution < 3 μm in the φ direction
  - Low power < 100 mW/cm^2
  - Integration time < 100 μs
- More test to do
  - Cosmic Muon and ^{90}Sr (Beta source)
  - Beam test and irradiation damage test

Outlook: Integration time 100 µs → 1 µs

- Hit registered at the **fast leading edge**
  - Customized D-Flipflop verified in JadePix3 (Sector 1)
  - Time walk ~ 1 µs
- Priority encoder **embedded into the column pairs**
  - Pixel size ~ 20 µm * 30 µm

  (still comply with the spec. for the tier 2)
- Time stamp at the end of columns
  - Readout time ~ 50 ns / hit
- Design expected in the 2nd half of 2021
  - JadePix-3 design team
  - Reuse of verified modules

Pulse shapes of different signal charge



JadePix3 study group

- IHEP: Ying Zhang, Yang Zhou, Zhigang Wu (graduated), Jing, Dong, Wenhao Dong / USTC, Yunpeng Lu, Qun Ouyang
- CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng (graduated), Anyang Xu (graduated), Sheng Dong, Hulin Wang, Xiangming Sun
- SDU: Liang Zhang
- Dalian Minzu Unv: Zhan Shi

Thank you for your time!