

Current Status and Future Plans for the MicroTCA.4 compliant LO and CLK Generation Module

The 2nd MTCA/ATCA Workshop for Research and Industry

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Agenda

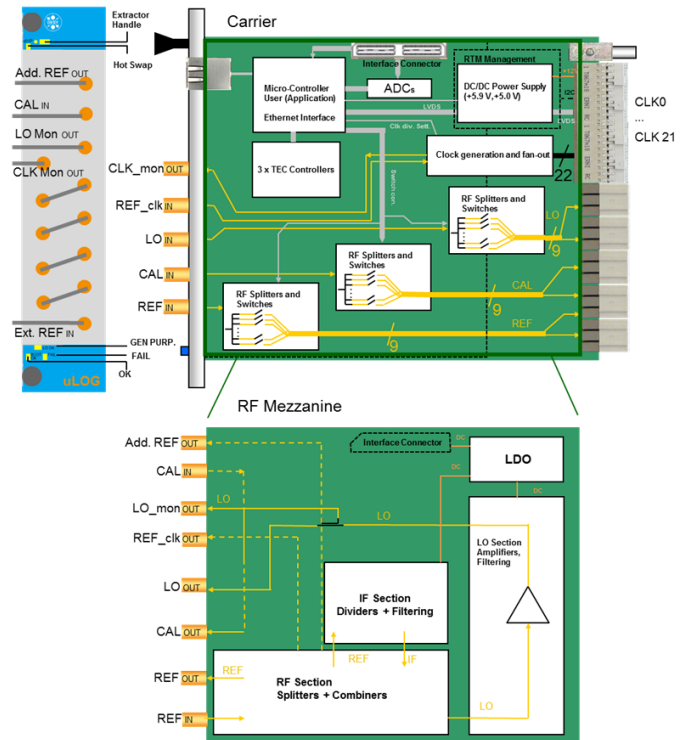
Part 1: Introduction of DeRTM-LOG

- DeRTM-LOG1300 – Technical Overview
- DeRTM-LOG1300 RF Performance
- DeRTM-LOG Test-Stand
- System Integration
- Future Developments
- Principles under Investigation
- Collaboration with KVG Quartz Crystal Technology GmbH

Part 2: Introduction of KVG Quartz Crystal Technology GmbH

DeRTM-LOG1300 – Technical Overview

- Generation and splitting of:
 - 9 LO signals (can be turned on/off individually)
 - 22 Diff. CLK signals (can be turned on/off individually)
- Splitting of 9 reference signals and 9 pilot signals.
- MicroTCA.4 compatible , includes MMC1.0 and is compatible with the uRF-Backplane.
- Located in slot 15 and slot 14 in the rear.
- Application control over PCIe from CPU located in front.
- Includes on-board active temperature control over Peltier elements.
- Monitoring of: RF power, DC voltages, temperature, humidity, current.



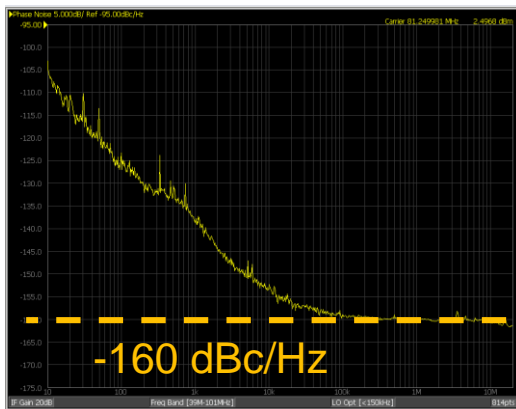
DeRTM-LOG1300 RF Performance

Challenging design points:

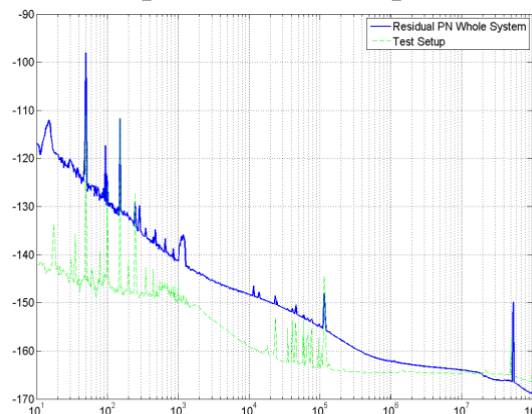
- Limited DC power (30 W)
- Limited cooling capability
- Limited space
- Demanding environment from EMI point
- High density of output channels (~50 RF grade signals)

RF Parameter	Measured Value (Worst Case)
Return Loss	>20 dB
LO Out Power	>29 dBm
Isolation	>80 dBc
Harmonics (2 nd , 3 rd)	<-80 dBc

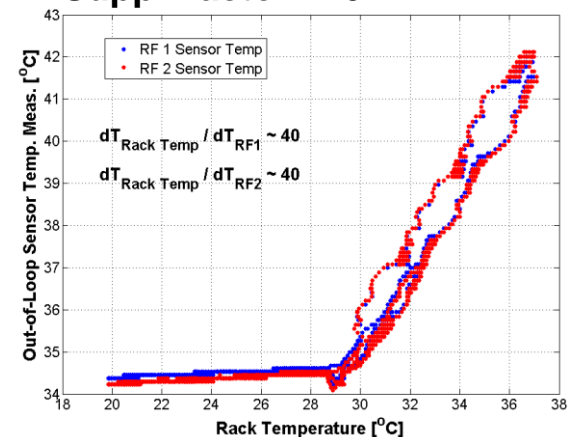
Typical CLK (81.25 MHz)
Absolute Phase Noise



Measured Residual Phase Noise of the LO
4.3 fs [10 Hz-10 MHz]

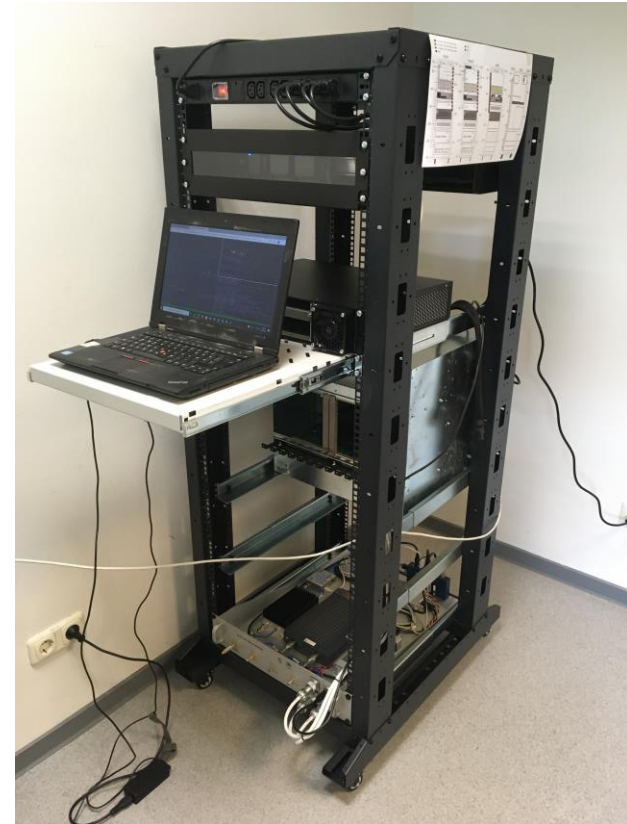


Measured Temperature Regulation on the Board
Supp. Factor ~40

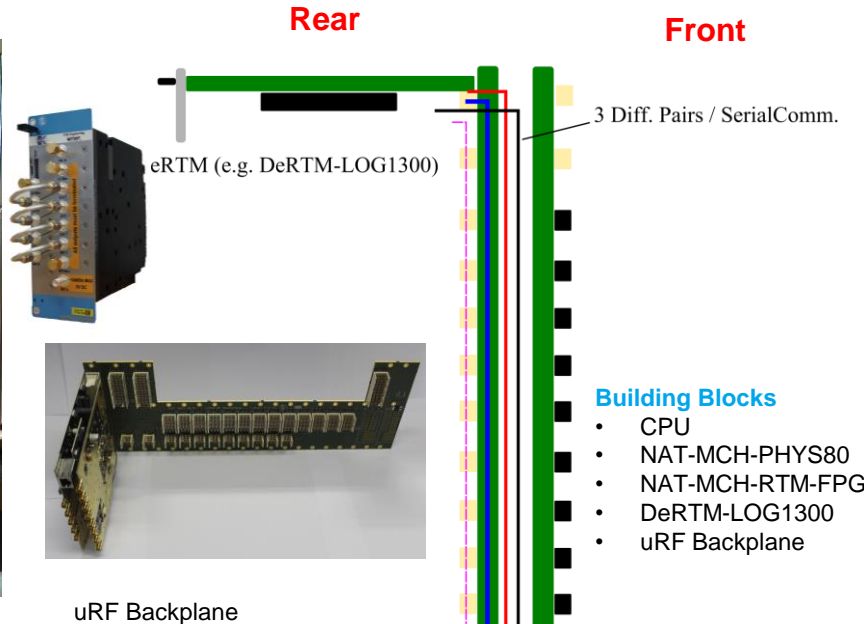


DeRTM-LOG Test-Stand

- Development of a fully automated test stand to check possible production errors.
- Will measure:
 - individual mezzanines (DC/DC mezz., RF mezz.,...)
 - A fully assembled module
- Will cover testing of CLK frequencies from 1 MHz to 500 MHz and LO, REF and pilot from 1 MHz to 6 GHz.



System Integration



```

mavric@mavric-VirtualBox:~$ cat show_fru
-----
FRU Information:
-----
FRU Device State Name
-----
0 MCH M4 MCH-CU
3 MCHC1 M4 NAT-MCH-MCHC
5 AMC1 M4 CCT AM 982/411
6 AMC2 M4 X2TIME
7 AMC3 M4 DAMC2V3
8 AMC4 M4 DAMC-TCK7
11 AMC7 M4 S1S308L2 AMC
12 AMC8 M4 S1S308L2 AMC
13 AMC9 M4 S1S308L2 AMC
14 AMC10 M4 S1S308L2 AMC
15 AMC11 M4 S1S308L2 AMC
16 AMC12 M4 S1S308L2 AMC
48 CU1 M4 Schroff UTCA CU
41 CU2 M4 Schroff UTCA CU
51 AMZ M4 PR-AC1800
60 Clock1 M4 MCH-Clock
01 HubRoot1 M4 MCH-PCIE
64 MCH1-RTM M4 MCH-RTM-CONEX
91 AMZ-RTM M4 X2TIMER8TH
92 AMC3-RTM M4 DAMC2RTH
93 AMC4-RTM M4 DAMC-TCK7-RTM
96 AMZ7-RTM M4 S1S308L2 RTH
97 AMC8-RTM M4 S1S308L2 RTH
98 AMC9-RTM M4 S1S308L2 RTH
99 AMC10-RTM M4 S1S308L2 RTH
100 AMC11-RTM M4 S1S308L2 RTH
04 eRTM15 M4 eRTM-LOG1300
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mavric
    
```

Building Blocks

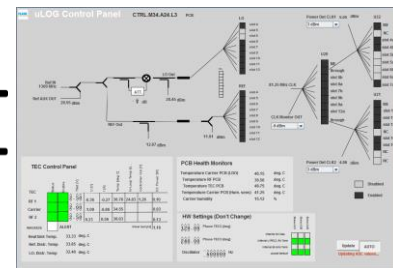
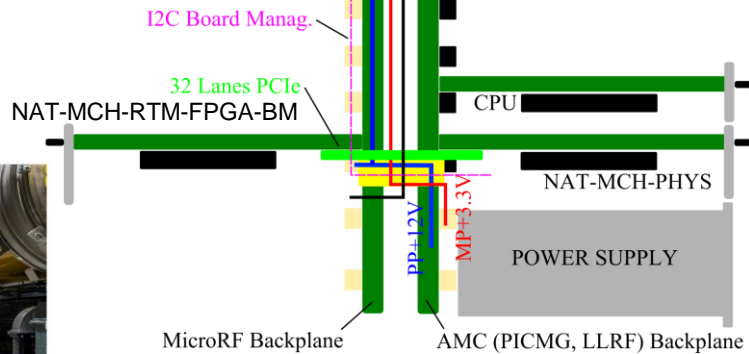
- CPU
- NAT-MCH-PHYS80
- NAT-MCH-RTM-FPGA-BM
- DeRTM-LOG1300
- uRF Backplane

```

mavric@xfelpulla24s:/dev$ ls
autofs          hugepages       loop0
block           hwrng           loop1
bgs             intelctl        loop2
btrfs-control   input           loop3
bus             kmsg            loop4
char            kvm              loop5
console         lightnvm        loop6
core            llrfadcs10     loop7
cpu             llrfadcs11     mapper
cpu_dna_latency llrfadcs12     mcelog
cuse           llrfadcs7       md
disk           llrfadcs8       md0
cryptfs        llrfadcs9       md1
fd              llrfadcs13     md2
full           log              md3
fuse           loop-control    me10
hpet           loop-control    me1
mavric@xfelpulla24s:/dev$
    
```

Commissioned on EuXFEL (L3)

- There are 42 DeRTM-LOG1300 modules installed in the EuXFEL.
- The bERLinPro at HZB has 2 units in operation



Thanks to N.A.T. GmbH for their support by integration.

Future Developments

New Frequency Variants

- Because of modularity (plugable mezzanine units) only the affected modules have to be redesigned
- The current architecture doesn't allow to cover various LO and CLK generation scenarios (e.g. fractional ratios)
- The design will cover reference frequencies like 3 GHz, 500 MHz,...

Improvement of RF performance

- Improvement of residual phase noise of the LO and CLK generation
 - < -165 dBc/Hz for white noise on LO
 - -165 dBc/Hz for white noise on CLK

Principles under investigation

Multipliers and dividers

- New low phase noise dividers on the market.
- Configurability is limited.

Standard PLL

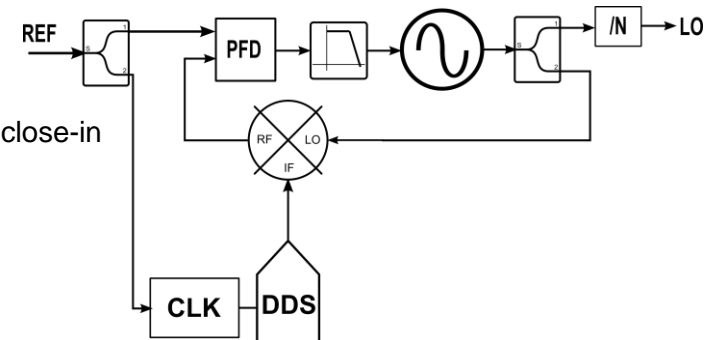
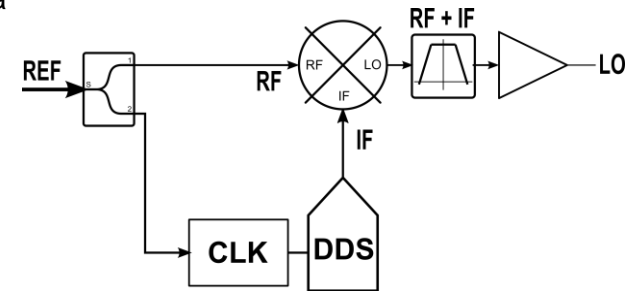
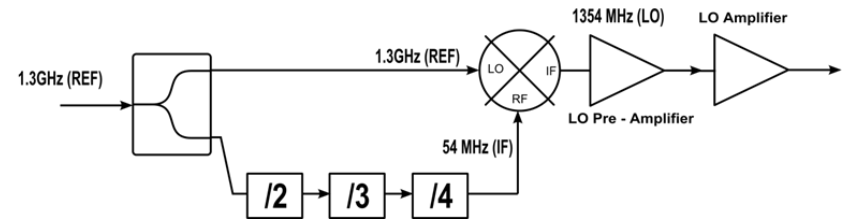
- New VCOs have very high Q – low phase noise.
- Configurability and overall phase noise is not the best (different frequency means a different VCO probably, phase detector limitations).

Up-conversion of IF generated with a DDS

- Currently some very low phase-noise DDS solutions available on the market.
- One design can cover all the possible frequencies.
- Still need of an output bandpass filter (has to change with output frequency).

Translation PLL

- Voids the problem of the divider in the feedback. A major improvement to the close-in phase noise.
- No sharp output bandpass filter needed.
- One design can cover all possible frequency generation scenarios.
- Higher complexity.



Collaboration with KVG Quartz Crystal Technology GmbH

- The company KVG Quartz Crystal Technology GmbH is taking over the production of DeRTM-LOG1300 and LOG1500. The production phase has started this month.
- KVG has a licensing agreement with DESY for all the future DeRTM-LOG variants.

It is possible to order the DeRTM-LOG modules at KVG Quartz Crystal Technology GmbH.



Quartz Crystal Technology GmbH



Thank you

Part 2:

**Introduction of KVG Quartz Crystal Technology GmbH
by Jiaoni Bai**