The X3Timer

A MTCA.4 based timing hardware for PETRA IV

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HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

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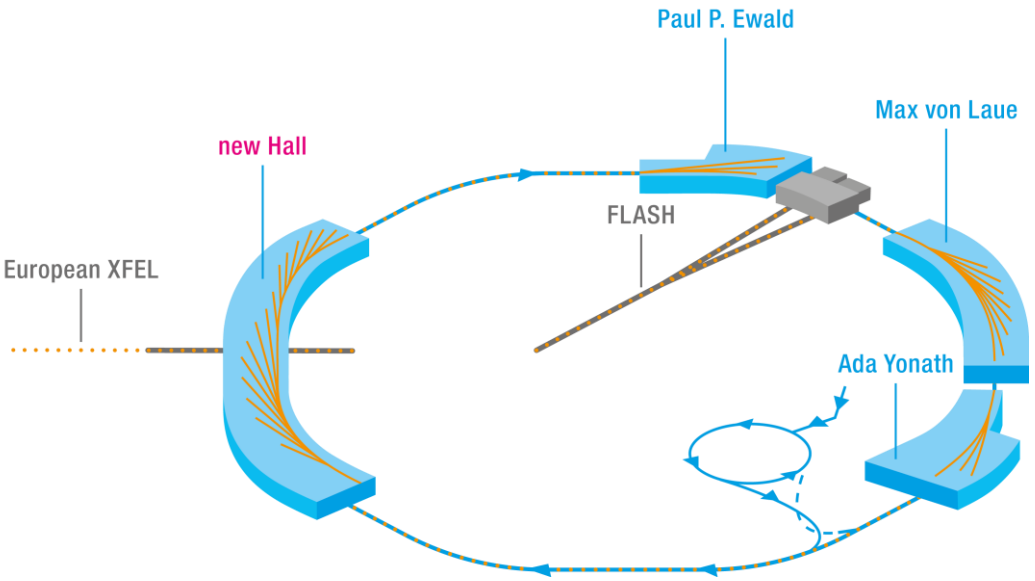
DESY.

Content

- **PETRA IV and the timing system work package**
- **Actual lab activities at DESYs MSK Timinglab**
- **Concepts for the X3Timer and development roadmap**

PETRA IV



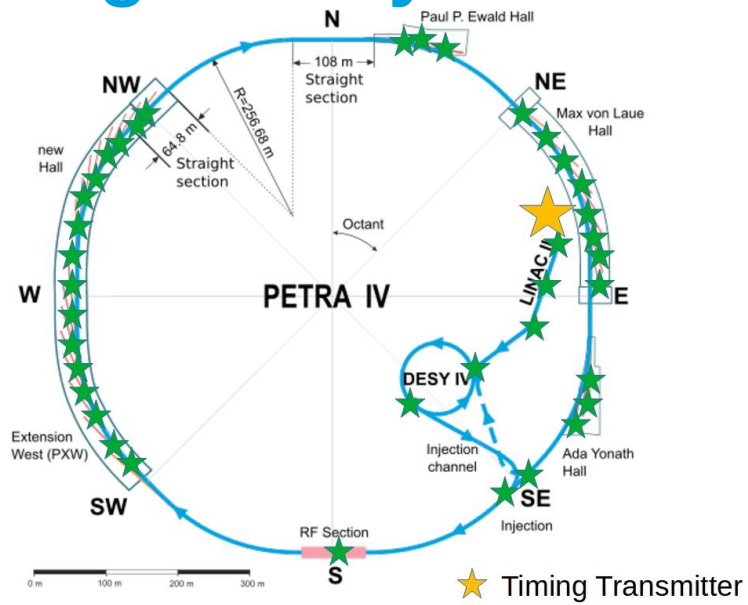
PETRA IV overview

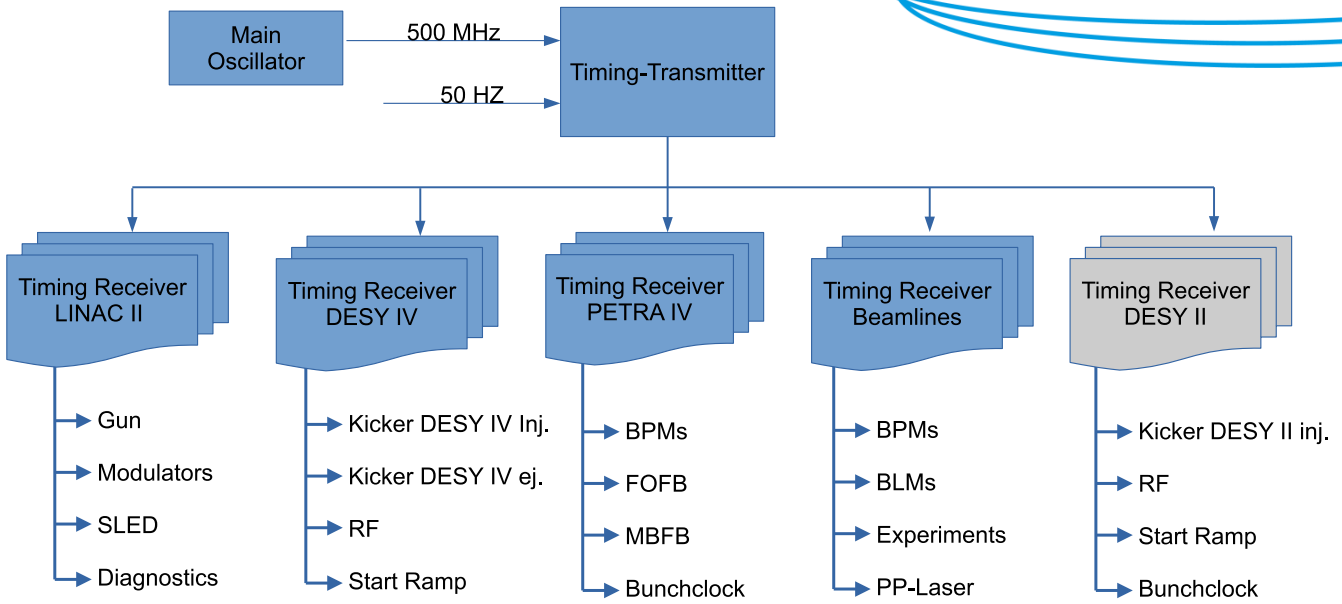
- 4th Generation Light source
- 6 GeV Storage Ring
- Circumference 2304 m
- 500 MHz RF
- low emittance: hor. 10-30 pm rad, vert. < 10 pm rad
- timing / brightness mode: 80 / 1600 Bunches
- Swap-In / Swap-Out injection
- 30 Beamlines in 4 Experimental Halls

PETRA IV will be a “New Machine” from ground on

- **MicroTCA.4 components will replace existing PETRA III hardware** for controls and diagnostics
- **Make use of experience from well-established Timing System concepts** as utilized at the FLASH and European XFEL facility
- **Keep the design flexible** to enhance functionality during life-cycle of PETRA IV
- **Expertise from DESY beam controls and control system group** are essential for the design.

Timing and Synchronization System Design





Key Requirements

- Distributing a continuous RF reference signal
- Provide low jitter clocks for ADC sampling
- Provide continuous timing signals & trigger events
- Provide beam-synchronous data as:
  - Timestamp / revolution counter
  - Beam mode / bunch pattern / bunch current
  - Bunch trains to be replaced in next swap-out/in
- Common hardware for timing transmitter and receiver
- Dedicated fiber network with drift compensation
- Common timing system for accelerator and beamlines

Integration into a overall control system

The Timing System has interfaces to almost every other subsystem. Ahead of trigger and clock distribution, the timing system will distribute beam-synchronous information as well. This beam-synchronous timing information is required for:

- Transient recorder
- Event archives
- Post mortem analysis
- Bunch-resolved data acquisition

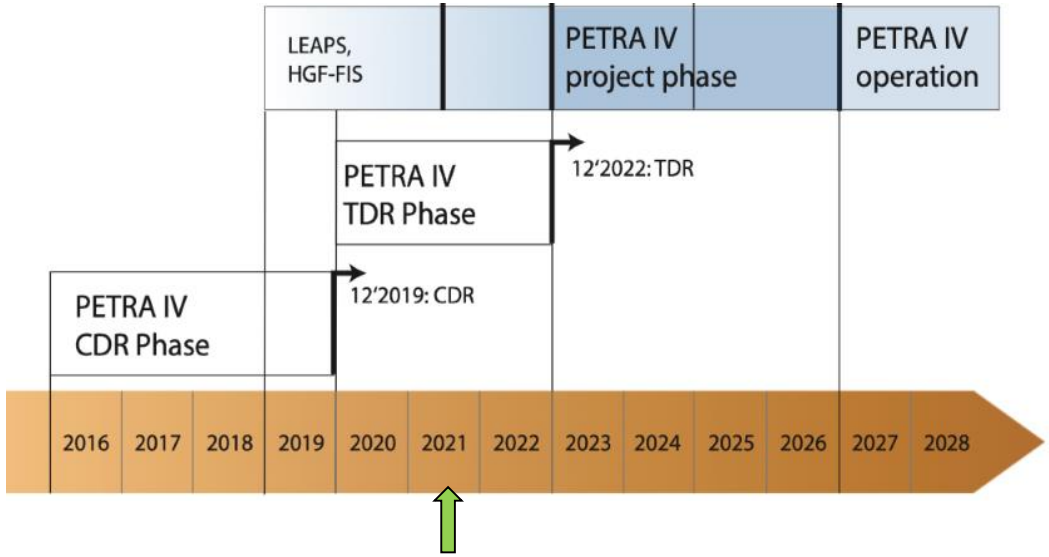
Timeline and milestones

Work package tasks

The PETRA IV project is in the Technical Design Report (TDR) phase where research and development for the later design report is made.

Major milestones for the timing and synchronization work package:

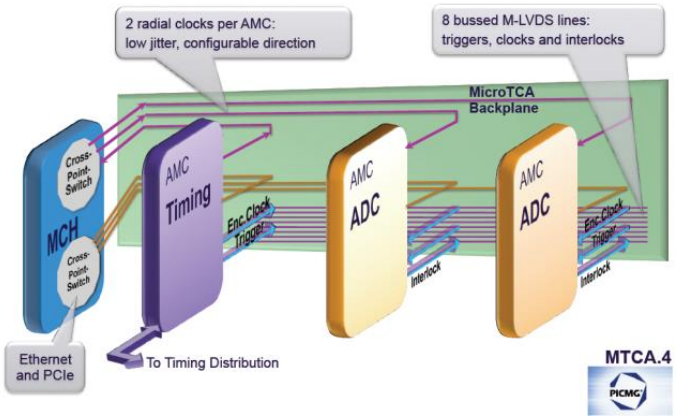
- Functional requirements for the Timing system
- Requirements for the RF Synchronization
- **X3-Timer demonstrator**
- System Design for the Timing system
- System Design for the RF Synchronization



The X2Timer

Well experienced Timing Hardware

- Developed together with DESY
- Can act as Transmitter and Receiver
- Provide continuous timing signals & trigger events
- Provide bunch meta-information
- Dedicated fiber network with optional drift compensation
- Successful in operation at FLASH and European XFEL



https://techlab.desy.de/products/amc/x2timer/index_eng.html

Design changes needed for PETRA IV

- Many components of the X2Timer are going end of life
- Output jitter can be improved
- CPU core for real-time calculation of advance delays
- Bunch-Metainformation differ from XFEL
- Front panel design
  - Save space
  - Additional interfaces (RF-Out / LEMO)
- RTM interface design by class recommendation

Lab-Tests on X2Timer hardware

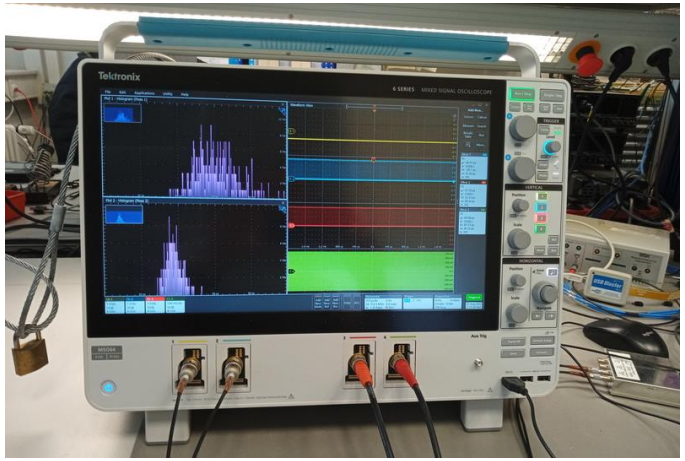
Test Setup

- RF-Generator (R&S SMA100A)
- MTCA 7-Slot Crate
  - MCH
  - CPU
  - 2 * X2Timer (Transmitter, Receiver)
- Jitter cleaner Eval-Board (LMK04832)
- measurement adapters
  - RJ45->SMA
  - SFP-> SMA

Measurement equipment

Tektronix MSO64B

- Sample rate 50GS/s
- Bandwidth 8Ghz
- vertical resolution 12 Bit
- Jitter and Eye analytics packet
- 8b10b serial decoder



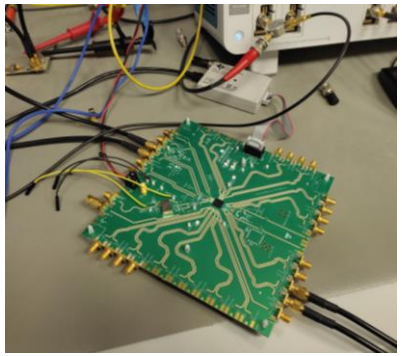
Goals

- Test concepts for the new timing card
- qualify components for their usability
- create test platforms for firmware and software development

Clock jitter cleanup

Dual loop PLL Jitter cleaner

- Created noisy clock by sending through 2 X2timers
- Feed noisy Clock to the LMK04832 jitter cleaner board
- Jitter can differentiated between
  - Random Jitter RJ
  - Deterministic Jitter DJ
  - Periodic Jitter PJ

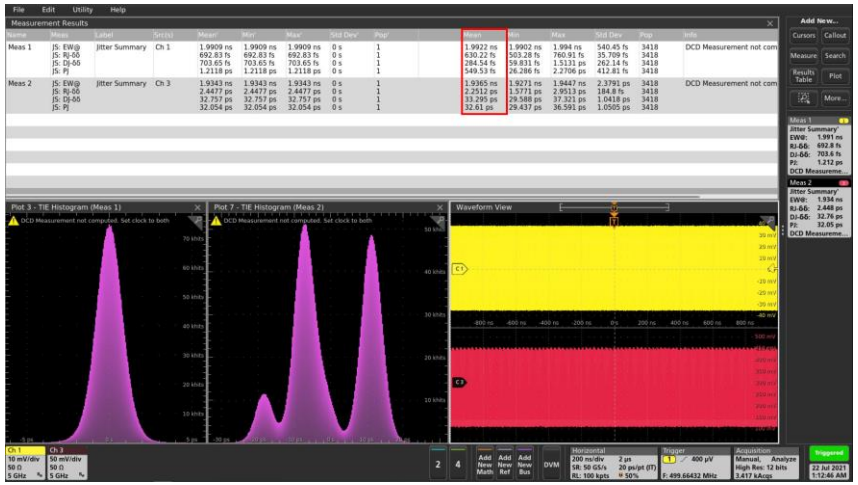


First results (Mean)

- LVDS-Output of X2Timer
  - RJ = 2.3 ps
  - DJ = 33.3 ps
  - PJ = 32.6 ps
- Output of LMK04832 (LVDS Level)
  - RJ = 630 fs
  - DJ = 285 fs
  - PJ = 550 fs

Next steps

- Compare Jitter of different RF frequencies
- Tests with longer optical cable
- Parallel test on phase noise analyzer



Transmitter – Receiver data stream analysis

8b/10b encoding

- DC balanced
- Many transitions for clock recovery

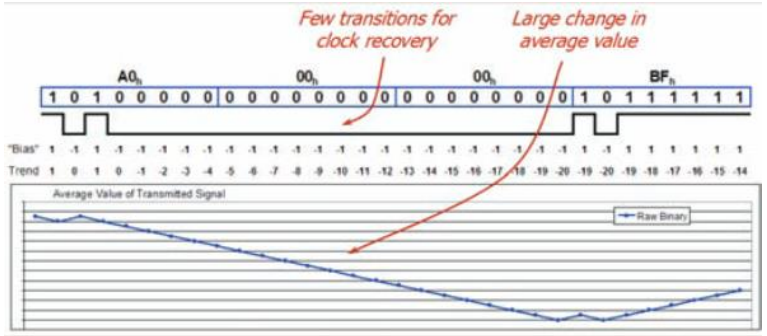


Figure 9. DC drifts without 8b/10b encoding.

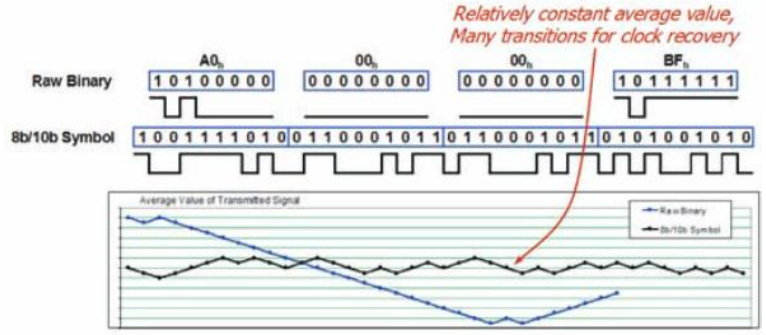
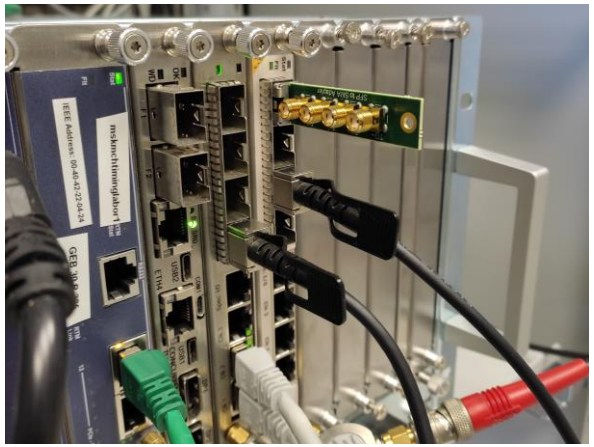


Figure 10. 8b/10b coding maintains DC level and ensures clock recovery.

https://download.tek.com/document/55W_26438_2.pdf

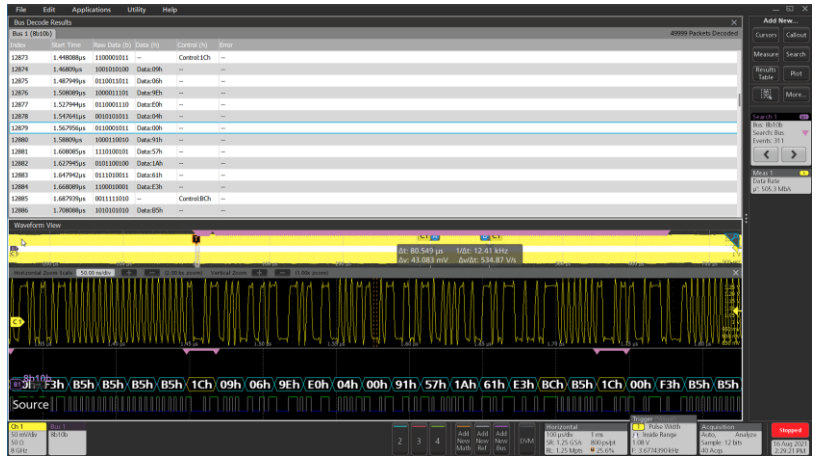


Link quality measurement

- Jitter and eye measurement
- Pass fail mask test

Protocol analysis

- Use 8b10b decoder function
- Detection of data packets
- Detection of transmission errors
- Verification against specification



Next steps in the lab setup

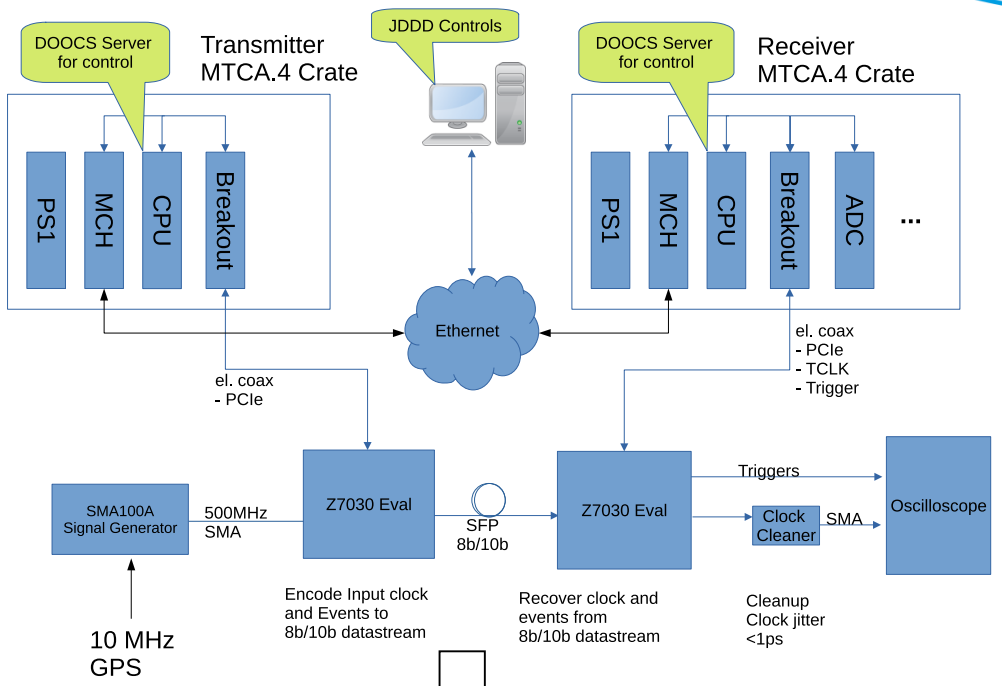
Distributed Test setup on Zynq evaluation boards

- Clock and trigger generation tests
- Output jitter measurement
- CPU-SoC interface
- Control system (DOOCS) interface
- Calculation of advance delays for bucket targeting on the SoC
- Firmware development
- Server and high-level controls development

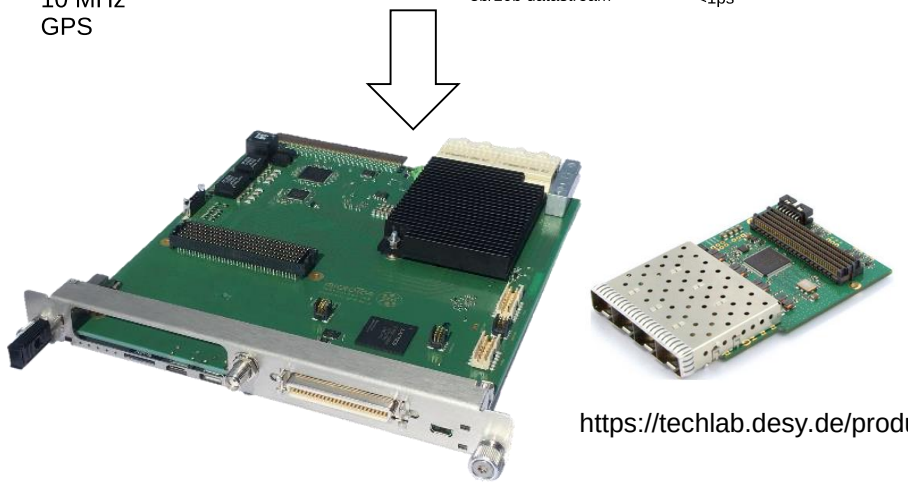
Integration into DAMC-FMC1Z7IO

(by DESY MTCA Technology Lab)

- Firmware integration into Xilinx Zynq SoC
- Test transmitter/receiver data communication over SFP fiber link
- improved RF input for 500MHz sine wave input
- redesigned bidirectional TCLK A/B Interface
- Possible early proof-of-principle



MMC Breakout board
https://techlab.desy.de



https://techlab.desy.de/products/fmc/dfmc_sfp4/index_eng.html

https://techlab.desy.de/products/amc/damc_fmc1z7io/index_eng.html

Interfaces of the X3Timer

Front Panel

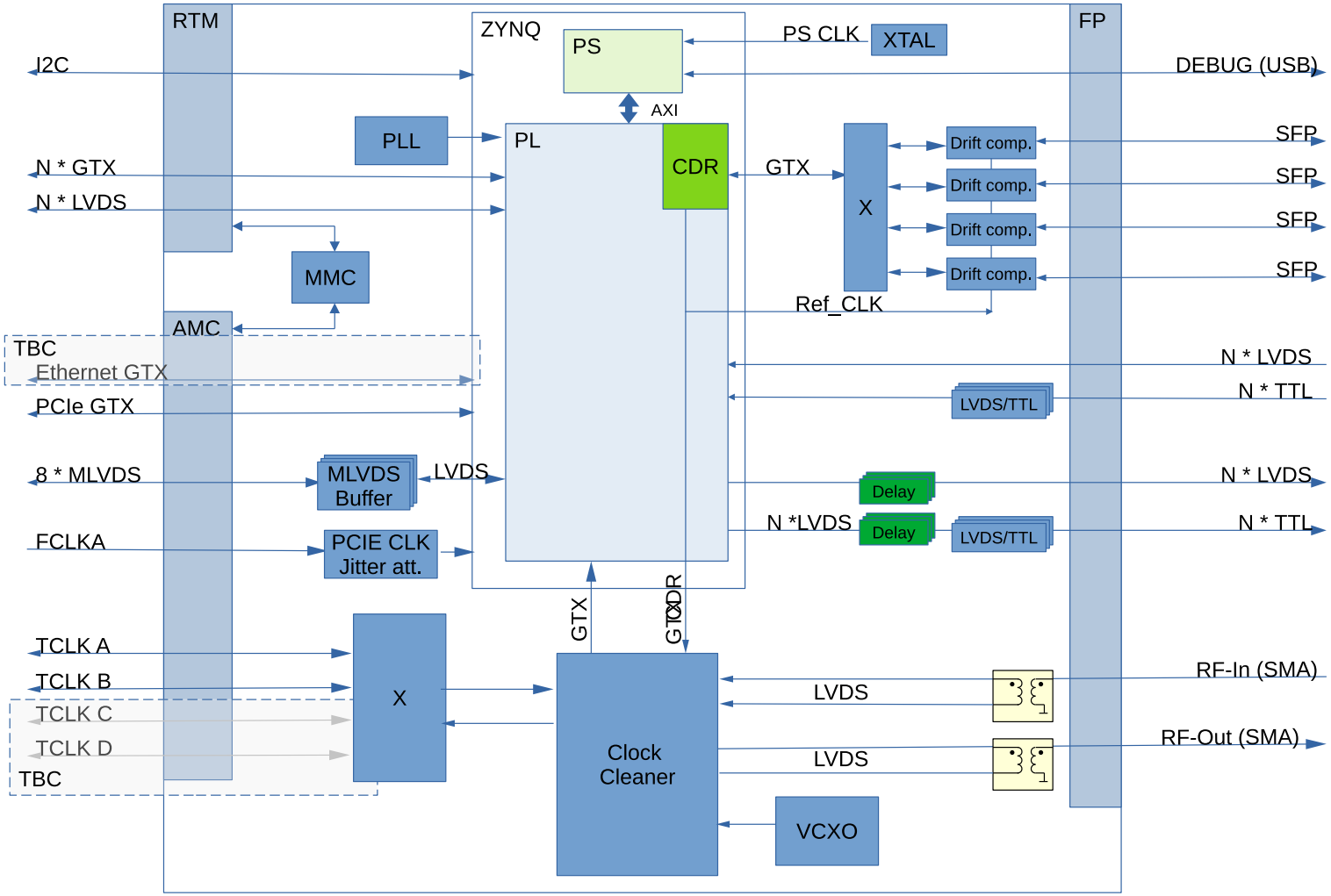
- (Q)SFP – for timing signal distribution
- LVDS Input /Output (RJ45)
- RF-Input/Output (SMA)
- TTL Trigger/Clock output (LEMO)
- I/O Input
- USB (Debug)

AMC - Backplane

- PCIe
- Ethernet
- TCLK A/B (C/D tbd.)
- Port 17-20 Trigger/Clock
- IPMI to MMC

RTM Zone 3

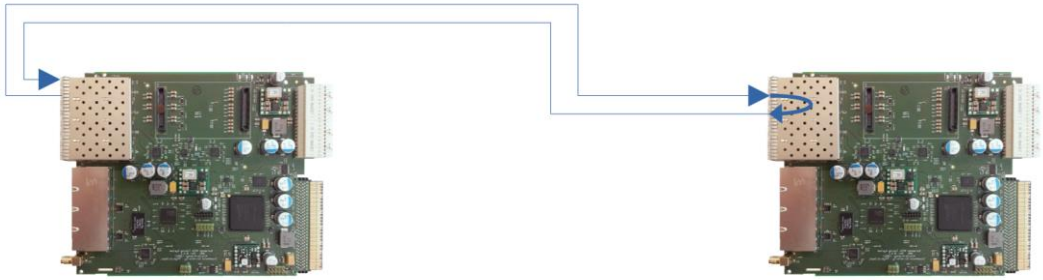
- MGT lanes
- LVDS Trigger / Clocks
- I2C to MMC
- I2C for configuration

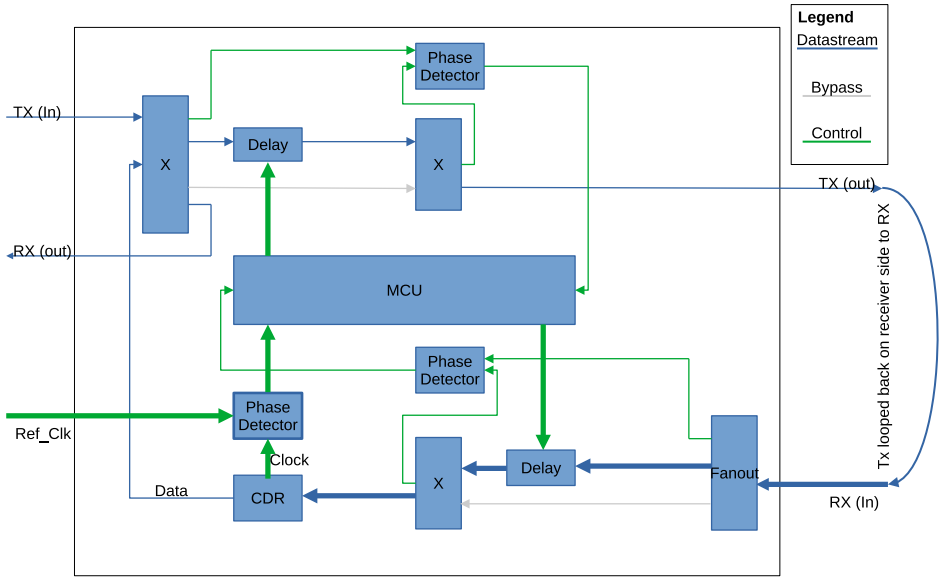


Drift compensation

All transmitting SFP connectors shall have an adaptive drift compensation which:

- Detects phase differences between Ref_CLK and recovered clock (looped back on receiver)
- Sets delays to keep the phase relation between TX and RX path
- Is able to read back the phase difference between direct and delayed path (for RX and TX)
- actively monitors the phase and adapts the delay by an module internal MCU
- Has the option to be bypassed
- Configurable from the control system through the FPGA
- For cost optimization separate module or equip option

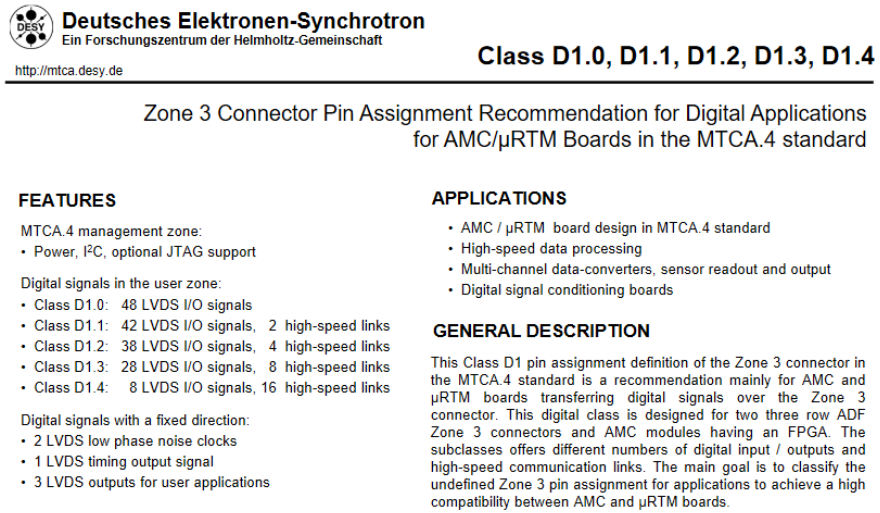




Possible RTM modules

Zone 3 (RTM-Connector)

RTM Class D1.1 or above (depends on the amount of required High-Speed links)
RTM class recommendation see:
https://techlab.desy.de/resources/zone_3_recommendation/index_eng.html



Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft
http://mtca.desy.de

Class D1.0, D1.1, D1.2, D1.3, D1.4

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Digital signals in the user zone:
- Class D1.0: 48 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 38 LVDS I/O signals, 4 high-speed links
- Class D1.3: 28 LVDS I/O signals, 8 high-speed links
- Class D1.4: 8 LVDS I/O signals, 16 high-speed links

Digital signals with a fixed direction:
- 2 LVDS low phase noise clocks
- 1 LVDS timing output signal
- 3 LVDS outputs for user applications

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-speed data processing
- Multi-channel data-converters, sensor readout and output
- Digital signal conditioning boards

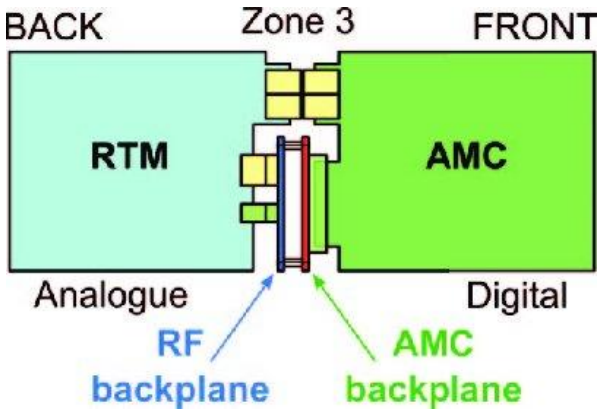
GENERAL DESCRIPTION

This Class D1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring digital signals over the Zone 3 connector. This digital class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The subclasses offers different numbers of digital input / outputs and high-speed communication links. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

https://techlab.desy.de/resources/zone_3_recommendation/index_eng.html

RTM modules

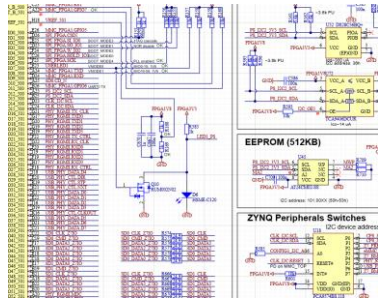
- Rear panel interfaces
  - LEMO
  - LVDS
  - Optical
  - NIM?
- RF-Backplane interface
  - Clock distribution
- Functional
  - Programmable delay line
  - SFP Fanout module

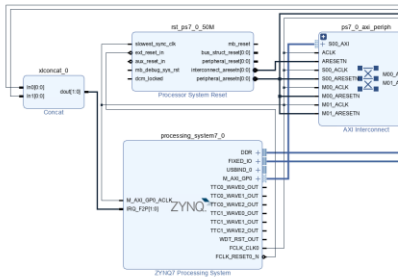


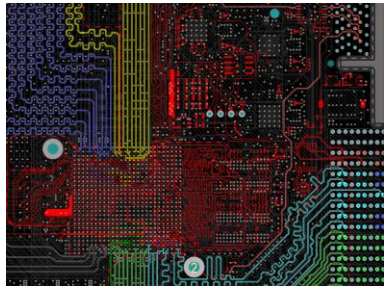
Roadmap

Roadmap 2021/2022

- Specify Requirements
- Derive MTCA.4 AMC and RTM architecture and interfaces from requirements
- Adapt existing AMC design for X3Timer demonstrator
- Hardware development and production
- Firmware development
- Server and high level controls development







	2021												2022											
Project name	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12
PETRA IV - X3 Timer Demonstrator																								

Symbol Legend:	
Specification	
Design	
Design/Production External	
Production	
Test	

Thank you for your attention!

Contact

DESY. Deutsches Elektronen-Synchrotron

www.desy.de

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