Recent developments from MicroTCA Technology Lab.

Jan Marjanovic for MicroTCA Tech Lab team

2021-08-24

2nd MTCA/ATCA Workshop for Research and Industry (China) at IHEP

MicroTCA TECHNOLOGY LAB

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

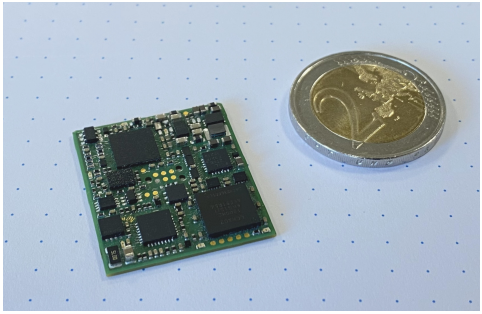
DESY.

Outline

- **DMMC-STAMP**
  Module Management Controller implementation
- **DAMC-FMC2ZUP**
  High-performance FMC/FMC+ carrier
  (Xilinx Zynq US+ MPSoC)
- **DAMC-FMC1Z7IO**
  Cost-optimized FMC carrier (Xilinx Zynq-7000)
- **DAMC-DS812ZUP**
  Ultra-low-latency high-speed 8-channel digitizer
  (Xilinx Zynq US+ MPSoC)
- **Other activities**
  Training courses

DMMC-STAMP

- Module Management Controller on a single board (SoM), ready-to-use, based on ARM Cortex-M4
- Full IPMI handling
- FPGA, FMC, and RTM control
- Tested with N.A.T. and Vadatech MCHs
- HPM firmware update: MMC, FPGA Flashes
- Solder-on component, firmware preprogrammed, SDK available
- Firmware deployed to hundreds of boards at DESY and worldwide

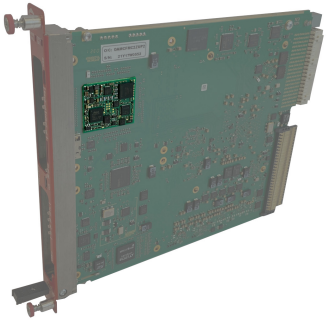


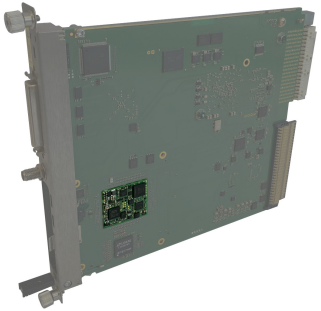
https://techlab.desy.de/products/module_management_controller/mmc_stamp/

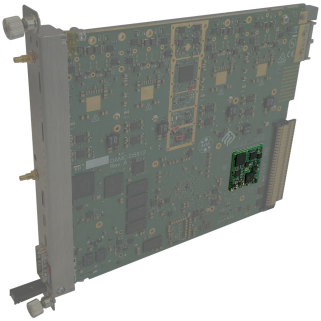
DMCS (Łódź University of Technology) also contributed to the development

DMMC-STAMP on a board

DMMC-STAMP can be mounted on the back side of an AMC, saving space on the front side.

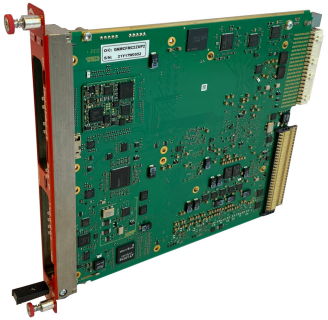




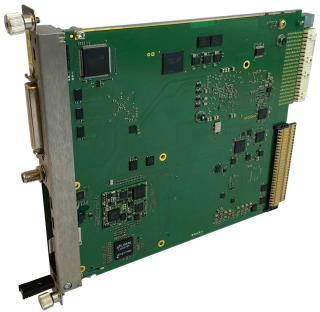


DMMC-STAMP on a board

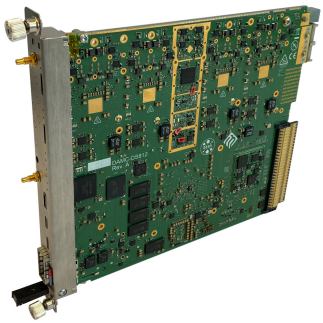
DMMC-STAMP can be mounted on the back side of an AMC, saving space on the front side.



DAMC-FMC2ZUP



DAMC-FMC1Z7IO

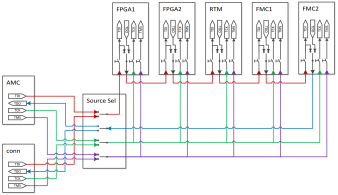


DAMC-DS812ZUP

Selected advanced features

On-board JTAG switch

- JTAG source: connector and backplane
- JTAG targets: FPGAs, FMCs, RTM



mmcterm (CLI over IPMI)

- full control over MMC remotely
- examples: Zynq boot mode, FMC Vadj, EEPROM and I2C

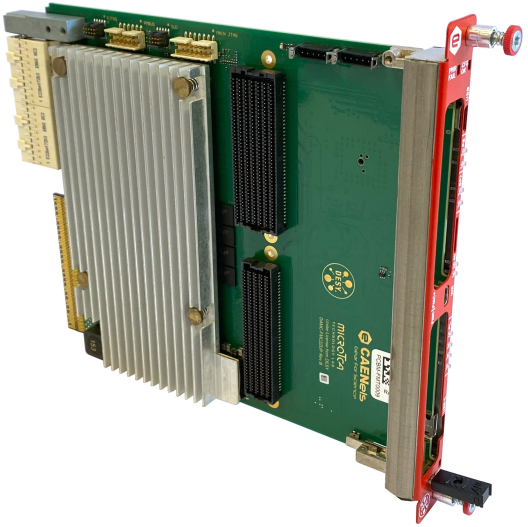
```
DAMC-FMC2ZUP@0x80 MMC>sj
EEPROM value = 0x23
source: bp, dest: fpga1
DAMC-FMC2ZUP@0x80 MMC>fmv
FMC VCC_Vadj set to autodetect
DAMC-FMC2ZUP@0x80 MMC>fru 2
FRU #2:
Product info: N/A
Board info: CAENELS FMC-4SFP+
            S/N 17006 P/N F
            Mfg_Date 2015-06-10 00:00:00
DC Load P1_12P0V: 12V (min 11.4, max 12.6) ~0mV, min 0mA / max 1mA
DC Load P1_3P3V: 3.3V (min 3.12, max 3.46) ~0mV, min 0mA / max 100mA
DC Load P1_VADJ: 2.5V (min 1.5, max 3.3) ~0mV, min 0mA / max 100mA
FMC size: single, clock dir: m2c, TCK max clock: 0
     P1: hpc, num signals: A 68, B 0, num Gbt trcv: 4
     P2: lpc, num signals: A 0, B 0, num Gbt trcv: 0

DAMC-FMC2ZUP@0x80 MMC>l2cd fmc1
Detecting peripherals on fmc1 I2C
-- -- -- -- -- -- -- --
-- -- -- -- -- -- -- --
```

FRU generator

https://github.com/MicroTCA-Tech-Lab/frugy

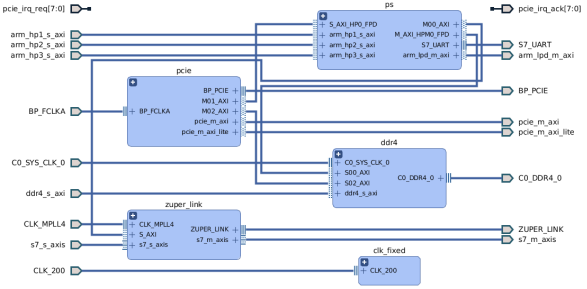
DAMC-FMC2ZUP

- Advanced Mezzanine Card, compatible with MicroTCA.4
- Xilinx Zynq UltraScale+ MPSoC
  - XCZU11EG: 653k logic cells, 2928 DSP
  - XCZU19EG: 1146k logic cells, 1968 DSP
- 52 transceivers (32 GTH, 16 GTY, 4 GTR)
- Quad-core ARM® Cortex-A53 and dual-core ARM® Cortex-R5
- 4GB DDR4 (PS) + 1GB DDR4 (PL)
- White Rabbit endpoint
- PCIe Gen3 x4, x8 in supported systems, can be used as a PCIe root complex
- DisplayPort and USB on the front panel



Commercially available at CAEN ELS
https://www.caenels.com/products/damc-fmc2zup/

Board Support Package




```
jan@ZUP-0555 ~ lsb_release -a
LSB Version:    n/a
Distributor ID: petalinux
Description:    PetaLinux 2020.1
Release:        2020.1
Codename:       zeus
jan@ZUP-0555 ~ uname -a
Linux ZUP-0555 5.4.0-xilinx-v2020.1 #1 SMP Thu Mar 4 22:37:31 UTC 2021 aa
ch64 GNU/Linux
jan@ZUP-0555 ~ free -h
              total        used        free      shared  buff/cache   ava
Mem:          3.8Gi       318Mi       3.3Gi       0.0Ki       267Mi
Swap:            0B          0B          0B
jan@ZUP-0555 ~ python3 --version
Python 3.7.6
jan@ZUP-0555 ~ gcc --version
gcc (GCC) 9.2.0
Copyright (C) 2019 Free Software Foundation, Inc.
This is free software; see the source for copying conditions.  There is N
warranty; not even for MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOS

jan@ZUP-0555 ~ cat /sys/class/fpga_manager/fpga0/state
operating
jan@ZUP-0555 ~ file /mnt/sd-mmcblk0p1/download-damc-fmc2zup.bit
/mnt/sd-mmcblk0p1/download-damc-fmc2zup.bit: Xilinx BIT data - from damc_
0=0XFFFFFFFF;Version=2020.1 - for xczu11eg-ffvc1760-2L-e - built 2021/03/
ta length 0x167d0ec
jan@ZUP-0555 ~
```

Includes FPGA part (Vivado project) and Yocto Linux.
Contact us for more information/access: `mtca-techlab@desy.de`
Linux PCIe driver: https://github.com/MicroTCA-Tech-Lab/xdma-metapackage

PCI Express gen 3 x8

Most MicroTCA crates support PCIe x4, some also support x8

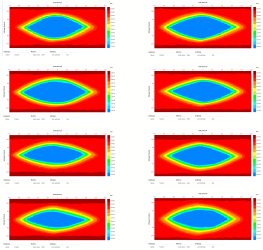
PCIe Link Status Menu

	AMC1	AMC2	AMC3	AMC4	AMC5		AMC6		OPT1
	4..11	4..11	4..11	4..11	4..7	8..11	4..7	8..11	
	-	-	x8	-	-	-	-	-	x8
Link Speed	-	-	8 GT/s	-	-	-	-	-	8 GT/s

DAMC-FMC2ZUP

optical uplink

Signal integrity in FPGA at 8 GT/s



DMA transfer (1 GB) with Xilinx DMA (xdma)

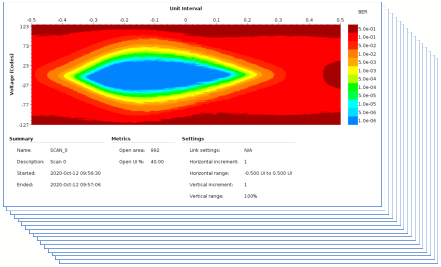
Width	Data rate	CPU	Mem	Access	Throughput
x4	8 GT/s	CCT AM G64/472	PL	Read	**2028** MB/s
x4	8 GT/s	CCT AM G64/472	PL	Write	**2948** MB/s
x4	8 GT/s	CCT AM G64/472	PS	Read	**2001** MB/s
x4	8 GT/s	CCT AM G64/472	PS	Write	**3006** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PL	Read	**1762** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PL	Write	**3304** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PS	Read	**1687** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PS	Write	**3415** MB/s

Preliminary measurements, will be improved in the future

FMC and FMC+ (400 Gbps)

- FMC+ slot
  - full LA and HA banks
  - DP[0:15] to GTY
  - DP[16:23] to GTH
- FMC slot
  - full LA and HA banks
  - DP[0:7] to GTH

16 lanes (GTYE4), 25 Gbps, PRBS31



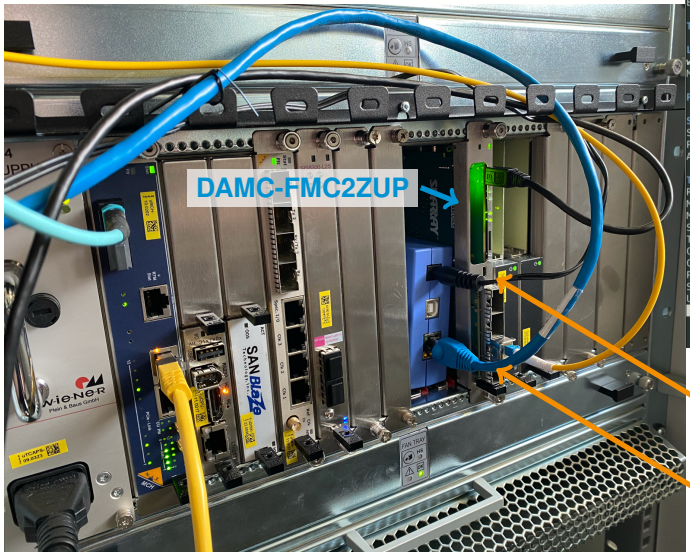
Test with an FMC+ loopback card

25 Gbps

Link Group 0 (16)							Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 0	Quad_128/MGT_X0Y4/TX (xczu11_0)	Quad_128/MGT_X0Y4/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 1	Quad_128/MGT_X0Y5/TX (xczu11_0)	Quad_128/MGT_X0Y5/RX (xczu11_0)	25.372 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 2	Quad_128/MGT_X0Y6/TX (xczu11_0)	Quad_128/MGT_X0Y6/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 3	Quad_128/MGT_X0Y7/TX (xczu11_0)	Quad_128/MGT_X0Y7/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 4	Quad_129/MGT_X0Y8/TX (xczu11_0)	Quad_129/MGT_X0Y8/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 5	Quad_129/MGT_X0Y9/TX (xczu11_0)	Quad_129/MGT_X0Y9/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 6	Quad_129/MGT_X0Y10/TX (xczu11_0)	Quad_129/MGT_X0Y10/RX (xczu11_0)	25.324 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 7	Quad_129/MGT_X0Y11/TX (xczu11_0)	Quad_129/MGT_X0Y11/RX (xczu11_0)	25.327 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 8	Quad_130/MGT_X0Y12/TX (xczu11_0)	Quad_130/MGT_X0Y12/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 9	Quad_130/MGT_X0Y13/TX (xczu11_0)	Quad_130/MGT_X0Y13/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 10	Quad_130/MGT_X0Y14/TX (xczu11_0)	Quad_130/MGT_X0Y14/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 11	Quad_130/MGT_X0Y15/TX (xczu11_0)	Quad_130/MGT_X0Y15/RX (xczu11_0)	25.319 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 12	Quad_131/MGT_X0Y16/TX (xczu11_0)	Quad_131/MGT_X0Y16/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 13	Quad_131/MGT_X0Y17/TX (xczu11_0)	Quad_131/MGT_X0Y17/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 14	Quad_131/MGT_X0Y18/TX (xczu11_0)	Quad_131/MGT_X0Y18/RX (xczu11_0)	25.315 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 15	Quad_131/MGT_X0Y19/TX (xczu11_0)	Quad_131/MGT_X0Y19/RX (xczu11_0)	25.340 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)

Bit Error Rate lower than 1E-14

White Rabbit endpoint




```
WR PTP Core Sync Monitor wrpc-v4.2
Esc = exit

TAI Time:                    Thu, May 18, 2017, 12:07:16

Link status:
wru1: Link up    (RX: 539, TX: 329) IPv4: 192.168.20.10 (static assignment)
Mode: WR Slave    Locked Calibrated

PTP status: slave

Synchronization status:
Servo state:                 TRACK_PHASE
Phase tracking:              ON
Aux clock 0 status:          enabled

Timing parameters:
Round-trip time (mu):              743439 ps
Master-slave delay:                370167 ps
Master PHY delays:          TX:    224037 ps, RX:    235977 ps
Slave PHY delays:           TX:         0 ps, RX:      8800 ps
Total link asymmetry:              -3105 ps
Cable rtt delay:                  274625 ps
Clock offset:                         -3 ps
Phase setpoint:                    15667 ps
Skew:                                  2 ps
Update counter:                      105
```

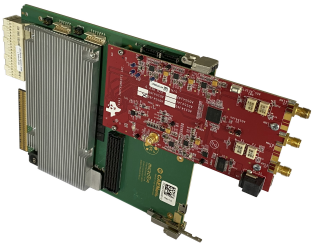
one GTH connected to the Front Panel
(special cable needed)

or **connection over FMC-4SFP+**

Applications

ADS54J60EVM

- 1 GSPS, 16-bit ADC
- 2 channels
- JESD204B (at 10 Gbps)
- subclass 1 for sync



DFMC-DSx00

- 500/800 MSPS, 12-bit ADC
- 2 channels
- LVDS interface
- very low latency

GigE Vision

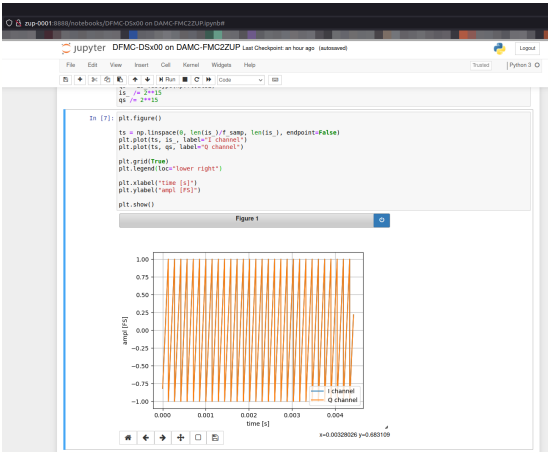
- 1 and 10 Gigabit Ethernet
- up to 8 channel
  (two FMC-4SFP+)
- FPGA + ARM CPU

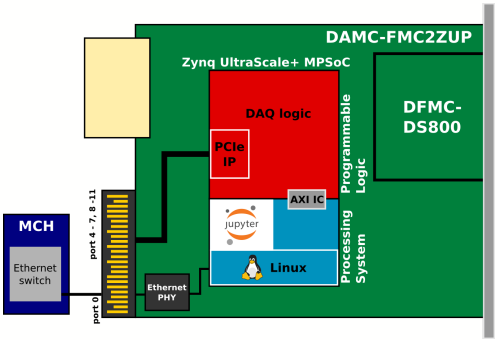
Latency comparison of ADCs with different interfaces,
https://indico.desy.de/indico/event/25669/session/2/contribution/52

Applications: Jupyter notebook

Jupyter notebook integrated with the DAQ subsystem

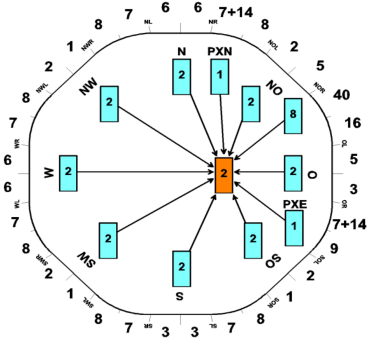
ADC (on FMC) → FPGA → AXI DMA → Python library (`pyudmaio`) → Jupyter → Ethernet → Web browser

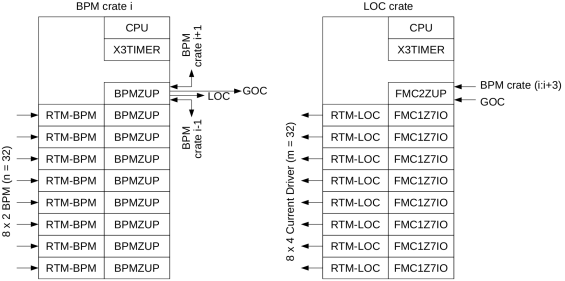




Applications: PETRA IV Fast Orbit Feedback

- DAMC-FMC2ZUP provides excellent connectivity; MGTs to PCIe x4/x8, 8 point-to-point links, 16+8+8 lanes to FMCs, 2 to Zone 3
  → data aggregation card
- different architectures for FOFB under consideration





courtesy B. Dursun (DESY)

DAMC-FMC1Z7IO

- Advanced Mezzanine Card, compatible with MicroTCA.4
- Xilinx Zynq-7000 SoC (XC7Z030, XC7Z035 and XC7Z045)
- 48 bidirectional IOs: 3.3V and true 5V
- FMC slot (full LA bank, 2/4 MGTs)
- PCIe x2 Gen2 (x4 optional)
- Dual core ARM processor
- HDMI and USB to front panel
- Zone 3 Class D1.0

https://techlab.desy.de/products/amc/damc_fmc1z7io/

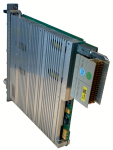
Applications

DRTM-AD84 - Rear Transition Module

- 8 channel 10 MSPS, 16 bit ADC
- 4 channel 1 MSPS, 16 bit DAC

DRTM-PZT4 - Rear Transition Module

- 4 channel piezo driver



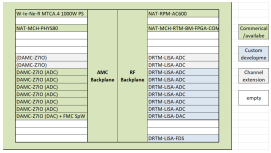
LISA phasemeter EGSE

- LISA = Laser Interferometer Space Antenna
- ground support for phasemeter (40 ch readout)
- Collaboration with University of Hamburg

Gefördert durch:
Bundesministerium für Wirtschaft und Energie
aufgrund eines Beschlusses des Deutschen Bundestages

Based on MicroTCA.4.1

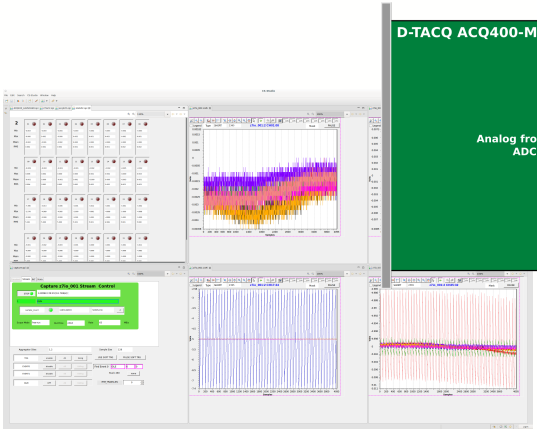
RF backplane is used to distribute pilot tone and ADC clocks

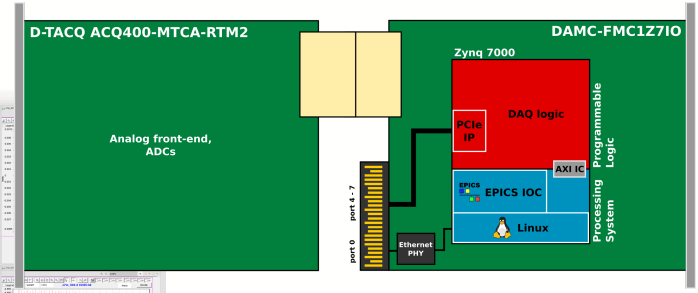


Applications: D-TACQ DAQ

D-TACQ Solutions Ltd (https://www.d-tacq.com/) is evaluating Z7IO for their systems.

Example: EPICS IOC running on Z7IO

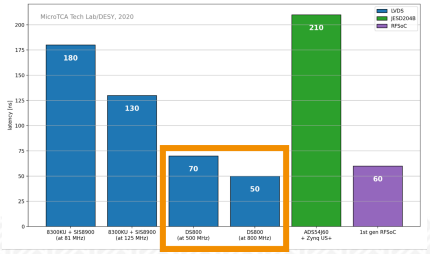


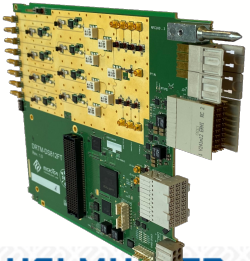


DAMC-DS812ZUP

- 8 channels, 800 MSPS, 12 bit digitizer
  (1600 MSPS with 4 channels)
- 2.7 GHz analog bandwidth (-3dB)
- Single-ended analog RTM connection (Class RF1.0)
  `https://techlab.desy.de/resources/zone_3_recommendation`
- Input from front (SSMC) or rear (RTM)
- Memory: 4GB DDR4-2666
- Dual-Loop Low-Jitter PLL On-board
- Ultra-low latency

AFE+ADC+interface latency





DRTM-DS812FT
Feedthrough RTM
(Class RF1.0)

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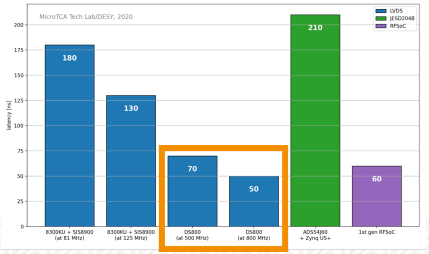
DAMC-DS812ZUP

- 8 channels, 800 MSPS, 12 bit digitizer (1600 MSPS with 4 channels)
- 2.7 GHz analog bandwidth (-3dB)
- Single-ended analog RTM connection (Class RF1.0)
  `https://techlab.desy.de/resources/zone_3_recommendation`
- Input from front (SSMC) or rear (RTM)
- Memory: 4GB DDR4-2666
- Dual-Loop Low-Jitter PLL On-board
- Ultra-low latency

AFE+ADC+interface latency



DRTM-DS812FT
Feedthrough RTM
(Class RF1.0)

Measurements in progress, stay tunned

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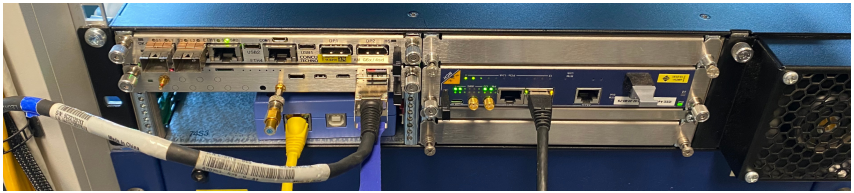
Connectivity



PCIe gen3 x8 - 4.3 GB/s reached

```
$ xdma-dma-from-device -d /dev/xdma/slot2/c2h0 -a 0x400000000 \
    -s $((1024*1024*1024)) -v -c 10
#0: CLOCK_MONOTONIC 0.368244053 sec. read 1073741824/1073741824 bytes
#1: CLOCK_MONOTONIC 0.227387605 sec. read 1073741824/1073741824 bytes
<...>
/dev/xdma/slot2/c2h0 ** Average BW = 1073741824, 4386.13818
```

AMC1	AMC2
4..11	4..11
x8	x8
8 GT/s	8 GT/s

40 Gigabit Ethernet (QSFP on front panel)

```
[  147.820192] i40e 0000:01:00.0 enp1s0: NIC Link is Up, 40 Gbps Full Duplex, Flow Control: None
[  147.836510] IPv6: ADDRCONF(NETDEV_CHANGE): enp1s0: link becomes ready
[  153.711976] i40e 0000:01:00.0 enp1s0: NIC Link is Down
[  156.334116] i40e 0000:01:00.0 enp1s0: NIC Link is Up, 40 Gbps Full Duplex, Flow Control: None
[17354.322730] i40e 0000:01:00.0 enp1s0: NIC Link is Down
```

Training courses

- Basic and Advanced training courses
- focus on experimental physics
- virtual format: Zoom + remote access
- starts at 15:00 (UTC+8), one hour break at 18:00 (UTC+8) and ends at 22:00 (UTC+8)[1]
- Custom training (for individual organizations)

Next dates:
Basic: 15 - 16 September 2021
Advanced: 8 - 9 September 2021

https://techlab.desy.de/services/training/

[1] times are flexible according to the audience

谢谢

Thank you

https://techlab.desy.de
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