Tutorial:
How to realize your application in MicroTCA.4

MicroTCA Workshop China 2021

Cagil Gumus
Hamburg, 25/08/2021

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

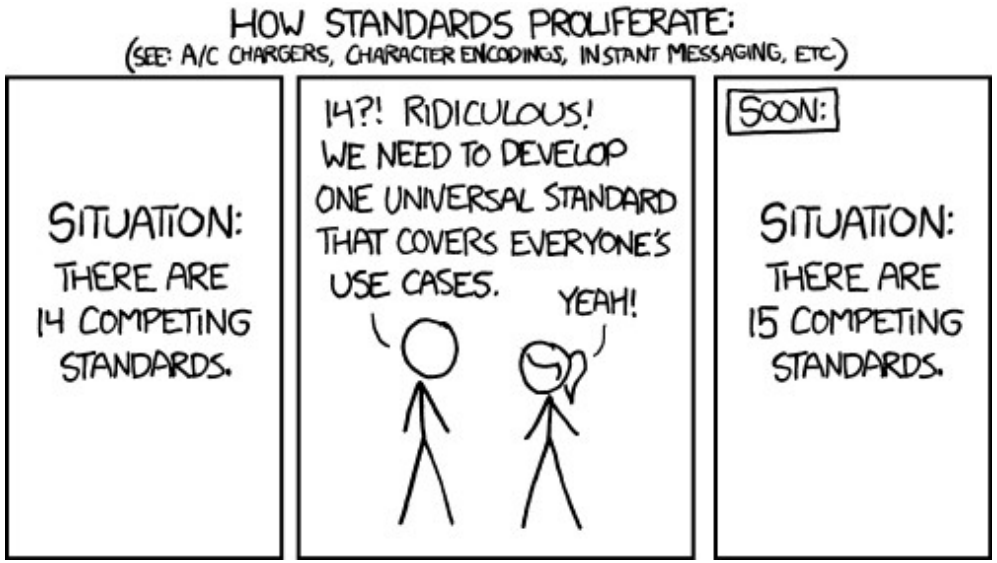
Motivation

MicroTCA can get very simple and very complicated.

Your application requirements can change the MicroTCA system significantly.

This talk will show some of the **critical questions** that one needs to ask during MicroTCA system design.

- More for beginners
- Main focus is on MicroTCA.**4**
- Interrupt me anytime.

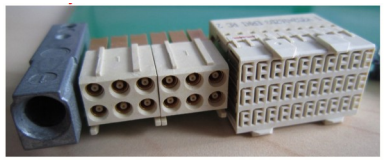


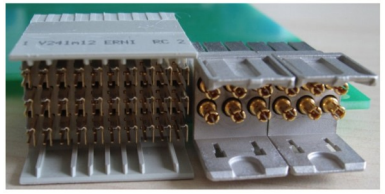
https://xkcd.com/927/

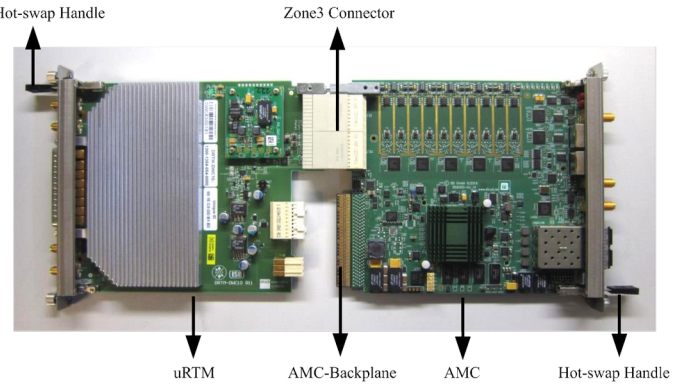
Motivation

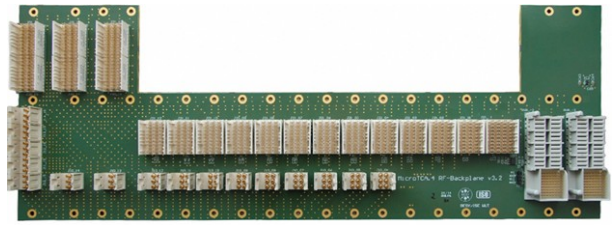
This talk will focus on following categories:

Hardware

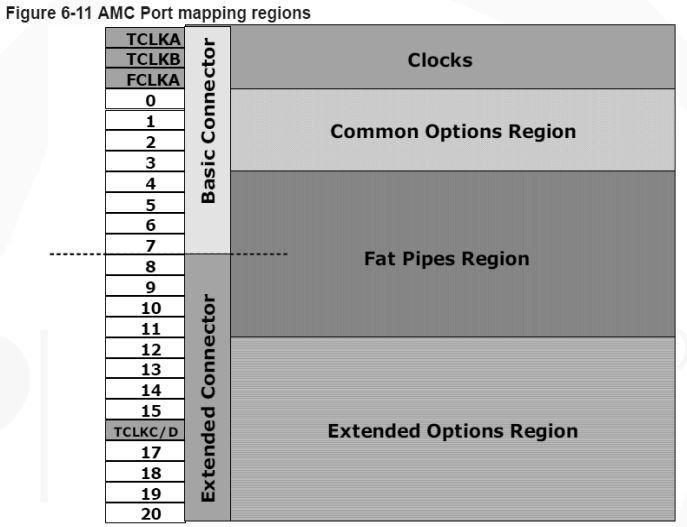


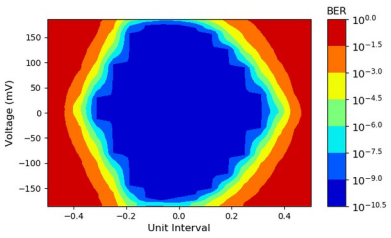




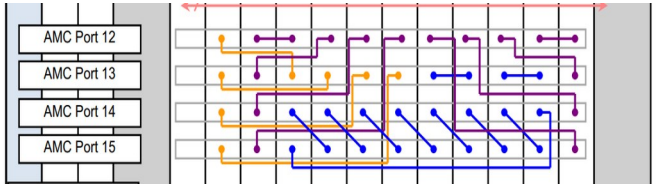


AMC Backplane





PCI EXPRESS®



Hardware

Choosing the right crate

Question #1: How many AMC boards? (+ Total Power Requirement)

Question #2: What is the reliability/redundancy requirement?

Question #3: How should be my AMC backplane? (More on this later)

Question #4: Need RF Backplane? (More on this later)

1U MicroTCA.4

- Integrated eMCH
- 2x Double Mid-Size AMC slots w/ RTM
- 2x Single Mid-Size AMC slots
- Integrated 400W PSU
- **No redundant part**

3U MicroTCA.4

- 4x Double Mid-Size AMC slots w/ RTM
- 1x Double Mid-size AMC slot
- 1x Double Full-size AMC Slot
- Discreete PSU
- **No redundant part**

5U MicroTCA.4 (Cube)

- 6x Double Mid-Size AMC slots w/ RTM
- 1x Double Full-size MCH slot
- 1x Double Full-size AMC Slot
- Discreete PSU
- **No redundant part**

9U MicroTCA.4

- 6x Double Mid-Size AMC slots w/ RTM
- 1x Double Full-size MCH slot
- 1x Double Full-size AMC Slot
- Discreete PSU
- **Redundant MCH + PM**
- RF Backplane capable
- JTAG Switch Module available

Choosing the right AMC

Family of AMC Specifications

- AMC connector has various specifications:
  - *AMC.0 → Base Specification*
    - AMC.1 → Added PCIe
    - AMC.2 → Added Ethernet
    - AMC.3 → Added Fibre Channel
    - AMC.4 → Added Serial Rapid I/O
- An AMC can have combination of specifications:
  - AMC.0 + AMC.1 + AMC.2

Family of Specifications

AdvancedMC for Serial Rapid I/O

PICMG#	NAME	CURRENT REVISION	DATE	DESCRIPTION
PICMG AMC.4	AdvancedMC for Serial Rapid I/O	1.0	2009-07-09	Defines additional requirements for Serial Rapid I/O

AdvancedMC for Storage

PICMG#	NAME	CURRENT REVISION	DATE	DESCRIPTION
PICMG AMC.3	AdvancedMC for Storage	Rev 1.0	2005-08-05	Defined additional requirements for Fibre Channel

AdvancedMC for Ethernet

PICMG#	NAME	CURRENT REVISION	DATE	DESCRIPTION
PICMG AMC.2	AdvancedMC for Ethernet	Rev 1.0	2007-03-01	Defines additional requirements for Ethernet interconnects

AdvancedMC for PCI Express

PICMG#	NAME	CURRENT REVISION	DATE	DESCRIPTION
PICMG AMC.1	AdvancedMC for PCI Express	Rev 2.0	2008-10-08	Defines additional requirements for PCI Express interconnects

AdvancedMC® Mezzanine Module

PICMG#	NAME	CURRENT REVISION	DATE	DESCRIPTION
PICMG AMC.0	AdvancedMC® Mezzanine Module	Rev 2.0	2006-11-15	Defines all electrical, mechanical, and system management requirements for building AMC's

Question #5: How the target AMC board uses the backplane?

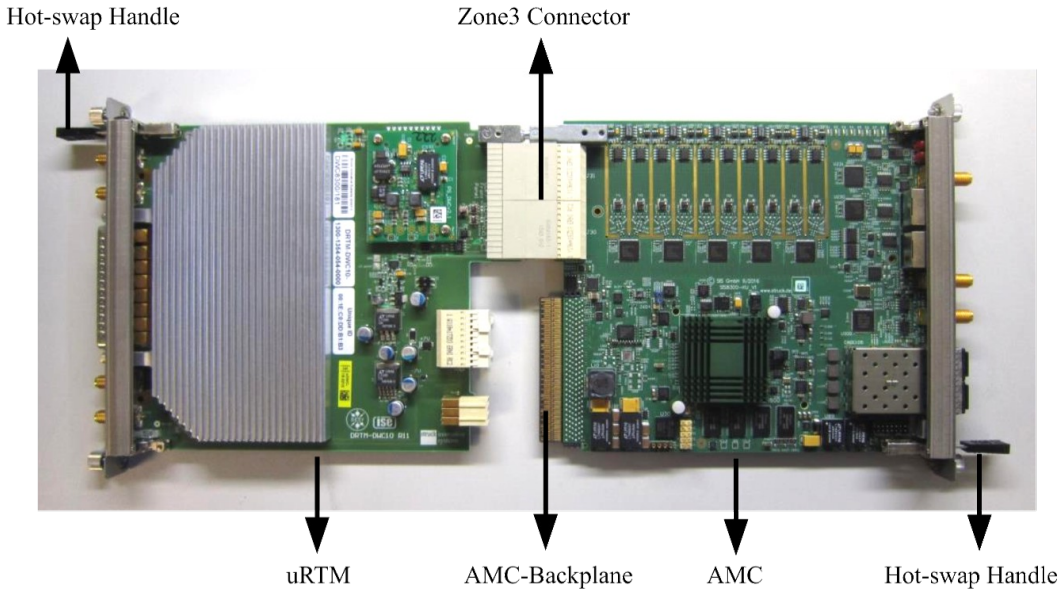
Choosing the right RTM

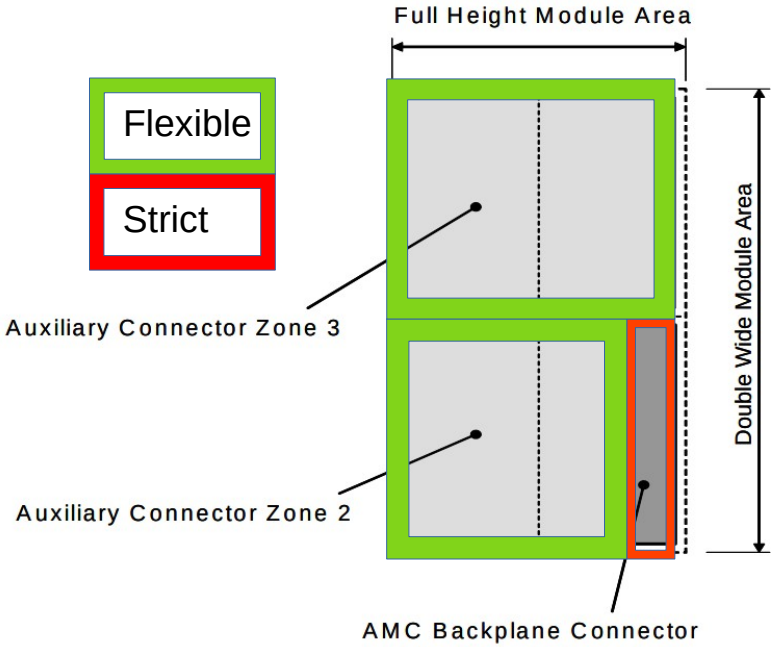
Importance of Zone2/3 Connectivity

- Mostly : AMC → COTS
- RTM → In-house development or COTS
- The MicroTCA.4 Standard does **not** dictates how Zone2 and Zone3 connector should be.

- There are recommendations done by companies/facilities.
- The interoperability might be an issue.
- Usually companies recommend RTM for their AMC cards

Question #6: AMC / RTM pair fits?





Choosing the right AMC + RTM

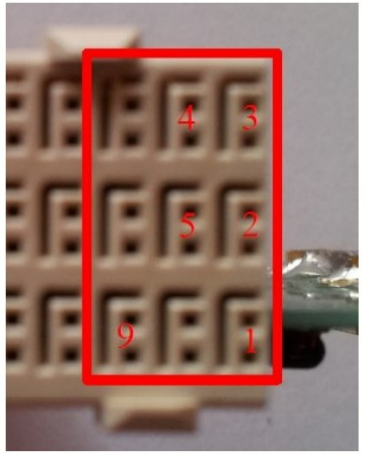
Analog signal performance of Zone3

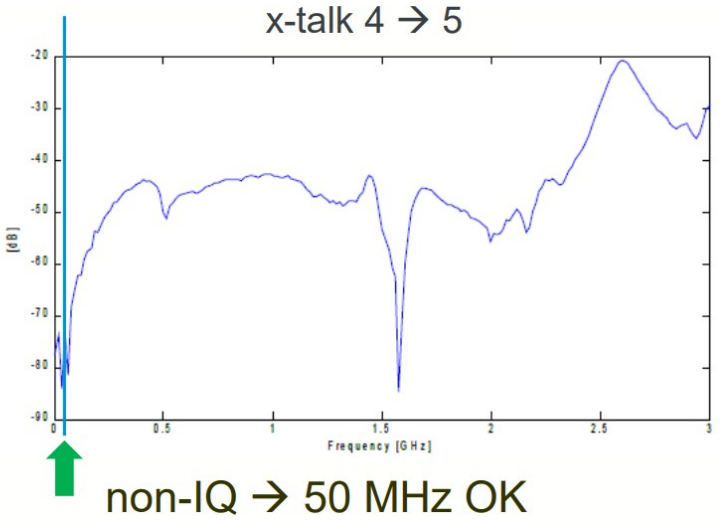
- Analog signal transfer over Zone3 can be limited in terms of maximum frequency >200MHz is problematic for LLRF applications
- New Zone 3 Class Recommendation by DESY Class RF.1.0 :
  - New connector → Up to 3GHz

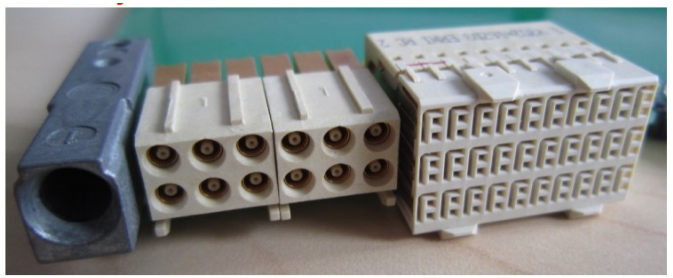
Question #7: How do I feed analog signal into AMC?

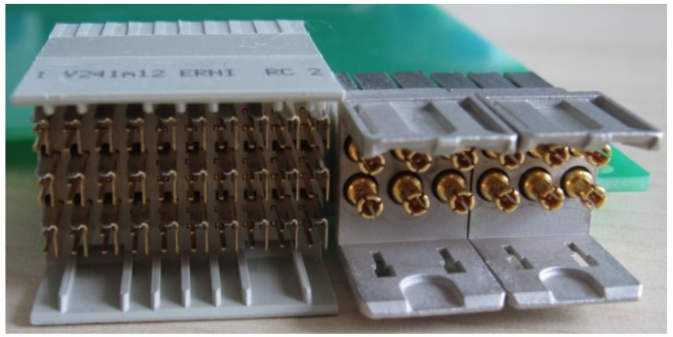
Question #8: What is the cross-talk requirement for an analog channel?

A new Zone 3 Class for RF Signals up to 3 GHz in MicroTCA.4 Johannes Zink, MTCA Workshop 2019







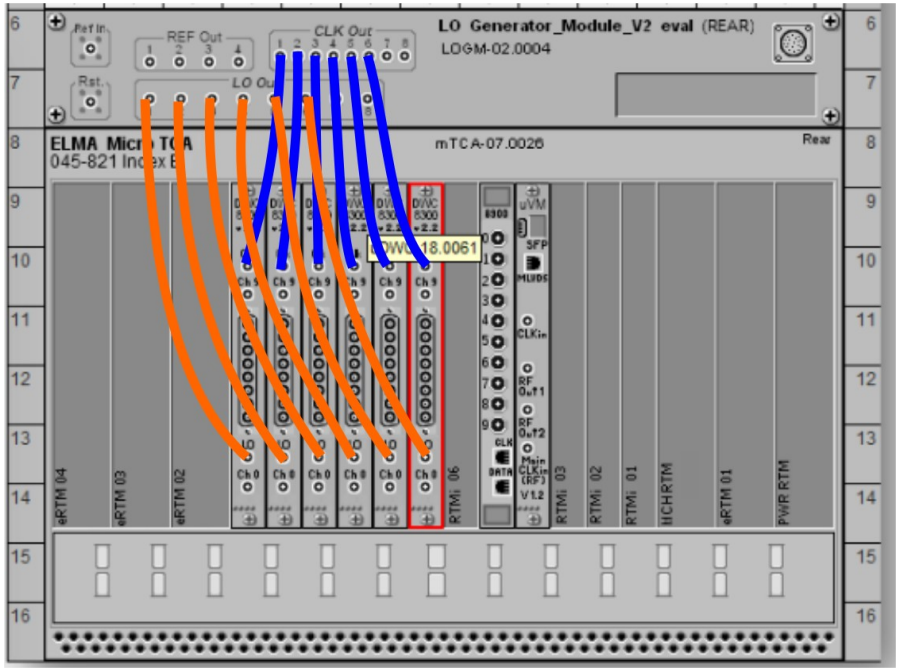


RF Backplane (MicroTCA.4.1)

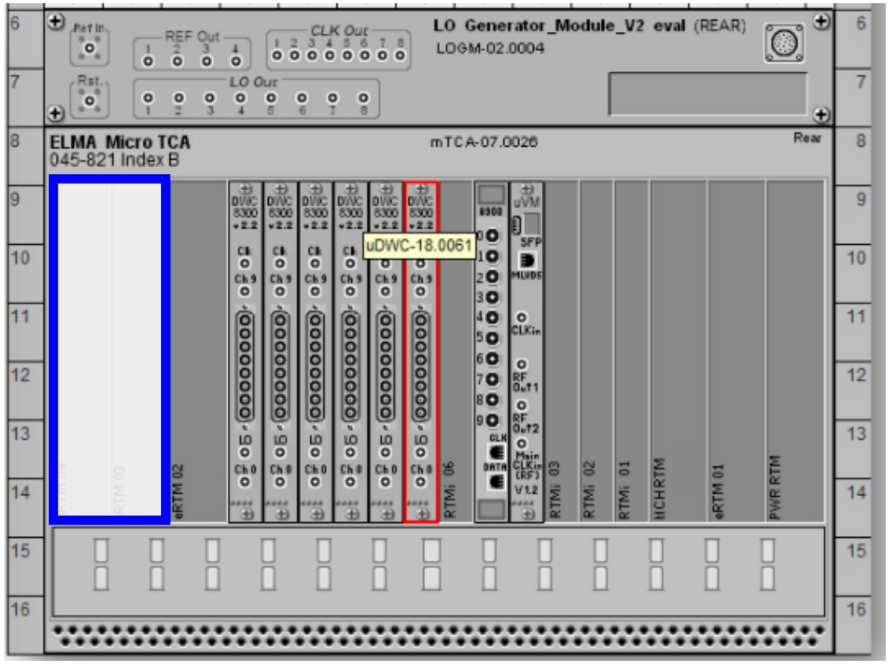
Motivation: Getting rid of spaghetti, better management for analog signal distribution

Question #9: How RTMs get their CLK, Reference, LO signals?

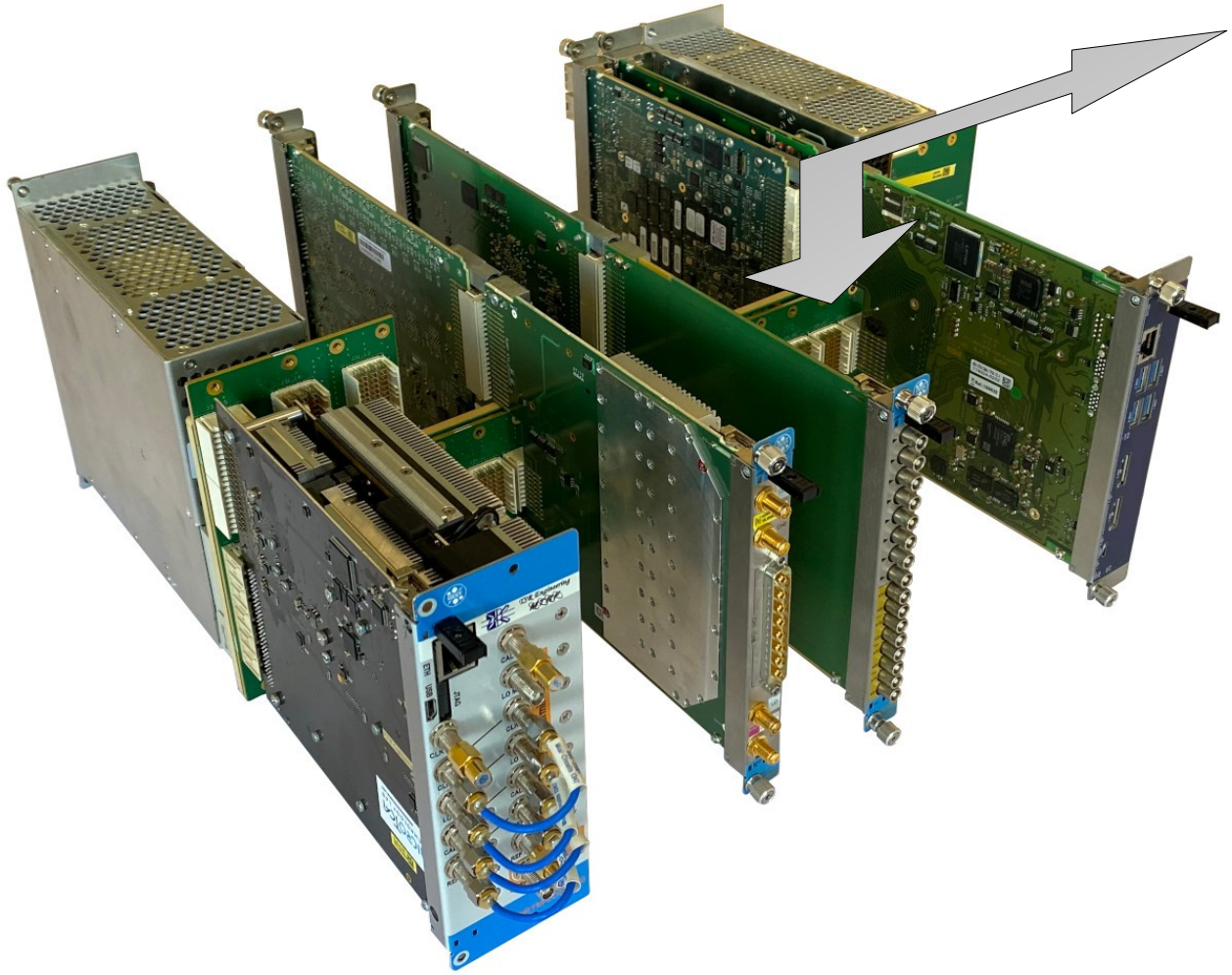
Before

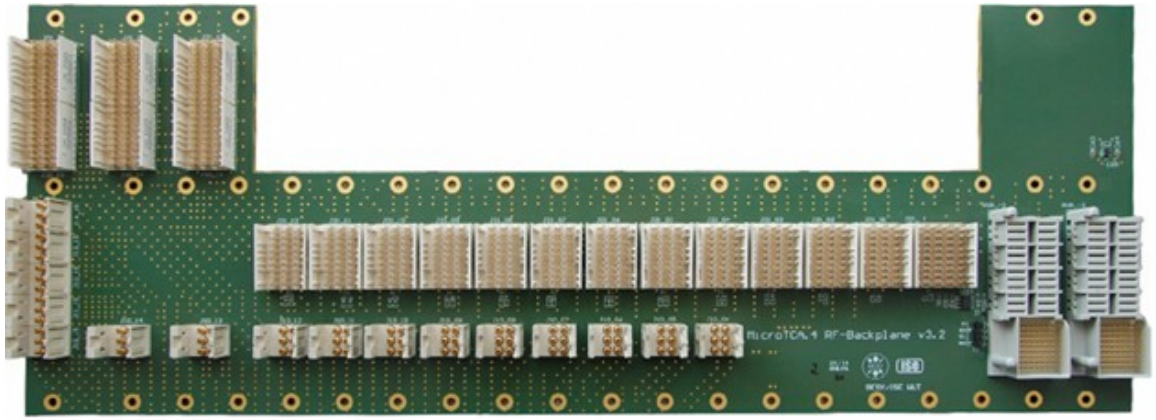


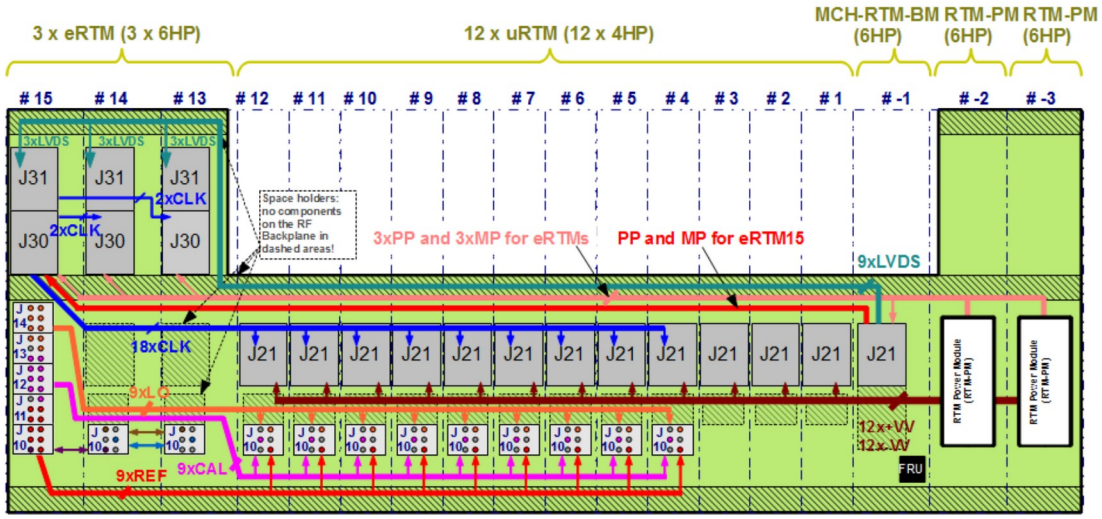
After



RF Backplane







Not many commercial solution available for eRTMs → In-house development might be necessary

AMC Backplane

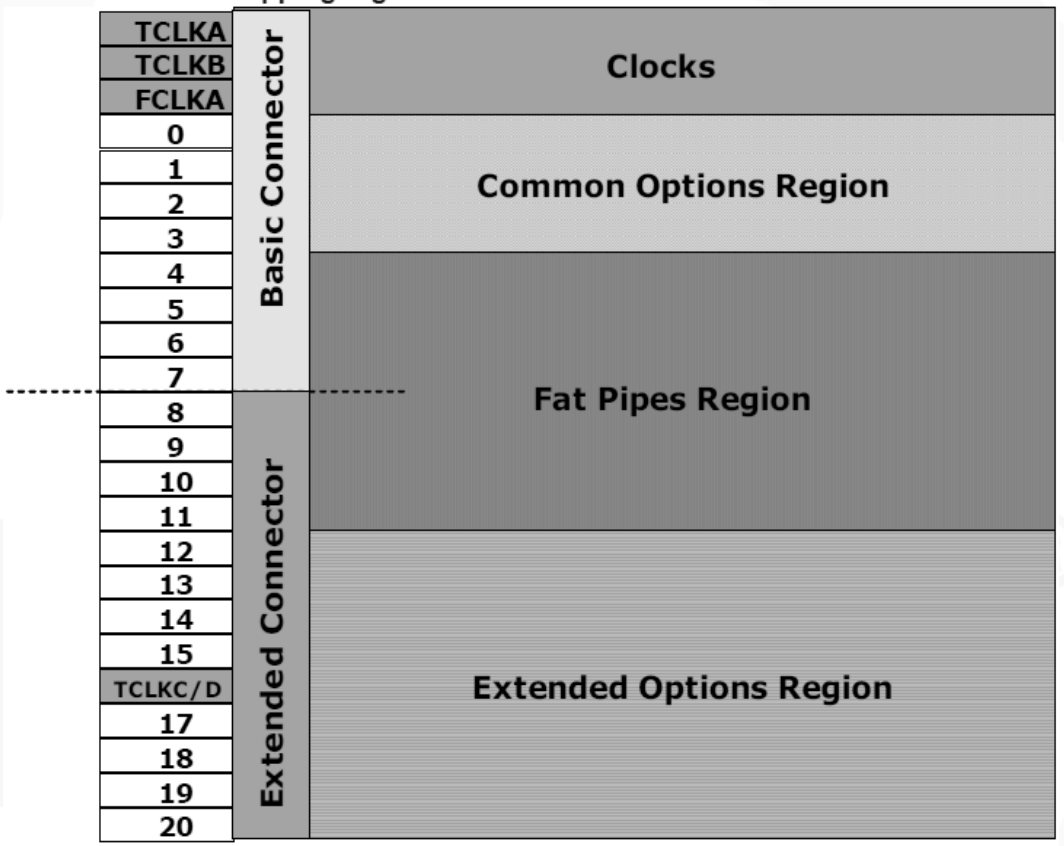
Know your AMC Backplane

Which ports to use on your application?

Protocols on the AMC backplane

- IPMI (Management)
- Gigabit Ethernet (Ports 0-1)
- SATA (Ports 2-3)
- Fat Pipe + Extended Fat Pipe (Ports 4-11)
  - PCIe*
  - SRIO
  - 10/40 GbE
- Point-to-Point Links* (Ports 12-15)
- MVLDS* (Ports 17-20)
- Clocks* (TCLKA,TCLKB TCLKC,FCLK)
- JTAG

Figure 6-11 AMC Port mapping regions



* → Will go more in detail

Fat Pipe (PCIe)

Know your AMC Backplane

PCIe

MicroTCA Crate can offer PCIe lanes in different ways:

Ports 4-7 (x4) → MCH #1

Ports 8-11(x4) → MCH #2 (Redundant)

Ports 4-11(x8) → MCH #1

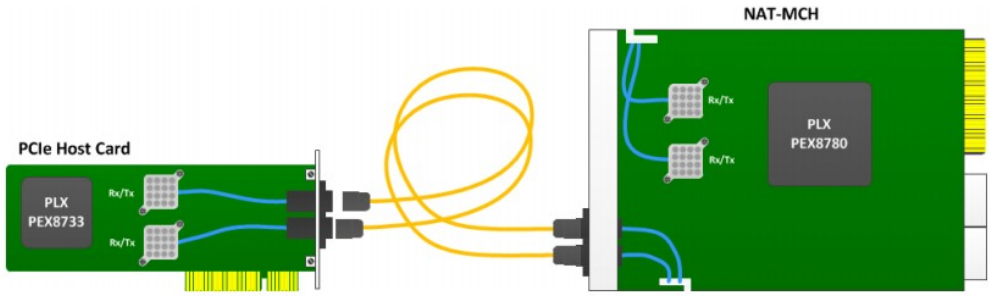
Question #10: How much bandwidth/latency does the application require (to CPU)?

PCI Express link performance[46][47]

Version	Intro-duced	Line code	Transfer rate[i][ii]	Throughput[i][iii]				
				×1	×2	×4	×8	×16
1.0	2003	8b/10b	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s
2.0	2007	8b/10b	5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
Now 3.0	2010	128b/130b	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0	2017	128b/130b	16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
Future 5.0	2019	128b/130b	32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6.0 (planned)	2021	128b/130b + PAM-4 + ECC	64.0 GT/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s	126.031 GB/s

PCIe Root Complex outside of the crate

Suffering from weak CPU-AMC? Here is your solution



Needed Parts:

- 4 x Finisar BOA
- 4 x Pig Tail
- 4 x Face Plate Adapter
- 2 x Patch Cord 5m
- Resulting Costs for a PCIe

GenIII x16 Uplink Connection:

Pros:

- Cheaper & Poweful PC outside of 80W limitation
- Many choices in the industry for parts
- Many more PCIe slots available on the motherboard for more cards

Cons:

- CPU is not managed by MCH
- Boot sequence of crate and PC has to be done properly

Question #11: How much CPU power do I need?

Question #12: Does my MCH need PCIe uplink?

Point to Point Links

Know your AMC Backplane

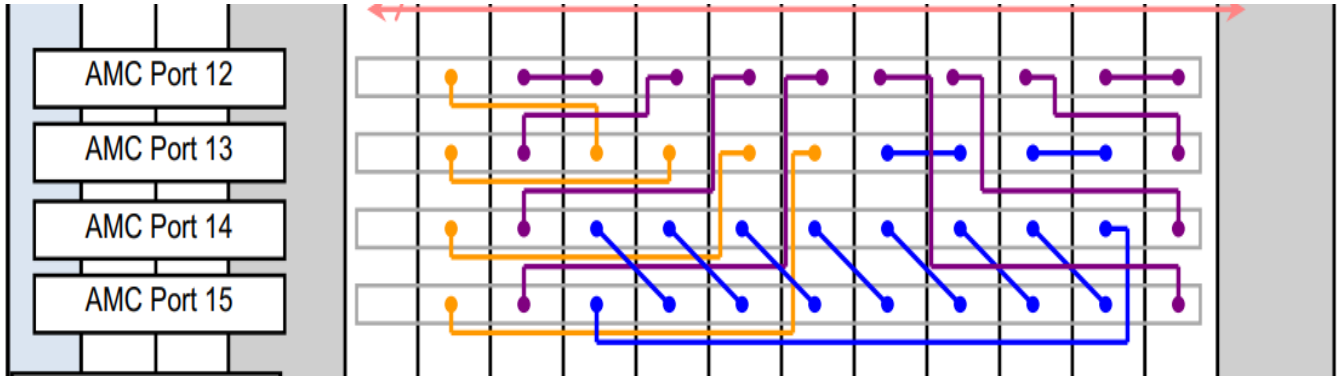
Point to Point Links

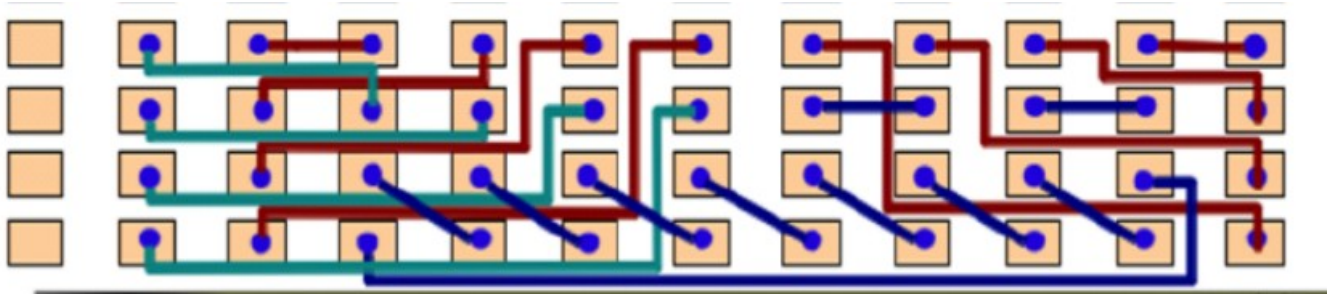
Point to Point links offer direct communication from chip to chip.

Used for data aggregation / fast feedback between boards

These lines are ‘hard wired’. Double check the connectivity before ordering.

EMI (and sometimes radiation) will significantly change the performance of the MGTs of the FPGA. Do a eye scan from the FPGA to look at the eye.





Question #13: Which cards need to communicate with each other at what speeds?

Know your AMC Backplane

Examples of P2P Links

Use Case Example:

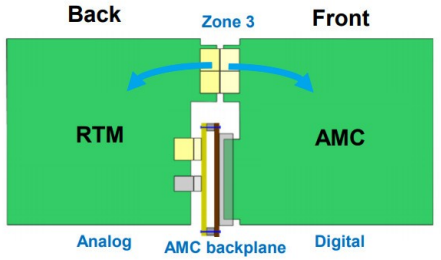
Data aggregation on point-to-point links on Europan-XFEL LLRF Crates:

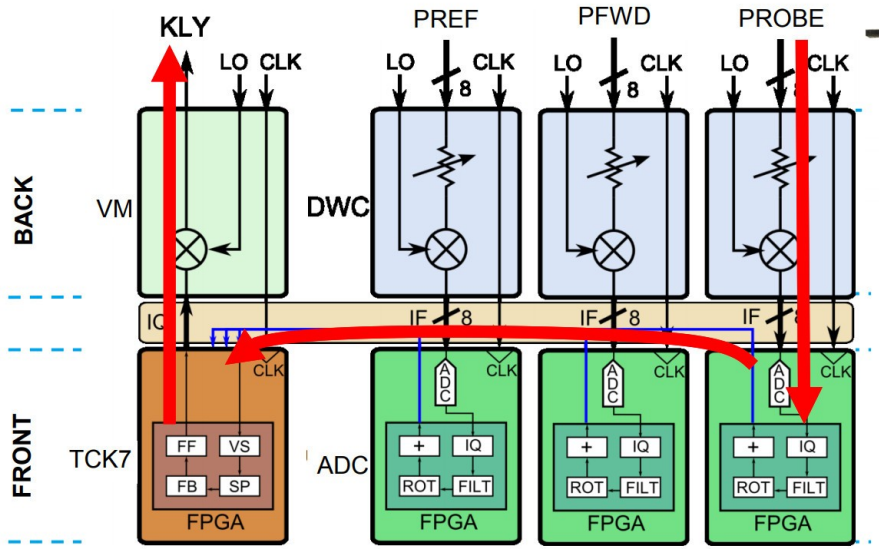
Probe + Forward + Reflected signals of 16 cavities gets send to main controller board.

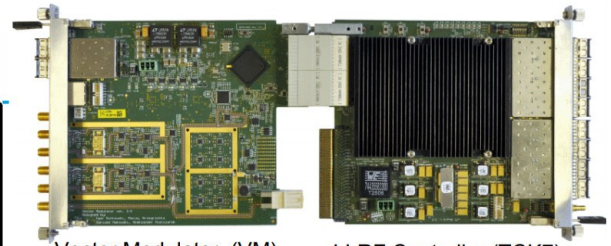
Some numbers:
6.25Gbps link rate
Sending 11x32 bits payload packet
End to End latency: ~344ns

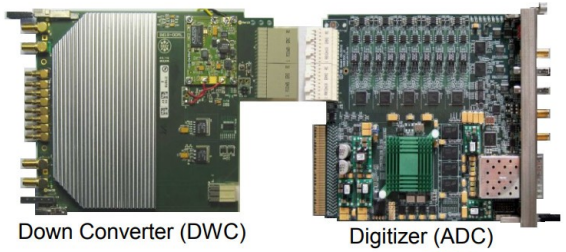
Higher data rates with fully occupied crates are harder to achieve because of big EMI issues.

- AMC: Advanced Mezzanine Card
- RTM: Rear Transition Module
- 12 slots, hot swap
- Redundant power supply









Julien Branlard | LLRF installation for the European XFEL | 7.12.2016 | Page 6

MLVDS

MLVDS

- Ports 17-20 Can be used to forward clocks, triggers and interlock to all other cards on the crate.
- Mesh Topology (excluding MCH)
- Multipoint LVDS is used in MicroTCA for communication between cards. On eac individual line one card (application specific) acts as a driver, other cards can be configured as receivers.
- Wired OR is also possible in MLVDS - more than one card can drive the same line (with the same polarity)

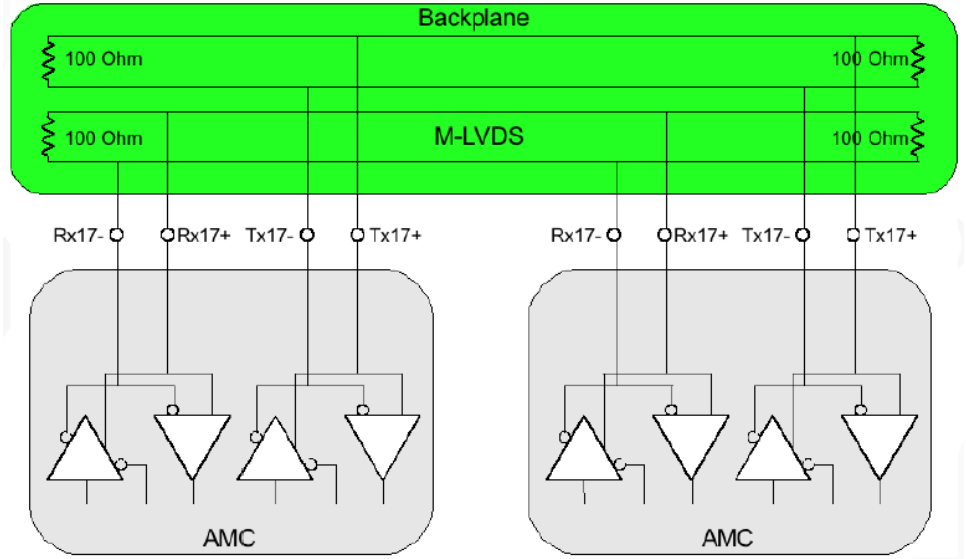


Figure 6-4: M-LVDS transceiver shown for port 17

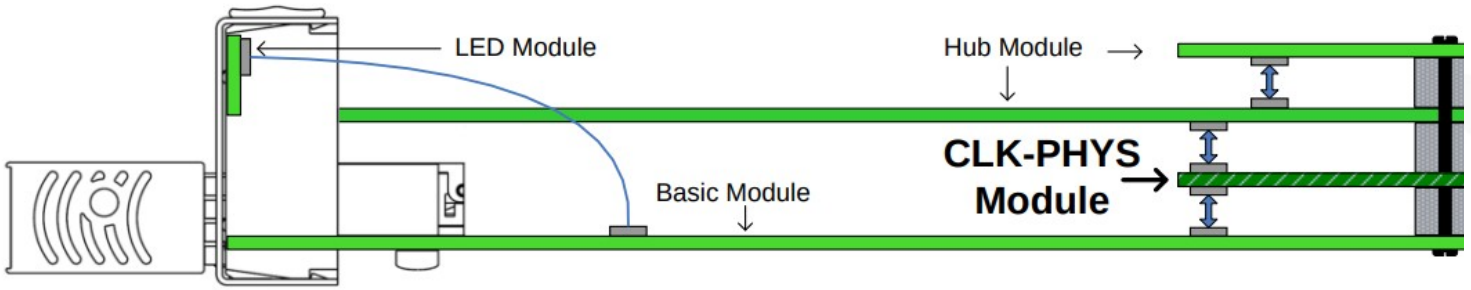
Table 6-1: Example usage of the 8 bus lines for triggers, interlocks and clocks

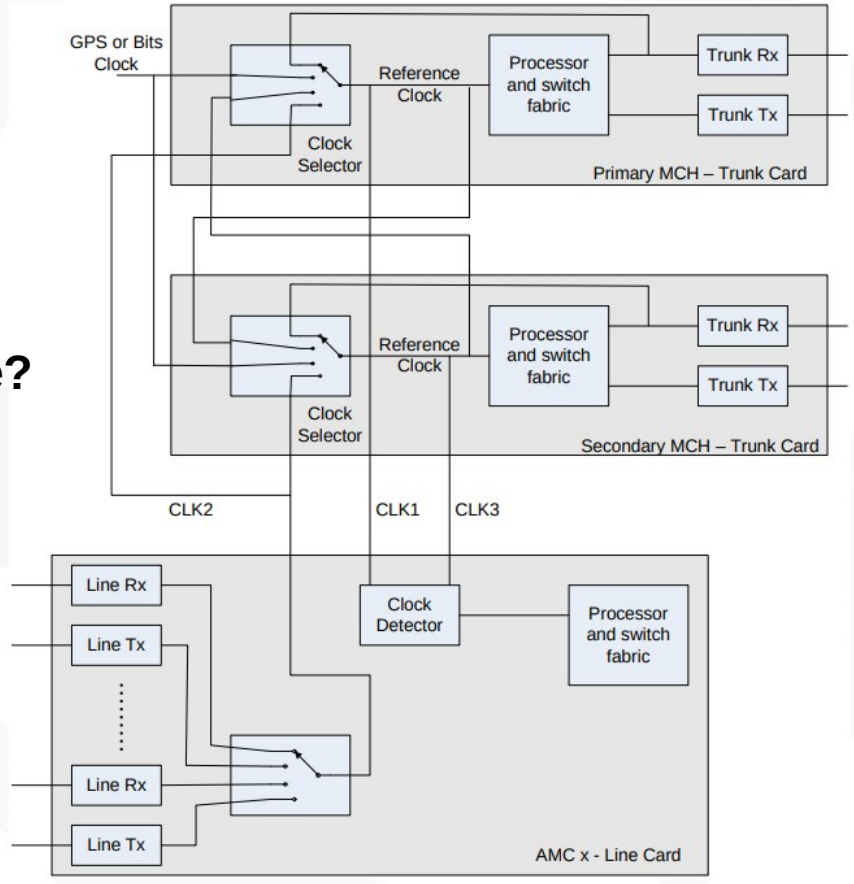
AMC Port	Name	Description	Usage
Rx17	TrigStart	Start sampling data	Triggers
Tx17	TrigEnd	Stop sampling data	
Rx18	TrigReadOut	Start data transfer to CPU	
Tx18	ClkAux	Low performance clock	
Rx19	Reset	Reset of counter, dividers	
Tx19	Interlock 0	Interlock line 0	3 interlocks to provide 2 out of 3 redundancy
Rx20	Interlock 1	Interlock line 1	
Tx20	Interlock 2	Interlock line 2	

Clock Distribution inside MicroTCA

- MCH can be used to distribute clocks inside the MicroTCA crate
- TCLKA/B/C/D and FCLK can be generated

Question #14: How should be the clocking distribution inside the crate?





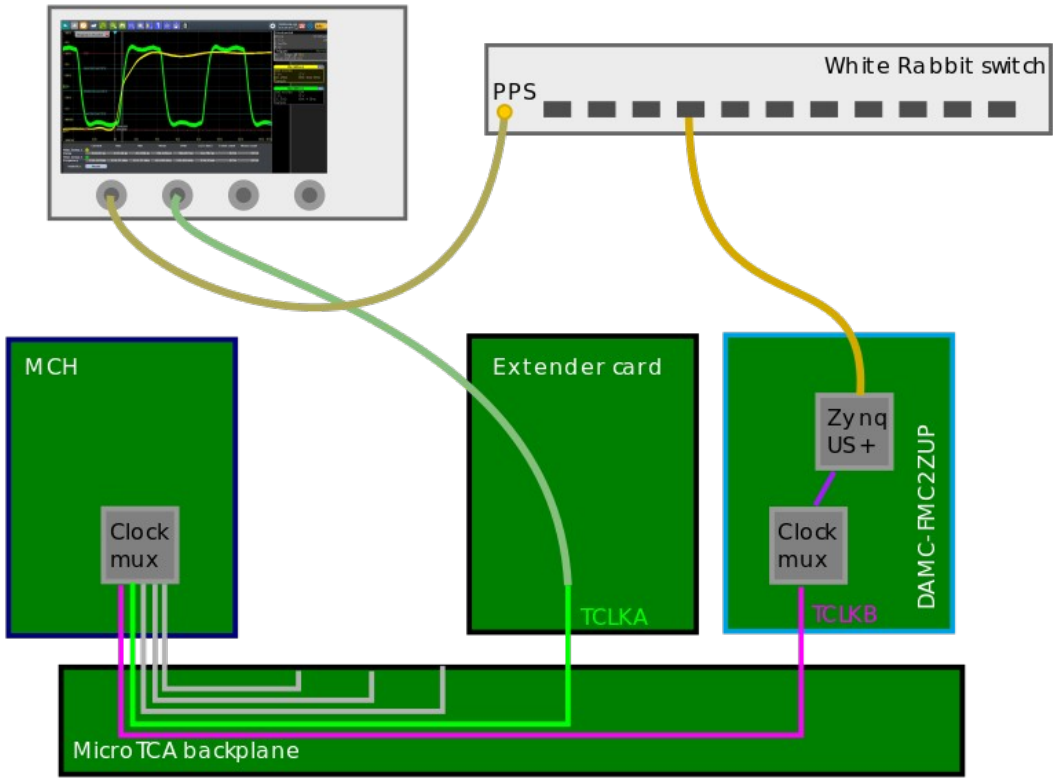
Clock Distribution on Backplane

For digitizers with high input frequencies, jitter of the ADC clock becomes important.

The amount of clock jitter will set the maximum SNR that you can achieve for a given input frequency

Measurement done at MicroTCA Technology Lab.
(courtesy of Jan Marjanovic)

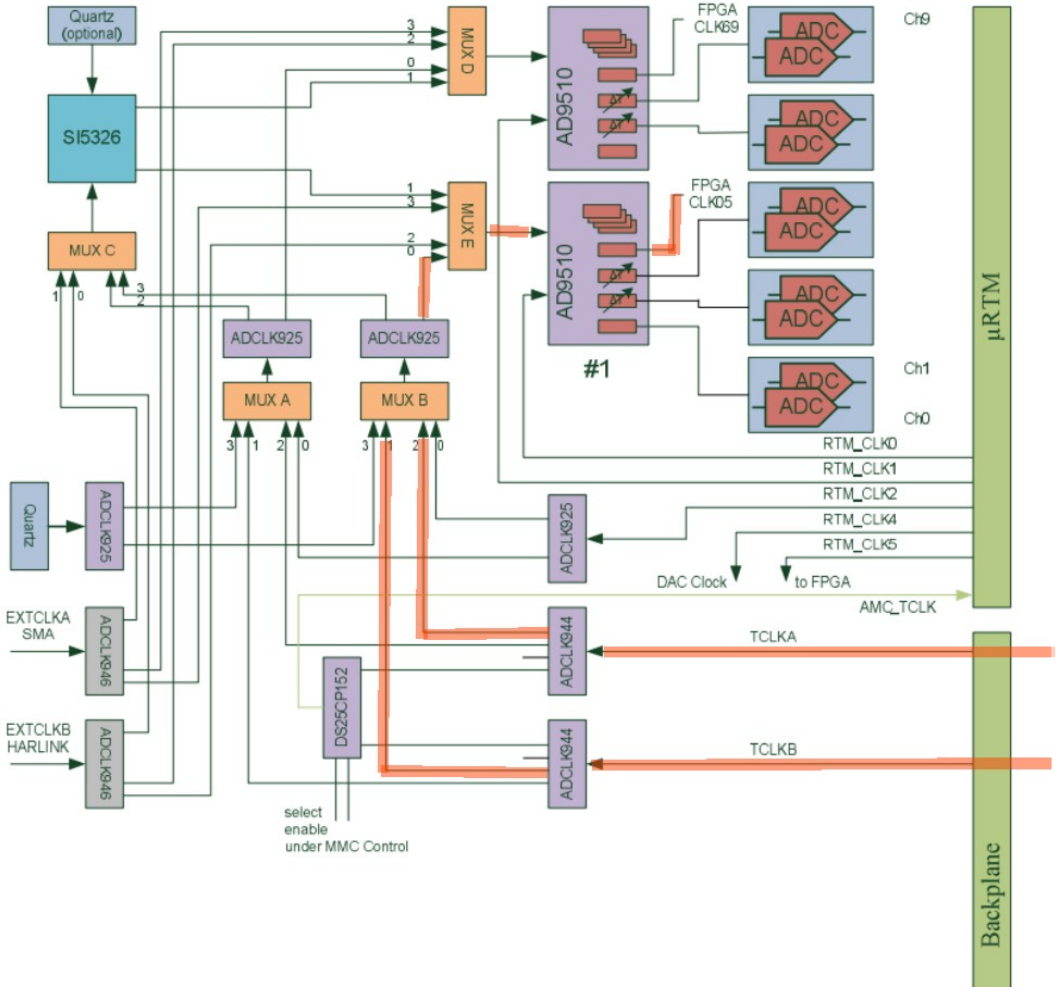
- Using DAMC-FMC2ZUP to recover clock coming from White Rabbit switch.
- AMC forwads the recovered clock to TCLKB,
- MCH loopsback the clock to TCLKA

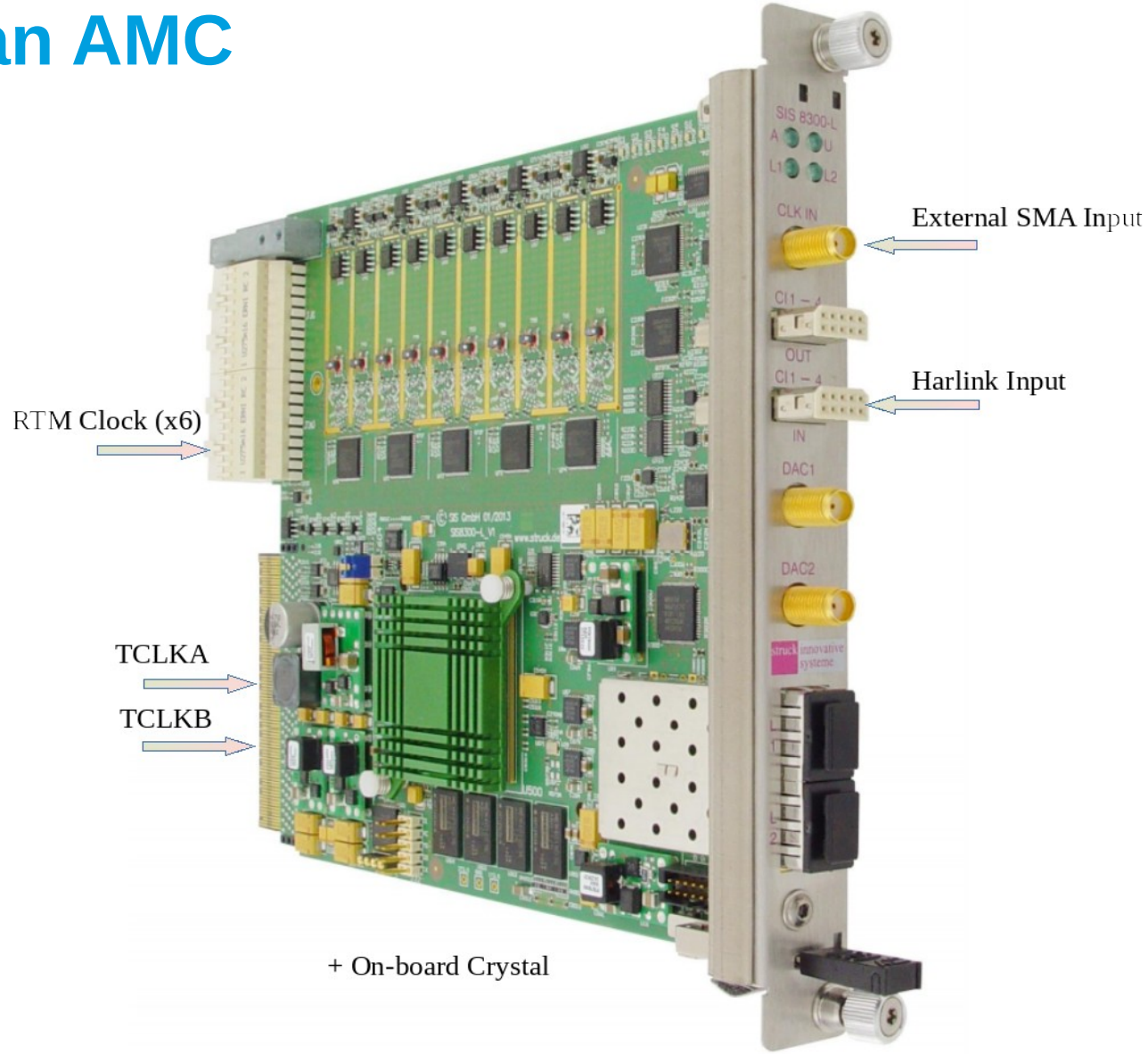


Measurement time: 1.5h
Jitter → 16ps

Clocking Distribution inside an AMC

Case in point: SIS8300-L2 from Struck GmbH

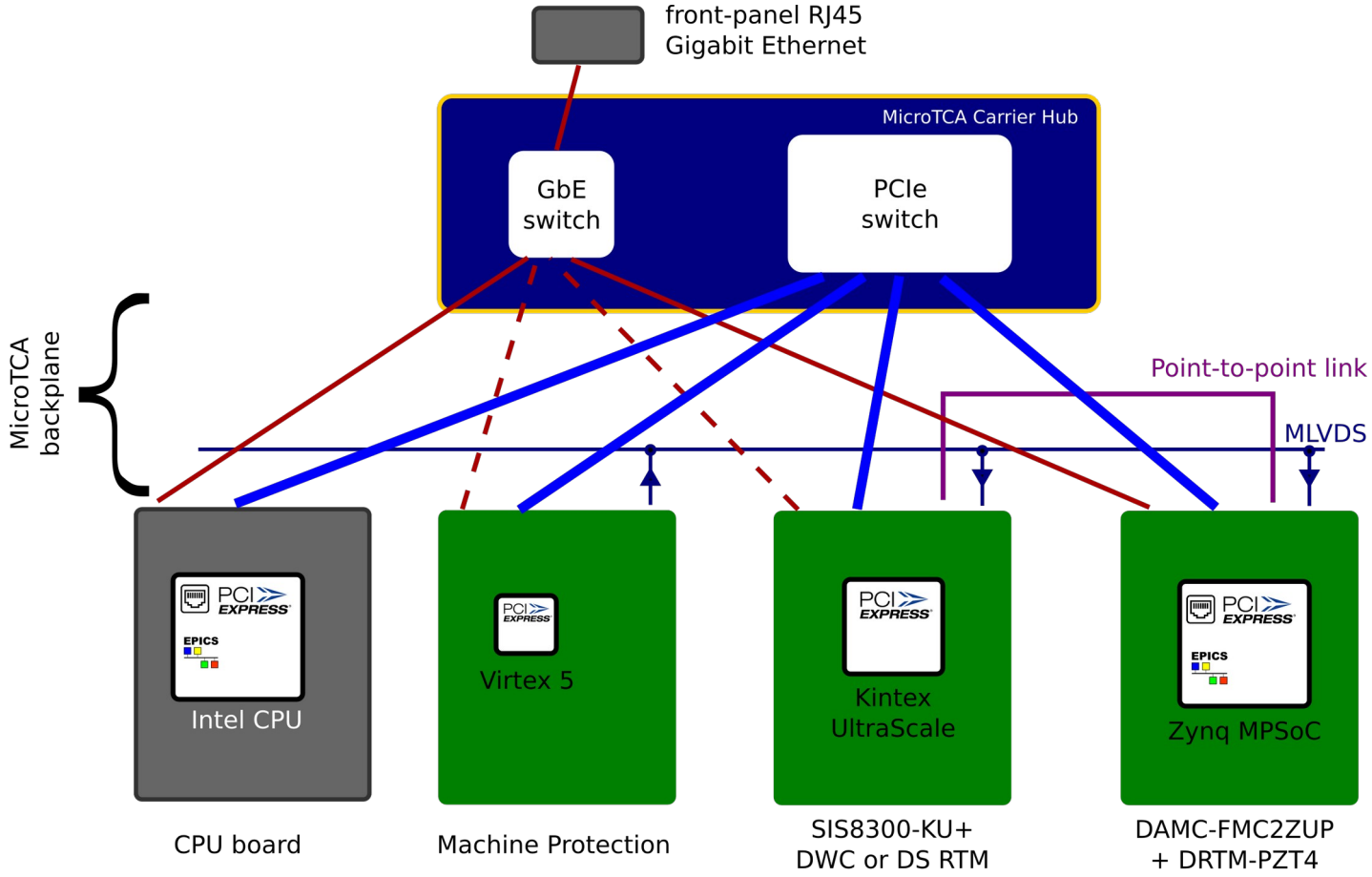




Data Transfer inside Crate

Question #14: How does the data flow looks like inside the crate

- Example: Single cavity LLRF controller for superconducting cavity with resonance controller + machine protection system
- Point-to-Point links used to send cavity detuning information for fast feedback on piezos
- MLVDS lanes used for interlocks
- GigE is used for control system
- PCIe is used for Data Acquisition



Summary

Critical Points

- Number of AMC cards
- AMC Cards capabilities (AMC.1, AMC.2 ...)
- RF Backplane?
- Redudancy on MCH/Power Module?
- Zone3 Compatability/Limitations
- PCIe lanes configuration
- Usage of PCIe Uplink?
- Point to Point connectivity of a backplane
- MLVDS lanes configuration
- ...

感谢您的关注

Contact

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