



MicroTCA.4 in LLRF of BEPCII and HEPS

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Outline

- 1. MicroTCA.4 Background
- 2. LLRF of BEPCII Linac upgrade
- 3. LLRF of HEPS Linac
- 4. interoperability



1、MicroTCA.4 Background

before 2019:

- MicroTCA.4 based LLRF started since ~2014;
- C-ADS Injector;
- BEPCII Linac SHB upgrade;

C-ADS (2014-2017) Injector I - CM1/CM2 C-ADS (2016-2018) - CM4



BEPCII Linac (2017-)
Sub-harmonic Bunchers

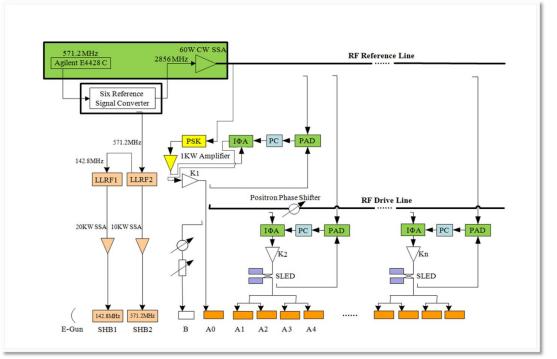








- BEPCII: Beijing E-/E+ collider;
- 200m, 2856MHz/2.5GeV, 4us pulsed Linac
- 20 sets high power microwave source and accelerating tubes;
- 20 old phasing system (2006-)











- Y19-20 upgrade 1
- Y20-21 upgrade 5

2019.10

Signal dist.

Power meter

Monior

MicroTCA Crate

RF front-end

1kW SSA

UPS



□Ref: 2856MHz;

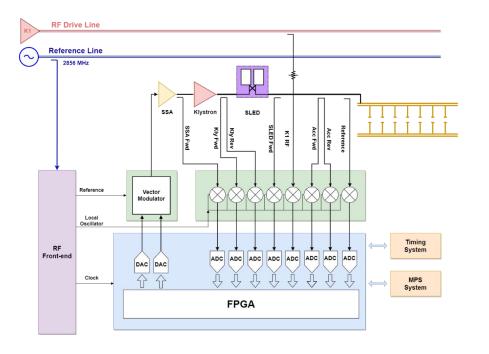
□Crate: ELMA-9U, PS: Wiener-1kW;

□MCH/CPU: NAT MCH-PHY80/RTM;

□SIS8300L2/DWC8VM1 from Struck;

□8 ADC; 2 DAC;

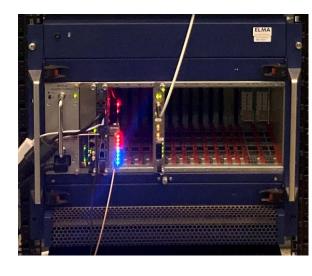
Timing: trigger through backplane;

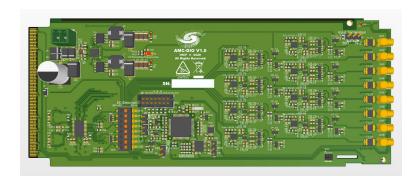




AMC board

- □ Digital IO board for 8 channels timing trigger fanout;
- MMC took Samway solution;



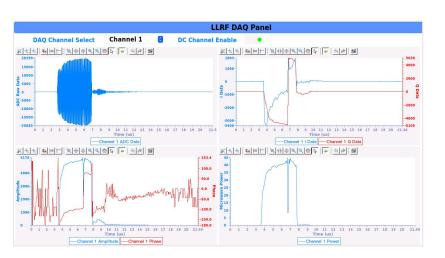


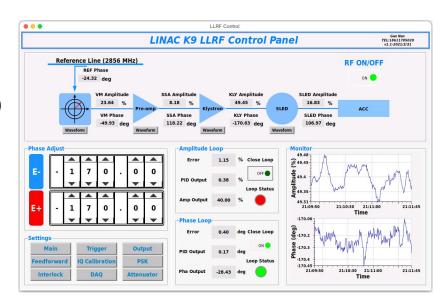


Courtesy by Gan Nan

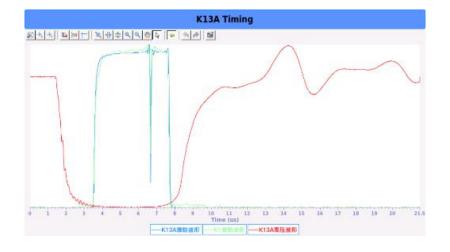


- downconvert 6 microwave signals AC coupled;
- ■1 Voltage/1 Current DC coupled ;
- monitoring high voltage and current of modulator:1) record perveance, 2) timing between HV and MW digitally;
- □digital PSK;
- □support E+/E- switch;
- □adjustable trigger of SSA/Mod/PSK;
- protection of klystron by reverse power;
- feedforward;
- □I/Q cali
- □interlock





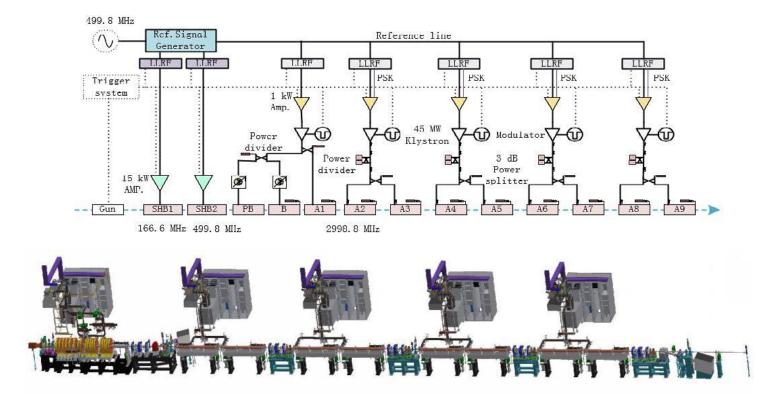
short-term stability: amp:1%(p-p), phase:0.5deg(pp)







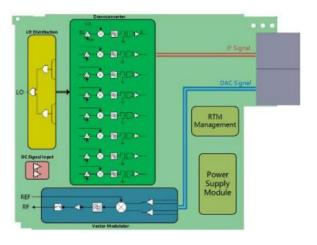
- 5 sets 2998.8MHz pulsed klyston and accelerating tubes; ~BEPCII Linac;
- □ 166.6MHz Sub Harmonic Buncher SHB1 and 499.8MHz SHB2;

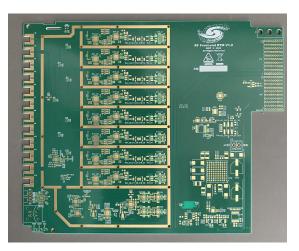




- Downconverter RTM board
- □ Input bandwidth: 300MHz-6GHz;
- 8 ADCs; 2 DACs;
- □ Input: RF, LO, ;

preliminary under full test







Courtesy by Gan Nan



Direct sampling RTM board Input bandwidth: 0-650MHz; **□** 99.96MHz clock jitter: 98fs (10Hz-10MHz) ; **□** 6 ADC , 2DAC ; Reference Line □ for 2 SHB bunchers LLRF; **FPGA**

Courtesy by Gan Nan





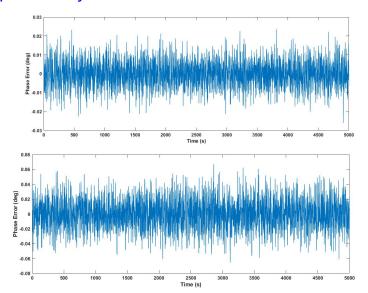


Courtesy by Gan Nan

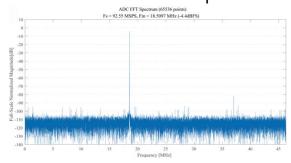
preliminary tested with Struck SIS8300L2

166MHz DS P-P Err $< \pm 0.02^{\circ}$ RMS Err = 0.007°

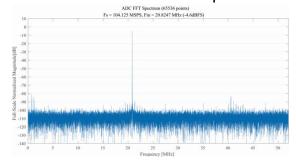
499MHz DS P-P Err $< \pm 0.07^{\circ}$ RMS Err = 0.019°



166.6MHz direct sampled



499.8MHz direct sampled

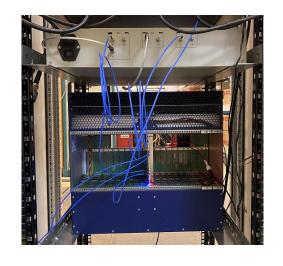


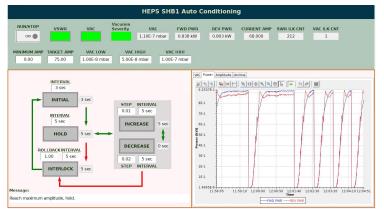
SFDR better than 80dB



DS RTM on HEPS SHB TB @166.6/499.8MHz

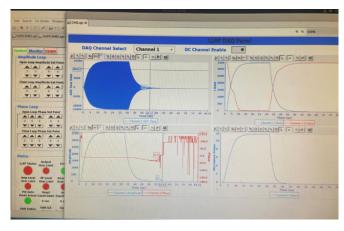
DWC RTM on HEPS TB @2998.8MHz





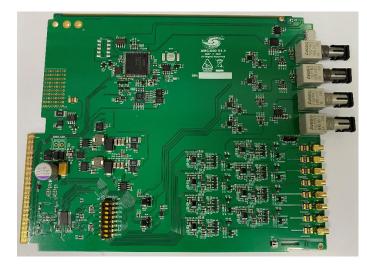








- □ Timing/interlock fanout board
- using openmmc;
- work well with NAT MCH;
- 8 electro-IOs & 4 optical-IOs to backplane MLVDS



MMC with basic functions based on OpenMMC FRU, HOTSWAP, PAYLOAD, SDR(TEMP, VOLTAGE, CURRENT), GPIO

#	SDRType	Sensor I	Entity	Inst	Value		State	Name
						-		
-	MDevLoc		0xc1	0x64				DIO 1.0
1	Compact	0xf2	0xc1	0x64	0x01			HOTSWAP AMC
2	Full	Voltage	0xc1	0x64	3.280	٧	ok	AMC +3.3V
3	Full	Voltage	0xc1	0x64	4.984	٧	ok	AMC +5.0V
4	Full	Voltage	0xc1	0x64	0.000	٧	<=lnr	RTM +12V
5	Full	Current	0xc1	0x64	1.824	Α	ok	AMC +3.3V Cur
6	Full	Current	0xc1	0x64	0.800	Α	ok	AMC +5.0V Cur
7	Full	Current	0xc1	0x64	0.000	Α	ok	RTM +12V Curr
8	Full	Temp	0xc1	0x64	27.5 (ok	TEMP 1
9	Full	Temp	0xc1	0x64	30.5 (2	ok	TEMP 2
10	Full	Temp	0xc1	0x64	27.5 0		ok	TEMP 3
11	Full	Temp	0xc1	0x64	28.5 (ok	TEMP 4
12	Compact	0xf0	0xc1	0x64	0x10			HS 008 AMC4

```
nat>show fruinfo 8
RU Info for device 8:
             : 0x01 0x00 0x00 0x01 0x07 0x10 0x00 0xe7
Internal Use Area : -
Chassis Info Area : -
                      : at offs=8, len=48
Board Info Area
Manufacturer(05)
                      : IHEP
Board Name(08)
                       : AMC-DIO
Serial Number(10)
                       : DIO-FRU
Product Info Area
                       : at offs=56, len=72
Manufacturer(05)
                       : IHEP
Product Name(08)
                       : AMC DIO
Product Number(08)
                      : DIO-1.0
Part Version(04)
                       : 1.0
Product Serial Number(10): SN:000000
                                      Courtesy by Gan Nan
Asset Tag(12)
                       : Generic FRU
FRU file ID(08)
                      : DIO-FRU
```



- Crates has been produced in China:
- □ ELMA 9U: 5 working on BEPCII Linac
- backplane is provided by ELMA@Germany, others re-design/in-production in China
- first delivery, test with the vendor using our borads;
- basic functions are OK, mechanical, assembling, wiring and engineering need improving in future.





- Crates has been produced in China:
- □ nVent 3U/9U:
- 3U/9U are made in nVent China factory, has been delivered and tested at LLRF and timing systems;

□ basic function OK with other boards; quite the same with the one

made in Europe.





9U tested for HEPS timing system Courtesy by LIU Fang



- Crates has been produced in China:
- Yuanzhong 10U: 1.5kW integrated PS
- work at BEPCII Linac over 6 months, function is OK.
- an optimized version is under test

LI Rui, MicroTCA system engineering, developing and domestic production. This workshop









■ MicroTCA.4 based LLRF system running:

x6 runing on BEPCII Linac

3 runing on testbench for HPMW conditioning and test









1 running 1 running for SC on for RefLine PAPS test







4. interoperability



interoperability

□ Vadatech MCH (UTC002):

- abnormal with DESY MMC(Struck), can't power-up;
- MCMC version <V2.8.0/2015 normal with Struck mmc/openmmc





Thank you for your attention!