





Vertexing/Tracking: A Summary

Klaus Dehmelt DESY

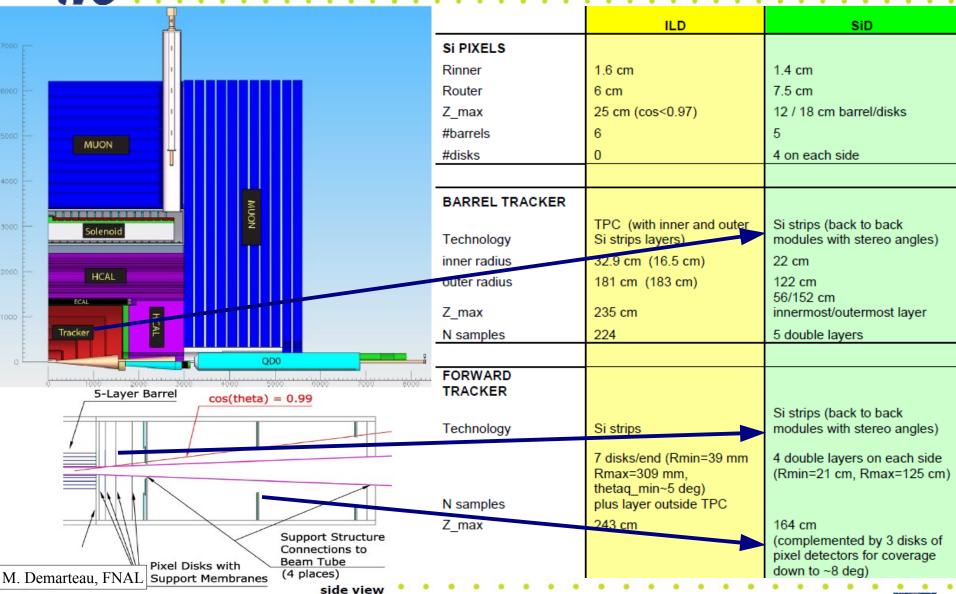
LCWS2010

Beijing, China March 30, 2010



Vertex & Tracking in SiD-ILD

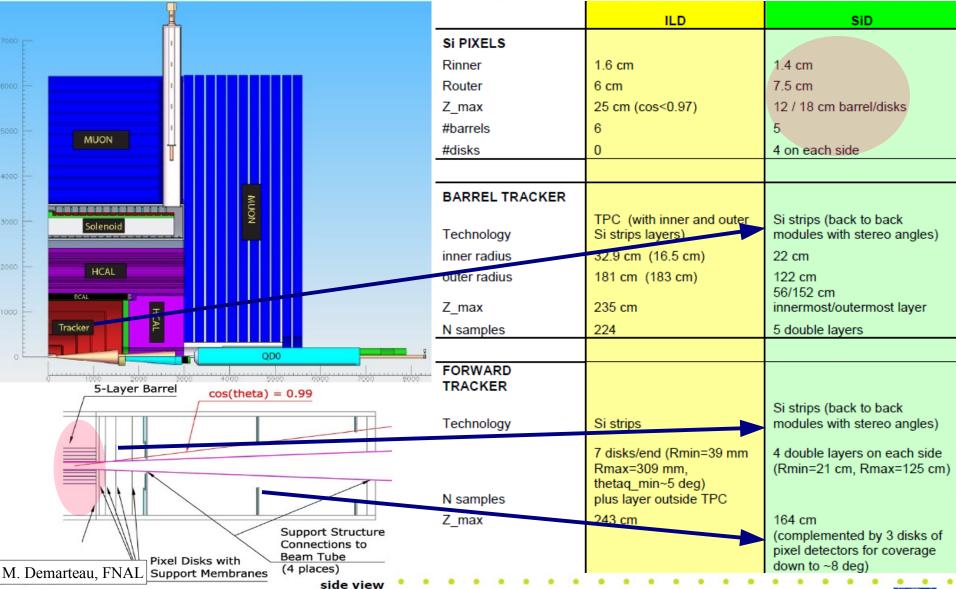






Vertex & Tracking in SiD-ILD

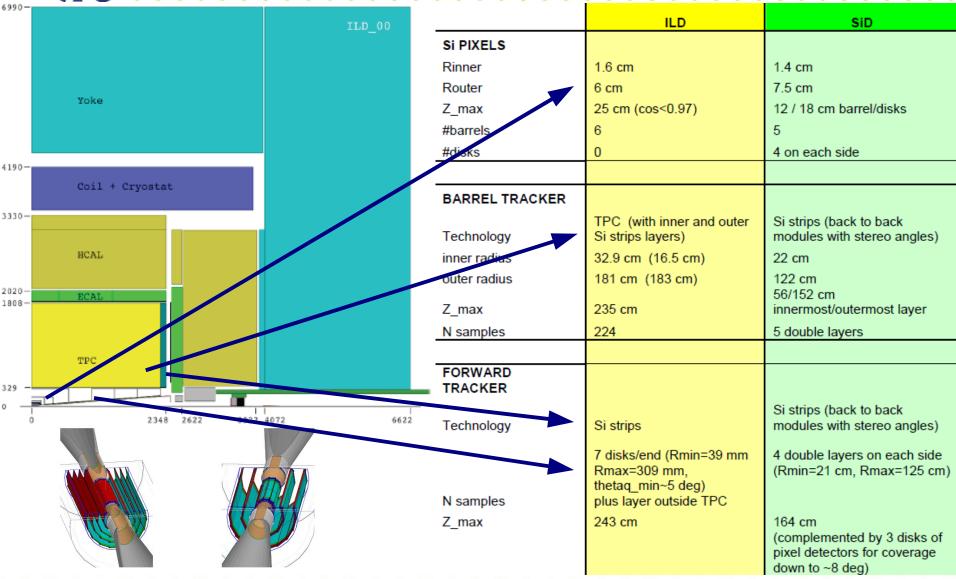






Vertex & Tracking in SiD-ILD







Vertex: Silicon Pixel



Both, SiD and ILD will use Si-pixel technology for vertexing

CPC2

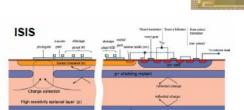
Vertex Detector Sensor Technology

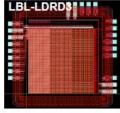


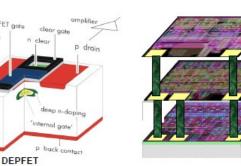
Broad spectrum of sensor technologies are a candidate technology for the ILC vertex detectors

p source

- CCD's
 - Column Parallel (LCFI)
 - ISIS (LCFI)
 - Split Column (SLAC)
- CMOS Active Pixels
 - Mimosa series (Ires)
 - INFN
 - LDRD 1-3 (LBNL)
 - Chronopixel (Oregon/Yale)
- SOI
 - American Semiconductor/FNAL
 - OKI/KEK
- DEPFET (Munich)
- Chronopixel
- 3D Vertical Integration (Fermilab)







SiD

• Sensor technology to be decided:

Chronopix, 3D, DEPFET

- Sensors glued on edges to form cylinders
- Gas cooled, power pulsed, low mass

A. White, UTA



Vertex: Silicon Pixel



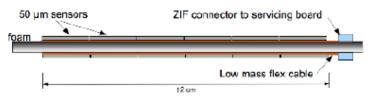
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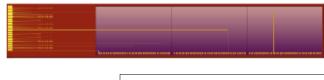
<u>ILD</u>

two designs: in sensor and ladder comb.

MIMOSA/FPCCD/DEPFET/APSEL/3D

- single/double sided
 - 5 / 6=2*3 layers
- mech. ladder
- innermost unsupported





T. Takeshita, Shinshu Univ.

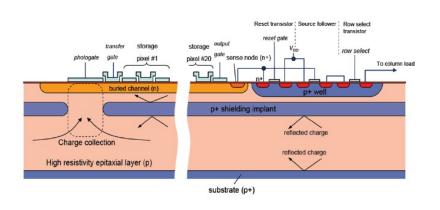


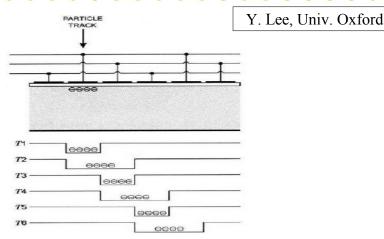


Vertex: ISIS



In-situ Storage Image Sensor





- · Charge is collected under photogate
- Charge is transferred into 20 in-situ storage pixels
- During the quiet time between bunch trains the charge is converted to voltage and read out

Proof-of-principle Device: ISIS1 X-ray Calibration

- Design bugs of ISIS2 to be fixed Charge Transfer Charge Transfer Efficiency
 - buried channel reset transistor
 - resistive polysilicon gate
 - logic of rolling shutter

Readout Time Minimization Full Array Readout

 ISIS3: larger sensor with more compact pixel geometry and data serialization.



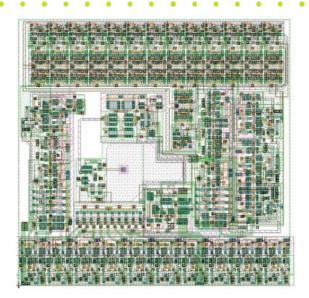




Vertex: Chronopixel



- Chronopixel design provides for single bunch-crossing time stamping
 - When signal exceeds threshold, time stamp provided by 14 bit bus is recorded into pixel memory, and memory pointer is advanced
 - Comparator threshold adjusted for all pixels
- Current design
 - 50x50 um² pixels
 - Two pixel architectures
 - Regular p/n-well design
 - Deep n-well design
 - Detector sensitivity: 10 μV/e
 - eq. to 16 fF
 - Detector noise: 25 e
 - October 2008
 - Design of test boards started at SLAC
 - o June 2009
 - Test boards fabrication. FPGA code development started.
 - o August 2009
 - Debugging and calibration of test boards
 - September 2009
 - Chronopixel chip tests started
 - o February 2010
 - Chronopixel chip tests completed



M. Demarteau, FNAL

N. Sinev, Univ. Oregon

Recorded time tag for each hit



hit assignment to bunch crossing

Chip tests included:

- Noise measurements (threshold scans)
- Power distribution
- Comparator threshold spread
- Fe55 tests
- Leakage currents



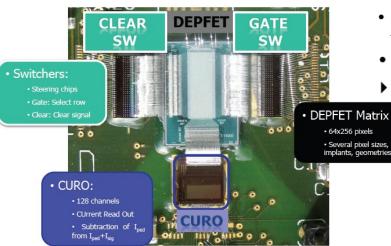




Vertex: DEPFET



F. Simon, MPI&ECU



 PXD5 chips tested in 2009

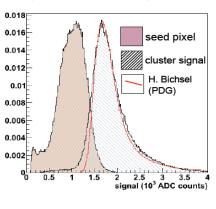
- unthinned devices: Silicon thickness 450 µm
- Production of thinned sensors (thickness 50 μm) in progress: PXD6

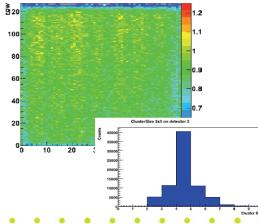
Test Beam Results: Resolution & MC Validation

- High spatial resolution for 24 x 24 μ m² pixels: $\sigma_x = 1.3 \pm 0.2 \ \mu$ m, $\sigma_y = 1.2 \pm 0.1 \ \mu$ m
- Simulation of detector response in good shape

Results: Test Beam 2008

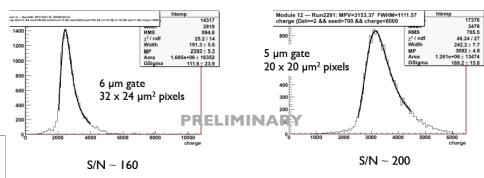
 Excellent performance observed: Clear detection of minimum ionizing particles, uniform response over the active area





Further Improvement: Test Beam 2009

- Improved clearing through capacitatively coupled clear gate
- Study of different lengths for the gate (shorter gate ⇒ higher gain)



Excellent signal to noise ratio for thick sensors: Internal amplification in the DEPFET sensor!



Vertex: Monolithic Active Pixel Sensor



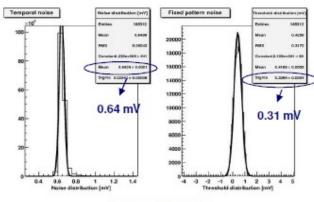
MIMOSA26 is a reticule size MAPS with binary output, 10 k images / s

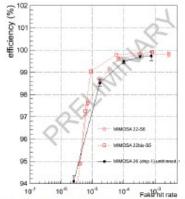
C. Hu-Guo, IPHC

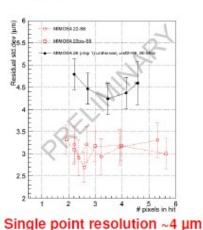
- Pixel array: 1152 x 576, 18.4 μm pitch
- Architecture:
 - Pixel (Amp+CDS) array organised in // columns r.o. in the rolling shutter mode
 - 1152 ADC, a 1-bit ADC (discriminator) / column
 - Integrated zero suppression logic
 - Remote and programmable



Lab. and beam tests: 62 chips tested, yield ~75%







ENC ~ 13-14 e-

- Efficiency 99.5% for fake rate 10-4
- MIMOSA26 can be operated at a high readout speed Clock frequency: from 80 MHz_{tvp.} (~110 μs) up to 110 MHz (~80 μs)
- → MIMOSA26: design base line for STAR Vx upgrade, CBM MVD Its performances are close to the ILD vertex detector specifications



Vertex: PLUME/SERWIETE



PLUME Pixelated Ladder with Ultra-low Material Embedding

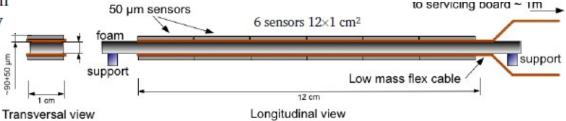
N. Chon-Sen, IPHC

Current concept:

- 6 × MIMOSA-26 thinned down to 50 μm
- Kapton-metal flex cable (SMD components on flex for decoupling/termination)
- Silicon carbide foam (8% density) stiffener, 2mm thickness
- Wire bonding for flex outer world connection
- Digital readout + servicing board ~ 1 m away

Baseline:

- MIMOSA-26 CMOS sensor (developed for EUDET-BT)
- Power pulsing (≤ 200ms period, ~1/50 duty cycle) and power dissipation (100mW/cm²)
- Air cooling



SERWIETE SEnsor Raw Wrapped In an Extra-Thin Enveloppe (HP2, EU-FP7)

Goals:

- to achieve a sensor assembly mounted on flex and wrapped in polymerised film with <0.15 % X₀ for 1 unsupported layer (sensors flex cable film)
- to evaluate the possibility of mounting supportless ladder on cylindrical surface like beam pipe (used as mechanical support).
 Proof of principle expected in 2012

Working program:

- prototype Nr. 1 (2010) made of 1 analog sensor:
 MIMOSA-18 (analog output, ~4 ms @16MHz)
- prototype Nr. 2 (2011) made of 3 digital sensors :
 MIMOSA-26 (binary output, ~100 µs @80MHz)



Fully functional microprocessor chip in flexible plastic envelope. Courtesy of Piet De Moor, IMEC company, Belgium



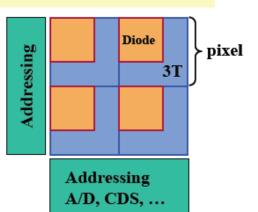
Vertex: 3-D Vertical Integration



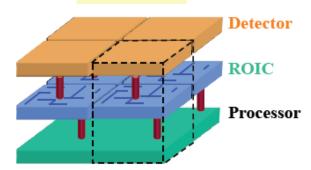
M. Demarteau, FNAL

- "Conventional MAPS"
 - Pixel electronics and detectors share area
 - Fill factor loss
 - Co-optimized fabrication
 - Control and support electronics placed outside of imaging area
- 3D Vertical Integrated System
 - Fully active sensor area
 - Independent control of substrate materials for each of the tiers
 - Fabrication optimized by layer function
 - Local data processing
 - Increased circuit density due to multiple tiers of electronics
 - 4-side abuttable
- Technology driven by industry
 - Reduce R, L, C for higher speed
 - Reduce chip I/O pads
 - Provide increased functionality
 - Reduce interconnect power, crosstalk

Conventional MAPS



3-D Pixel



Fermilab started to actively pursue the 3D technology, initially with MIT Lincoln Laboratories (MIT-LL), who had developed the technology that enables 3D integration





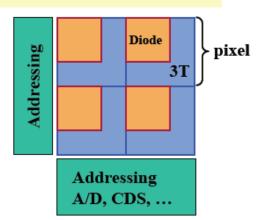
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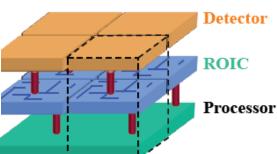
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- 3D technology driven by industry; started an initiative with one of the leaders in 3D technology, Tezzaron (Naperville), willing to accept MPW runs

Conventional MAPS



3-D Pixel



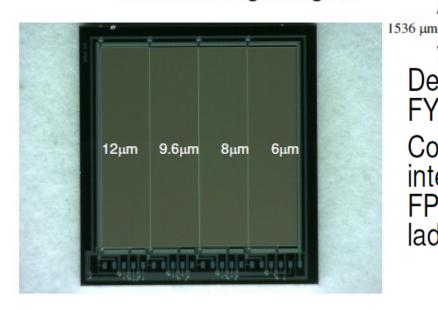


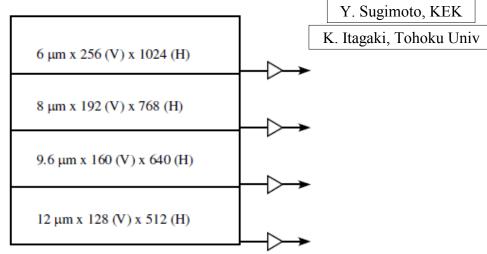
Vertex: FPCCD



Fine Pixel CCD

- FPCCD in 2010
 - Chip size: 6.1mm (image area)
 - Pixel size: 12, 9.6, 8, and 6 μm
 - Reduced CR of Al line for horizontal register gate





Detailed study on the FPCCD will be done in FY2010-2011

Cooling system using 2-phase CO2 is an interesting option for FPCCD VTX because FPCCD VTX has main heat source only at the ladder ends

Readout ASIC for FPCCD developed Required performance regarding power consumption, readout rate, noise level has been accomplished



Spanish Efforts in Vertex/Tracking



A. Ruiz-Jimeno, IFCA

 DEPFET (good resolution and sensitivity, low power consumption, low material budget, good Signal over Noise)

□ Thin active pixels, readout by TIMEPIX (time stamping capable, thinning needed on the sensor and the chip, power cycling to be studied)

 CMOS Single Photon APD's (high gain, simple readout electronics, so low power consumption, extremely fast response)

□ Others (contacts with MAPS, FPCCD)

Sensor developments for the endcap tracker

Studies of technologies for the vertex

- □ More relaxed conditions of material budget (~0.25 % X0 first three disks, ~0.65 % X0 last four disks), spatial resolution of 7 μm in Rφ. Very thin (150-200 μm thick) silicon microstrip sensors, pitch of ~ 40 μm. Low power FEE
- Both pixel and micro-strip silicon technologies are being considered
- Characterization of the sensors in the lab
- Edgeless studies to reduce dead zones, removal of pitch adapter to increase signal over noise
- Readout electronics, connectivity
- Integration, mechanical and thermal studies
- Alignment sensors, FOS sensors
- Test beams







Spanish Efforts in Vertex/Tracking



25 % X0

n thick) power

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Others

LongTerm: participate in the design and construction of the forward tracker and vertex detectors of the FLC

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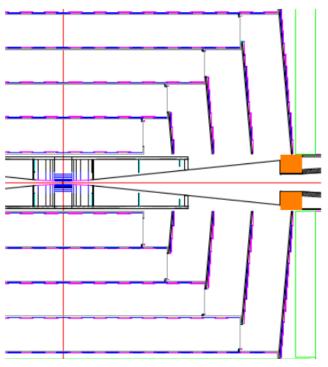


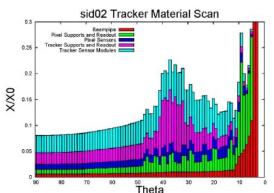




Tracking: SiD → All Si-Tracker







Five-layer Si-strip main tracker

- Five barrels \rightarrow ϕ -measurement
- Four double disks per end \rightarrow r- ϕ -measurement
- Support by CF cylinders
- Barrel-disk strucure should have no more than $0.8\%X_0$ per layer
- Outer tracker and vertex detector are considered to be <u>one</u> integrated detector

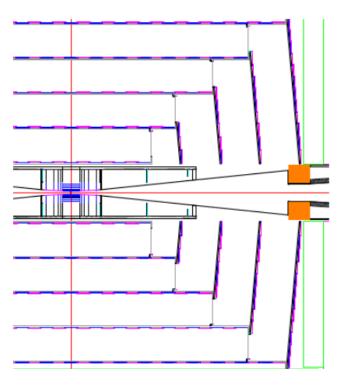
Material budget $X/X_0 < 0.2$

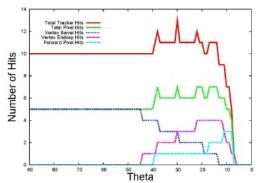




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Uniform coverage of at least 10 hits per track down to small angles

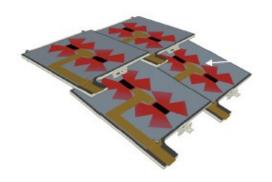


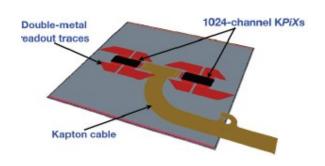


Tracking: SiD → All Si-Tracker



Sensors and readout: Modular low mass sensors tile CF cylinders

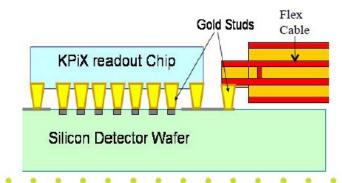




~10 cm x 10 cm; 320 μ m thick; 25 μ m sense pitch; 50 μ m readout (prototype fabricated); S/N > 20: <5 μ m hit resolution Bump bonded readout with 2 KPiX chip; no hybrid

KPiX measures amplitude and bunch # in ILC train, up to 4 measurements per train Pulsed Power: 20 μ W/channel avg; ~600 W for 30 M channels; gas cooling SILC is revisiting this design applying some of its new ideas and advances

kPix readout ASIC Flexible readout cable

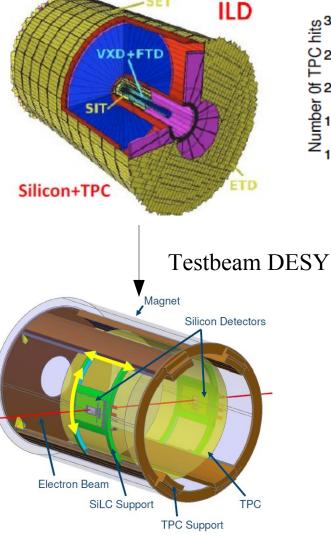


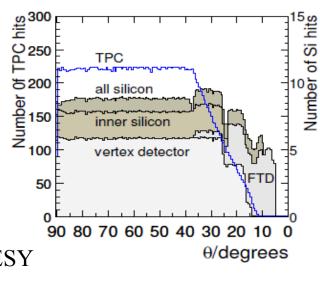
A. Savoye-Navarro, Univ. PMC

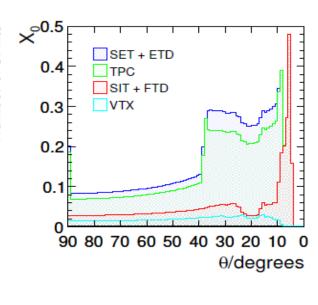












Total #ch: 10⁷ for SIT+SET+2 x ETD Total area: 180 m2 for SIT+SET+2 x ETD 5k modules

A. Savoye-Navarro, Univ. PMC



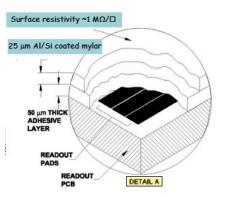


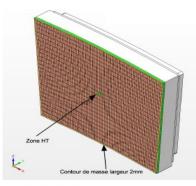
IC Tracking: ILD → Hybrid-Tracker



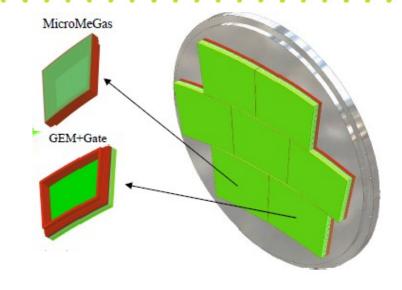
Large Prototype test beam DESY

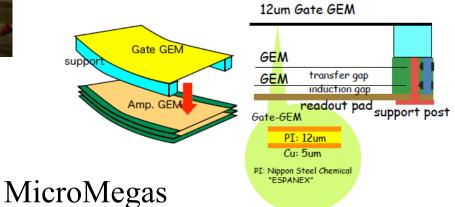






Detector side





- GEM-gate device
 - 12 µm thick PI (Nippon Steel Chamical "ESPANEX")
 - Hole: 90 μ m φ , 140 μ m pitch

K. Ikematsu, KEK

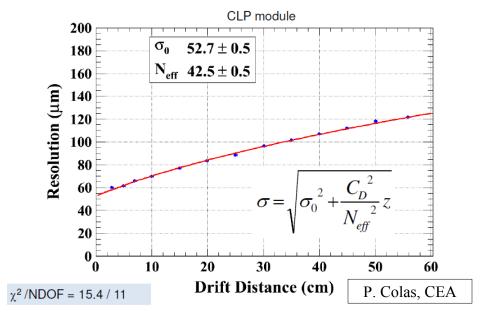




Tracking: ILD → Hybrid-Tracker



MicroMegas Resolution vs Drift Distance

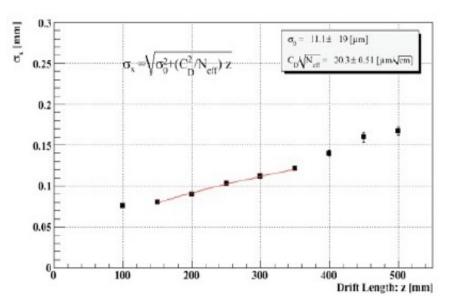


A first measurement z resolution for Micromegas with charge dispersion readout:

$$\sigma_0(z) \sim 550 \ \mu m$$
 (fast gas, $v_{Drift} = 73 \ \mu m/ns$) $\sigma_0(z) \sim 100 \ \mu m$ (slow gas, $v_{Drift} = 25 \ \mu m/ns$)

M. Dixit, TRIUMF/Carleton Univ.

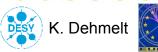
GEM



GEM-gate was not ready last year!

- Metal posts facing drift volume produced local distortion...
- TPC moving stage was not available last year!
 - Displacing TPC in PCMAG for z-scan introduced different B field for each drift...

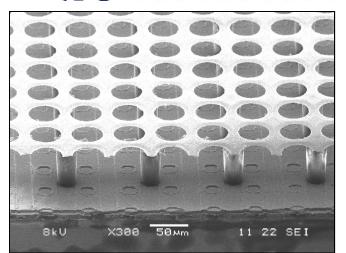
K. Ikematsu, KEK





Tracking: ILD → Hybrid-Tracker





Full post-processing of a TimePix Timepix chip + SiProt + Ingrid LP module with 8 Timepix+Ingrid chips in preparation. Readout working with 8 'naked'

chips.

Timepix chip:

- 256x256 pixels
- pixel: 55x55 μm²
- active surface: 14x14 mm²

J. Timmermans, NIKHEF

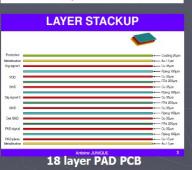
P. Colas, CEA

current LP1 endolate.

Compares to 18.87 kg aluminum for the

2009-03-04, reported on design of the hybrid (aluminum/carbon fiber) design: 7.35 kg Aluminum, 1.29 kg carbon, for LP1, 0.072 X₀. T. Matsuda, KEK

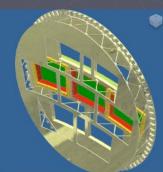
Mass is currently 12kg, but will be reduced to about 8 kg after thinning the uninstrumented areas.















SiLC



Plenty of Sensor-activities:

- HPK sensors for alignment
- Edgeless strip sensors
 - Planar
 - SOI like
- 3-D based technology
- Direct connection sensors-FEE
- Sensors w/ integrated pitch adapters

A. Savoye-Navarro, Univ. PMC

ELECTRONICS ROADMAP

- Go to 256 channels
- ➤ Go to deeper DSM when mature (90 or 65 nm)
- > Thinning (50 μm)
- > Direct connection chip onto sensor
- Design/strategy of the DAQ architecture on detector:
 - => synchronization
 - => data processing, compacting & buffering
 - => cabling
- Linking with general DAQ
- ➤ Adapting FE to CLIC cycle
- Bunch tagging at CLIC
- > Pursue developing TOT alternative





Power Distribution



```
S. Dhawan, Yale Univ.
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CMS ECAL: 5 Oodles (50 Kamps).

Power Supply output = 315 KW

Power loss in Leads to SM = 100 KW

Power loss in Regulator Card = 90 KW

Power Delivered @ 2.5 V = 125 KW
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# of Power Supplies ~ 700
# of ST LDO Chips = 35 K LHC Radiation Hard made by ST Microelectronics
# of LVR Cards = 3.1 K.

Yale: Designed, built, burn-in and Tested.
```

Q: Is there a better way to distribute power, in high radiation environment, in magnetic field ~ 4T, load w/ 1V and kA, feed high voltage and convert, w/ commercial technologies

- DC/DC (Buck) Converters are potential solutions for these needs.
- The environment requires that these converters operate in high radiation environments and high magnetic fields at high switching frequencies in a small size/mass package.
- Target technologies for the switches are radiation hard GaN and 0.25 μm LDMOS. High frequency controllers driving small sized nonmagnetic/air core inductors are also required.
- Many of these components have been tested and now need integration to produce a working prototype. This is the next step in our R&D program.





Conclusion



Vertex

- Very active R&D program underway
- Many pixel R&D groups, technology choice to be made
- Both, SiD and ILD are within pixel R&D groups
- Many improvements, many new ideas
- Extensive test beam activities

Tracking

- Two different concepts: SiD as full Si-tracker, ILD as hybrid-tracker
- SiD-Tracker/SiLC and LCTPC/SiLC as very active collaborative efforts
- Extensive test beam activities
- Progress towards final detectors

Vertex and tracking are working extensively towards DBD, but there is no time to take a rest

