Data Acquisition & GDN
- not a summary

- **Examples from the detector sessions**
- **GDN ?**
- **Summary/Outlook**

G. Eckerlin
DESY
LCWS 2010
Beijing, March 30, 2010

TPC with AFTER readout

The Saclay-Carleton 7-module project

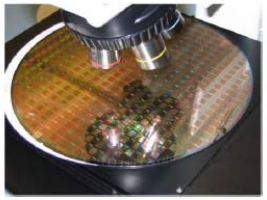
D. Attié, P. Baron, D. Calvet, C. Coquelet, E. Delagnes, M. Dixit, A. Le Coguie, R. Joannes, S. Lhénoret, I. Mandjavidze, M. Riallot, S. Turnbull, Yun-Ha Shin, W. Wang, E. Zonca

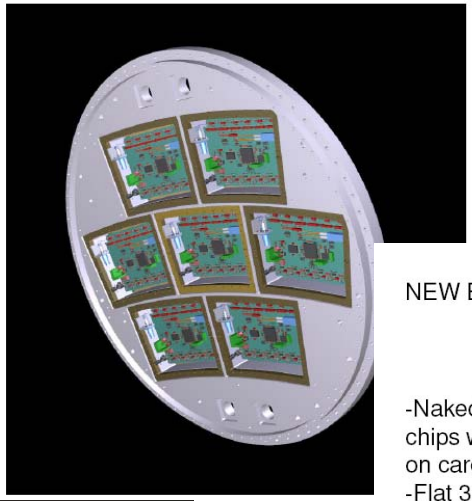
P. Colas

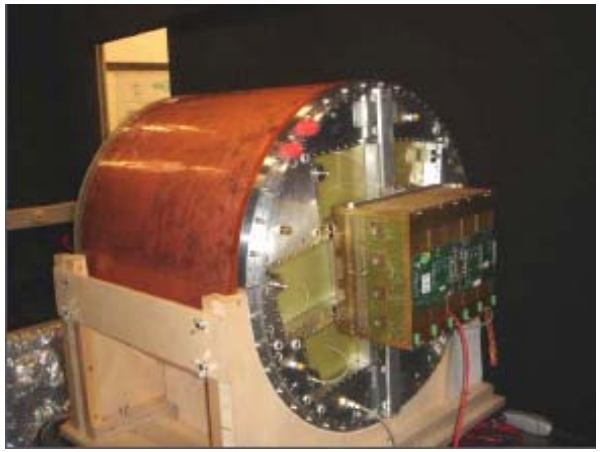
Goal : Fully equip 7 modules with more integrated electronics, still based on the T2K AFTER chip.

First prototype in June 2010
Tests at fall 2010

Then production and characterization of 9 modules in 2011 at the CERN clean room

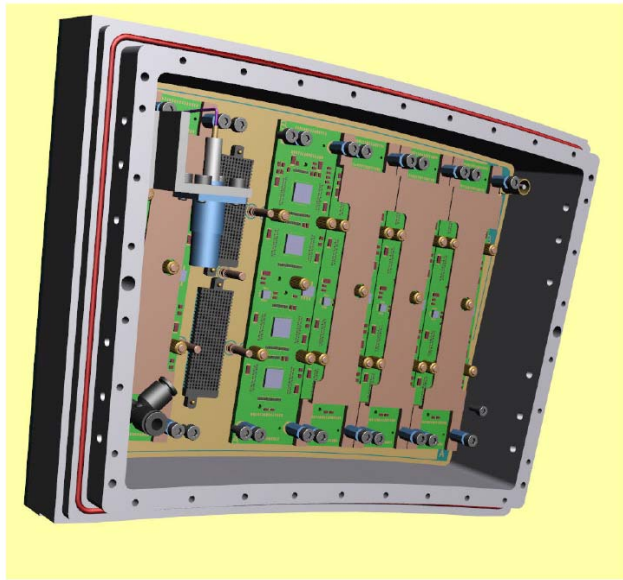






NEW ELECTRONICS – FLAT ON THE BACK OF THE MODULE

-Naked AFTER chips wire-bounded on cards
-Flat 300-point connectors
-New mezzanine bearing ADCs and regulators
-Air cooling

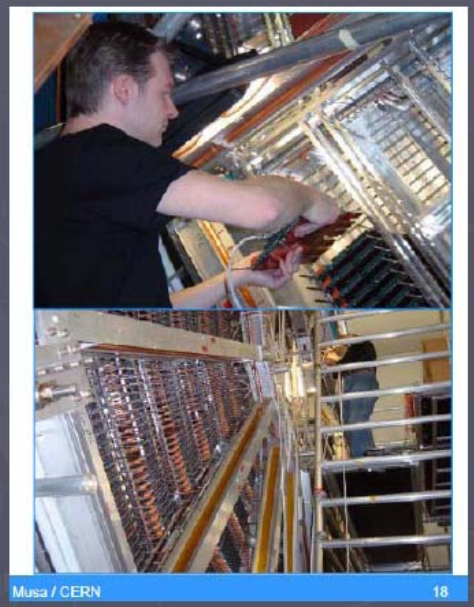


TPC with ALTRO readout

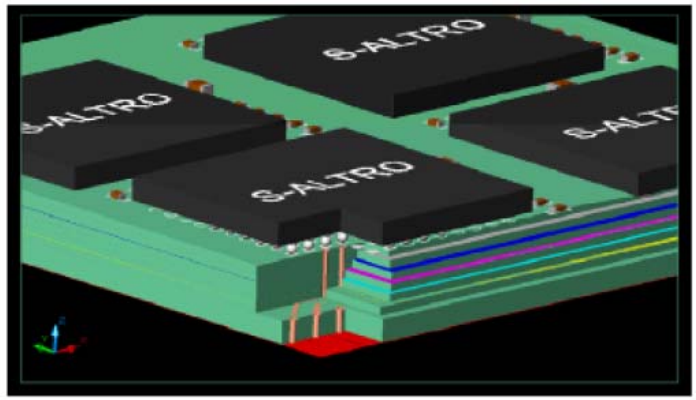
T. Matsuda

Advanced Endplate: S-ALTRO

High density, low power , low material electronics for TPC



ALICE TPC



The S-ALTRO team at CERN

P. Aspell, H. Franca Santos, E. Garcia,
A. Junique, M. Mager, C. Patauner,
A. Ur Rehman, L. Musa

ILC (ILD) TPC

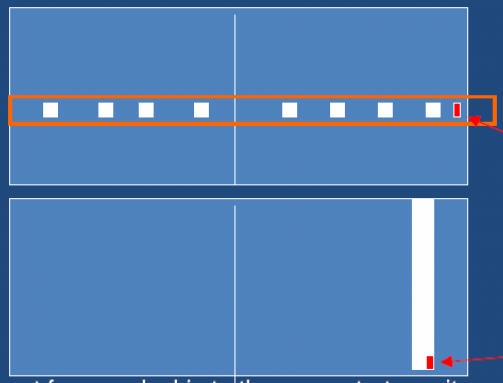
11

SiLC

A. Savoy-Navarro

DAQ step 1: very preliminary schematics

Explored solutions at the module level



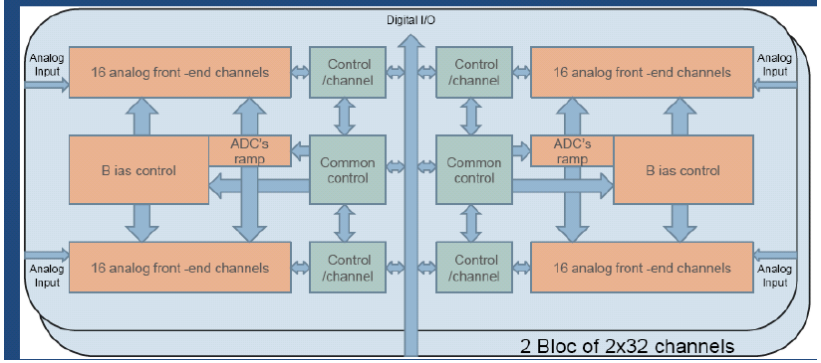
8 SiTR_256 on kapton TAB linked to a buffer 1st concentrator level/unit

8 SiTR_256 Gathered on a Superchip Including the 1st concentrator unit

- Data are sent from each chip to the concentrator unit on module
- Synchronization via the bunch trains:
  - bunch adressing is perfomed at chip level by the internal chip clock
  - module & train synchronization from global DAQ via the concentrator unit

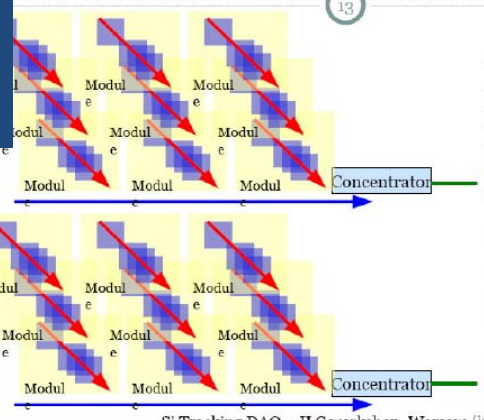
3/27/2010 FEE-RO, DAQ for Strips at LC, A. Savoy-Navarro, LCWS2010 18

NEW SiTR_IBM130-128



DAQ Silicon tracking architecture

A global schematic view of the Silicon DAQ architecture



3 "floors":

F1: chip on sensor, full readout chain in a single chip (A/D, zero suppression, multiplex ...)

F2: on detector sides, daisy chains chips, data buffering, preprocessing ...

F3: processing, azimuthal sector, track reconstruction

Si Tracking DAQ – ILC workshop, Warsaw (June 08)

Total number of modules:
500 (SIT) + 2500 (SET) + 2000 (ETDs)
5000 modules of 1792 channels

Total number of channels:
10^8 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)
10×10^6 channels
~5.12 Gbytes

Not taken into account:
FTD data
Zero suppression ...

Just starting to work on this item: lot to be done!!

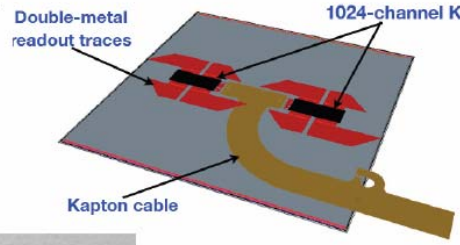
3/27/2010 FEE-RO, DAQ for Strips at LC, A. Savoy-Navarro, LCWS2010 20

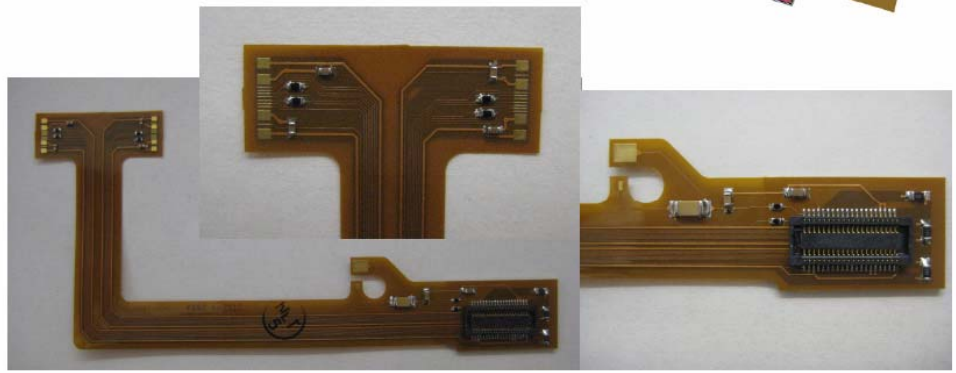
SiD tracking

continues progress on kPiX readout

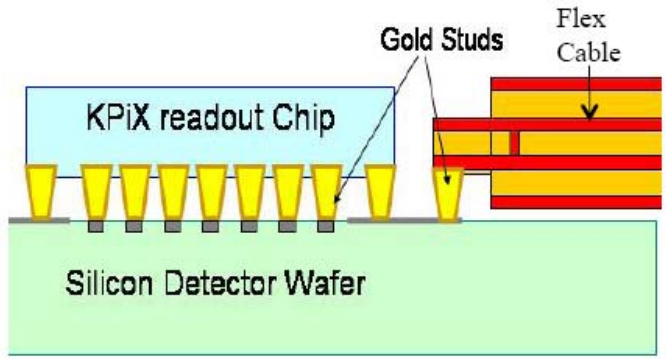
Readout Cable

- Cables for DM-SiD sensors produced (New Mexico/Fermilab)
  - Being characterized at NM
- All components in hand to develop full KPiX/Double-Metal prototype assembly for performance studies
  - Plan calls for studies with test structures first





- kPix readout ASIC
  - Sensor read out with two kPix chips bonded to the sensor
  - kPiX-8 with 256 channels in hand
- Flexible readout cable
  - 2-layer, ¼ oz. Cu on 50µm Kapton
  - 2 power + ground pairs
  - 8 control/ro lines
  - Provides sensor HV bias



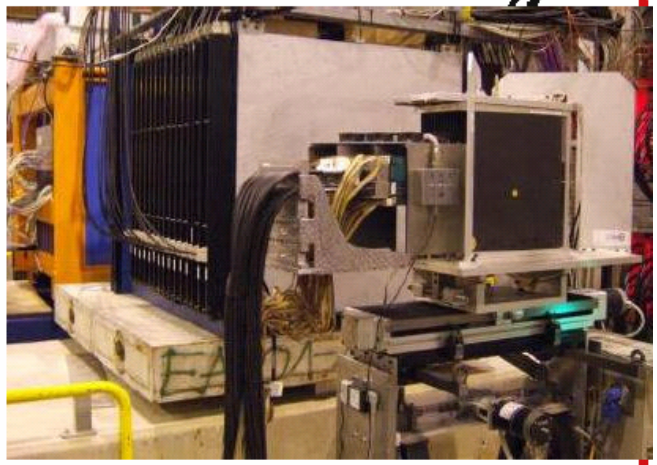
M. Demarteau

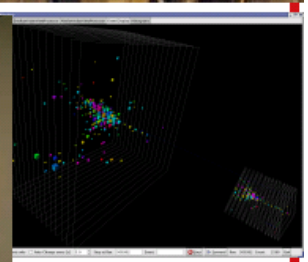
Calice/EUDET physics prototypes

CALICE physics prototypes

C. de la Taille

- 1 m^3 **prototype for physics** tests
  - Goal : study particle flow algorithm and validate Geant 4
- SiW ECAL
  - 9 600 readout channels since 2004
  - FLC_PHY3 chip [LAL] 18ch analog
- 1 m^3 Analog HCAL : tiles + SiPM
  - 8400 channels since 2005
  - FLC_SiPM chip [LAL]
- 1 m3 Digital HCAL : RPCs
  - 400 000 readout channels
  - DCAL chip [FNAL], 64ch 0.25µm
  - In fabrication, see talks by J. Repond and H. Weerts
  - Alternative R&D with GEMs & µMegas : see talks by A. White and M. Chefdeville





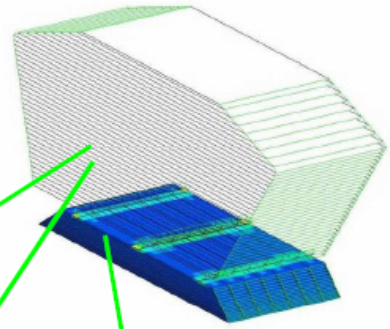
28 mar 2010 CdLT : ASIC developments in CALICE/EUDET LCWS 2010 2

CALICE/EUDET technical prototypes

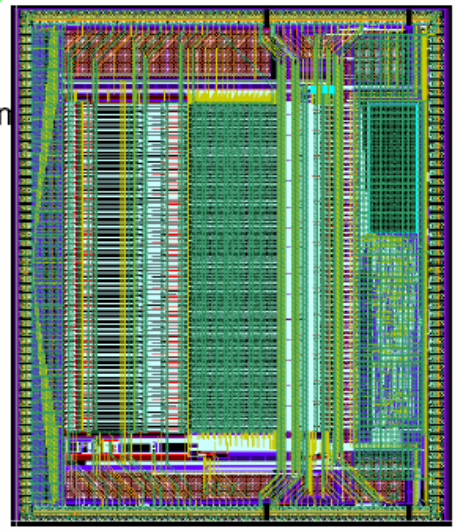
Second generation ASICs

Omega

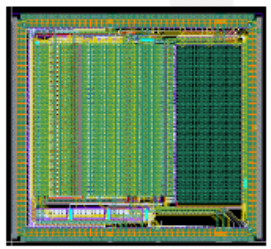
- Add auto-trigger, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ…)



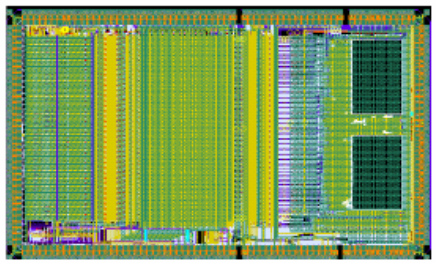
SKIROC2
ECAL Si
64 ch. 70 mm



HARDROC2
SDHCAL RPC
64 ch 16 mm²



SPIROC2
AHCAL SiPM
36 ch 30 mm²



FLC_PHY3 (2003)

28 mar 2010 CdLT : ASIC developments in CALICE/EUDET LCWS 2010 3

C. de la Taille

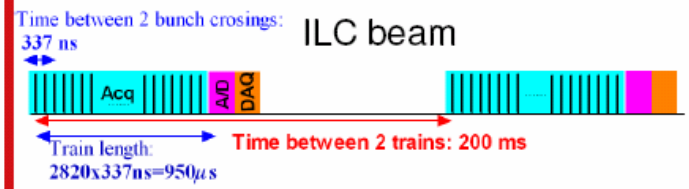
CALICE/EUDET - ILC like readout

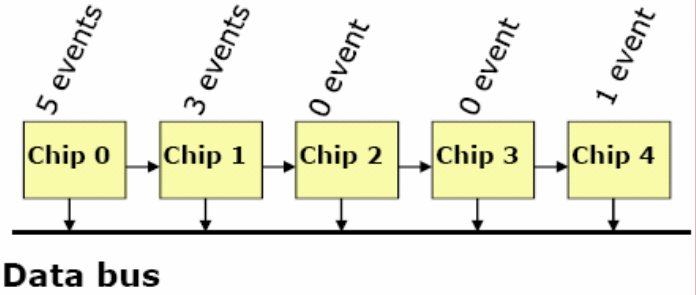
Read out: token ring

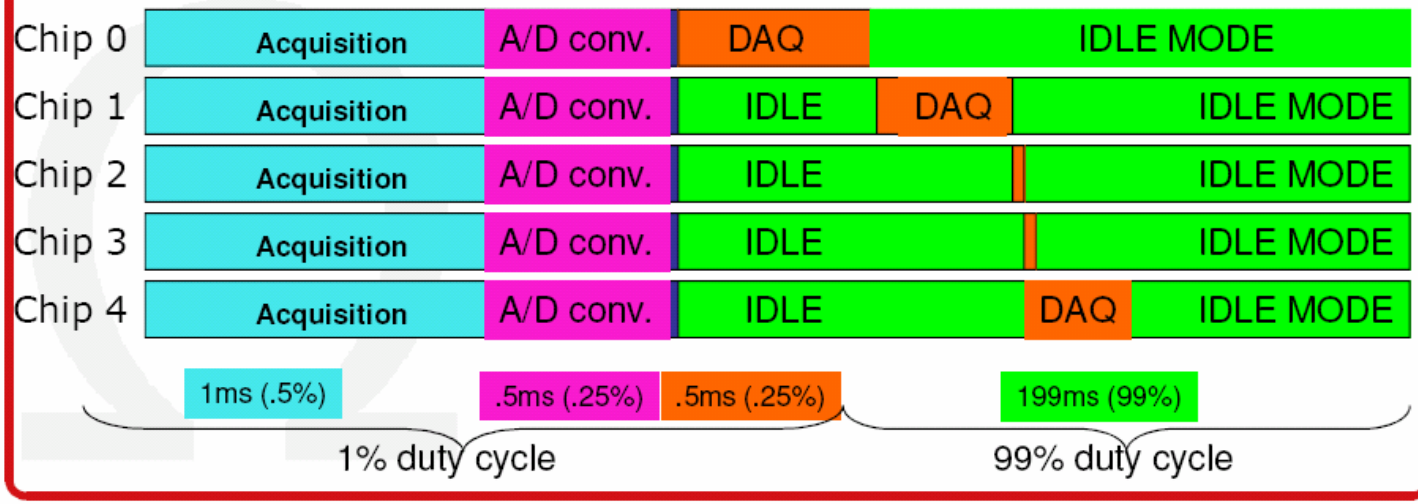
Omega

- Readout architecture common to all calorimeters
- Minimize data lines & power

C. de la Taille







CALICE DAQ

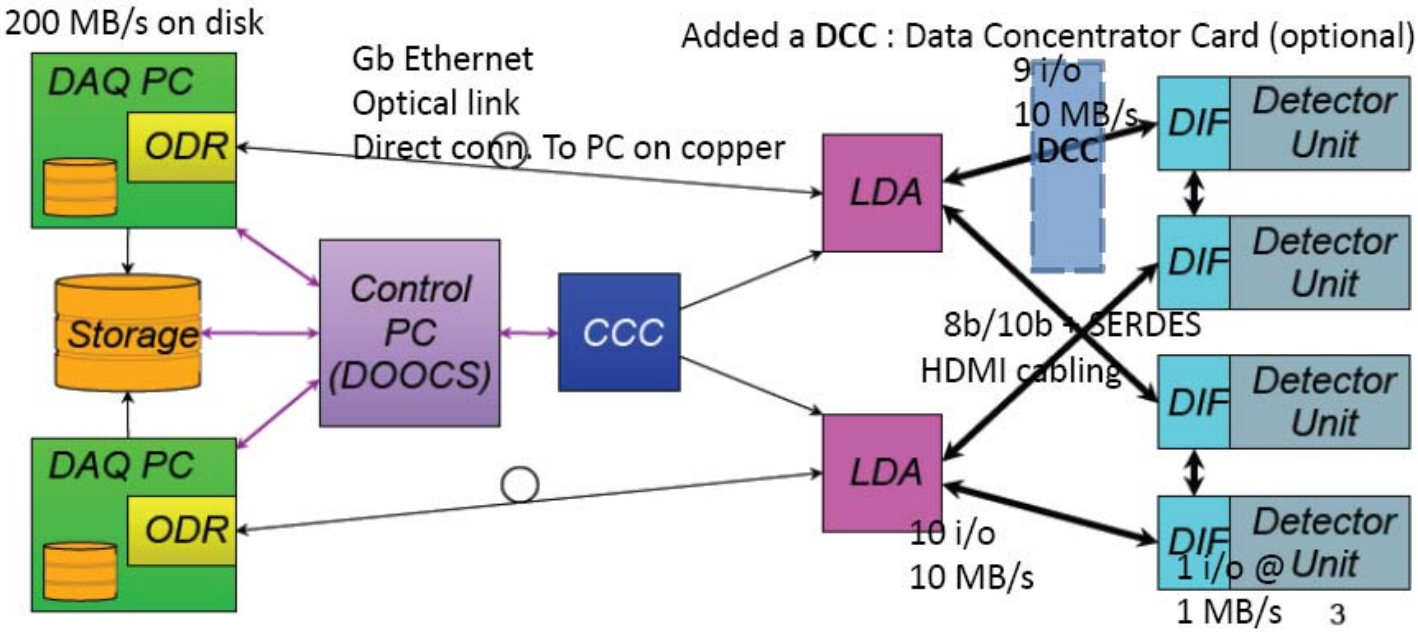
UCL

DAQ system overview

R. Cornat
DAQ Session
ILD Workshop Jan '10

(**Detector Unit** : ASICs)
DIF : Detector InterFace connects generic DAQ and services
LDA : Link/Data Aggregator fans out/in DIFs and drives links to ODR

ODR : Off-Detector Receiver is PC interface
CCC : Clock and Control Card fans out to ODRs (or LDAs)
Control PC : Using DOOCS



ILD workshop, 27/01/10, LLR – Rémi CORNAT 7

Summary of DAQ activities

- Continues progress on front end readout
- Many efforts towards technical prototypes
- Test beam activities profit from common DAQ approaches (like CALICE-DAQ or EUDAQ)
- First attempts on fully integrated DAQ system

What about GDN ?

- Reminder : ILC is a global project which should enable remote partners to participate in machine and detector commissioning and operation
- Apart from EUDET test beam activities little GDN yet
- Need to keep GDN aspects in mind during detector design stage already
- DAQ & detector control should be GDN aware !

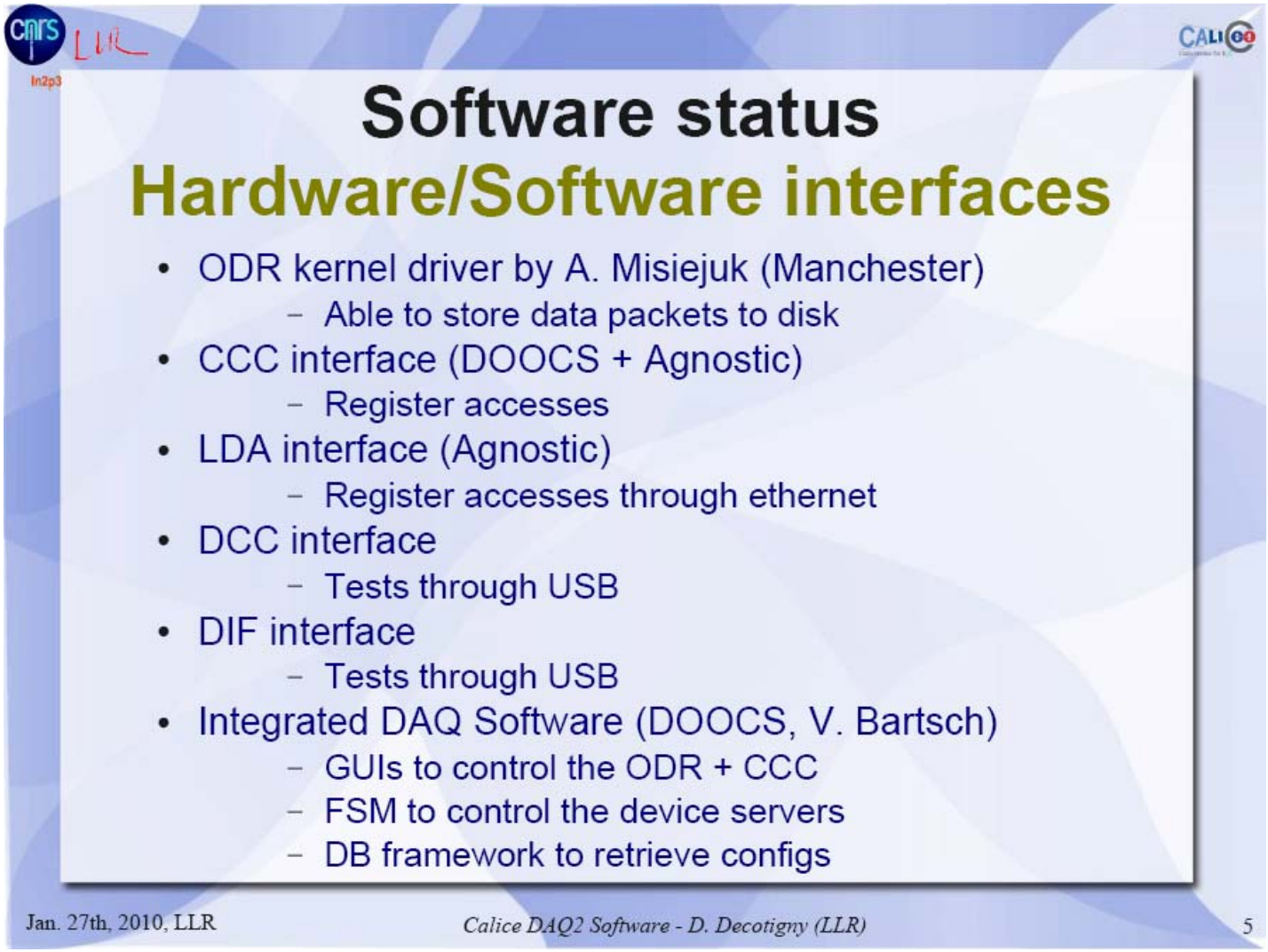
Until 2012 …

- Full integrated DAQ ?
  - CALICE/EUDET DAQ is a good start for test beam
  - But not yet fully integrated DAQ system (Run/SlowControl/DB)
  - (first attempts with DOOCS, XDAQ, EUDAQ …)
- EUDET $\Rightarrow$ AIDA
  - EUDET will (hopefully) be followed by AIDA
  - (common DAQ, commercial readout boards, interface boards)
- How much DAQ is needed for the DBD ?
  - DAQ concept or demonstrator or ILD/SiD DAQ prototype ?
  - Proof of calibration, alignment, BX tagging, … ?
  - Costing ?

Thank you !

Further details

CAICE DAQ-2



D. Decotigny
DAQ Session
ILD Workshop Jan '10

TPC readout

T. Matsuda

TPC Large Prototype Beam Test: LP1 in 2010

"Demonstrate full-volume trucking in non-uniform magnetic field, trying to provide a proof for the momentum resolution at LC TPC"

2010:

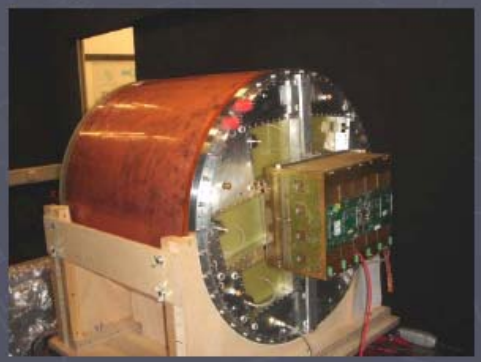
Spring-Summer

- 3-4 Asian GEM Modules w/ gating GEM (10,000ch ALTRO electronics)
- DESY GEM modules (w/ wire gating?) (10,000ch ALTRO electronics)

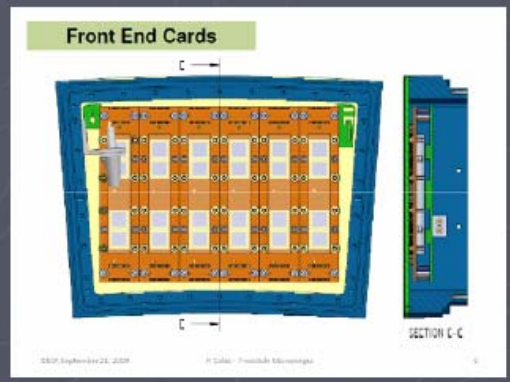
Fall

- 7 MicroMEGAS modules w/ resistive anode (12,000ch T2K electronics)

MicroMEGAS module 2008-2009



Over sized electronic in 2008-2009



MicroMEGAS modules in 2010

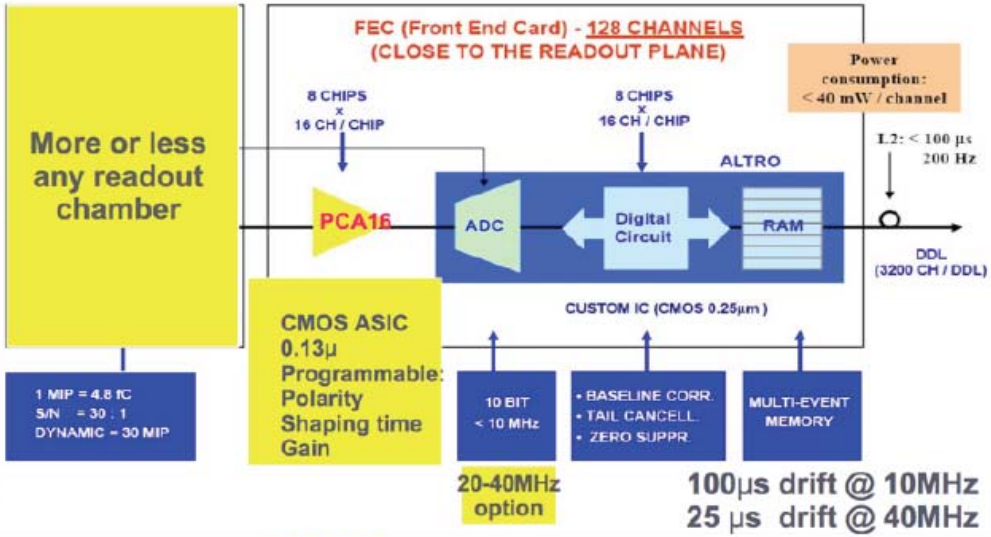
(Unfortunately T2K electronics can not be used at ILC TPC!)

7

TPC readout – ALTRO

The front end card (FEC)

K. Ikematsu



- **PCA16**
  - Programmable charge sensitive amplifier
  - Gain: 12, 15, 19, 27 mV/fC
  - Shaping time: 30, 60, 90, 120 ns
  - Can also be run in non-shaping mode with variable decay time
- **ALTRO**
  - ADC digitizes the PCA16 analogue signal of 1.2 V to a 10 bit digital value
  - Sampling frequency: 20 MHz (40 MHz)
  - Buffers data while waiting for store/discard decision
  - Perform pedestal subtraction and zero suppression

Katsumasa Ikematsu (KEK) / LCWS 2010 Beijing

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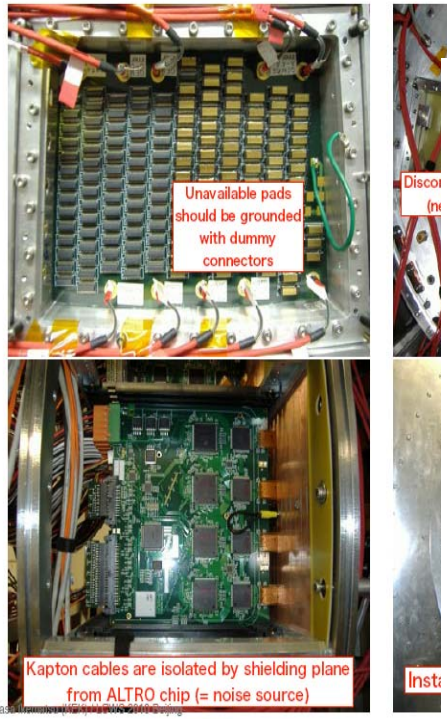
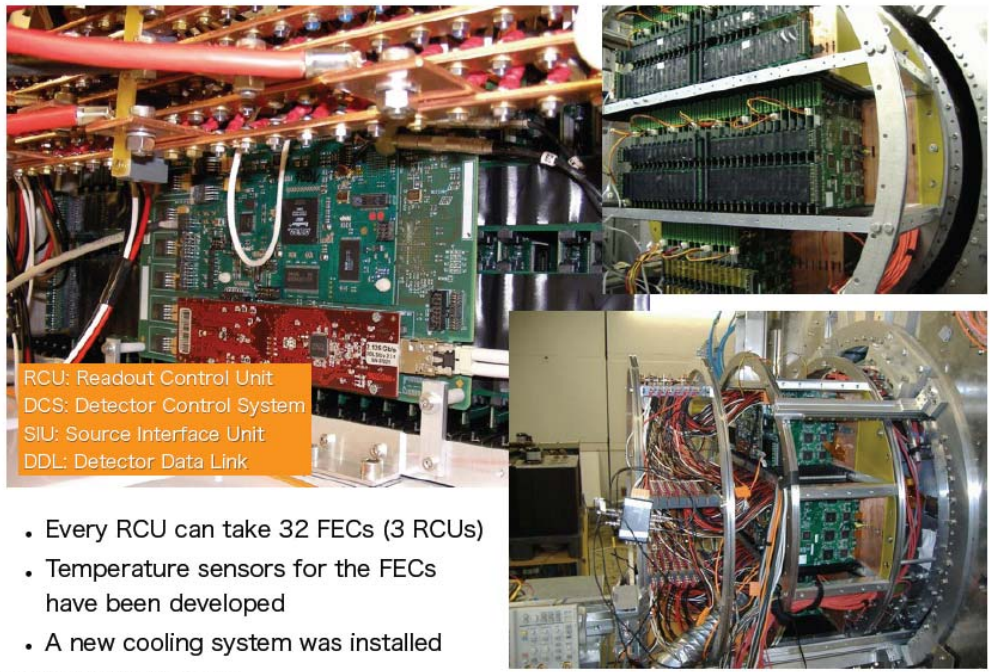
TPC – test setup

K. Ikematsu

Pad <-> FEC implementation in LP1



Integrated ~10k readout electronics



- Every RCU can take 32 FECs (3 RCUs)
- Temperature sensors for the FECs have been developed
- A new cooling system was installed

Katsumasa Ikematsu (KEK) / LCWS 2010 Beijing

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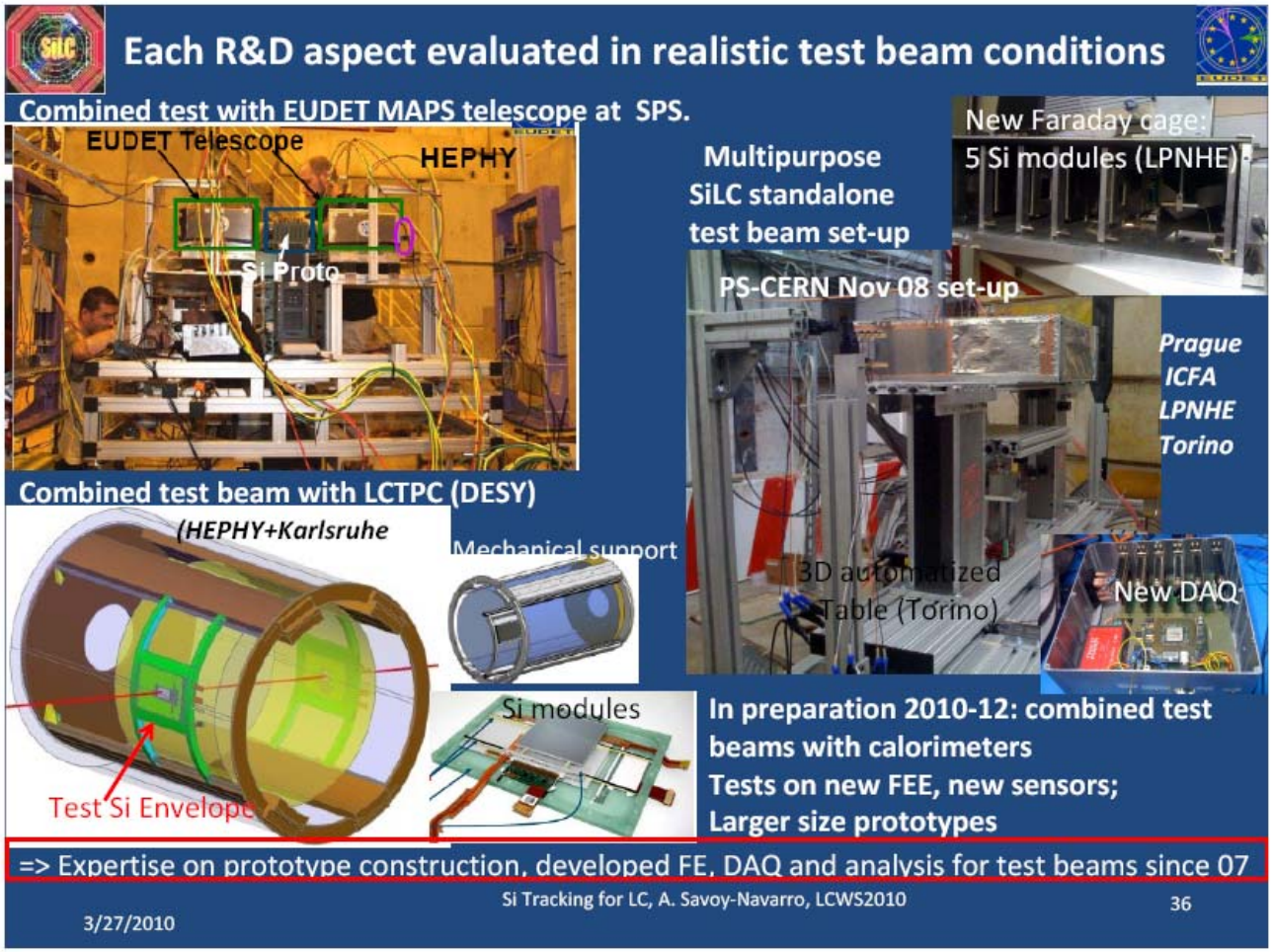
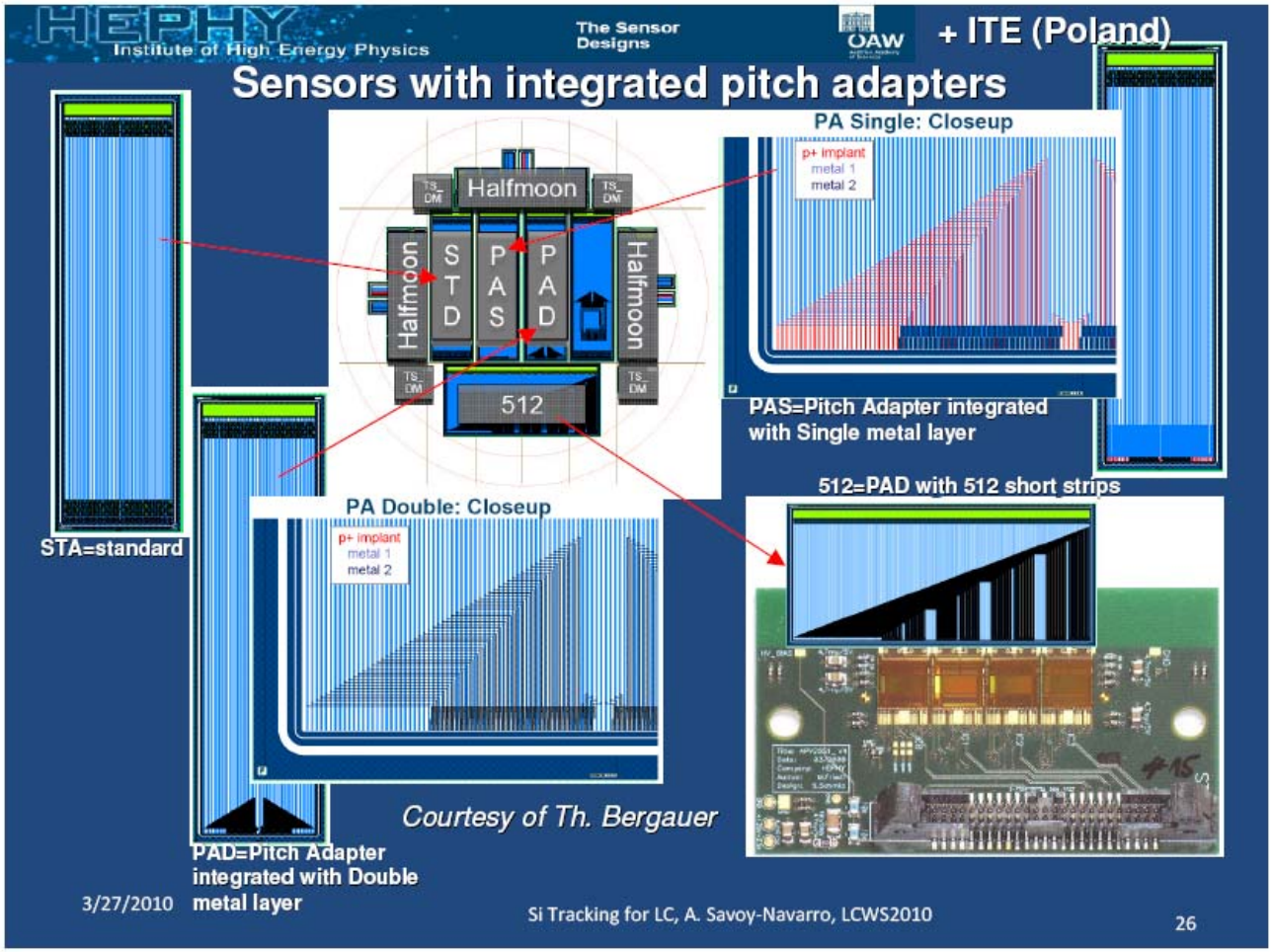
Si Tracking Test beam setups

A. Savoy-Navarro



Sensors with integrated pitch adapter

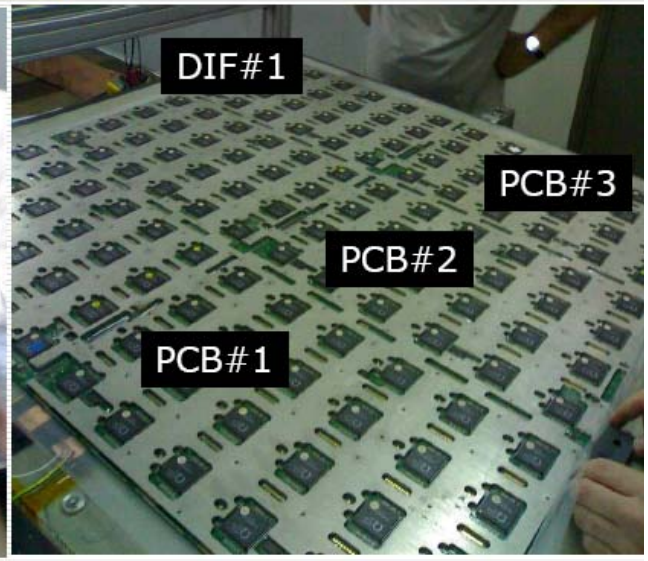


A. Savoy-Navarro

SDHCAL – technical prototype

N. Lumb

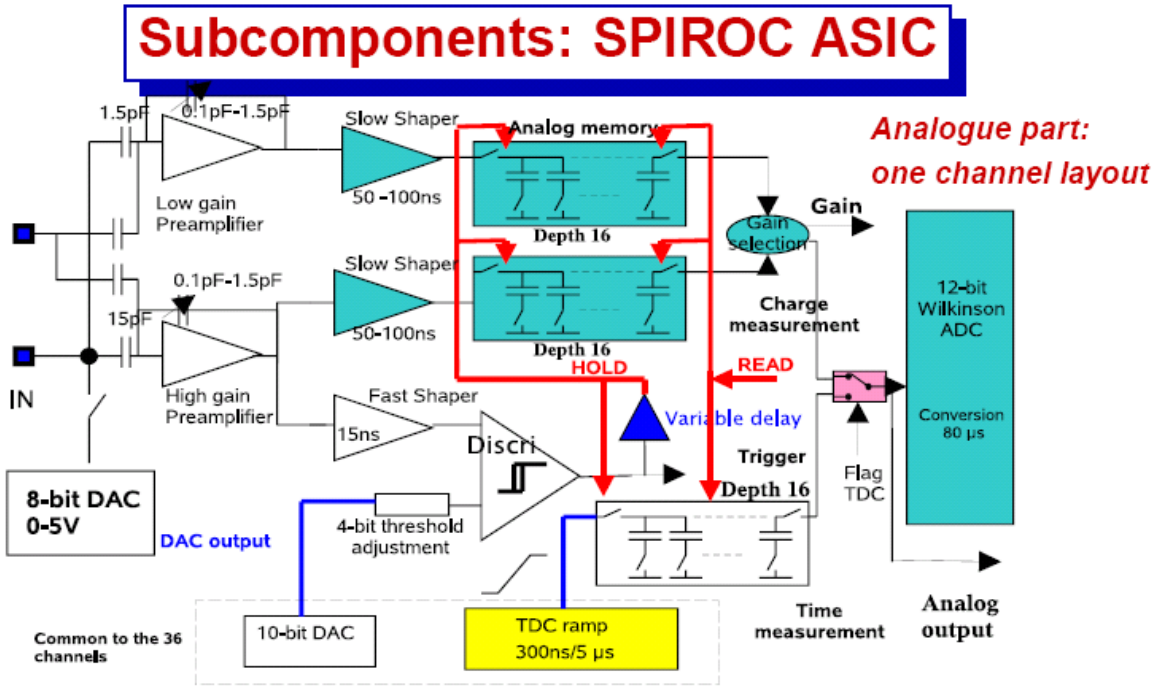
Electronics boards + support



- 144 ASICs, 9216 channels per m^2
- $1m^3$ project: almost 400,000 channels!
- $1m^3$ project will use Hardroc 2b chip

Nick Lumb

AHCAL - SPIROC



R. Fabbri

- Designed/developed by LAL (Paris)
- Handle 36 input signals (36 SiPMs)
- Internal ADC, autotrigger mode, low power dissipation
- Commissioning ongoing at DESY (strong support from LAL and Heidelberg)

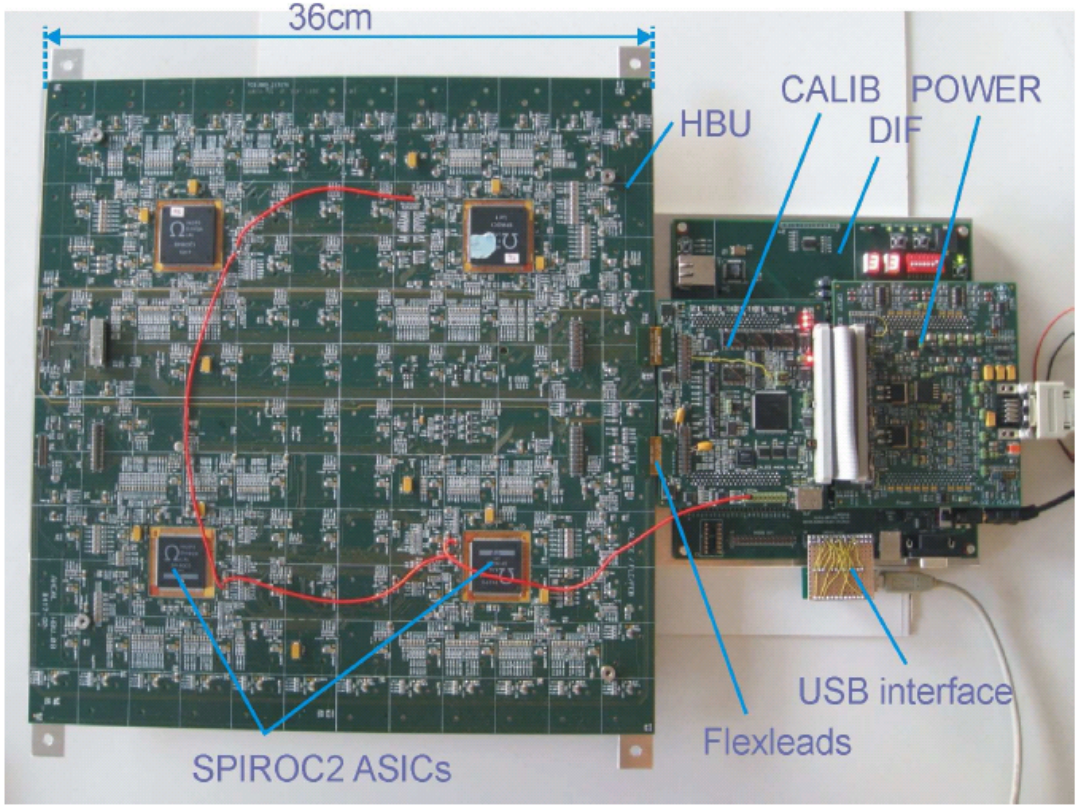
$\Longrightarrow$ Results on analogue part finalized in arXiv:0911.1566/EUDET-Report-2009-05

Riccardo Fabbri LCWS 2010 CALICE 2nd Generation AHCAL Developments – p.4

AHCAL - HBU

Subcomponents: HBU (HCAL Base Unit)

R. Fabbri



- Two setups in operation (one in Lab., one in Test-beam area)

Riccardo Fabbri LCWS 2010 CALICE 2nd Generation AHCAL Developments – p.5

DHCAL

Square meter plane with Readout boards

J. Repond

17

DHCAL

Status of DCAL Production

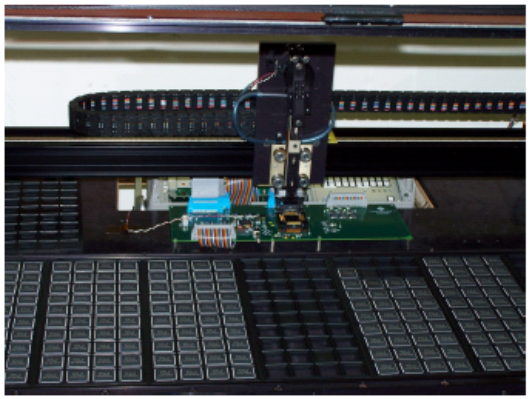
Chip fabrication

11 wafers, 10,300 chips fabricated and packaged

Chip testing

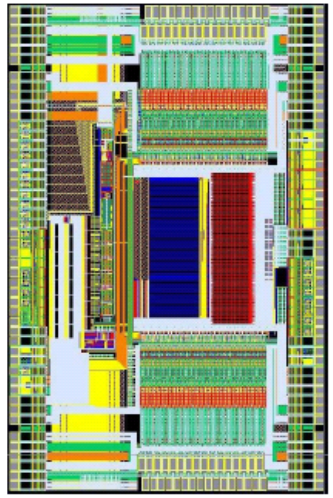
Extensive tests on a small number of chips at Argonne
Robotic test of all chips at Fermilab

→ 8644 good parts = 84% yield
(need 5472 for cubic meter)



Robotic Chip Tester

Chip Storage (~1/2 total)



DCAL3 Layout

Fermilab

⇨ *Complete*

J. Repond

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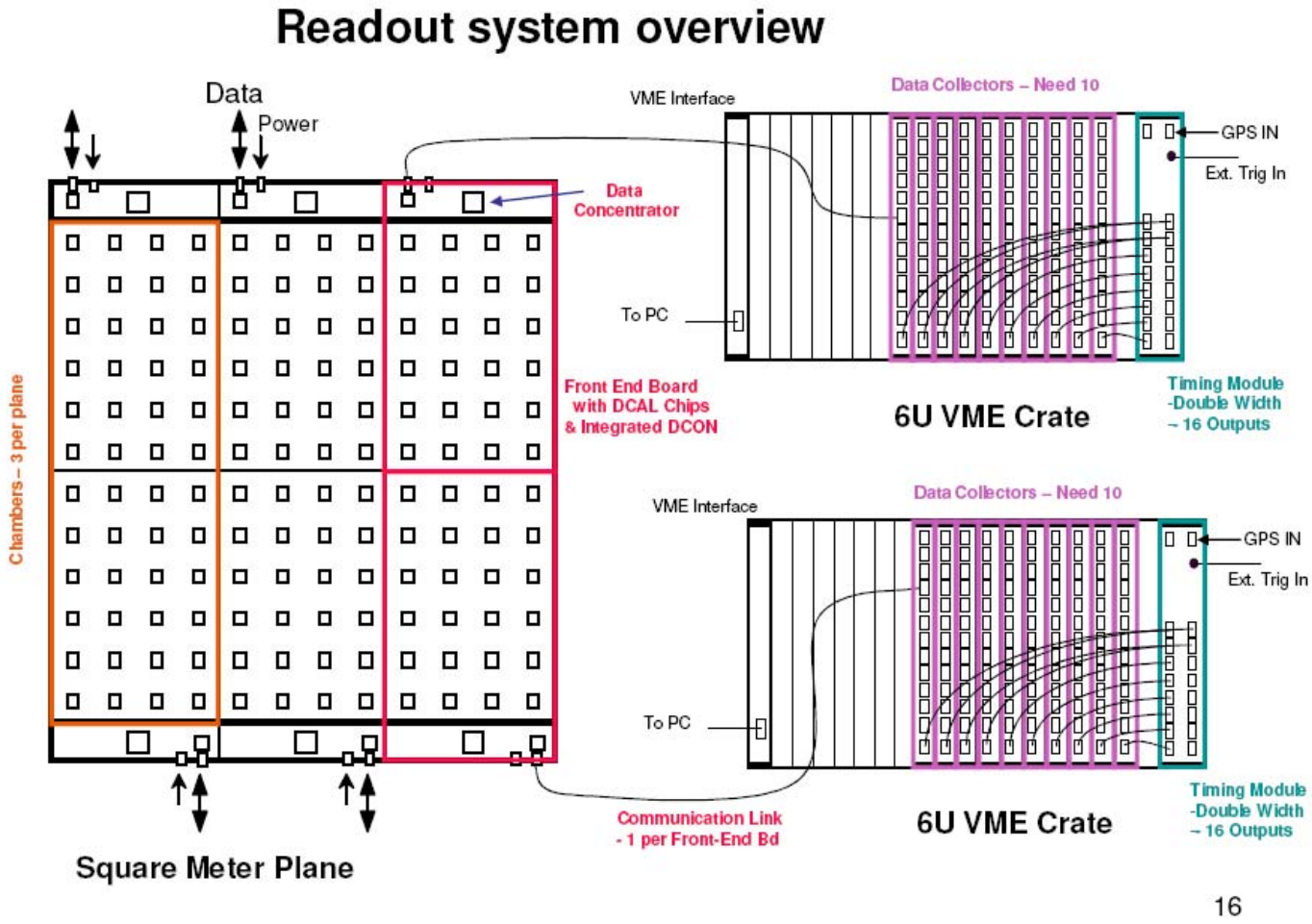
DHCAL - readout



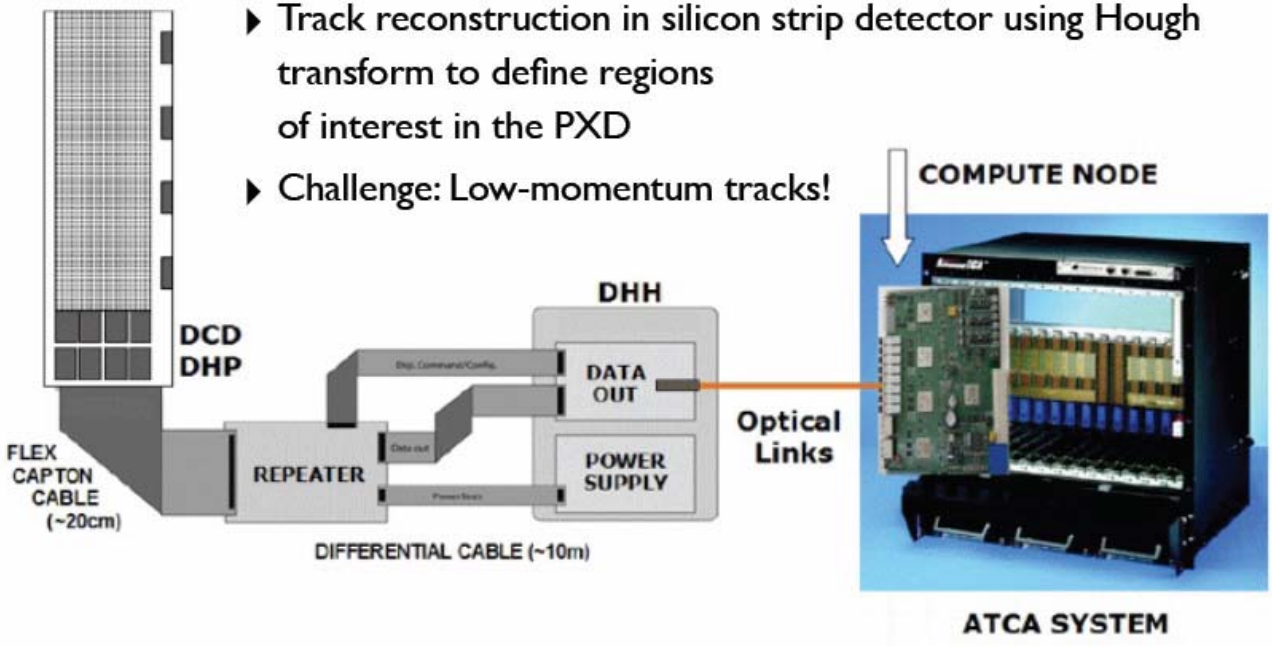
J. Repond

DEPFET – Belle II -PXD

DAQ Concept

F. Simon

- Extreme data volume: The PXD generates up to 10 GB/s of data
- Data transfer with high-speed optical links to DAQ system
  - Fast online reduction of data volume needed:
    - Track reconstruction in silicon strip detector using Hough transform to define regions of interest in the PXD
    - Challenge: Low-momentum tracks!



TPC – S-ALTRO

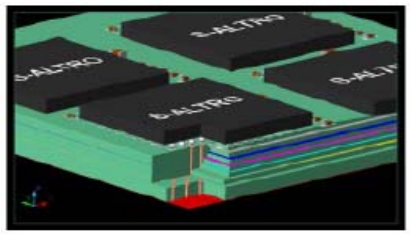
Advanced Endplate: S-ALTRO

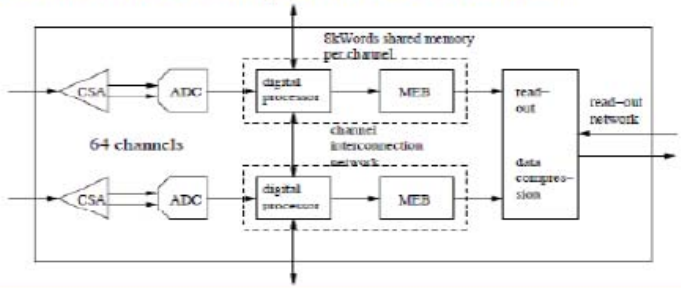
High density, low power electronics for TPC

A multi purpose readout chip for TPC detectors

A multi-purpose readout chip for TPC detectors

- 64 complete readout channels (from detector pad to data link)
- programmable charge sensitive amplifier
  - sensitivity to a charge in the range ~10^2 - ~10^6
  - programmable shaping time in the range 30 to 300ns
- 10-bit 40 MSPS ADCs
- 8k multi acquisition memory per channel (dynamically allocated)
- digital signal conditioning (4th order IIR filter and FIR filter) for baseline correction
- 3-D zero suppression
- lossless data compression
- readout net work controller
- output bandwidth 160 Mbyte/sec





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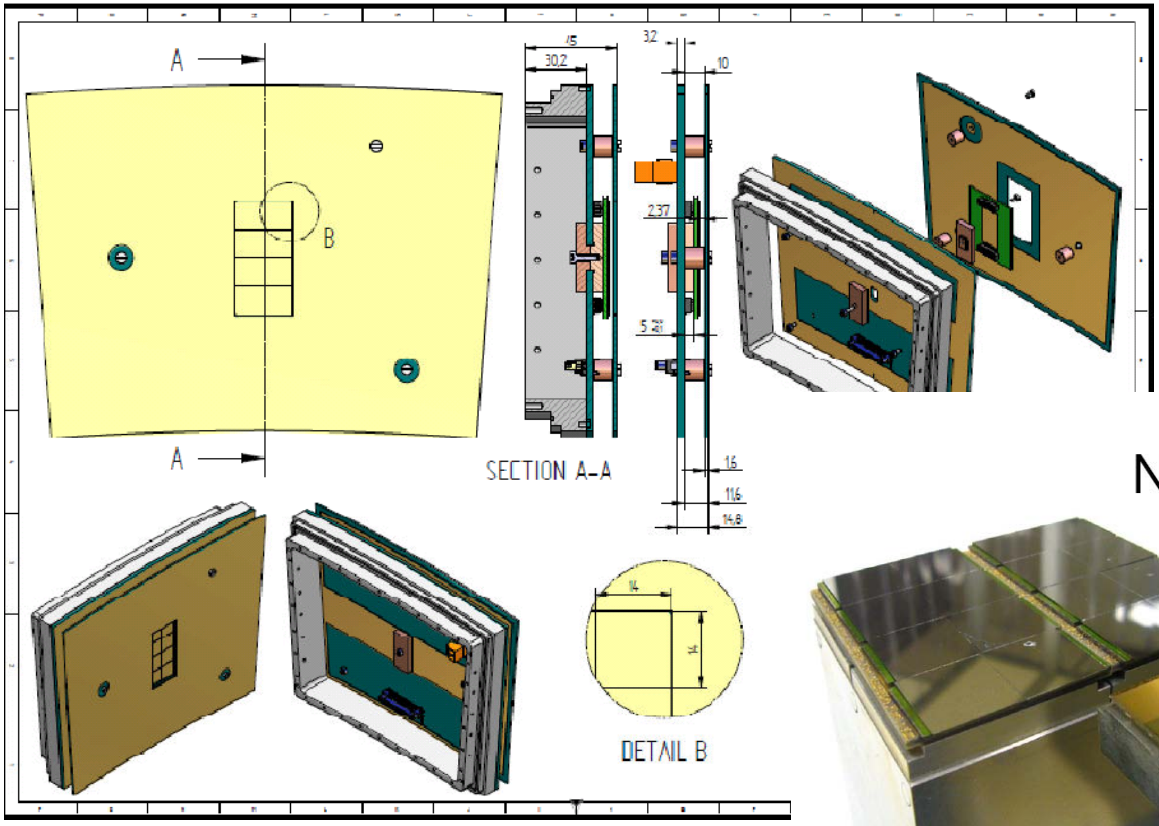
Digtial TPC readout - TimePix

2×4 TimePix/InGrid matrix module for the LPTPC



J. Timmermans

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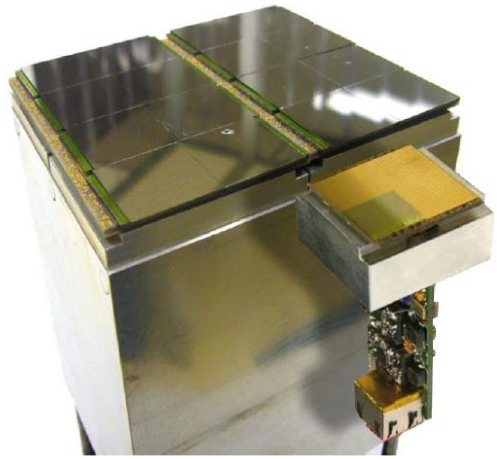

- within Relaxd project: 4x4 Medipix chips in compact mounting
- Will evolve in 8x8 Timepix chips for EUDET/LCTPC