Silicon Tracking at the Linear Collider(s): advances, issues & perspectives

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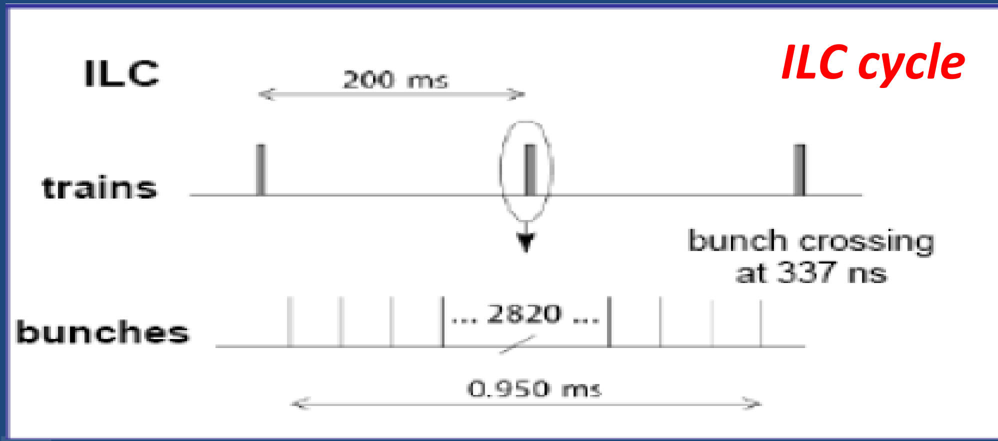
Outline

The work & results reported here are from the R&D activities of the SiLC R&D Collaboration to develop the next generation of large area semi -conductor trackers for the Future Linear Collider (LC)

- The Future Linear Collider tracking issues
  - The environmental and Physics constraints
- The R&D basic activities and present status on:
  - sensors
  - interface sensor/FEE on detector (direct connection)
  - associated FEE and DAQ (see next talk)
- Applications to the LC tracking concepts & Integration issues
- Synergies and perspectives

The ILC machine: impact on sensors & FEE

ILC: cold technology & relatively slow machine.



- Contrary to LHC/sLHC, radiation hardness is NOT a main issue here
- => Possibility to work at room temperature with ΔT=10º C
- Allow for relatively long shaping time (typically 0.5 µs) and
- relatively long strips (typically 10 to 30cm) at least in some regions
- Material budget is a severe constraint *(vs gaseous trackers)*
- Pulse cycling is feasible & included to avoid cooling AMAimP
- Push pull is a severe constraint on the design of the LC detector
- Time stamping is requested (especially tough for CLIC)

The constraints imposed by Physics

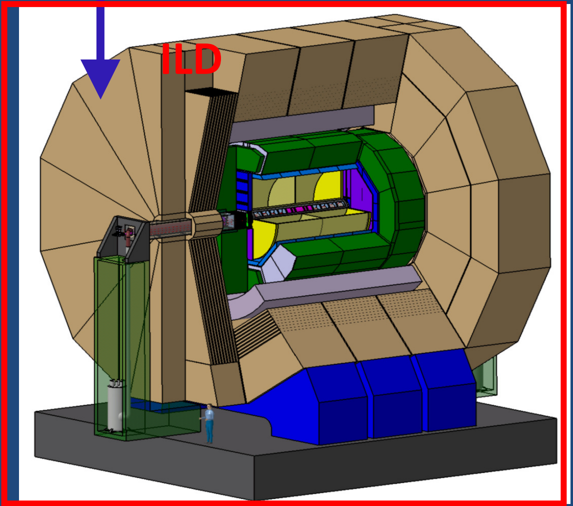
Very high precision measurements have to be performed in order to best benefit from this machine. Thus:

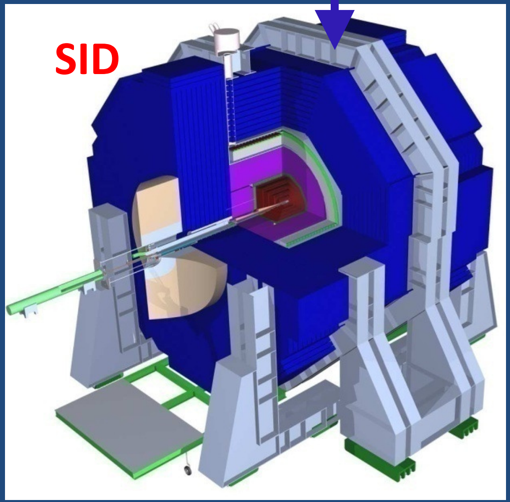
- High performances in momentum and spatial resolution
- Full angular coverage (large angle and forward regions)
- Very precise alignment is mandatory because of required high spatial resolution and of push pull (only 1 detector running at a time).

And in addition and more generally

- Robustness, easy to build and to run and highly fault tolerance (redundancy) are requested but this need is still reinforced here by the push pull option.
- The integration issues are especially severe when merging gaseous with Silicon devices

SiLC (Silicon tracking for Linear Collider)





TPC+Si Envelope **All Si**

Two tracking strategies: Hybrid versus All Si.

Generic & horizontal R&D Collaboration applied to the 2 tracking concepts
Goal: To develop the next generation of large area Silicon trackers
Synergy with the construction of LHC Si trackers & their upgrades, SuperBelle, New g-2 project (J-Parc-KEK)

***SiLC**: U. Michigan, U. of Barcelona, UMB-CNM/CSIC, U. Helsinki & VTT, Karlsruhe U., Moscow St. U., NRNU-Obninsk, LPNHE-UPMC/CNRS-IN2P3,Charles U. Prague, RAL, SCIPP&UC Santa Cruz, IFCA CSIC & U. Cantabria, U. S. Compostela, Seoul Nat U., Korea U., Yonsei U., SKKU-Seoul, Kyunpook Nat. U., INFN Torino & Torino U., IRST-Trento U., IFIC-CSIC, HEPHY-Vienna, HPK-Japan*

Close contacts: CERN (bonding Lab&Microelectronics), FNAL & DESY (testbeams), EUDET E.U.

The R&D on sensors: the roadmap

- The microstrip sensors
  - => Standard but new planar strips
  - => Alignment-friendly strips
  - => Edgeless planar strips
- 3D technology based sensors
  - => “SOI-like” Edgeless strip sensors
  - => 3D short strips
  - => 3D pixels

Standard to new

The sensor baseline: strip sensors

In 2007 was launched an effort on new single sided strip sensors:

GOALS = get the industrial firms to produce:

- **Larger wafer (6''to 8'': KNU), thinner 200 μm, smaller pitch (50μm)**
- **Possibly DSSD, now 6'', 320 μm thick, 50 μm pitch (new HPK)**
- **decreased non-active edge (from a few hundreds down to 10-20 μm)**
- **direct connection of FEE onto the strip sensor (see later).**

AND:

Because of gained expertise for LHC (HEPHY in CMS):

Test structures included for detailed characterization and further studies (many different options added this way for testing improved features)

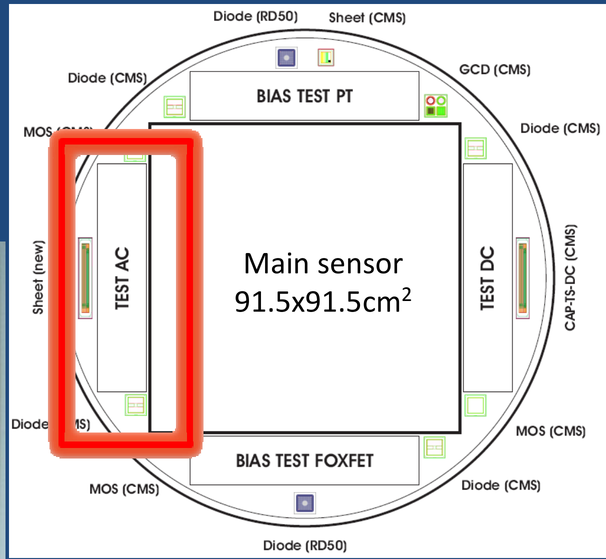
AND:

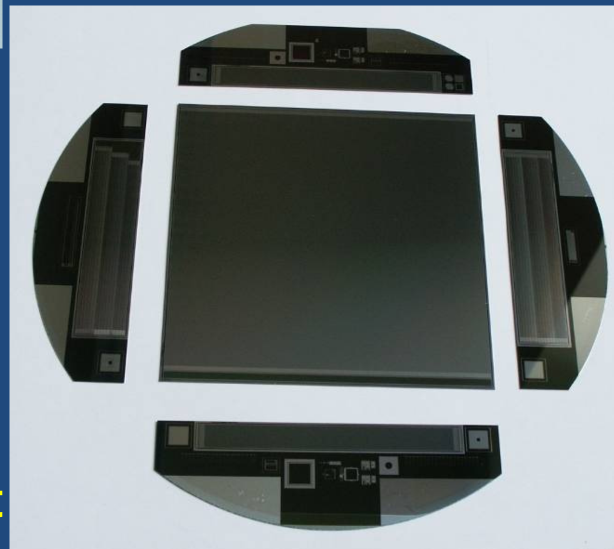
Alignment special treatment for some of them

SiLC Sensor order to HPK (end 2007)

SiLC Collaboration ordered at Hamamatsu (HPK):

- 30 pieces single-sided 6” wafer
- 5 pieces. alignment sensors of same layout, but hole for laser in backplane metallization





Specifications:

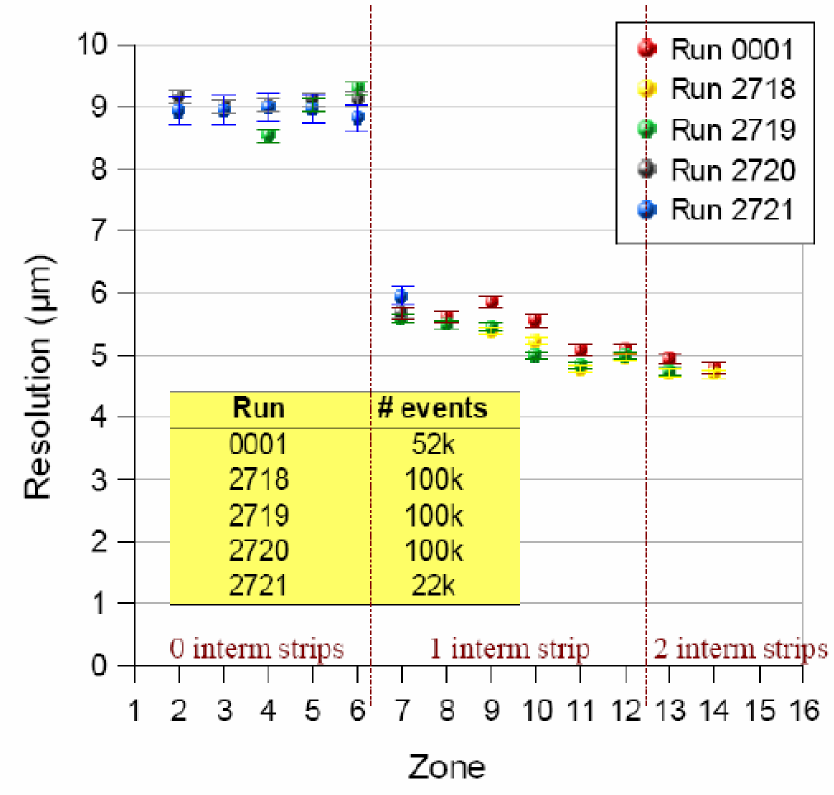
- Wafer thickness : 320 µm
- Depletion voltage around 75V
- 1792 AC-coupled strips, individually biased via poly-Si resistor (20MOhm)
- Strip pitch: 50 µm pitch,
- Strip width: 12.5µm
- No intermediate strips
- Additional test structures around the wafer

Already a new step compared to those in current LHC trackers.
Have been deeply tested in order to establish the next steps (test structures)

2008-09 SPS beam on test structures

Spatial resolution vs strip geometry

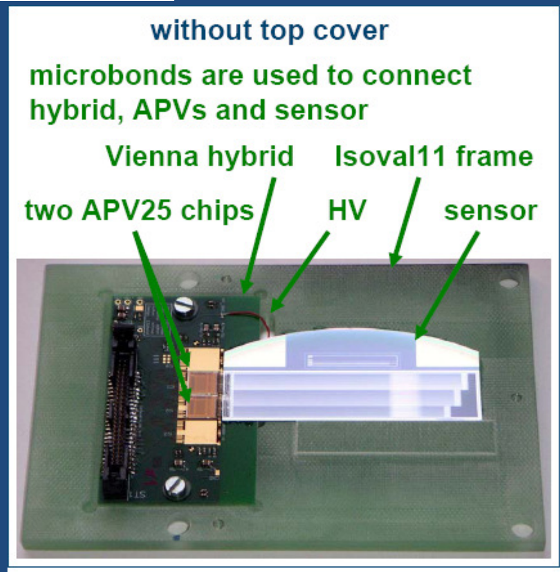
CU Prague



Run	# events
0001	52k
2718	100k
2719	100k
2720	100k
2721	22k

TESTAC:

strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double



- ➢ **9 µm resolution if no intermediate strip**
- ➢ **5 or 6 µm resolution if 1 or 2 intermediate strip**

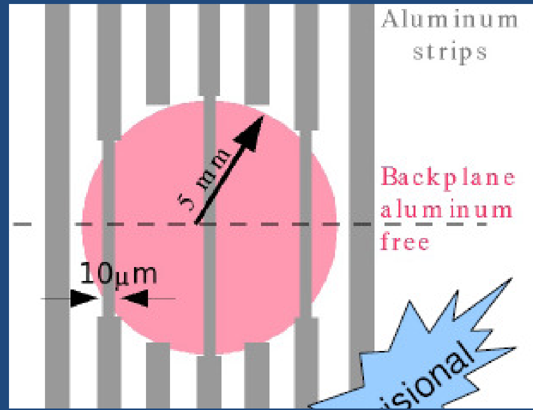
HPK strip sensors for alignment

Implemented:

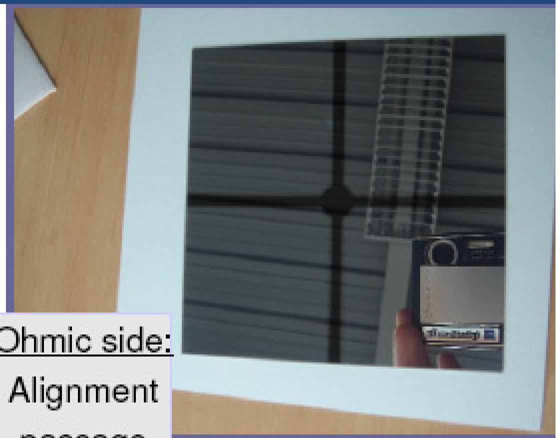
- ∅~10 mm window where Al back-metalization has been removed

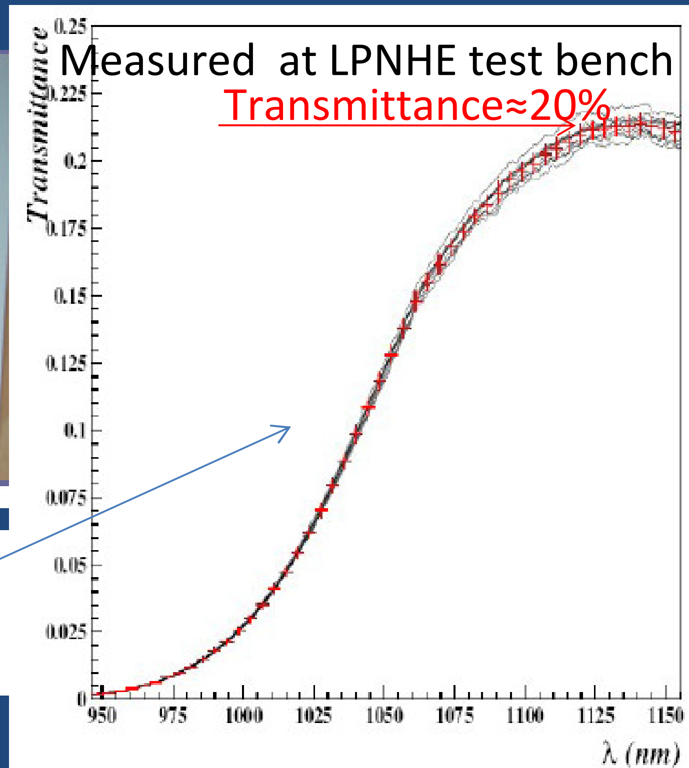
Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)




Strip's side

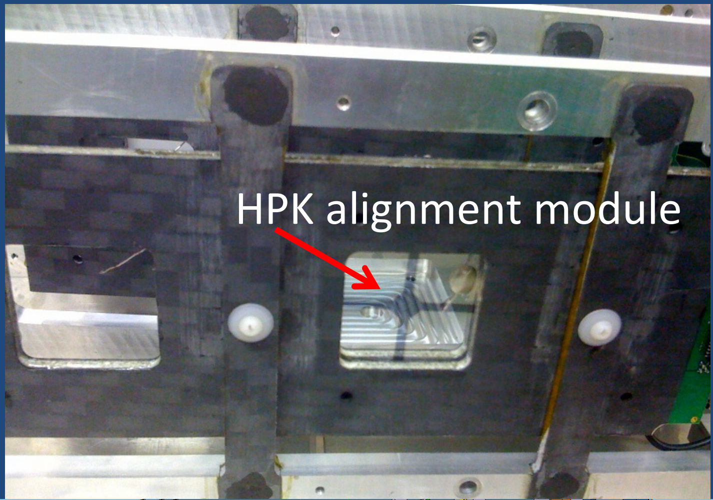

Ohmic side: Alignment passage

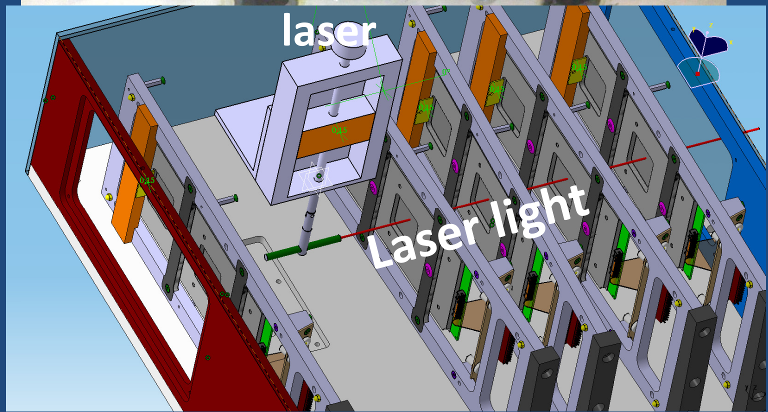


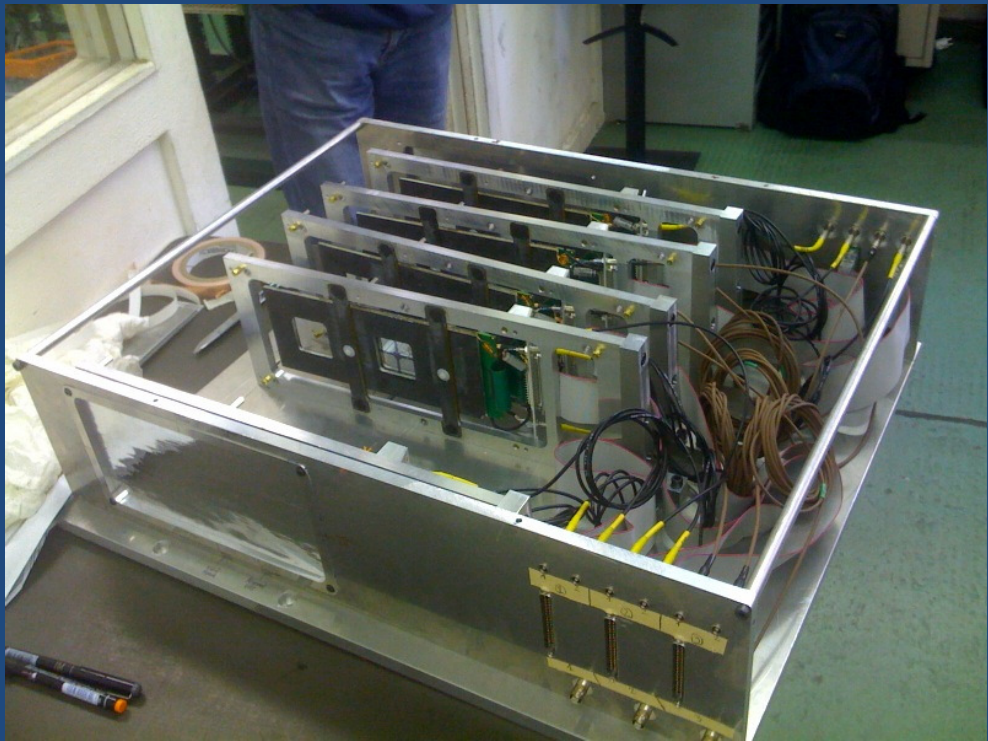
- They are alignment friendly, but not optimized for transmittance: no Anti-Reflection Coating (ARC).

Alignment test set ups (here with HPK equipped modules)

These HPK alignment friendly (AF) sensors have been fully characterized at HEPHY Lab test bench. A set up has been set-up in Paris for laser test of modules with these sensors and later with new A.F. sensors



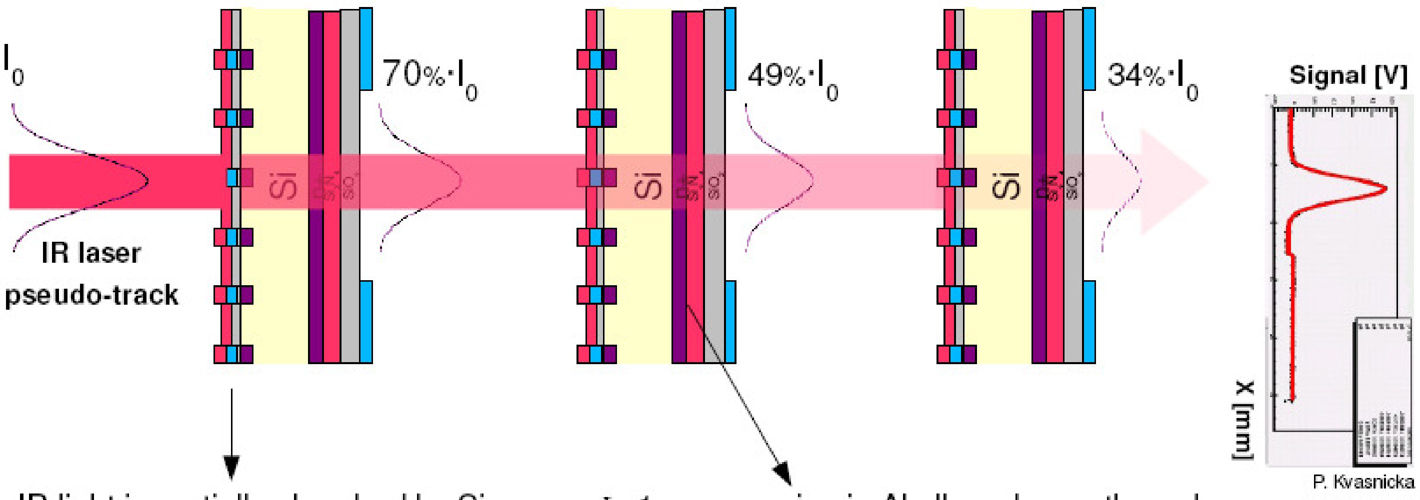


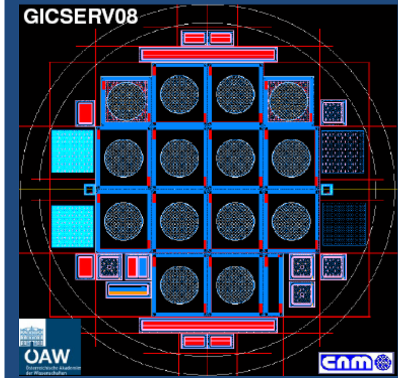


One of the test system: Faraday cage with 3 alignment module + 2 standard modules for test beam and laser tests.
Will go at SPS test beam in May for extensive tests.

A.F. sensors developments

- Aim: align Si microstrip sensors using IR laser tracks *(See A. Ruiz's presentation)*





- 5+1 wafers
- 12 μstrip detectors per wafer (6 with intermediate strips, without metal contacts)
- 50 μm RO pitch (25 μm interm. strip)
- 256 RO strips
- 1.5 cm length varying strip width (3,5,10,15 μm)

- Higher %T ⇒ simpler implementation of the system:

Transmittance	90%	80%	70%	60%	50%	40%	20%
Traversed	30	15	10	7	5	4	2

SiLC HPK

- System features:
  - Laser intensity~200 MiPS ⇒ **sharing same DAQ as Si detector**
  - Silicon modules are directly monitored, **no external fiducial marks**
  - Laser intensity~200 MiPS ⇒ **sharing same DAQ as Si detector**
  - Silicon modules are directly monitored, **no external fiducial marks**

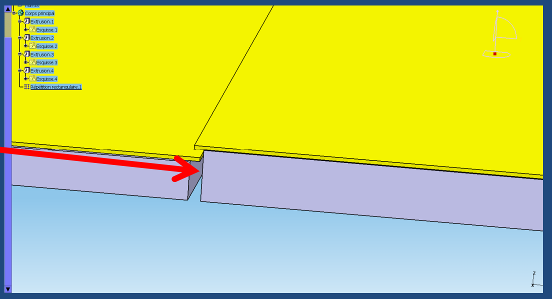
Goal: transfer to Industry by end 2011 after achieving R&D

Edgeless strips sensors: Why?

Edgeless sensors decrease the non active edge regions of sensors (usually of a few hundreds of microns) down to about 10 to 20 µm.

Our interest in edgeless or active edge sensors is motivated by:

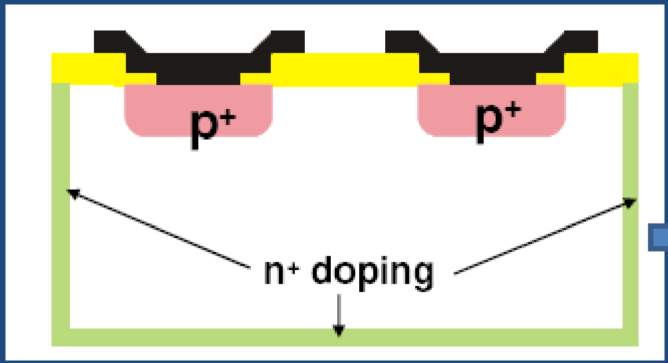
- ✓ allow building large area Silicon trackers seamlessly tiled detector matrices,
- ✓ thus no need for sensor overlap
- ✓ easier to build
- ✓ decrease of the material budget
- ✓ improvement of the tracking performances both in momentum and spatial resolution.

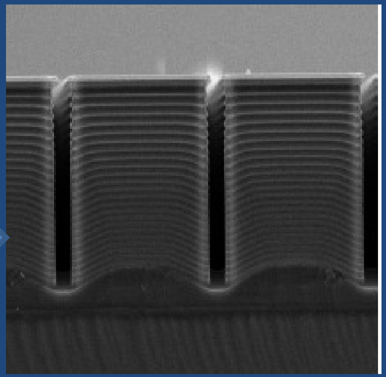


Two solutions based on the edgeless strip based on Edgeless planar and edgeless SOI-like technologies are pursued.

Edgeless planar strips (FBK-irst-U. Trento/INFN)

(*Gian Franco Dalla Betta*)





Schematic cross-section (left view) and photograph (right view) of a planar strip detector with active edge on n-type substrate

Collaborative effort with prototyped sensors 2.5x5cm^2 (Trento & Paris)

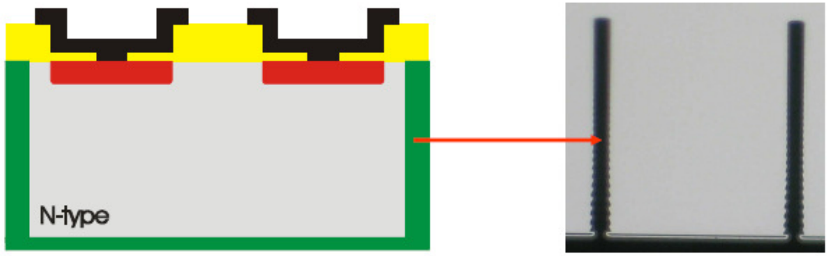
Goal:

Wafer bonding treated (contacts with EDGETEK or SOITEC in France)

Build 5x5cm^2 sensors and read out by VA1' chips

Full characterization at Lab followed by beam test & comparison with standard planar strips (HPK) & SOI based edgeless prototypes (see next)

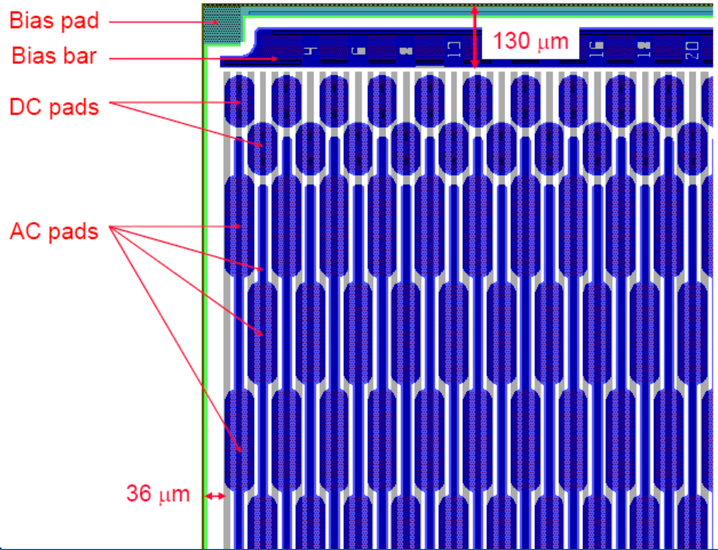
Next steps (2): Planar detectors with active edge



- Trench etching steps investigated on test wafers
- TCAD simulations for breakdown prediction
- Layout complete (p-on-n, mainly strips)

EDGELESS STRIP SENSORS

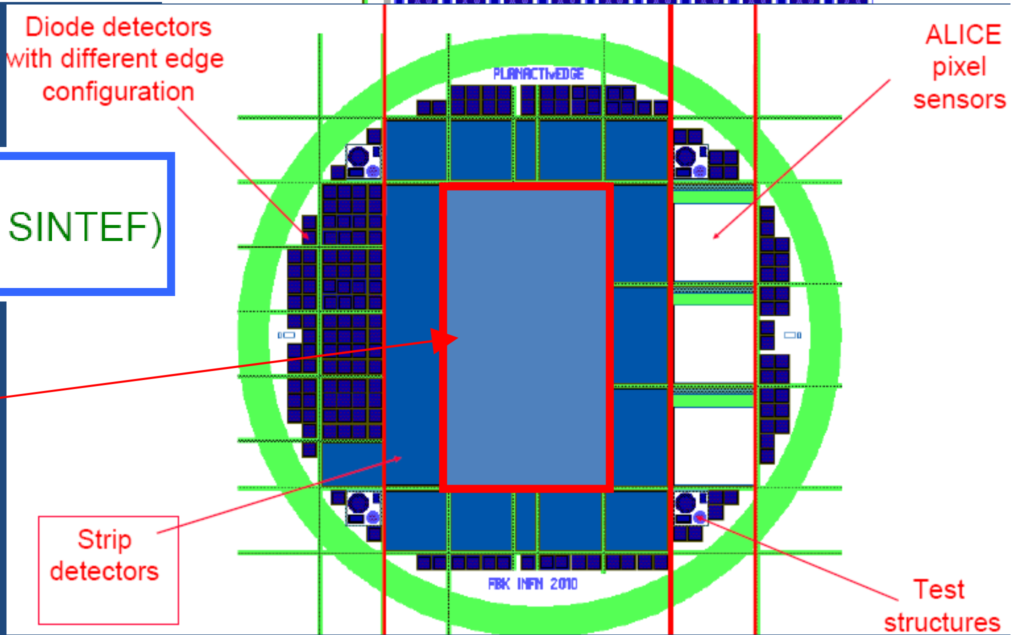
(2.5x5.0 cm^2, 498 read-out strips, pitch 50 μm, with floating strips)



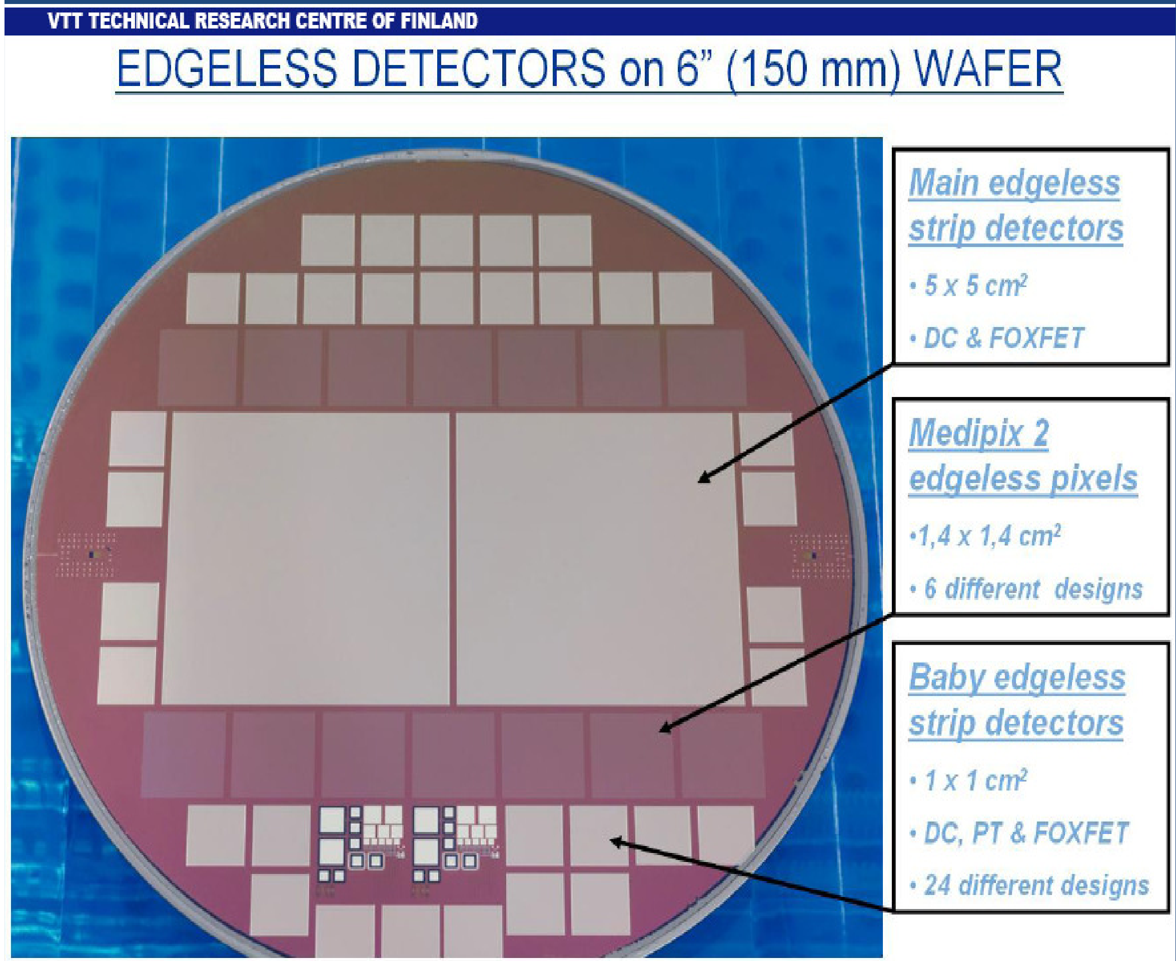
Planar – active edge.

Started, 18 wafers with bonded support (made at SINTEF) to be completed by March 2010

A test module will be built by LPNHE with these new sensors (2x[2.5x5]cm2) read out with VA1 chips, To be ready for 2010 beam test (Nov)



SOI-like Edgeless strip detectors



(*courtesy Juha Kalliopuska*)

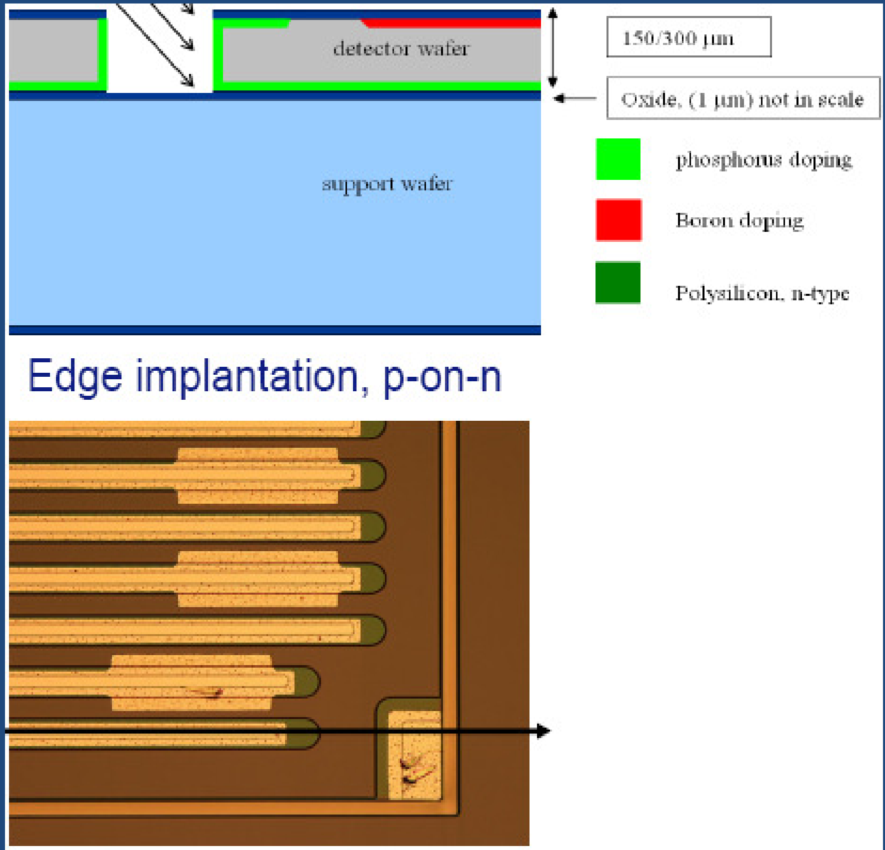
VTT achieved fabricating:

- edgeless strips & pixels sensors
- on 6'' SOI wafer
- based on alternative fabrication process w.r.t 3D processing with poly-Silicon filling
- Proving to be easier and more feasible fabrication line.
- Two different designs produced: p-on-n and n-on-n and
- Electrically characterized:

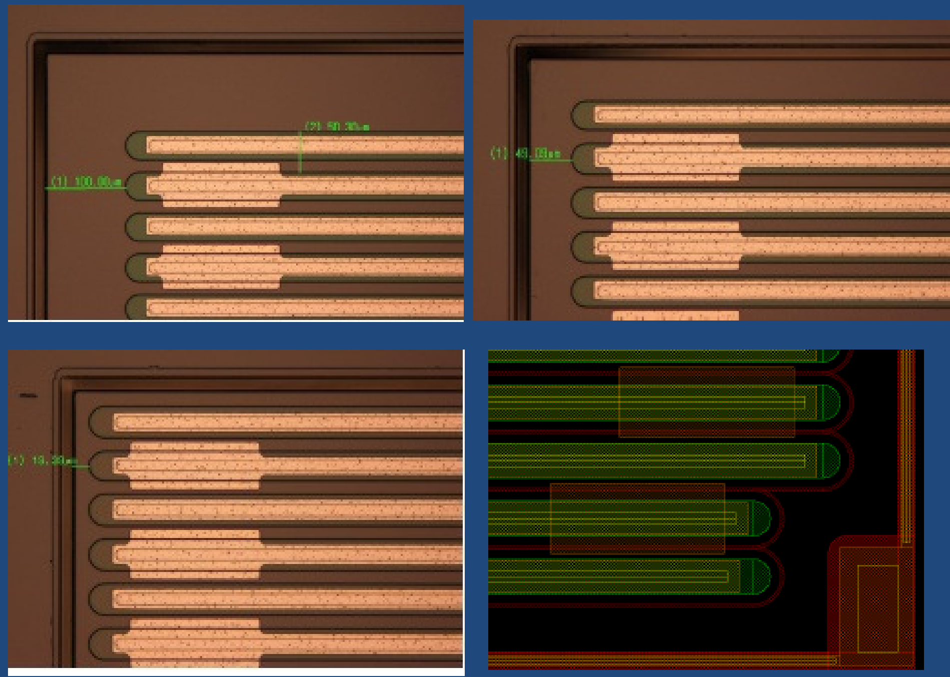
CV, IV and breakdown voltage

SOI Edgeless strip detectors

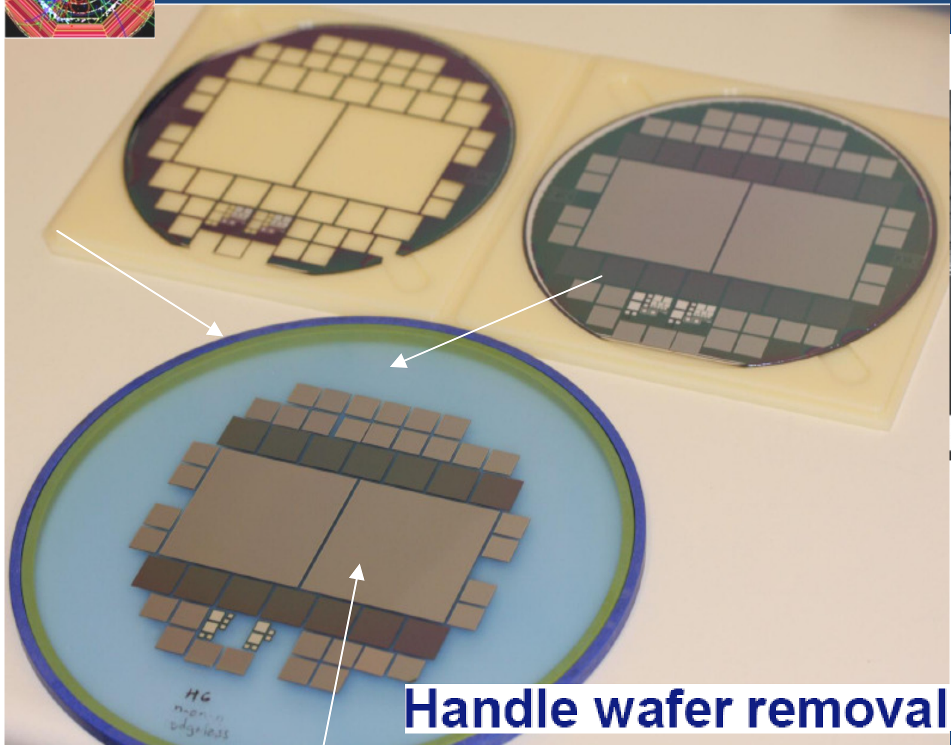
New fabrication procedure:



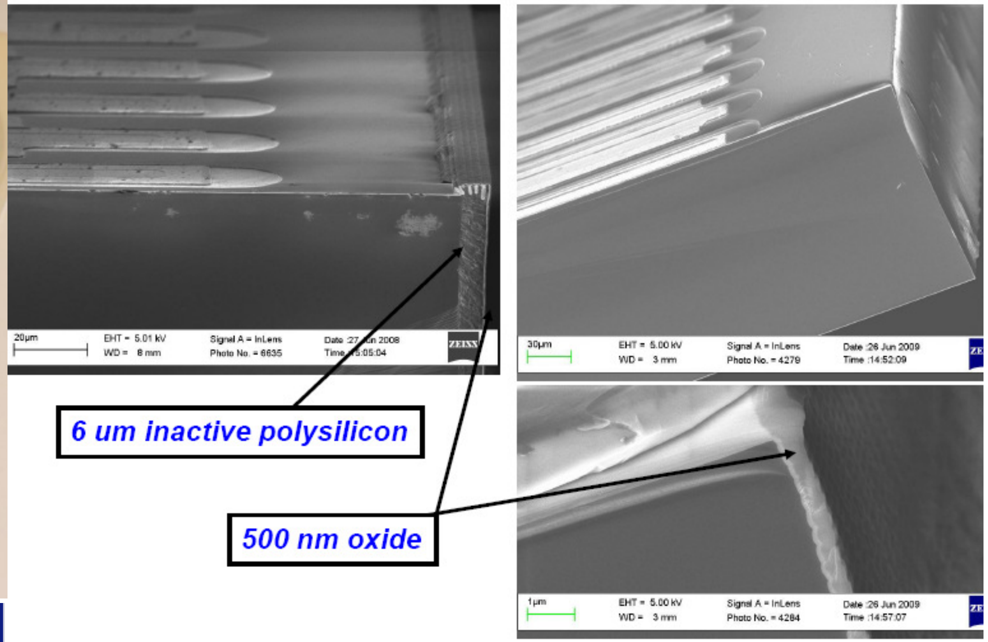
DC strip p-on-p & n-on-n designs with different active edges distances (100, 50 and 20 µm)



- No need for polySi filling, planarization & separate ICP dicing
- Fast process and no bowing of the wafer
- Detector sustain handling – no edge cracking
- Physical inactive edge region ~ 1µm
- Requires non-planar lithography => readiness available at VTT



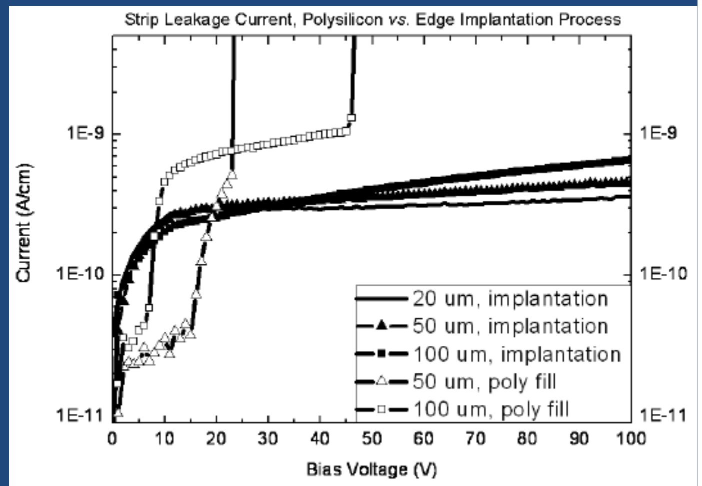
Poly process **Edge implantation**



Two such detectors at Lab in Paris for test

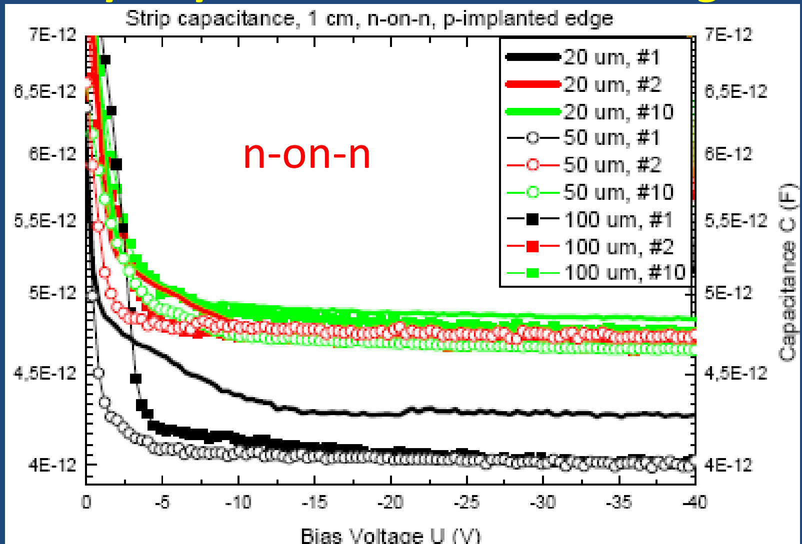
Strip leakage current: p-on-n implantation vs. poly

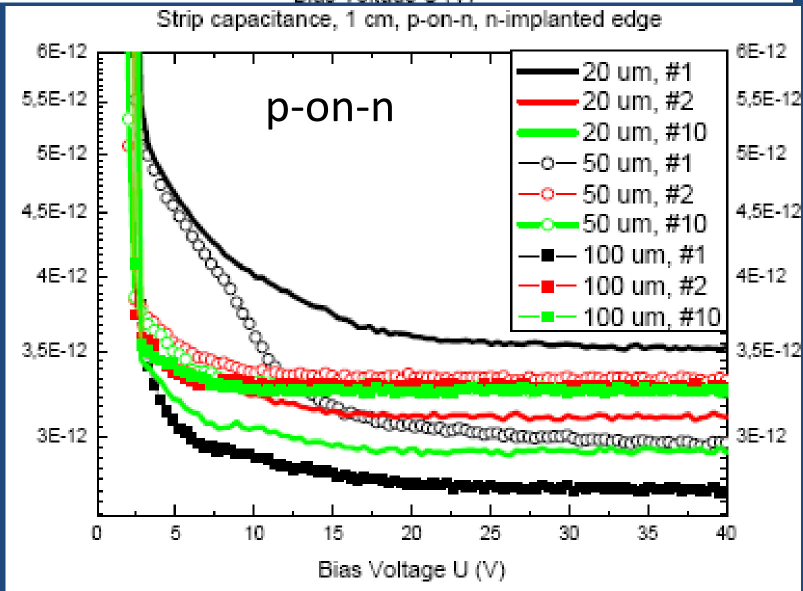
- Low leakage currents for both process approaches
- Very early breakdown voltages for poly filling
- Leakage current depends on the active edge distance



SOI Edgeless strip detectors: characteristics

***Strip capacitance vs Bias voltage*:**



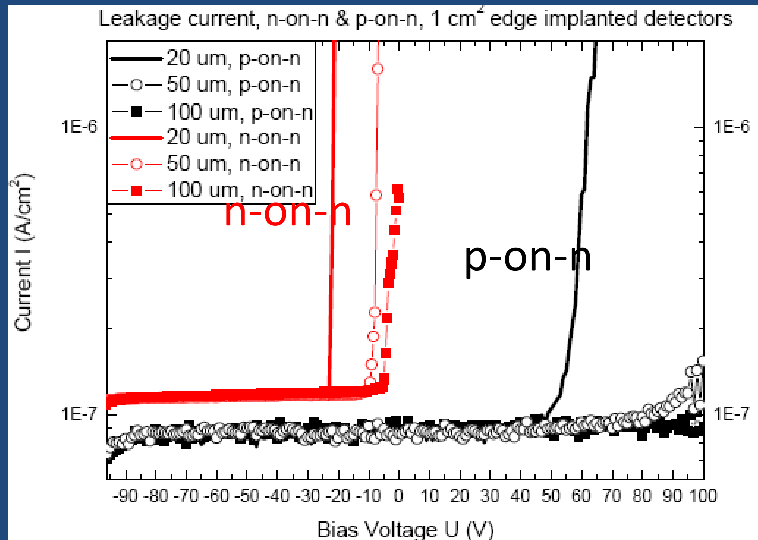


Front-to-backplane depletion: 7V (p-on-n)
4V (n-on-n)

Full depletion: 25-40V (p-on-n)
13-25V (n-on-n)

Strip capacitance of 3 to 3.5pf/cm (p-on-n) (about 2 to 2.5 worse than planar strips)

Leakage current vs Bias Voltage



Looks promising!

SiLC will compare these two edgeless technos including on prototyped devices at test beams

3D based technology developments: short strips and pixels

Interest for higher granularity &/or thinner devices (examples later)

➢ **3D based short strips (fabricated by FBK-irst)**

FONDAZIONE BRUNO KESSLER

Since 2009 collaborative contacts IRST-U.of Trento/LPNHE in SiLC on developments of short strips (1-2cm) based on 3D technology. We can benefit from the advantages of 3D without suffering of the high strip capacitance of these strips.

Goals:

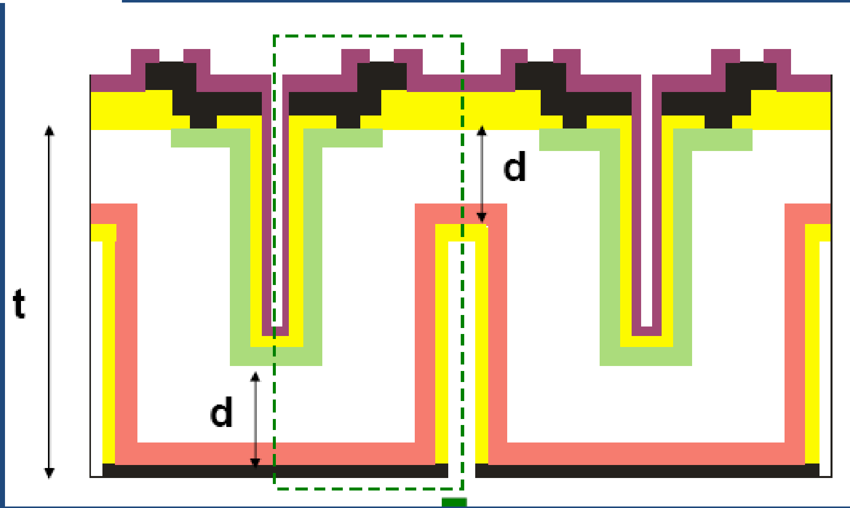
1)Use first the recycled 3D-DTC-2b batch with non passing-through columns (see next slide), to build first short strip based detector area for test beam equipped with VA1' reference read-out.

2)3D-DTC-3: n-on-p, 250 µm thick substrate, full 3D detectors and passing through columns.

New double-sided process defined, no need for support structure, allow dual read-out strip. Available fall 2009, for test in 2010.

3DDTC-2b produced by FBK

Courtesy Gian Franco Dalla Betta

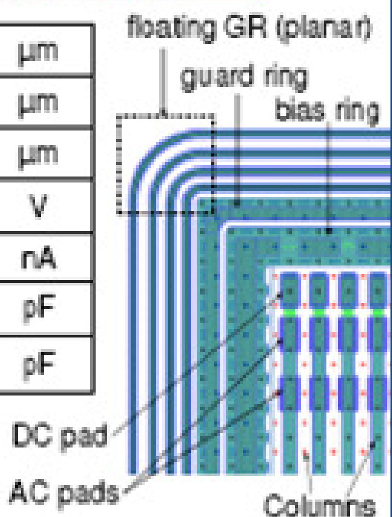


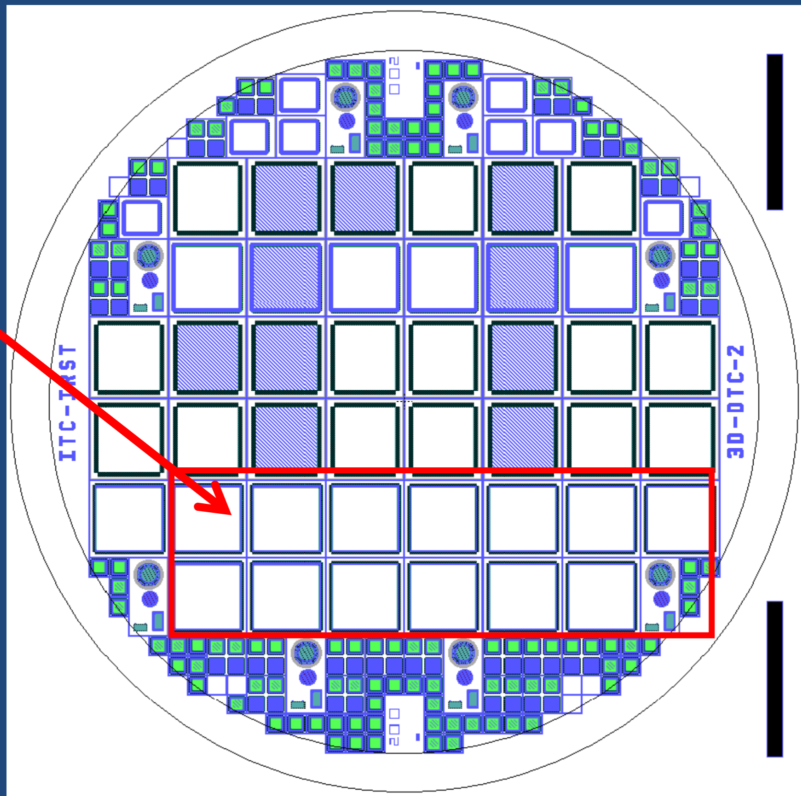
Batch	3D-DTC-2b
Substrate type	p-type
Substrate thickness (μm)	200
Junction column depth (μm)	160-170
Ohmic column depth (μm)	190
Completed by	April 2009

Microstrip detector features

Substrate thickness	220	μm
Junction column depth	120	μm
Back column depth	190	μm
Lateral depletion	~20	V
Strip leakage current	~1	nA
Strip capacitance	~7	pF
Coupling capacitance	50	pF

102 x 102 columns array
80μm inter-column pitch





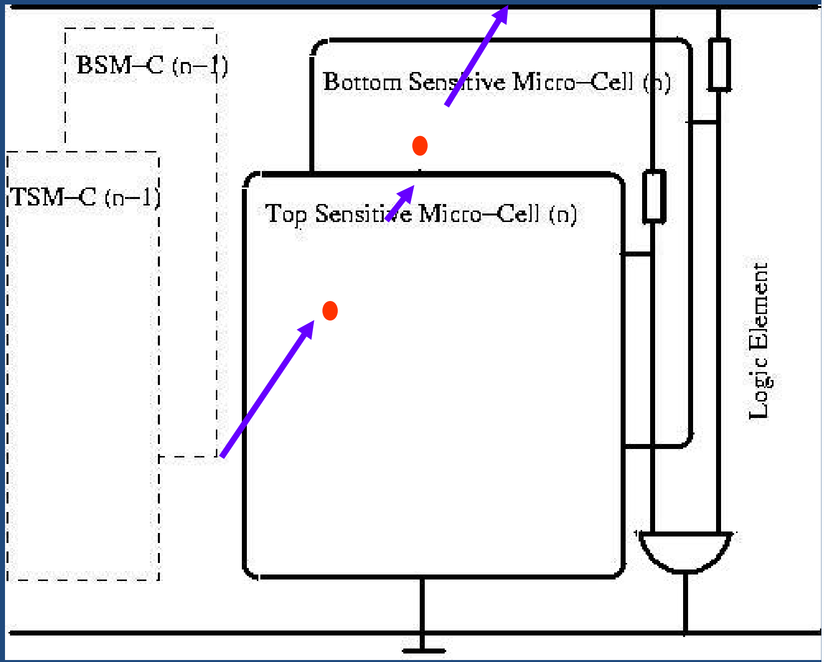
Low material budget & high intrinsic gain 3D pixels

Avalanche Pixel Sensor (APS) for Tracking (NRNU-Obninsk)

NRNU Obninsk

PRINCIPLE:

The charged particle crosses two identical breakdown mode microcells on top and bottom of the wafer. Two breakdown processes are thus created and produce the output coincidence signal. The quenching elements stop the avalanche processes. Then the microcells recover from the breakdown state.



Courtesy V. Saveliev

Low Material Budget & High Gain 3D pixels:

Main parameters:

✓Pixel sizes: 10x10 up to 100x100 µm²

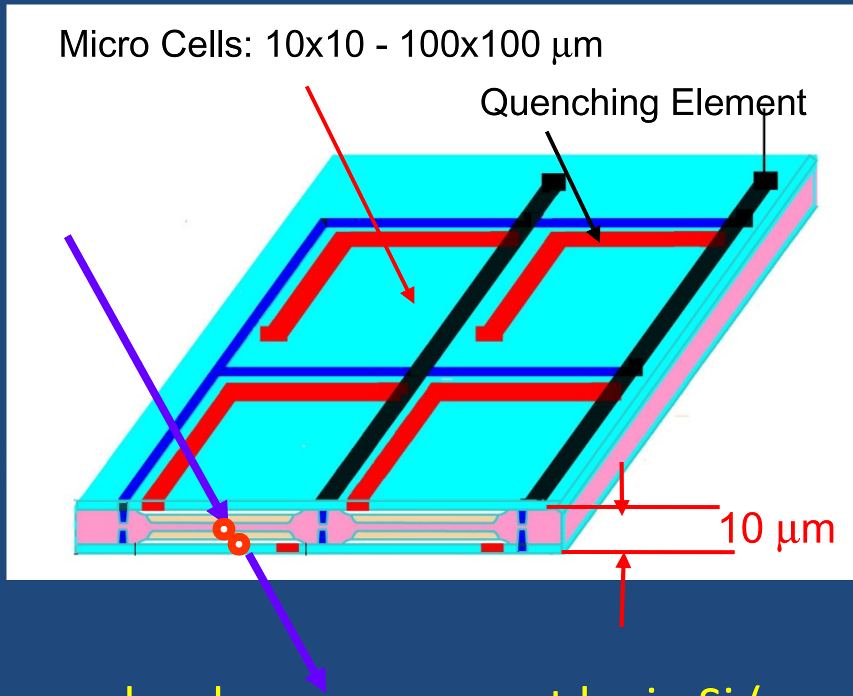
✓ Intrinsic Gain (breakdown mode) equivalent ~10⁶ :

✓ Thus fully digital device

✓Thickness of the detecting structure: 4µm

✓ Operating conditions
- Low Operational voltage ~ 50-60V
- Room Temperature
- Non sensitive to Magnetic Field
- No need for Analogue VFE

✓ Standard CMOS technology
So easy mass production

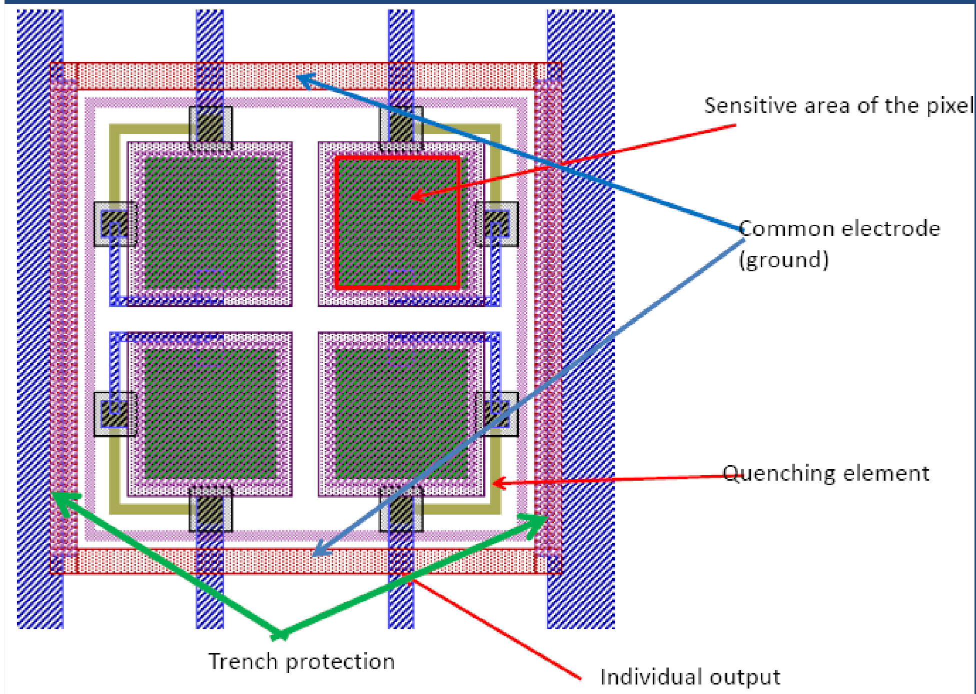


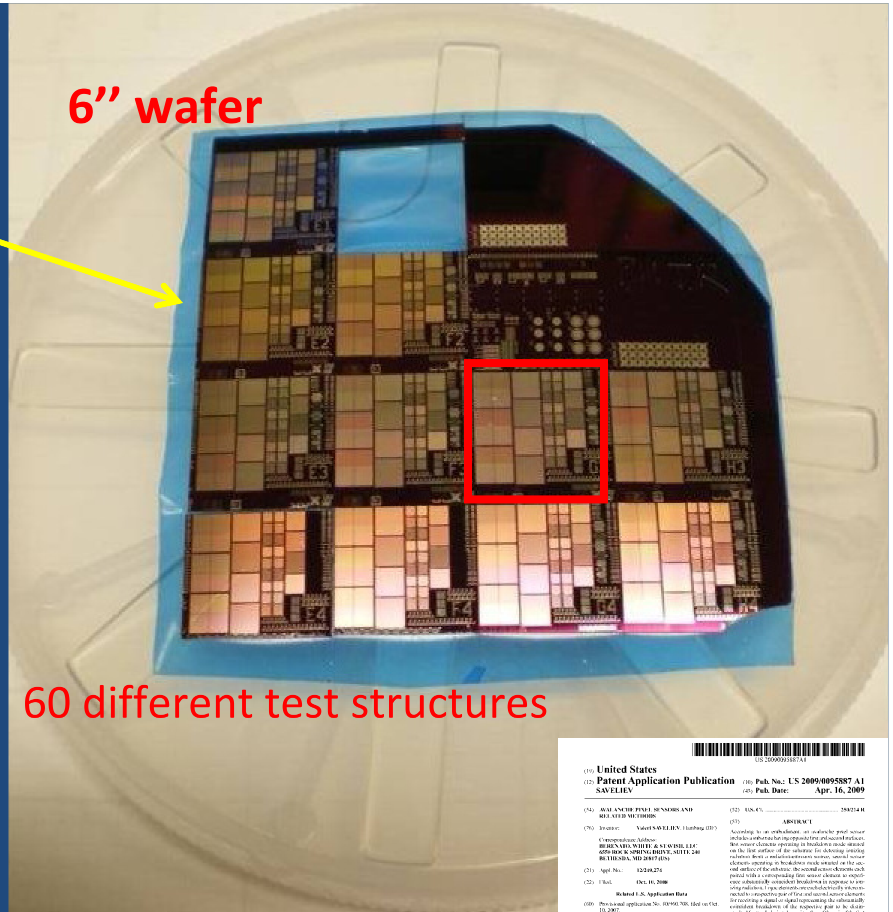
✓ The quenching elements for quenching the avalanche process must be in Si (passive)

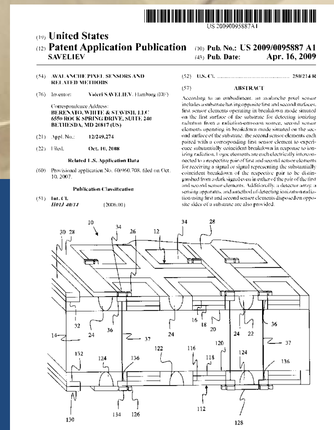
APS Manufacturing by:

KOTURA Inc. Monterey Park Ca (USA)

Ex : test structure made of 4 indpt. pixels 25x25µm^2





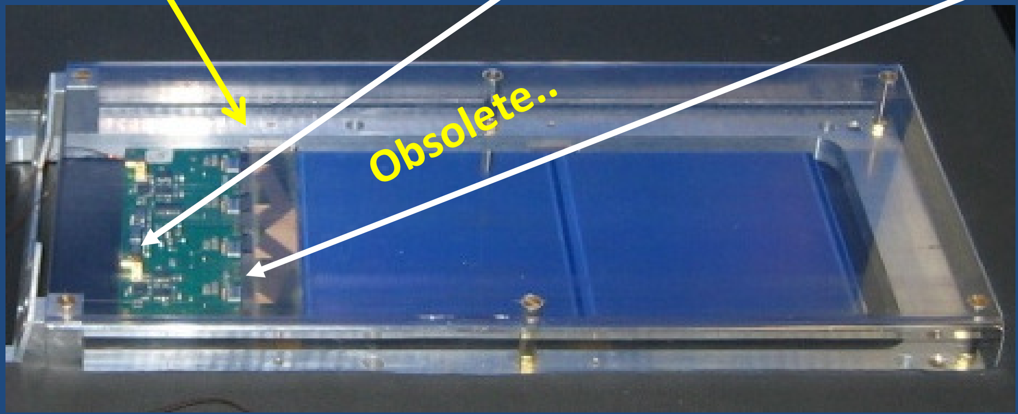


Manufactured APS by KOTURA will be further characterized by SiLC , including test structures both at Lab and test beams (beam telescope prototypes) in 2010

Direct connection sensors-FEE

Major R&D objective: NO MORE Hybrid FEE board +pitch adapter

⇒New module concept under development



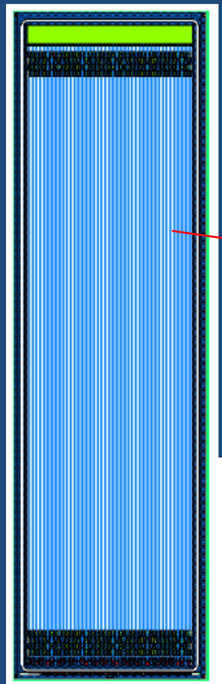
ALL-in-ONE SOLUTION => direct connection of FE chip on the sensor

- ❖ material budget,
- ❖ simplification of elementary module (tile) and
- ❖ of overall detector construction (burden put on sensor and FEE chip),
- ❖ improvement in performances
- ❖ Use high tech advances (cost?)

SiLC is pursuing with the different steps: wiring onto the sensors: HEPHY + Polish firm (proto at CERN t.b); bump bonding: HPK+LPNHE (proto sensor+FE chip in 2010); going in // to 3D vertical interconnect (part of the worldwide 3D interconnect effort)

+ ITE (Poland)

Sensors with integrated pitch adapters



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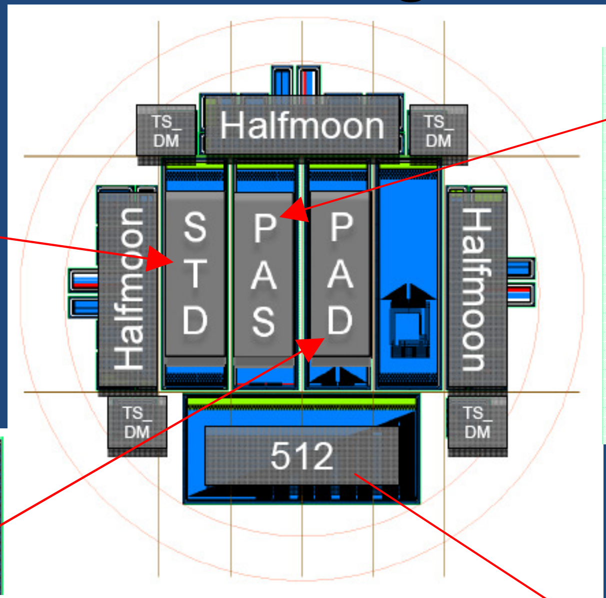
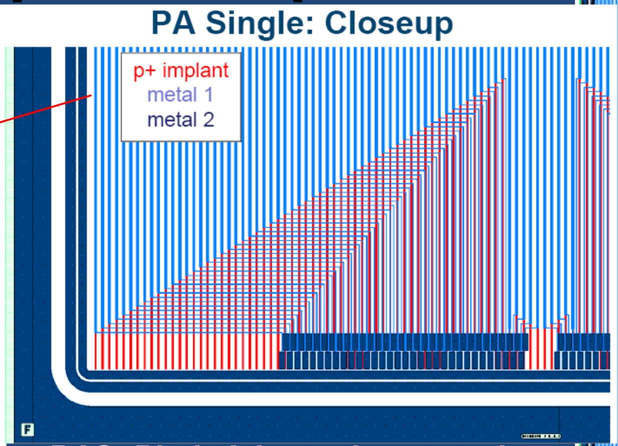
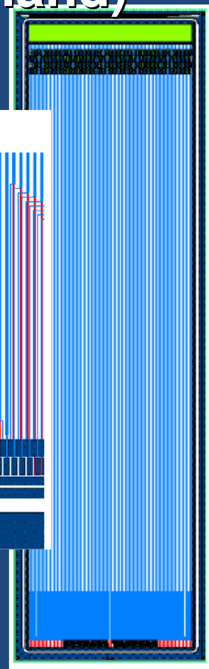
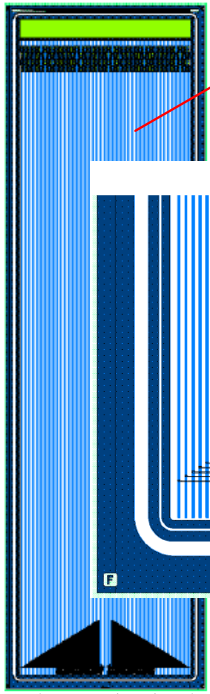


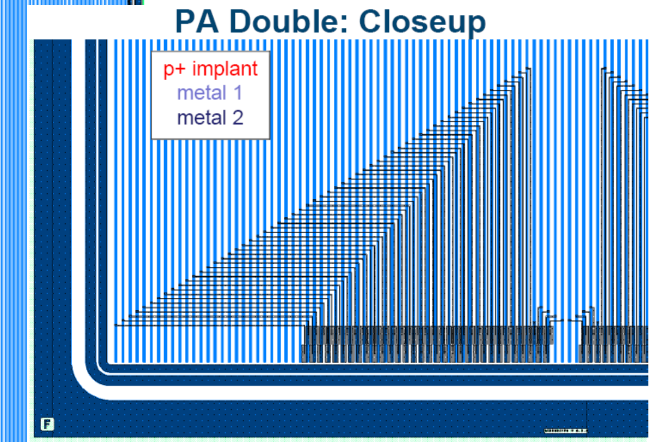


PAS=Pitch Adapter integrated with Single metal layer

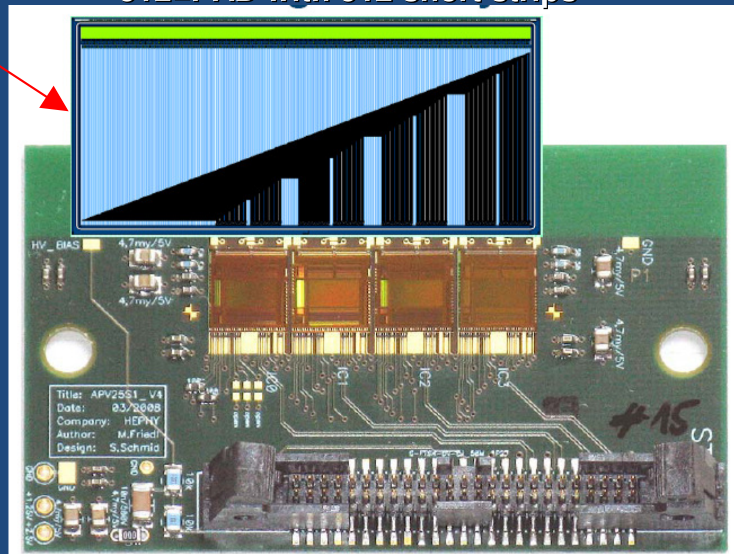




PAD=Pitch Adapter integrated with Double metal layer

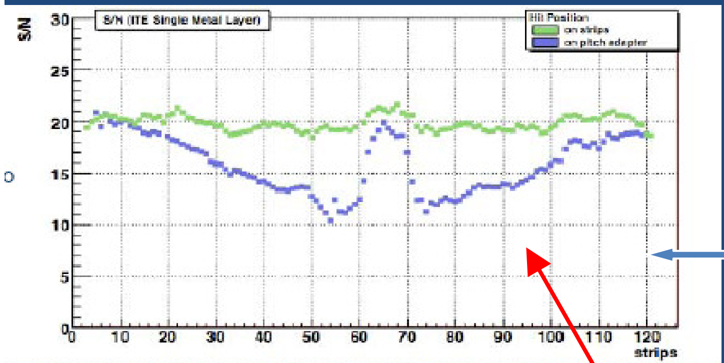


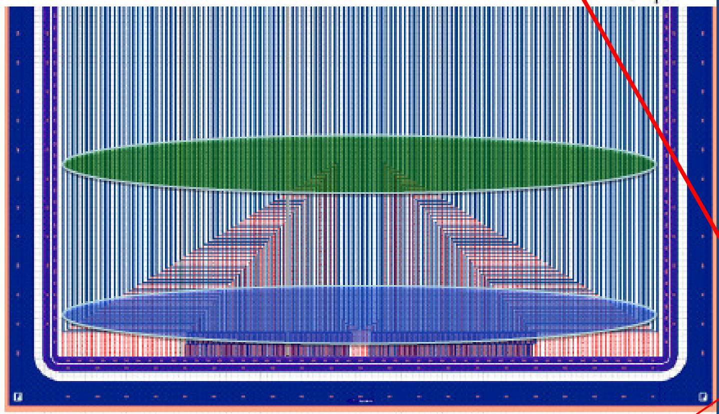
512=PAD with 512 short strips

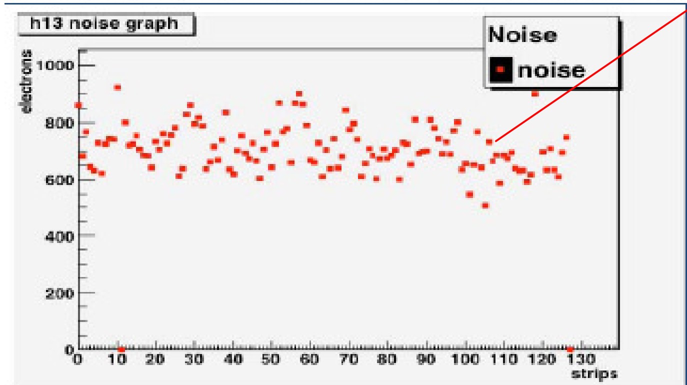


Courtesy of Th. Bergauer

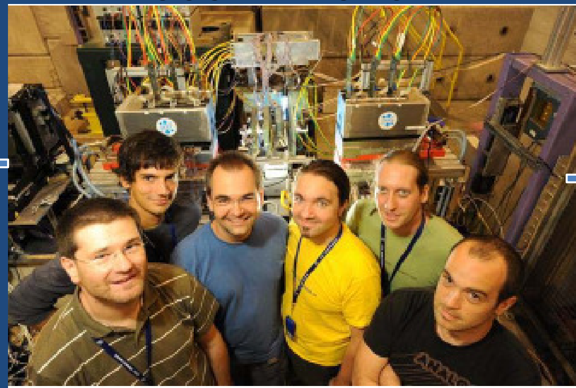
Test beam at SPS-beam 2009 → 2010







Results from 2009 test beam



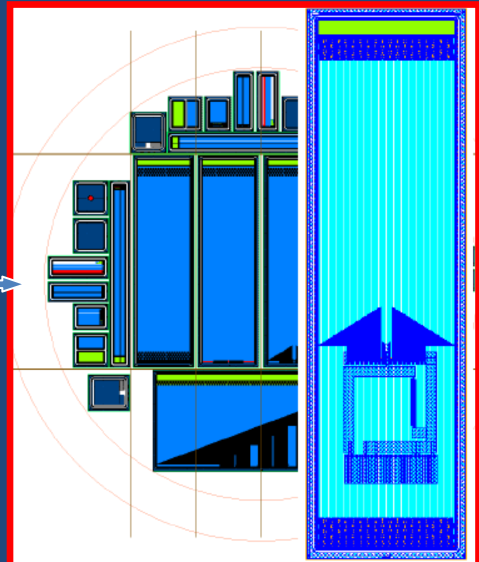
Courtesy Th. Bergauer

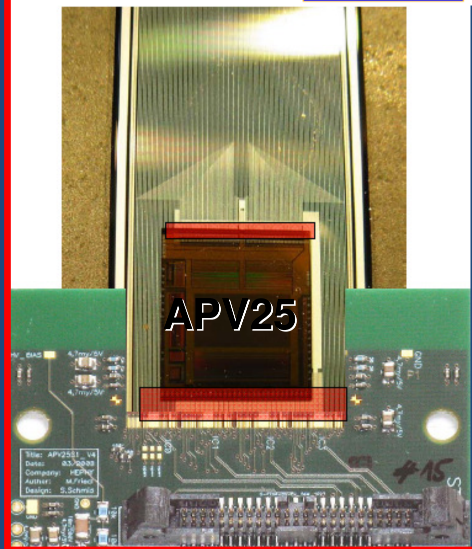
Not due to noise increase but to signal loss

Reason:

- capacitance of integrated coupling capacitor gets extremely low when metal strip moves away from implant in routing region
- Remedy: routing on dedicated, second, metal

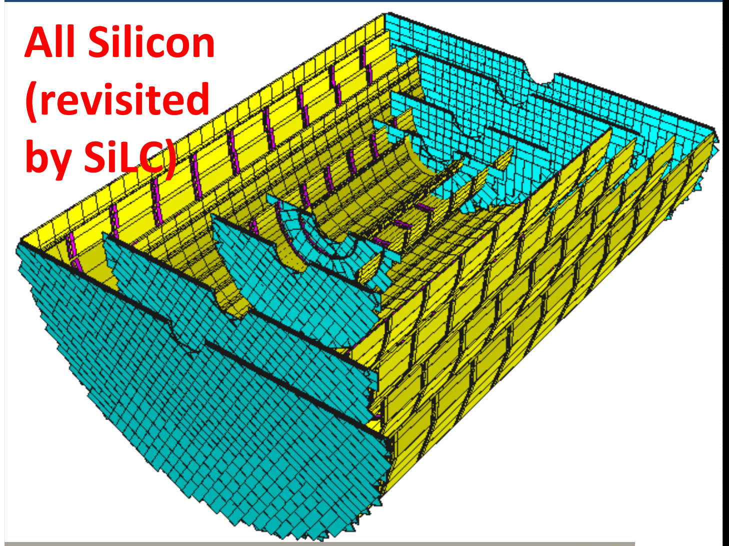
Next: to be tested in 2010

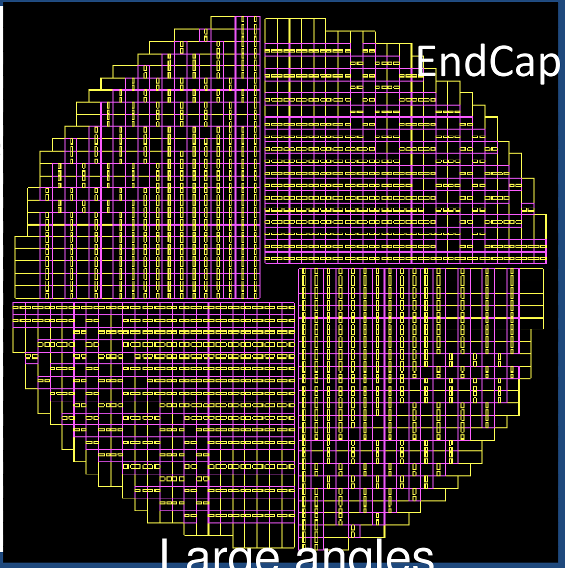


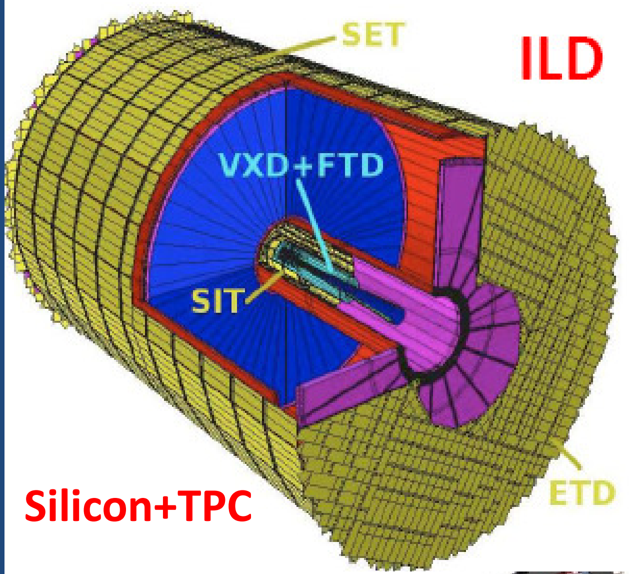


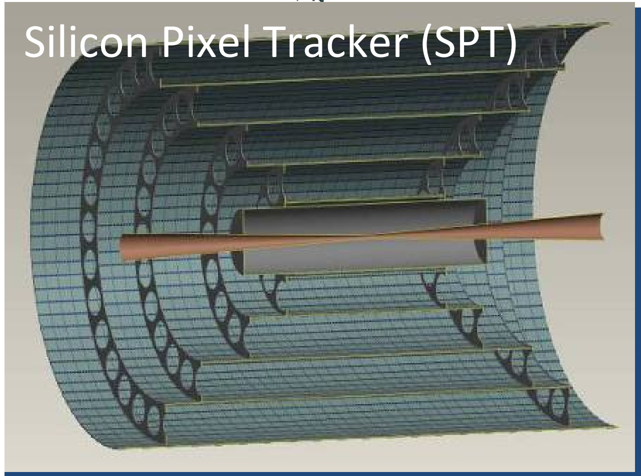
Chip glued on sensor: wire or bump bonding

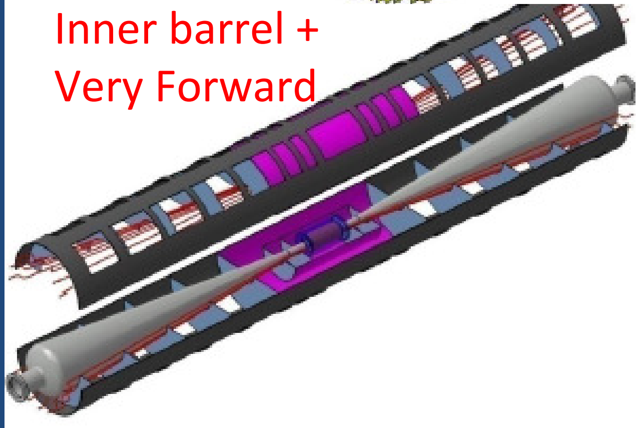
Tracking concepts at LC: All-Si vs Hybrid











Geant4 based simulation: edgeless strip detectors with a unique sensor type (but SPT)

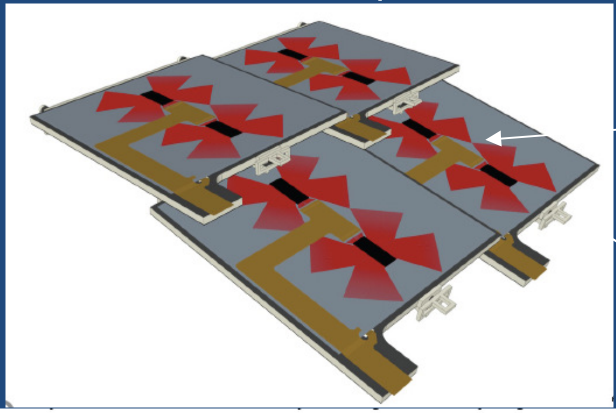
Detail study performed already for LOIs. Going for a ready -for -construction design end 2012.

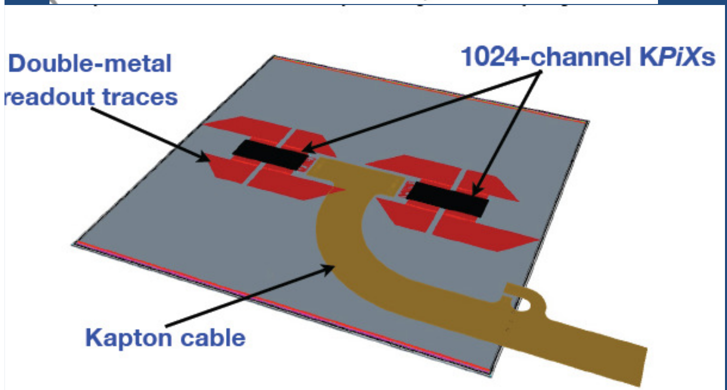
An All Silicon tracker for ILC

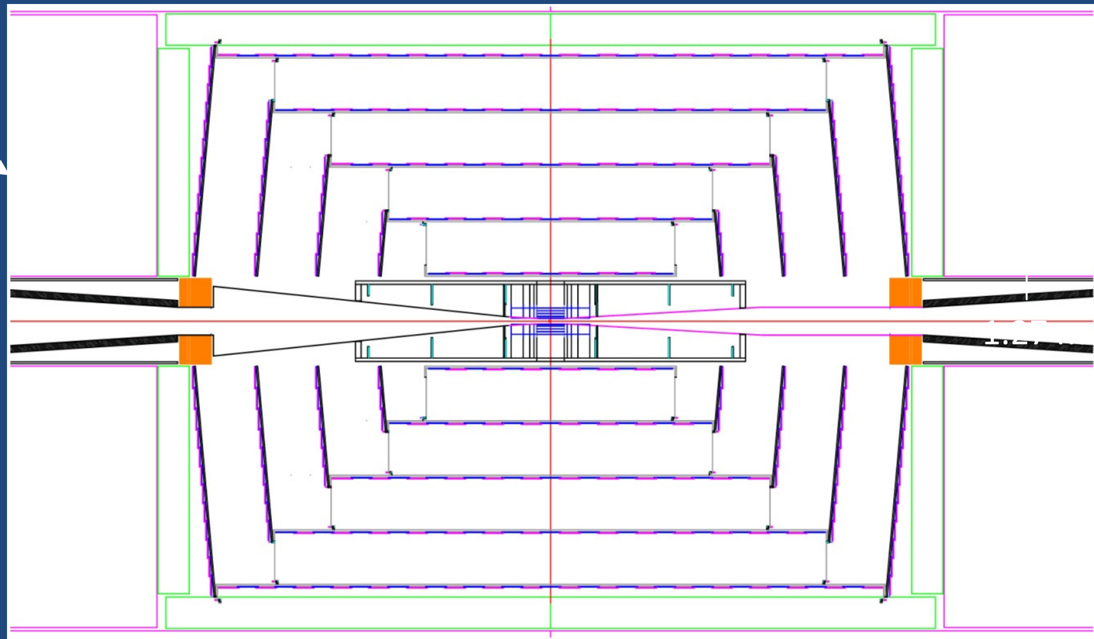
~100 m^2 Si Strips: Barrel single sided (r-ϕ); endcaps double sided

Courtesy SiD

Modular low mass sensors tile CF cylinders







~10 cm x 10 cm; 320 μm thick; 25 μm sense pitch; 50 μm readout (prototype fabricated); S/N > 20; <5 μm hit resolution

Bump bonded readout with 2 KPiX chip; no hybrid

KPiX measures amplitude and bunch # in ILC train, up to 4 measurements per train

Pulsed Power: 20 μW/channel avg; ~600 W for 30 M channels; gas cooling

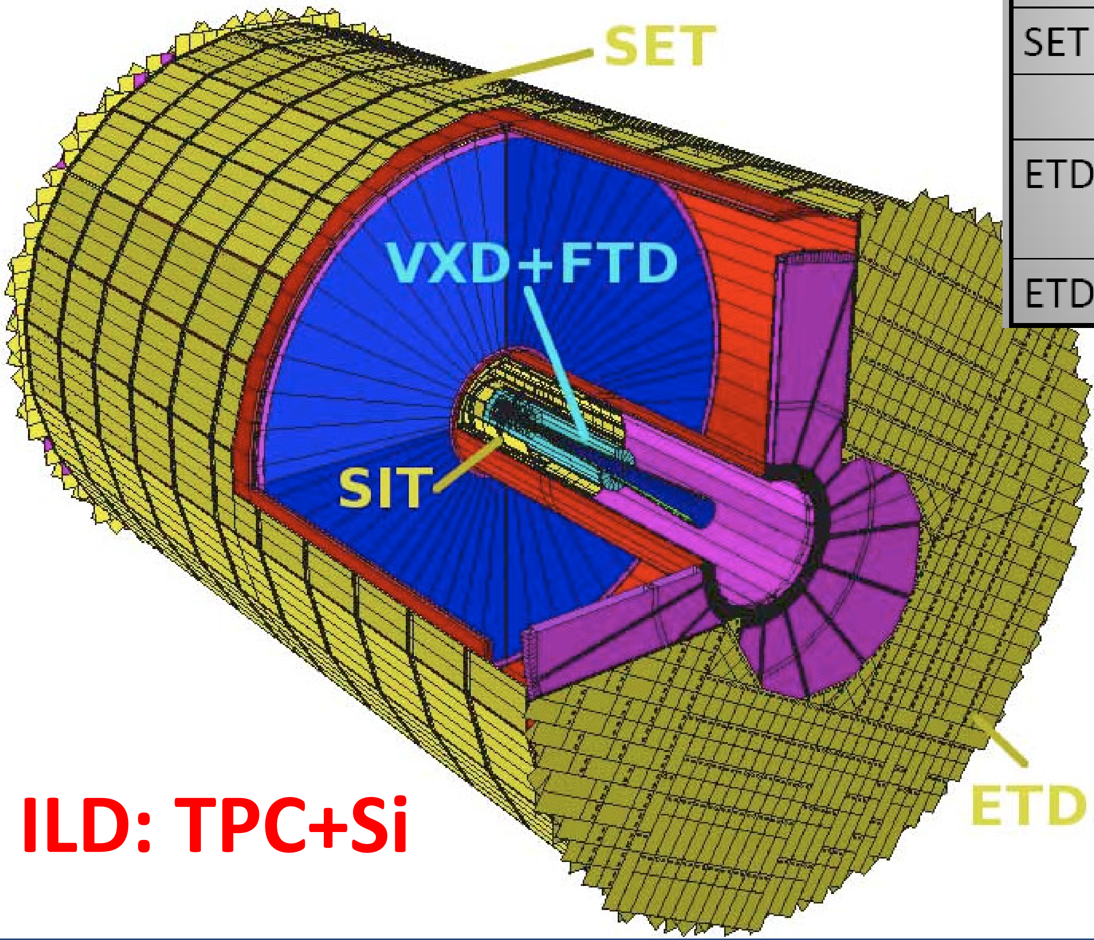
SiLC is revisiting this design applying some of its new ideas and advances

ILD Hybrid tracking:

The Silicon Envelope

(in numbers as currently in the ILD LOI)

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30



ILD: TPC+Si

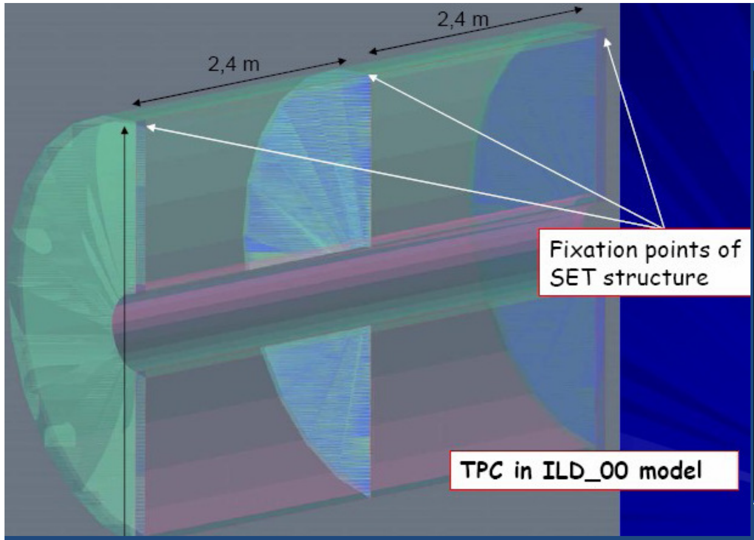
Total number of channels:
10^6 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD) = **$10\ x10^6$ channels**

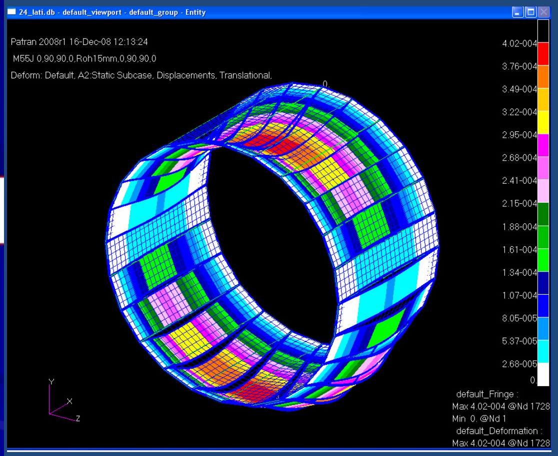
Total area:
7 (SIT)+110 (SET) +2x30(ETDs) = **180 m^2**

Total number of modules:
500 (SIT) + 2500 (SET) + 2000 (ETDs)=
5000 modules with unique sensor type **(but for FTD)** but ***variable strip length*** (10-30 cm) depending module location.

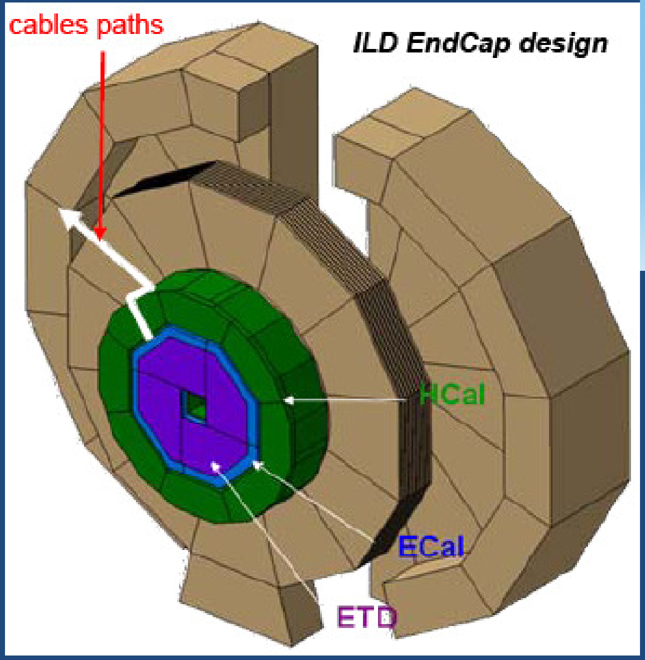
GEANT4 simulation **(here)& mechanical design** (CATIA) in progress

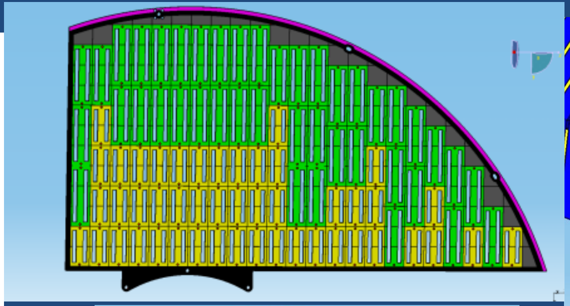
SET/ETD: CAD & INTEGRATION

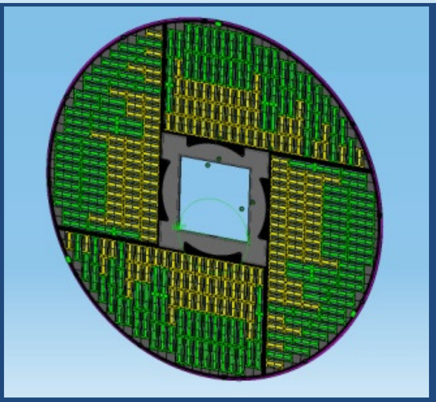


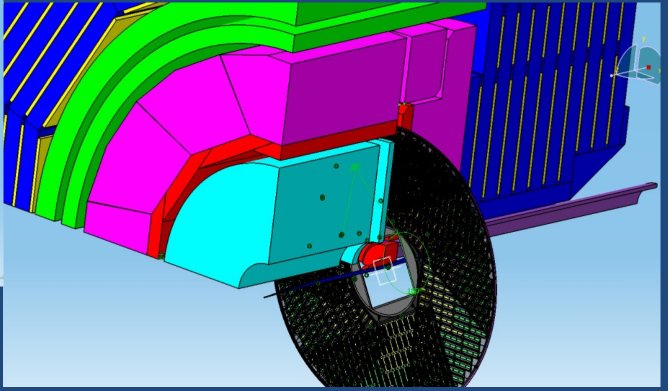


Restarting work on CAD design of the SET and SIT/SET possible common support (Torino)









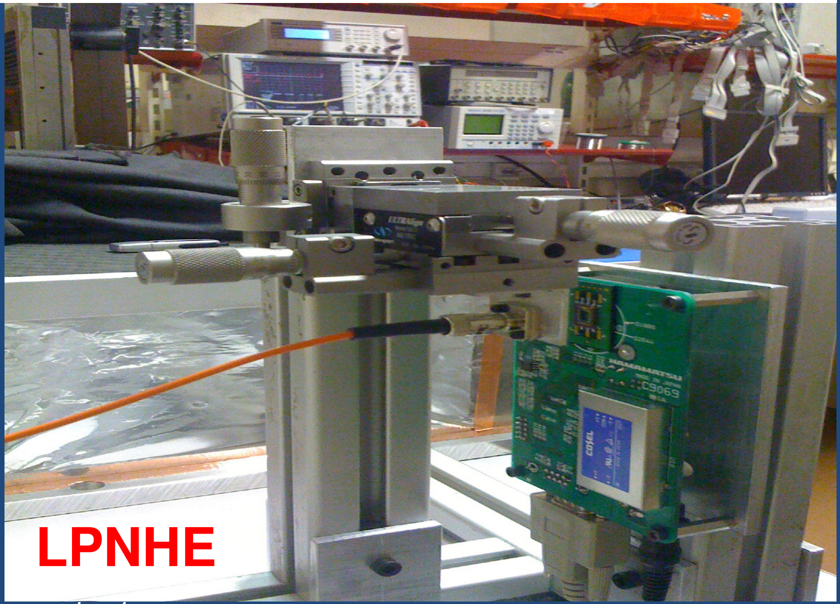
Progress made on detailed CAD for ETD (LPNHE)
=> to be pursued with calorimetry and full integration design

Main issue: alignment

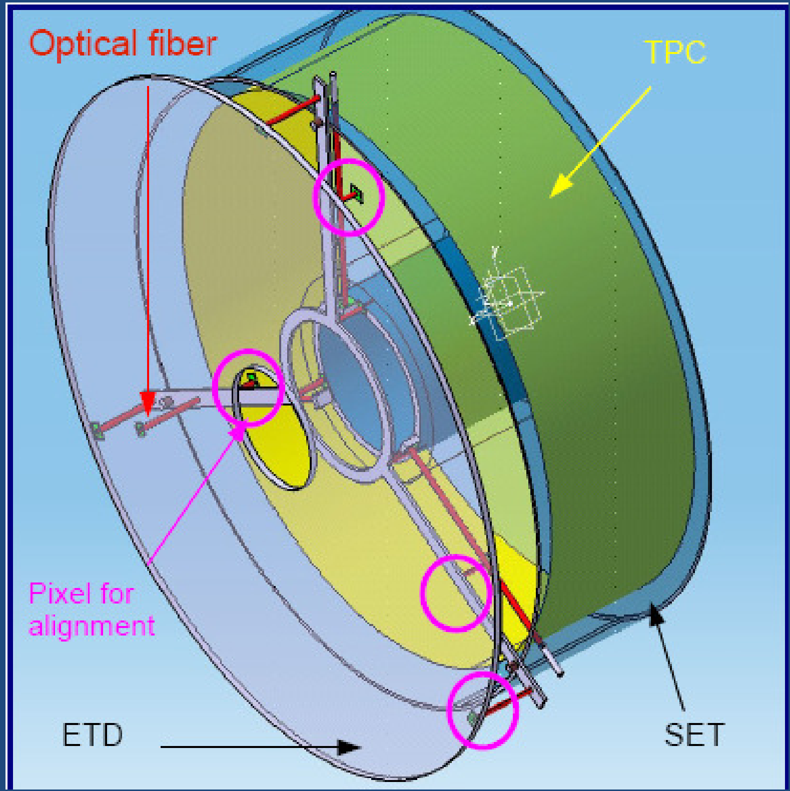
- Alignment between several layers as developed by AMS experiment and then in CMS: better adapetd to an all-Silicon tracking but in the ILD case; need more =>
- ***Alignment between different Silicon components & between Silicon and other tracking components***: crucial aspect in a hybrid tracking system as the case for ILD (TPC+Si)

•<u>Purpose:</u>
→ monitoring of the relative displacement of the STS and TPC/VXD (push-pull and environmental vibration)

•Laser + dedicated pixel sensors at the strategic position. All parts are equipped:
- with sensors for alignment
- direct optical fibre



ALIGNMENT SYSTEM BETWEEN COMPONENTS



- Feasibility studies and conception of this calibration in progress at Lab test bench

The Silicon Pixel Tracker (RAL & Oxford U.)

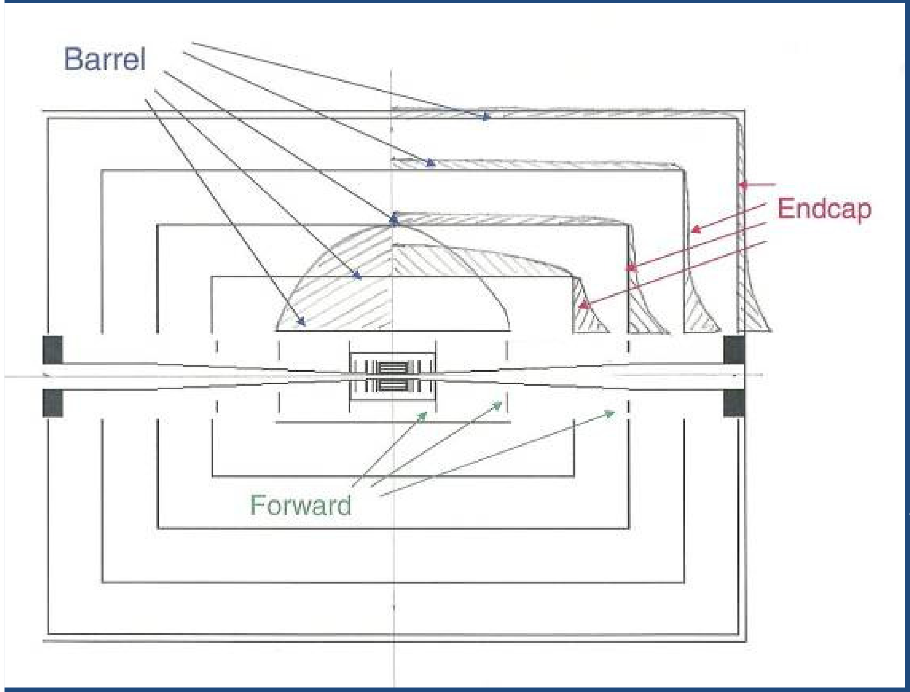
Courtesy of C. Damerell

Among the motivations:

- Develop a tracking system of unprecedented **transparency** **(aim: 0.6% X0 /layer)** so that nearly all photons down to 7° θ_P will convert in the ECAL, and complications due to hadronic interactions in the tracker will be rare.

-Maximise performance: pixels provide unambiguous space points on each layer.

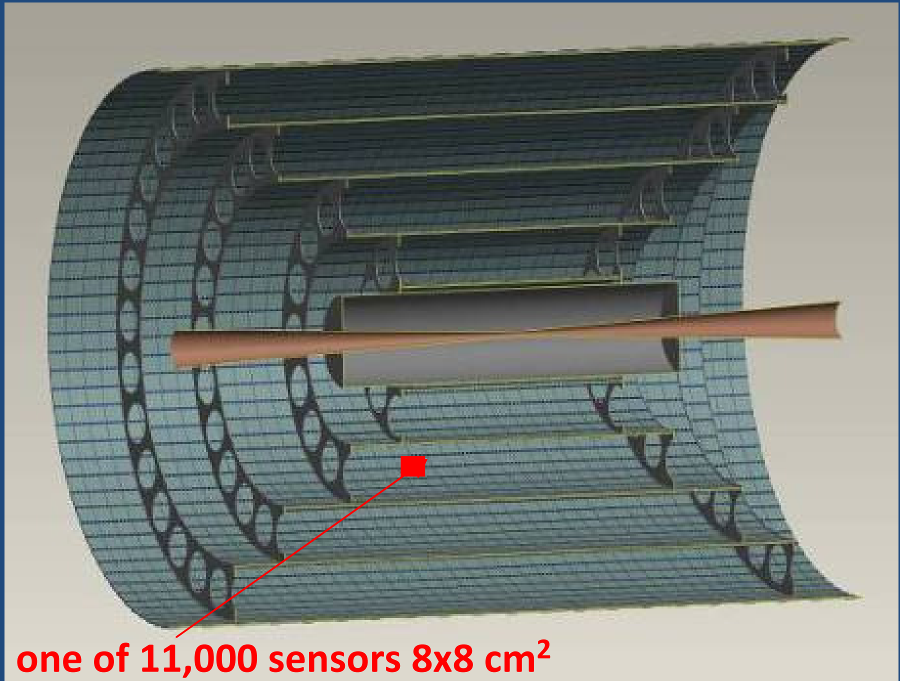
- Basic principle is to strip out all feature that aren't strictly necessary, and which would increase the material in front of the calorimeter



Proposed pixel technology CCD CMOS (see ISIS talk)

- **Total hit density ranges from 2.5/cm²/train (layer 1 barrel) to 1/10 of that (outermost barrel)**
  - **occupancies in SPT are everywhere < 10^{-4}**
- **Forward disks: densities exceed 600/cm² /train, so pixels with short sensitive windows will be needed. But area to be covered is small.**

SPT preliminary design (RAL/Oxford)



The mechanical issues of such a detector design are addressed : The expertise from LCFI R&D is instrumental

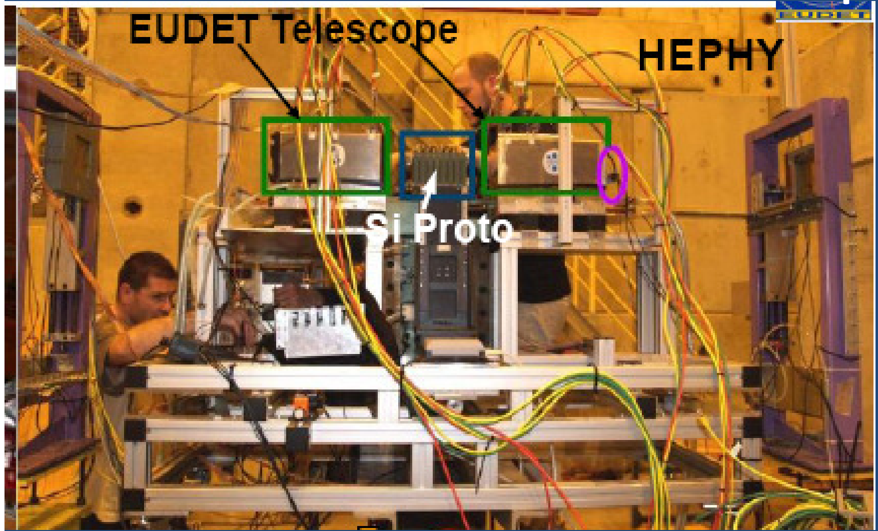
(*See Yining Li's talk on ISIS for the Currently proposed technology by RAL/Oxford)*

Some features: ~0.6% X_0 per layer, seems achievable , 3.0% X_0 total, over full polar angle range
Unique pixel size of 50 μm diameter
30 Gpixels, in line with trends in astronomical wide-field focal plane systems by 2020 ***(multi-Gigapixel focal plane arrays in astronomy (eg LSST))***

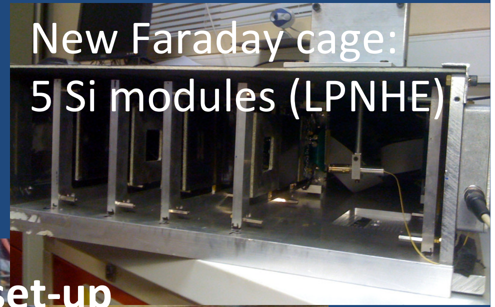
SiLC has included this line of research in its actual work plan but studying various possible pixel technologies: Beyond Baseline Alternative.

Each R&D aspect evaluated in realistic test beam conditions

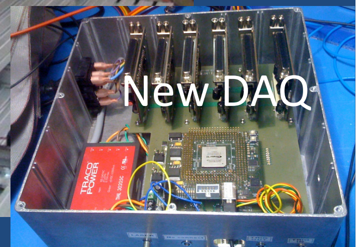
Combined test with EUDET MAPS telescope at SPS.



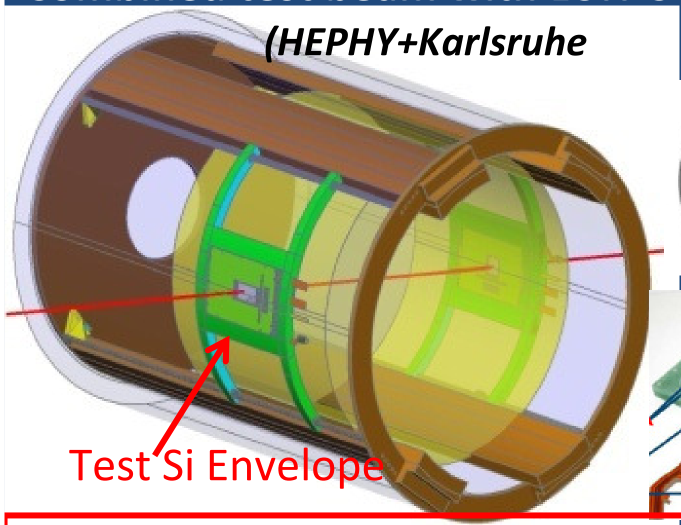
Multipurpose SiLC standalone test beam set-up



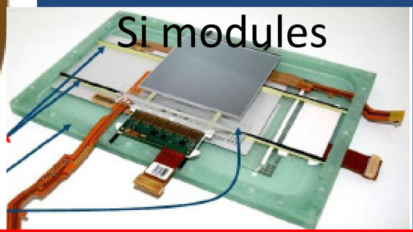
Prague
ICFA
LPNHE
Torino



Combined test beam with LCTPC (DESY)



Mechanical support



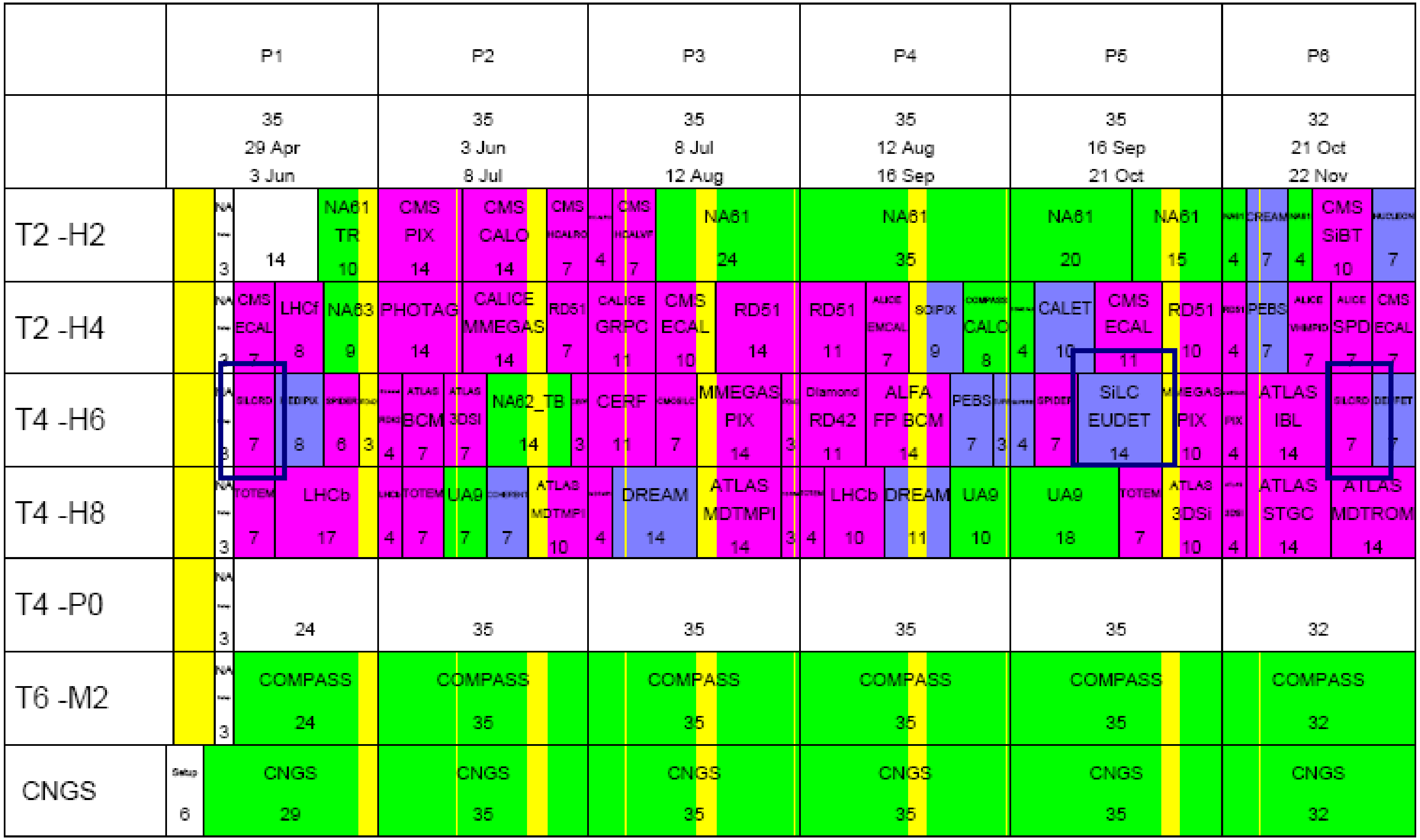
In preparation 2010-12: combined test beams with calorimeters
Tests on new FEE, new sensors;
Larger size prototypes

=> Expertise on prototype construction, developed FE, DAQ and analysis for test beams since 07

26-February-2010 2010 SPS Fixed Target Programme

Version 1.0

Colour code: green = SPS-exp ; purple = LHC-exp ; dark blue = Outside exp ; yellow = not allocatable or Machine Development



SPS/PS-Coordinator: Horst Breuker

E-mail: SPS.Coordinator@cern.ch

phone: 73777 (ext. +41 22 767 3777)

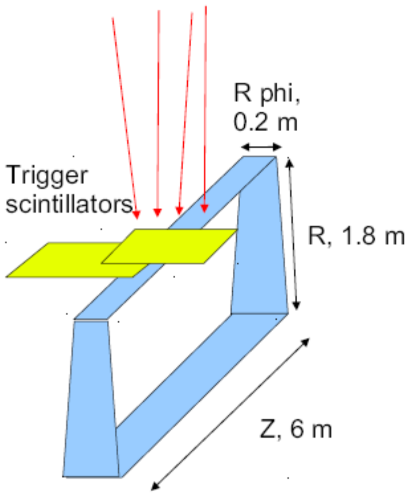
mobile: 164212 (ext. +41 76 487 4212)

Comments:

- no comments

Combined test at CERN with ATLAS tile calorimeter in 2010

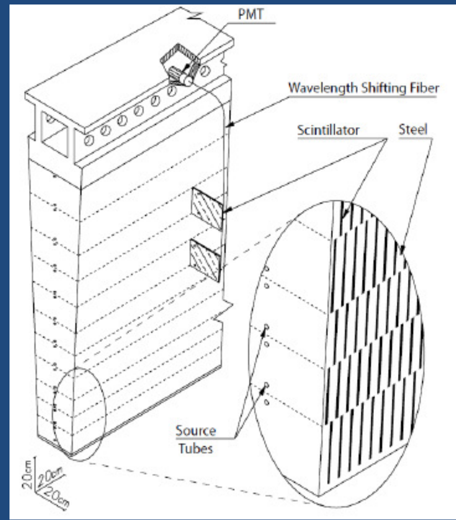
Cosmic setup at CERN-Meyrin, B175



Interest:

- Measure z coordinate of the impact point and phi
- Precision:
  - z: < 1 mm
  - Phi: < 2 mrad
- Area:
  - ~100 mm z
  - ~200 mm R x phi
- Rate: 0.01 /cm^2 /s

- ATLAS Hadronic Calorimeter Tilecal
- Sandwich of iron and scintillator
- Segmentation period
  - Iron: 5+4+5 mm
  - Scintillator 3 mm



Possible arrangement

- 2 SiLC modules above
- Strips perpendicular to z
- Angular precision: 100 microns/100 mm=1 mrad
- DAQ: synchronized with common trigger and busy signals (at rate ~ 1 Hz/wafer should be no problem)

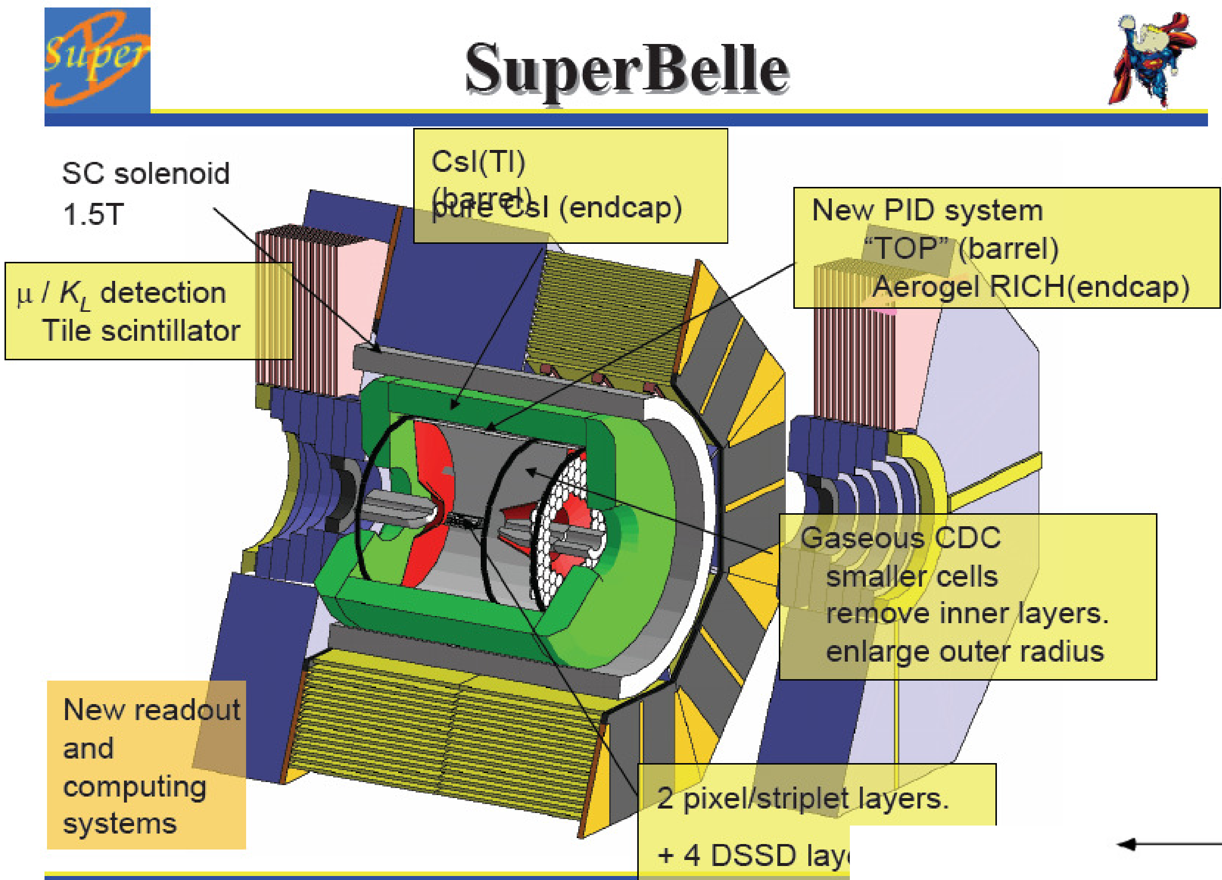
Synergies

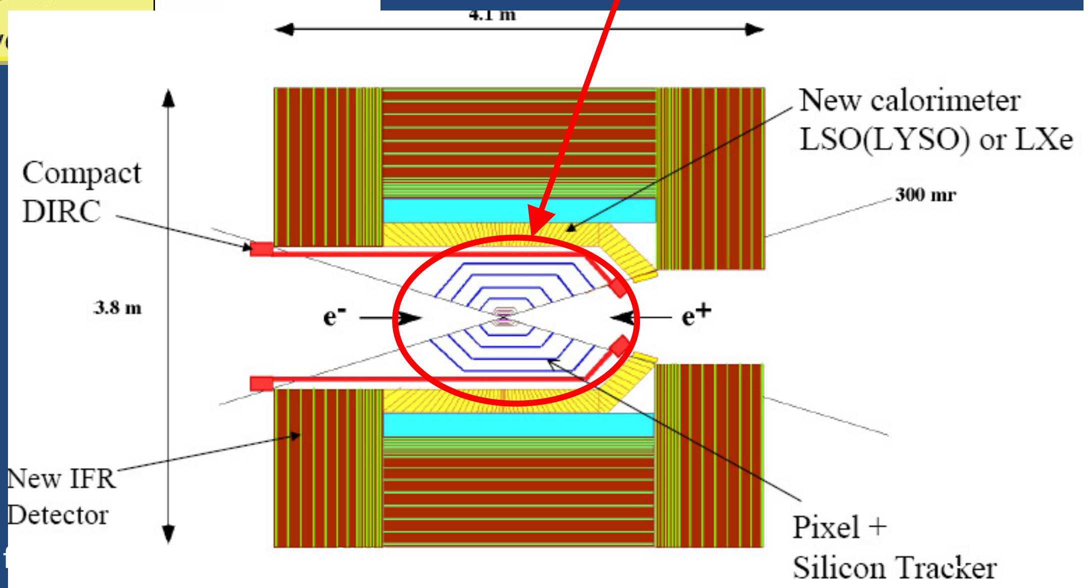
- LHC construction (since the very start of SiLC: many of the SiLC members have been main LHC Si tracking builders: ATLAS & CMS)

  Has been instrumental for the launching and progress of this R&D collaboration.
- LHC upgrades & SLHC: several of the SiLC members are actively participating to the ATLAS and CMS upgrades including for SLHC
- Other ready to start or projected experiments: BELLE II, future muon g-2/EDM at J-Parc…
- SiLC is developing still further these synergies

Synergy with SuperBelle Si tracker

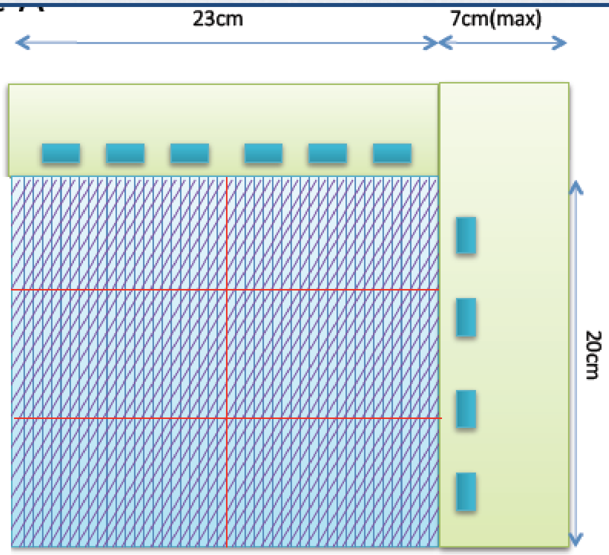
CU {Prague}, HEPHY Vienna, IEKP



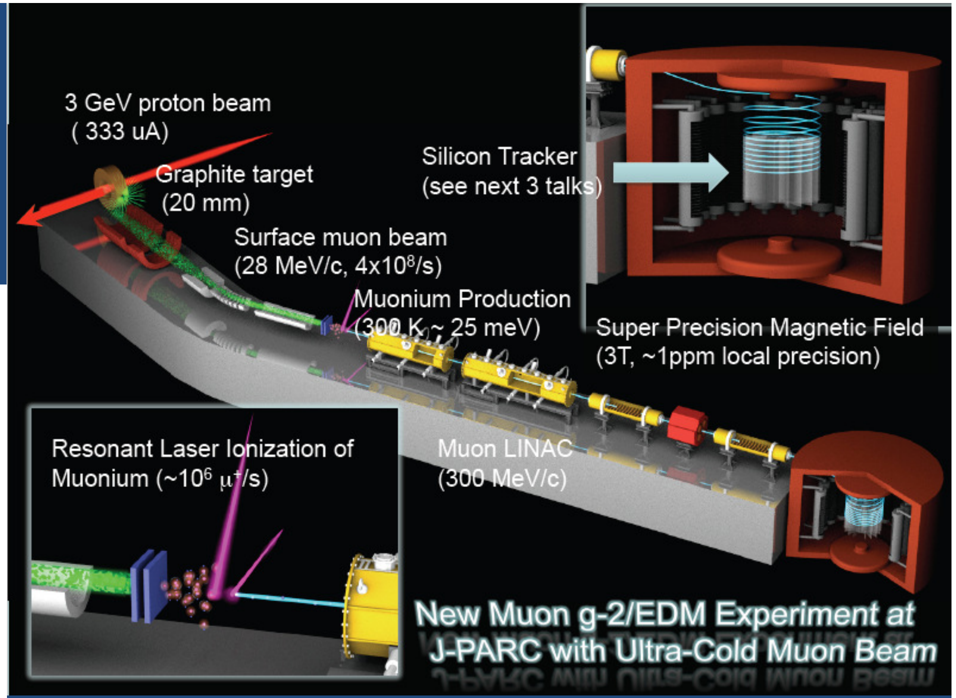


Detector Concept

- Tracking device with hi-rate capability
  - 5 K tracks in 33 micro seconds,
  - ~10 tracks in the first 7.5 nsec period
- Silicon detector would work → next three talks!

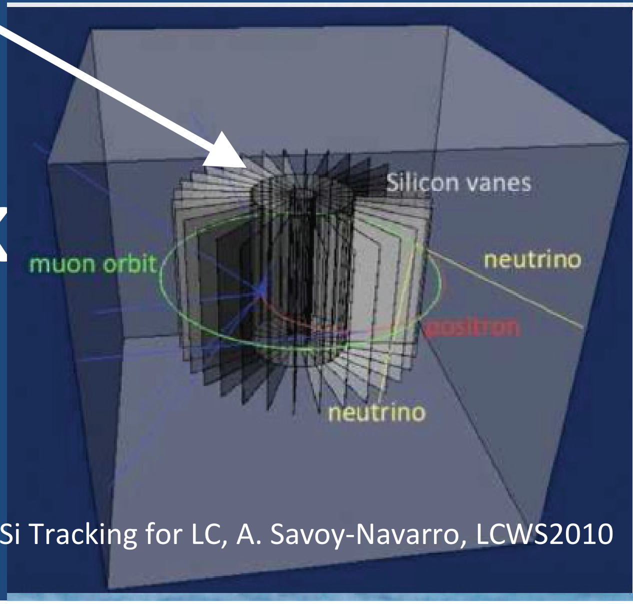


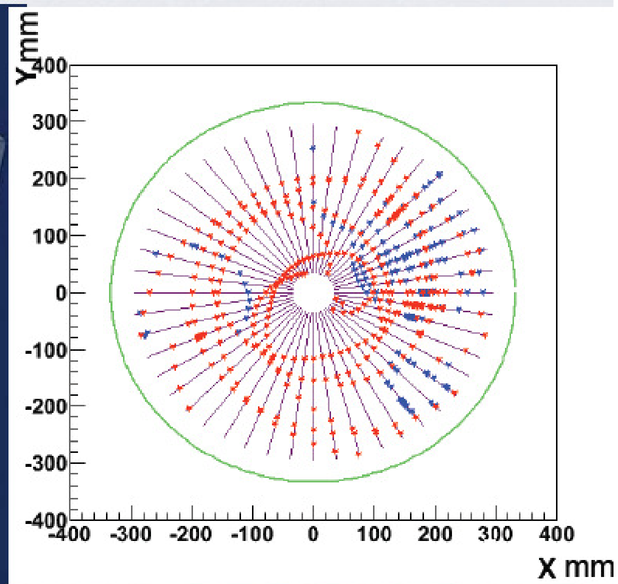
- Straight strips
  - Sensitive to radial coordinate
- Stereo strips
  - Sensitive to up-down coordinate as well
- ASD chips
  - Wire-bonded to the strips
- Sensitive area is covered by 6 sensors
  - connected by wire bonding.



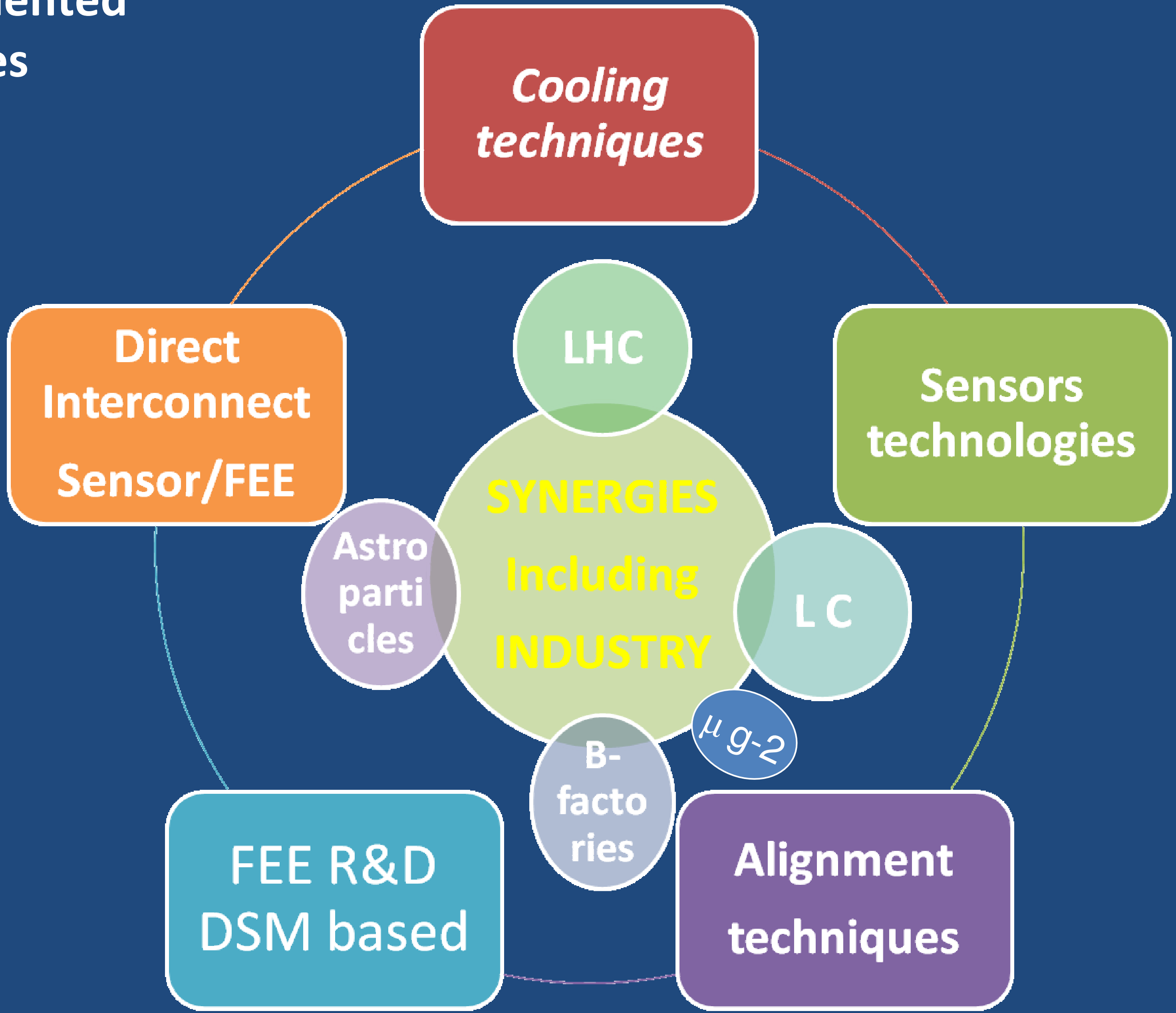
Courtesy of N. Saito in g-2 & EDM Workshop Paris, February 26-27, 2010

Synergy with New project at J-Parc-K





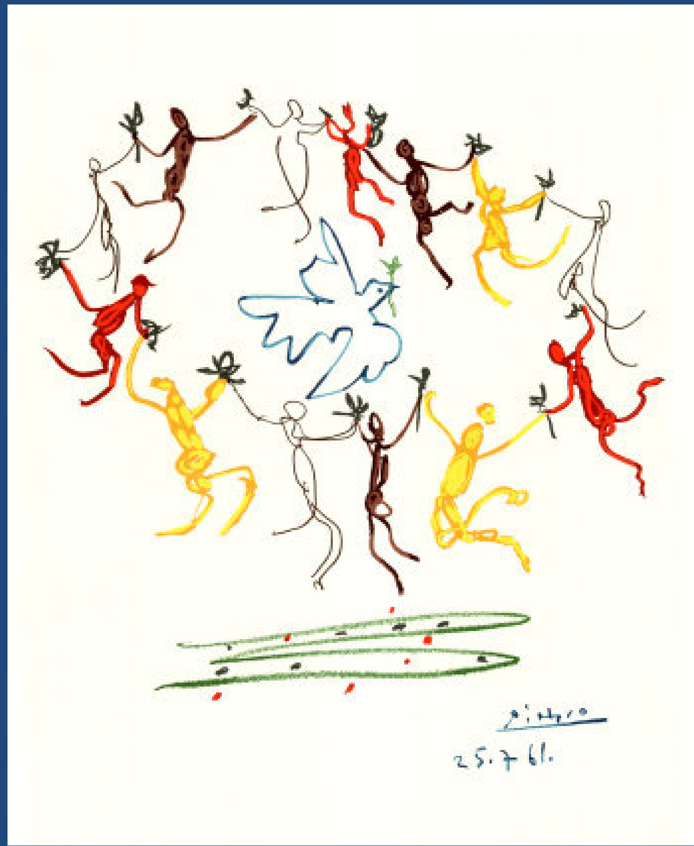
Experimented synergies



Conclusion & perspectives

- As for the other major sub-detectors, an active R&D is ongoing on Si tracking for the future LC , driven by a rather hard-line schedule (despite unknowns..): next major milestone in 2012 (a "ready-to-construct" TDR).
- Test beams are a major aspect for all aspects of this R&D. These next 2 years the prototypes will increase in dimension thus in cost!
- Tracking is a Key issue and semi-conductor based trackers play a major role in both tracking strategies (All Si or hybrid)
- Because unknown on time scale and machine(s), the R&D must provide "very soon" a "*conservative R&D line*" but also keep *an innovative R&D line*; the tracking we are proposing may/will be quite different of what will be built at the end (ex: SPT alternative).
- This applies first of course to the basic R&D objectives: sensors, FEE
-Key words: Synergies with other R&Ds on the field and collaboration with Industry.

As for all LC-R&D: FINANCIAL MEANS & PEOPLE are crucial issues!!



With many thanks to all the SiLC collaborators for their contributions to the preparation of this talk

With special thanks to Manuel Lozano, Marcos Fernandez Garcia, Thomas Bergauer, Stephan Haensel, Gian Franco Dalla Betta, Juha Kalliopuska, Simo Eranen, Valeri Saveliev, Chris Damerell. Thanh Hung Pham, Didier Imbault and collaborators, Alexandre Charpy, and many others...apologies to all the ones not mentioned here.