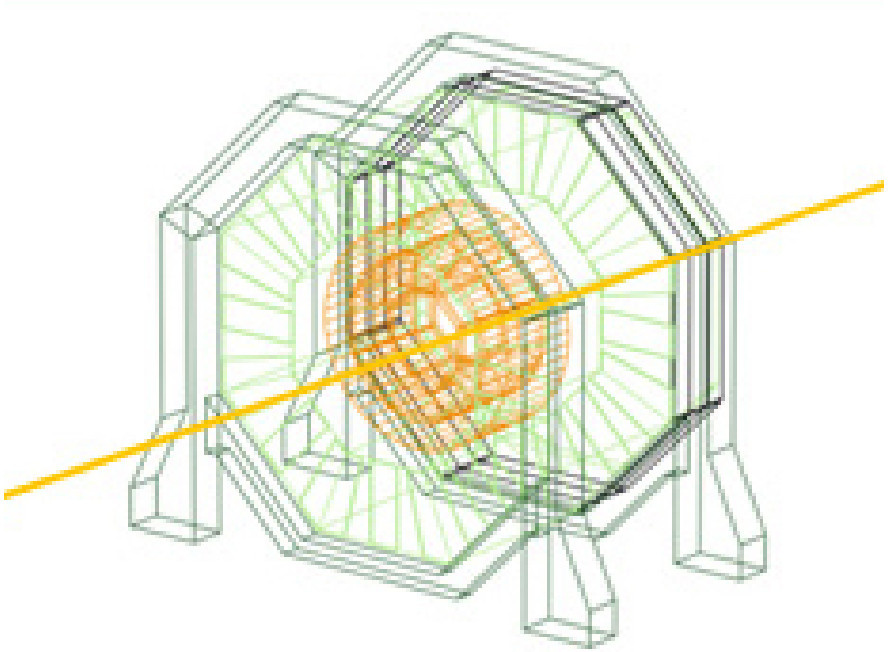
SiD Vertex and Tracking Detector

Status Report



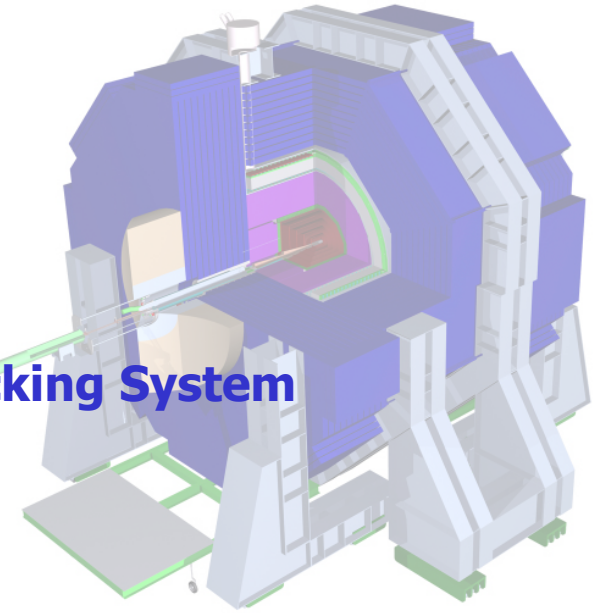
Marcel Demarteau
Fermilab

For the SiD Vertex-Tracking Group

LCWS10
Beijing, March 26-31, 2010

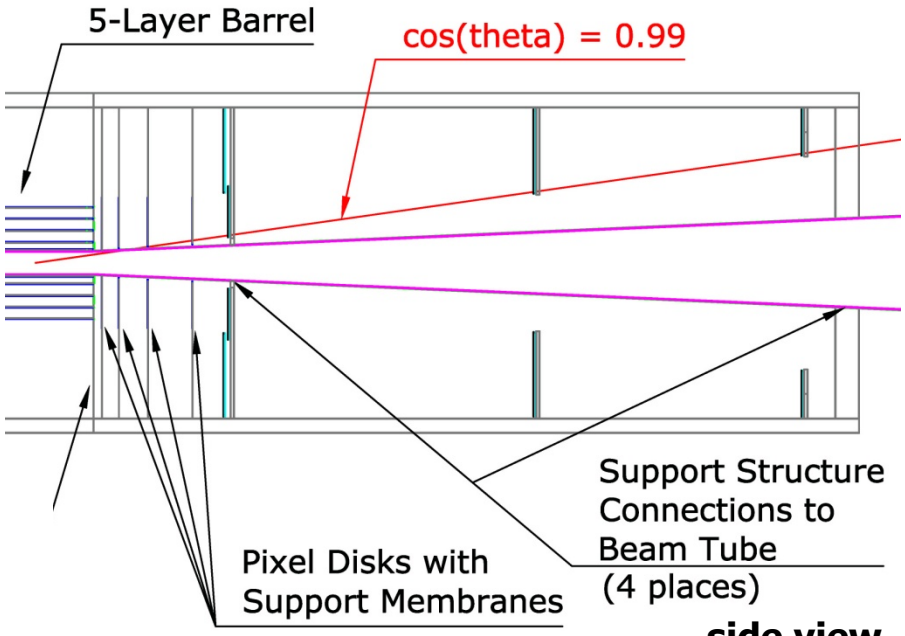
Outline

- **Pixel Detector**
  - **Status of 3D Technology**
- **Tracking Detector**
  - **Status of Tracker Elements**
- **Performance of Integrated Vertex and Tracking System**
- **Concluding remarks**

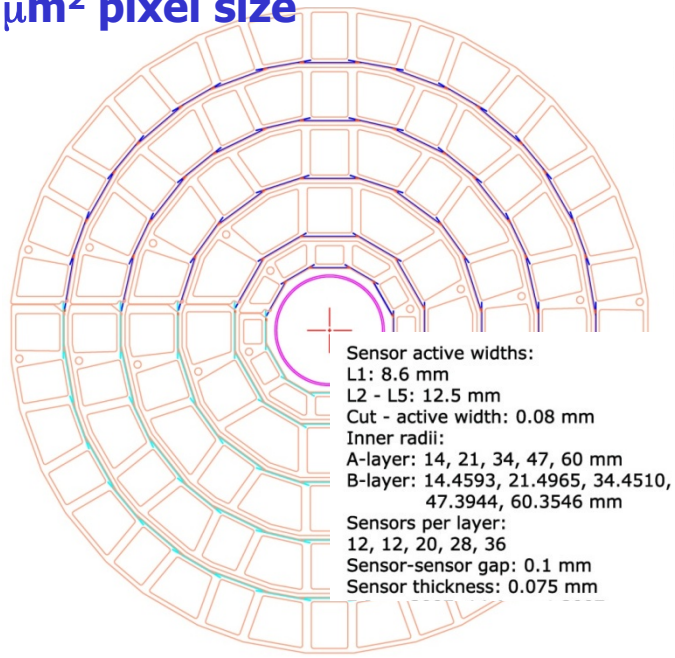


Pixel Detector Design

- **Baseline vertex detector:**
  - **Central: 5-layer barrel, consisting of two sub-assemblies clam-shelled around beam pipe**
  - **End cap: two 4-plane end disk assemblies and three additional disks per end for extended coverage**
- **All Silicon layout to mitigate CTE issues**
- **All elements are supported indirectly from the beam tube via double-walled, carbon fiber laminate half-cylinder**
- **Sensor thickness of 75 μm assumed, with 20x20 μm² pixel size**



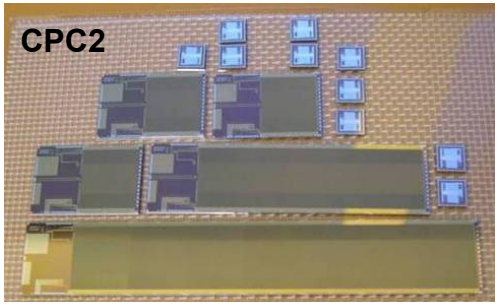
side view

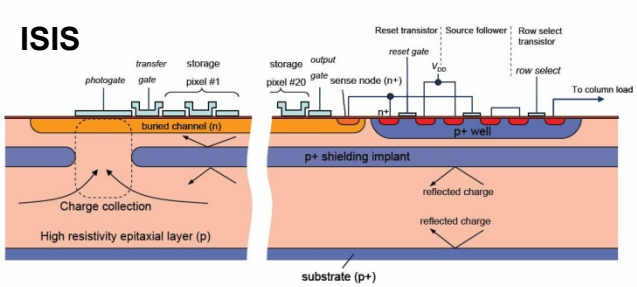


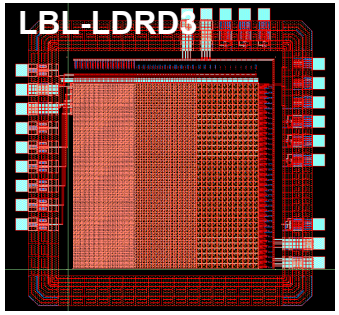
end view

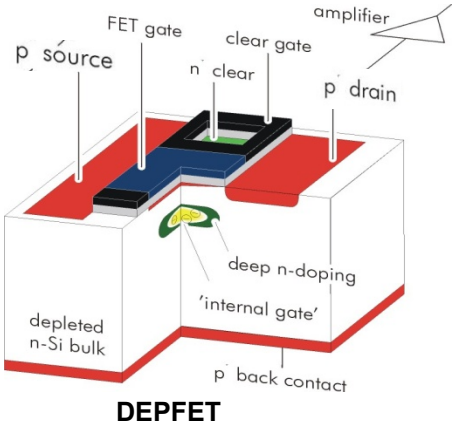
Vertex Detector Sensor Technology

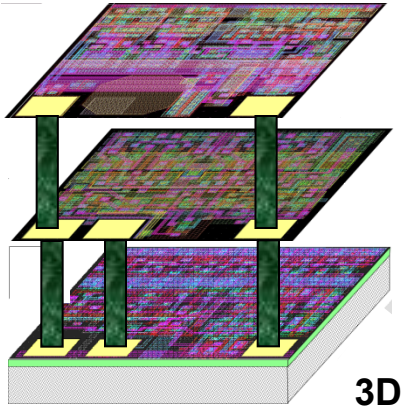
- **Broad spectrum of sensor technologies are a candidate technology for the ILC vertex detectors**
- **CCD's**
  - **Column Parallel (LCFI)**
  - **ISIS (LCFI)**
  - **Split Column (SLAC)**
- **CMOS Active Pixels**
  - **Mimosa series (Ires)**
  - **INFN**
  - **LDRD 1-3 (LBNL)**
  - **Chronopixel (Oregon/Yale)**
- **SOI**
  - **American Semiconductor/FNAL**
  - **OKI/KEK**
- **DEPFET (Munich)**
- **Chronopixel**
- **3D Vertical Integration (Fermilab)**





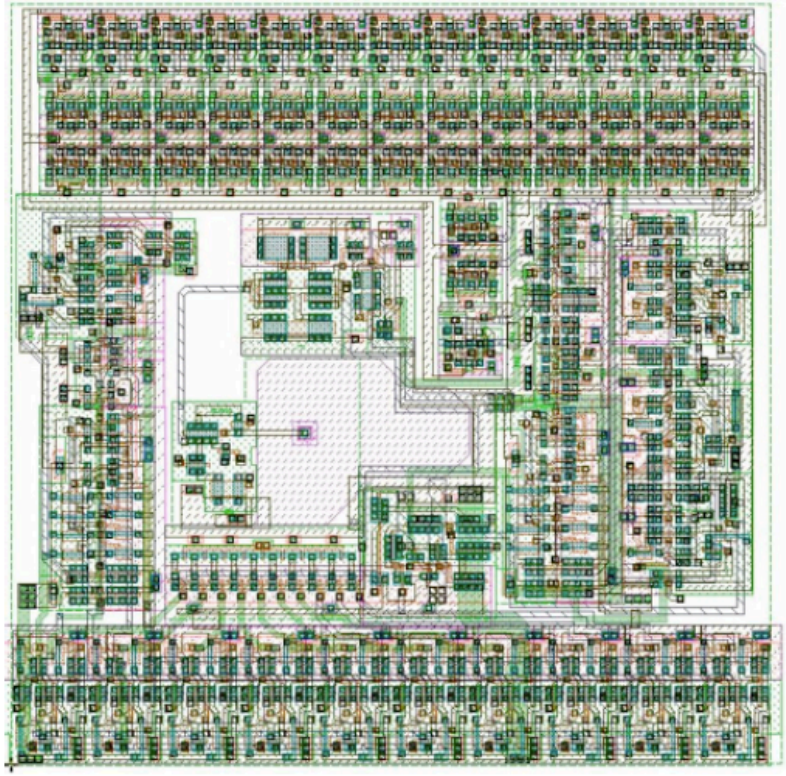






Chronopixel

- **Chronopixel design provides for single bunch-crossing time stamping**
  - **When signal exceeds threshold, time stamp provided by 14 bit bus is recorded into pixel memory, and memory pointer is advanced**
  - **Comparator threshold adjusted for all pixels**
- **Current design**
  - **50x50 um^2 pixels**
  - **Two pixel architectures**
    - Regular p/n-well design
    - Deep n-well design
  - **Detector sensitivity: 10 μV/e**
    - eq. to 16 fF
  - **Detector noise: 25 e^-**



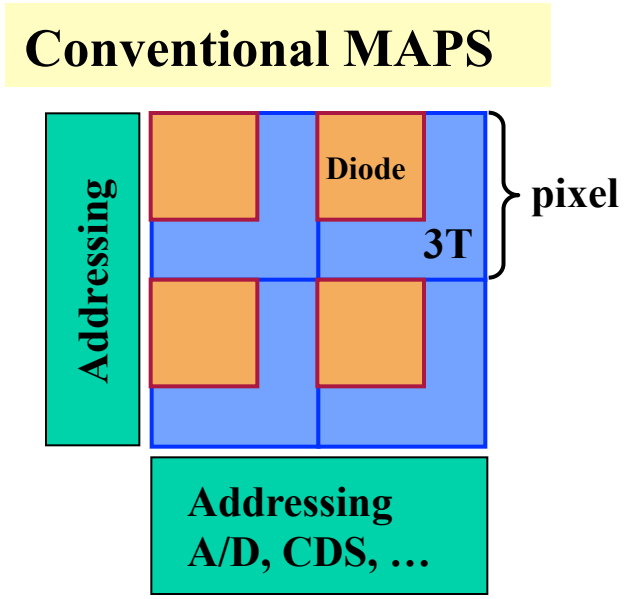
- **Please see dedicated contribution on Chronopixel status by Nick Sinev**

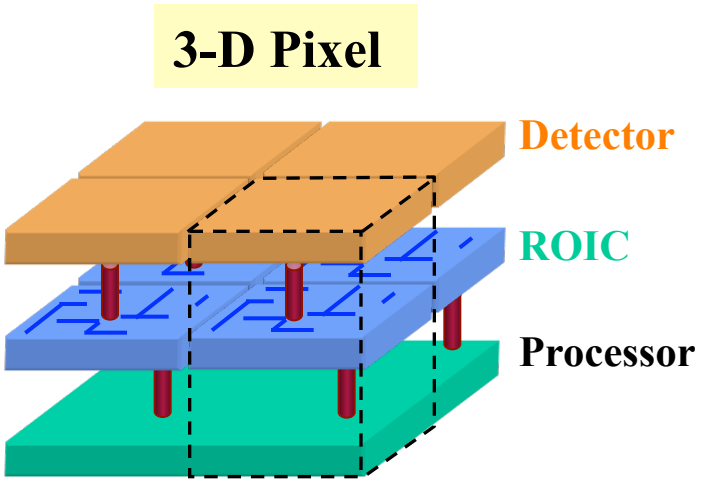
Vertical Integrated Circuits – 3D

- "Conventional MAPS"
  - Pixel electronics and detectors share area
  - Fill factor loss
  - Co-optimized fabrication
  - Control and support electronics placed outside of imaging area

- 3D Vertical Integrated System
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
  - Fabrication optimized by layer function
  - Local data processing
  - Increased circuit density due to multiple tiers of electronics
  - 4-side abuttable

- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

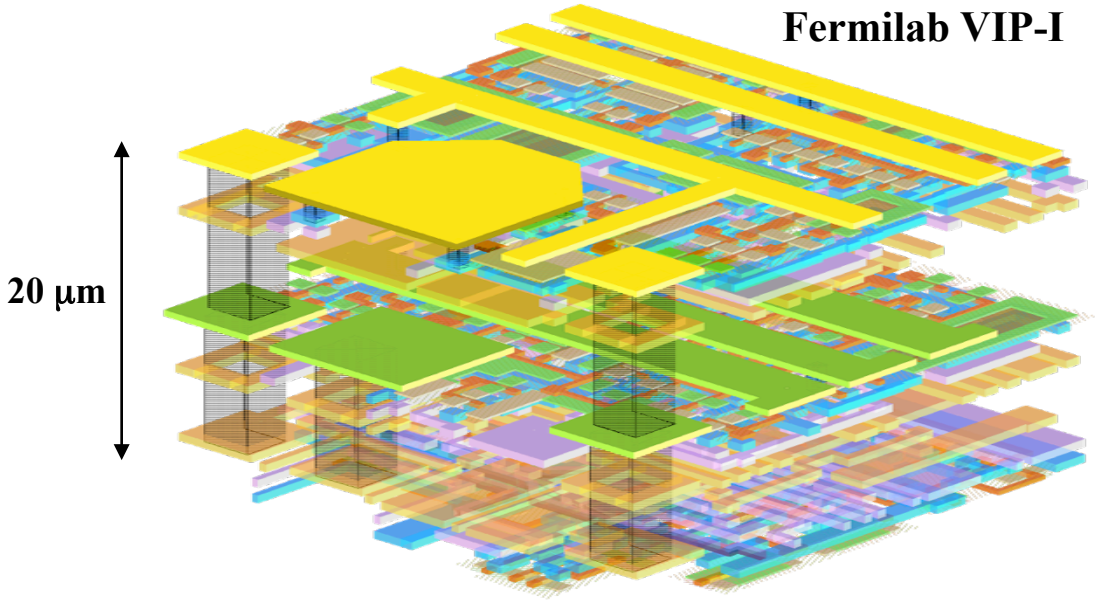




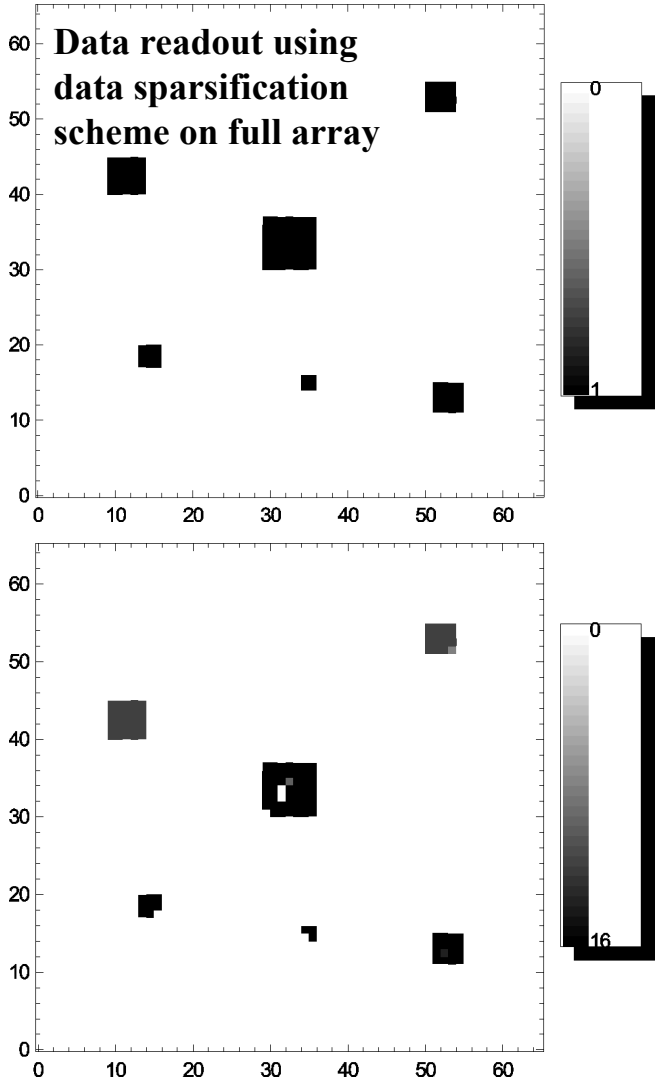
VIP Chip

- Fermilab started to actively pursue the 3D technology, initially with MIT Lincoln Laboratories (MIT-LL), who had developed the technology that enables 3D integration
- MIT-LL offers DARPA funded 3-tier multi-project run, 180nm SOI process

- Designed Vertical Integrated Pixel (VIP) chip for ILC pixel detector
  - Pixel array 64x64, 20x20 μm^2 pixels; design for 1000 x 1000 array
  - Provides analog and binary readout information
  - 5-bit Time stamping of pixel hit
  - Token passing readout scheme
  - Sparse readout
- Chip divided into 3 tiers
  - ~ 7 μm / tier
  - 175 transistors / pixel
- No integrated sensor



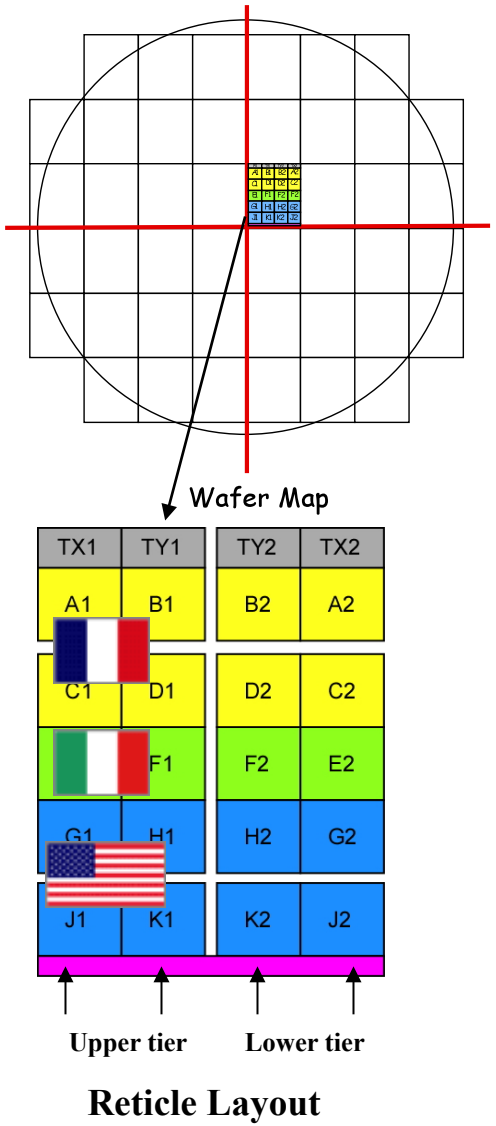
VIP-1 and VIP-2a



- VIP-1 chip submitted Oct. 2006; ~20 devices delivered late 2007; chip works !
- Major breakthrough in the development of advanced ASICs and integrated detector systems
- An improved version of VIP-1 has been submitted to MIT-LL on October 13, 2008 (150nm, SOI, 3 tiers): VIP-2a
  - Different power and grounding layout;
  - Redundant vias and larger traces in critical paths
  - Added diagnostics
  - Slightly larger pixels
- 3D technology driven by industry; started an initiative with one of the leaders in 3D technology, Tezzaron (Naperville), willing to accept MPW runs

Preselected Injection (top) and Readout (bottom) pattern of pixels reported as hit using data sparsification

Fermilab 3D Multi-Project Run



Reticle Layout

- **Fermilab formed a 3D consortium and hosted a 3D multi project run with Tezzaron**
  - **Two layers of electronics fabricated in the Chartered 130 nm process, useful reticule size is 16x24 mm**
  - **Wafers will be bonded face to face**
  - **Submission closed September 2009**

- **17 Participating institutions in the MPW run**

Fermilab, Batavia	CPPM, Marseilles	AGH University, Krakow
University at Bergamo	IPHC, Strasbourg	Brookhaven
University at Pavia	IRFU Saclay	LBNL
University at Perugia	LAL, Orsay	
INFN Bologna	LPNHE, Paris	
INFN at Pisa	CMP, Grenoble	
INFN at Rome	University of Bonn	

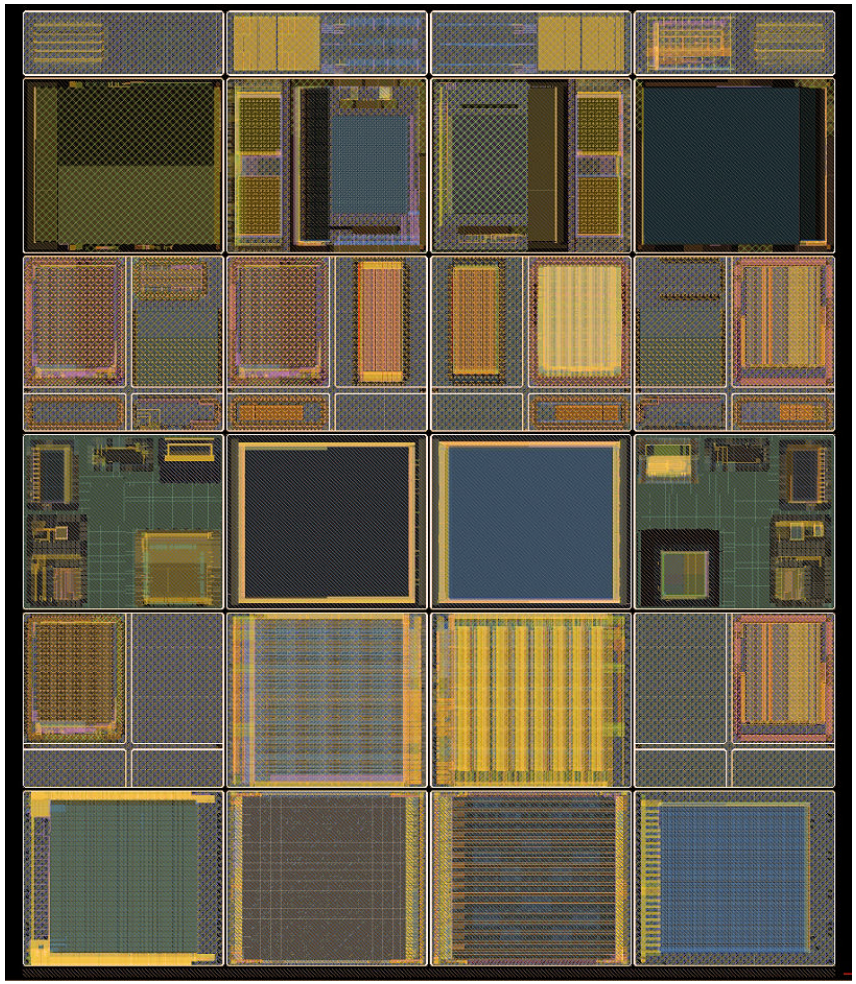
- **Frame divided into 12 sub-reticules for consortium members**

- **More than 25 two-tier designs (circuits and test devices)**

MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

Subreticules:
A, B, C, D,
E, F, G, H, I, J
5.5 x 6.3 mm

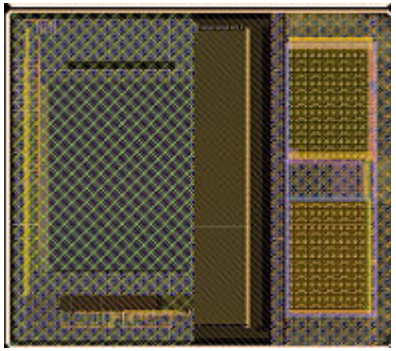


Notice
Symmetry
about vertical
center line

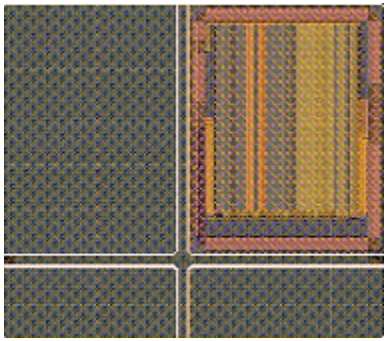
← Top tiers → ← Bottom Tiers →

Sub-Reticules

- Sub-reticule A (Strasbourg, Saclay, Pavia) :
  - FE to be bonded to sensors from XFAB
- Sub-reticule B (CMP, Strasbourg, Saclay):
  - MAPS for ILC
- Sub-reticule C (CPPM, Bonn):
  - ATLAS 2D pixel design (FEI4)
- Sub-reticule D (CPPM, Bonn, LAL)
  - ATLAS 3D pixel design
- Sub-reticule E (Roma, Pavia, Bergamo, Pisa):
  - 3D MAPS
- Sub-reticule F (Pavia, Bergamo):
  - 3D MAPS
- Sub-reticule G Sub-reticule G (Orsay/LBNL)
  - ATLAS Pixel FE
- Sub-reticule H (FNAL/CPPM/LBNL):
  - Vertically Integrated CMS TRigger chip
- Sub-reticule I (FNAL):
  - VIP, adapted to two layers
- Sub-reticule J (FNAL/AGH-UST/BNL):
  - VIPIC: demonstrator for X-ray Photon Correlation Spectroscopy



B Right

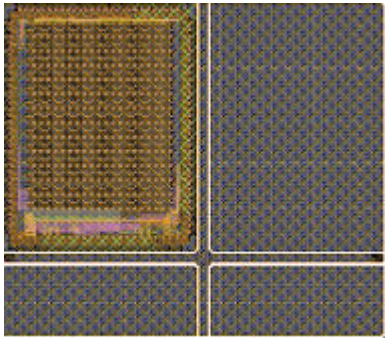


G Right

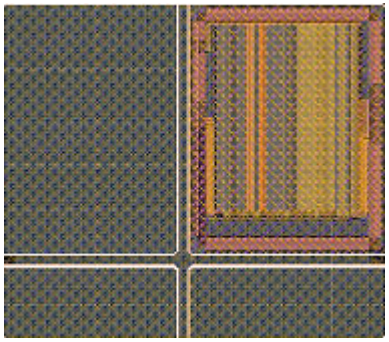
Sub-reticules F & G

F Left

F Right



G Left

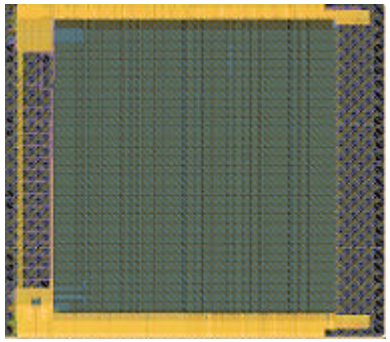


G Right

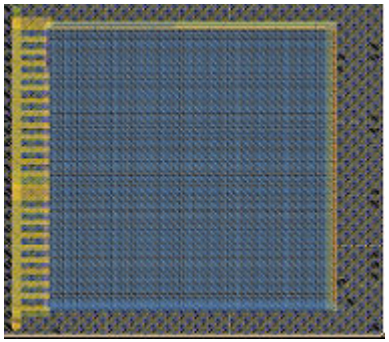
- **Sub-reticule F: 3D MAPS (Pavia, Bergamo)**
  - **3D MAPS device with 256x240 array of 20x20 um^2 pixels with Deep N-Well sensors and sparsification for ILC**

- **Sub-reticule G: ATLAS Pixel FE (Orsay/LBNL)**
  - **ATLAS 2D pixel design based on FEI4 design in IBM 130 nm**
    - Left (analog) side – 14x60 array of 50x166 um^2 pixels with simple readout
    - Analog tier designed for opposite polarity input from circuits in sub-reticules C and D.
    - Mating side comprised of counter to study coupling with the left tier with different shielding ideas.

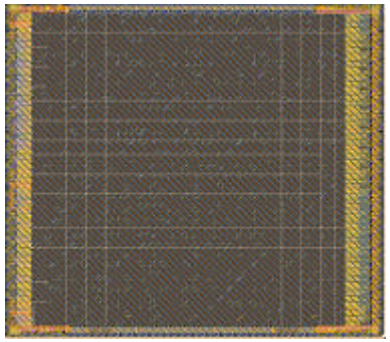
Sub-reticules I & J



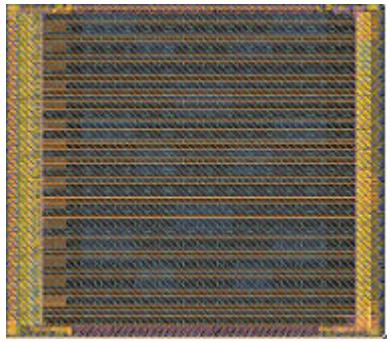
I Left



I Right



J Left



J Right

- **Sub-reticule I: VIP2b 3D demonstrator chip for ILC vertex detector with separate bonded sensor (FNAL)**
  - **Adapted from earlier MIT LL designs in SOI technology**
    - 192 x 192 array of 24x24 um^2 pixels
    - 8 bit digital time stamp
    - Data sparsification
    - DCS analog signal info output
    - Separate test input for every pixel cell
    - Serial output bus

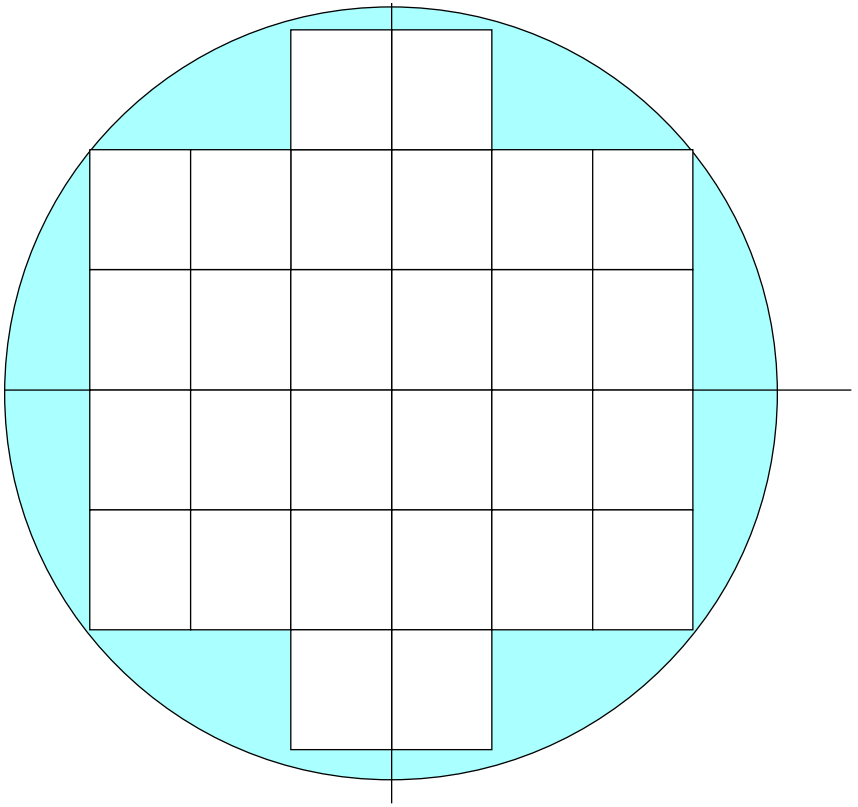
- **Sub-reticule J: VIPIC 3D demonstrator chip for X-ray Photon Correlation Spectroscopy (FNAL/AGH-UST/BNL)**
  - **Characteristics:**
    - 64 x 64 array of 80x80 um^2 pixels
    - Separate analog and digital tiers
    - Sparsified, binary readout
    - High speed frame readout
    - Trigger-less operation
    - 16 Parallel serial output lines
    - Two 5 bit counters/pixel for dead timeless recording of multiple hits per time slice
    - Innovative binary tree pixel addressing scheme

Timeline and Schedule

- **All designs were received by Fermilab in May 2009**
- **June 2009 – March 2010 spent preparing and reviewing the submission(s)**
  - **Note, this was the first time for Fermilab and Tezzaron to organize a MPW run and there were a large number of 'growing pains'**
  - **A large number of problems were discovered**
    - Frame and street definitions
    - Design kit incompatibilities, software bugs
    - TSV issues: protection, spacing, bond interface
- **March 6, 2010: Fabrication started**
- **At the end of April: 2D wafers expected out of foundry**
  - **3 wafers to be diced and parts sent to designers**
- **May – June 2010: 3D wafers expected to be completed**
- **June 2010: 3D characterization to start**
- **July 2010 or so: wafers prepared for bonding to sensors**

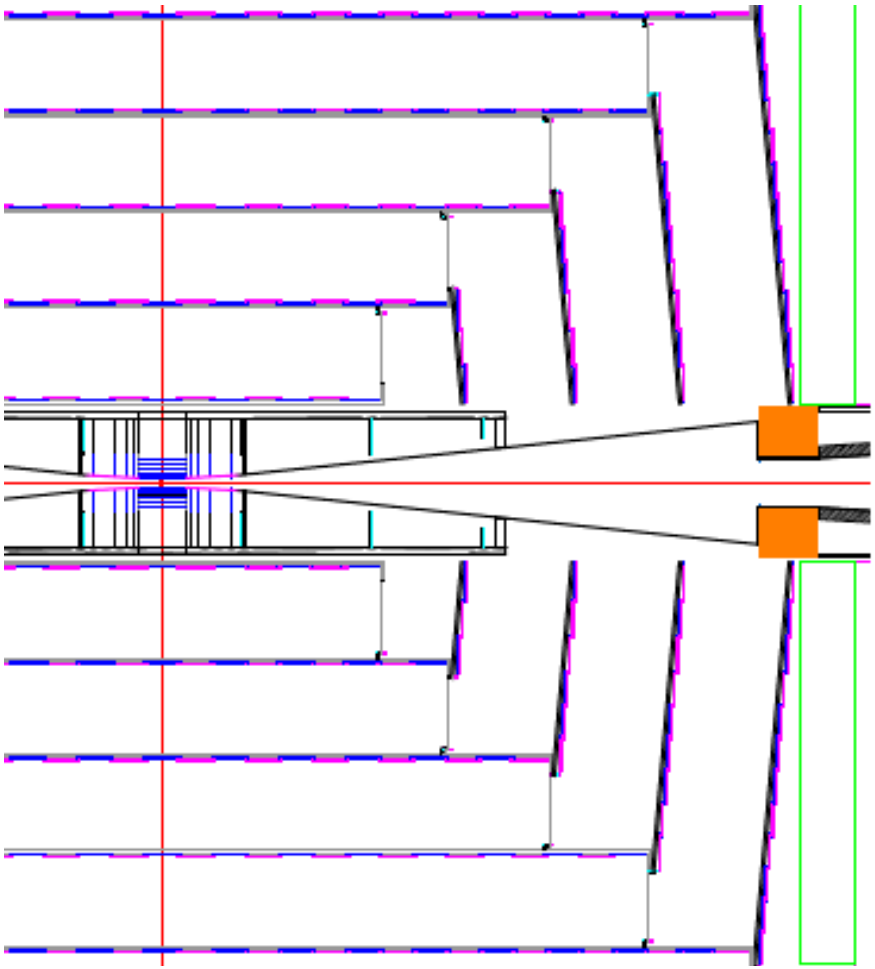
Production and Parts Count

- Procured one lot of 31 wafers, with 28 full reticules per wafer
- Partition of wafers:
  - 3 wafers will be used for 2D wafer testing
- Available for 3D bonding 28 wafers, which yields 14 3D wafers
- There are 14 3D assemblies per wafer
- If one assumes a yield of 50%, seven working 3D wafers available
  - 98 assemblies of each sub-reticule
- A lot of work ahead !



Tracker Design

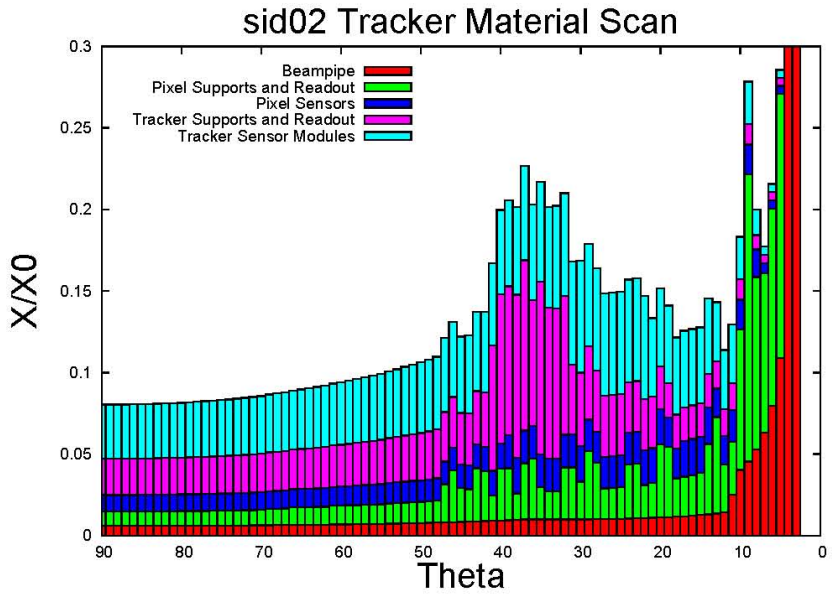
- 5-Layer silicon strip outer tracker, covering R_{in} = 20 cm to R_{out} = 125 cm
- Barrel – Disk structure: goal is 0.8% X_0 per layer

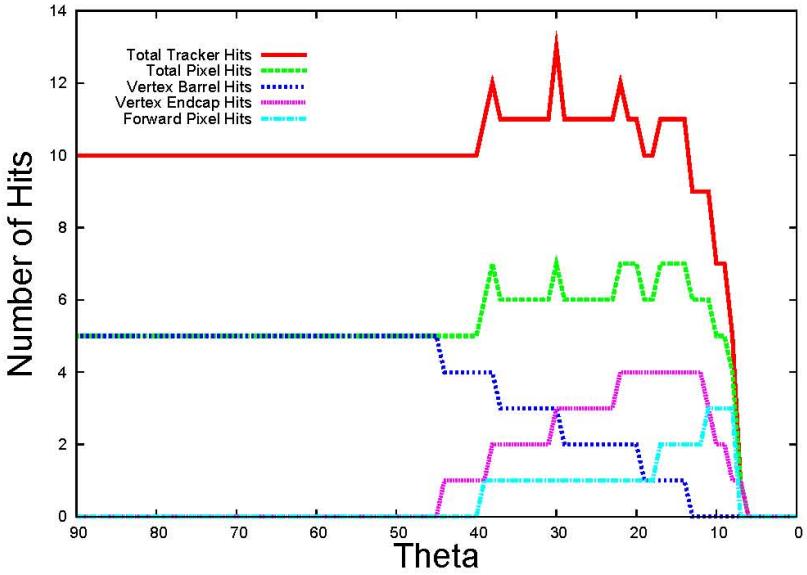


- Support
  - Double-walled CF cylinders
  - Allows full azimuthal and longitudinal coverage
- Barrels
  - Five barrels, measure Phi only
  - 10 cm z segmentation
  - Barrel lengths increase with radius
- Disks
  - Four double-disks per end, lampshade geometry
  - Measure R and Phi
  - Varying R segmentation
  - Disk radii increase with Z
- Note: simulations carried out with disks at 90 degrees to beam line

Overall Features

- **Although from a technological and mechanical point of view the vertex detector and the outer tracker are individual sub-detectors, we wish to view it as one integrated detector**
  - **5 barrel + 7 disk pixel inner vertex detector**
  - **5 barrel (axial strip) + 4 disk (stereo strip) outer detector**

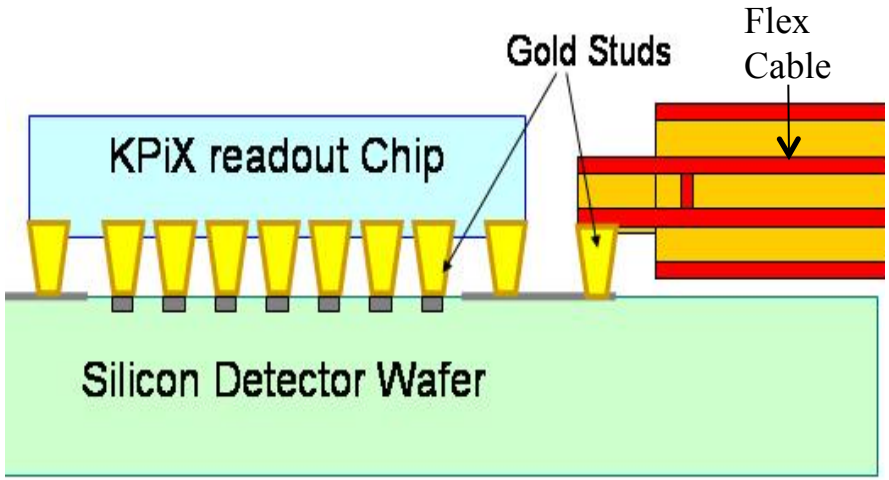




- **Material budget $X/X_0 < 0.2$ throughout the tracking volume**
- **There is a uniform coverage of a minimum of 10 hits per track down to small angles**

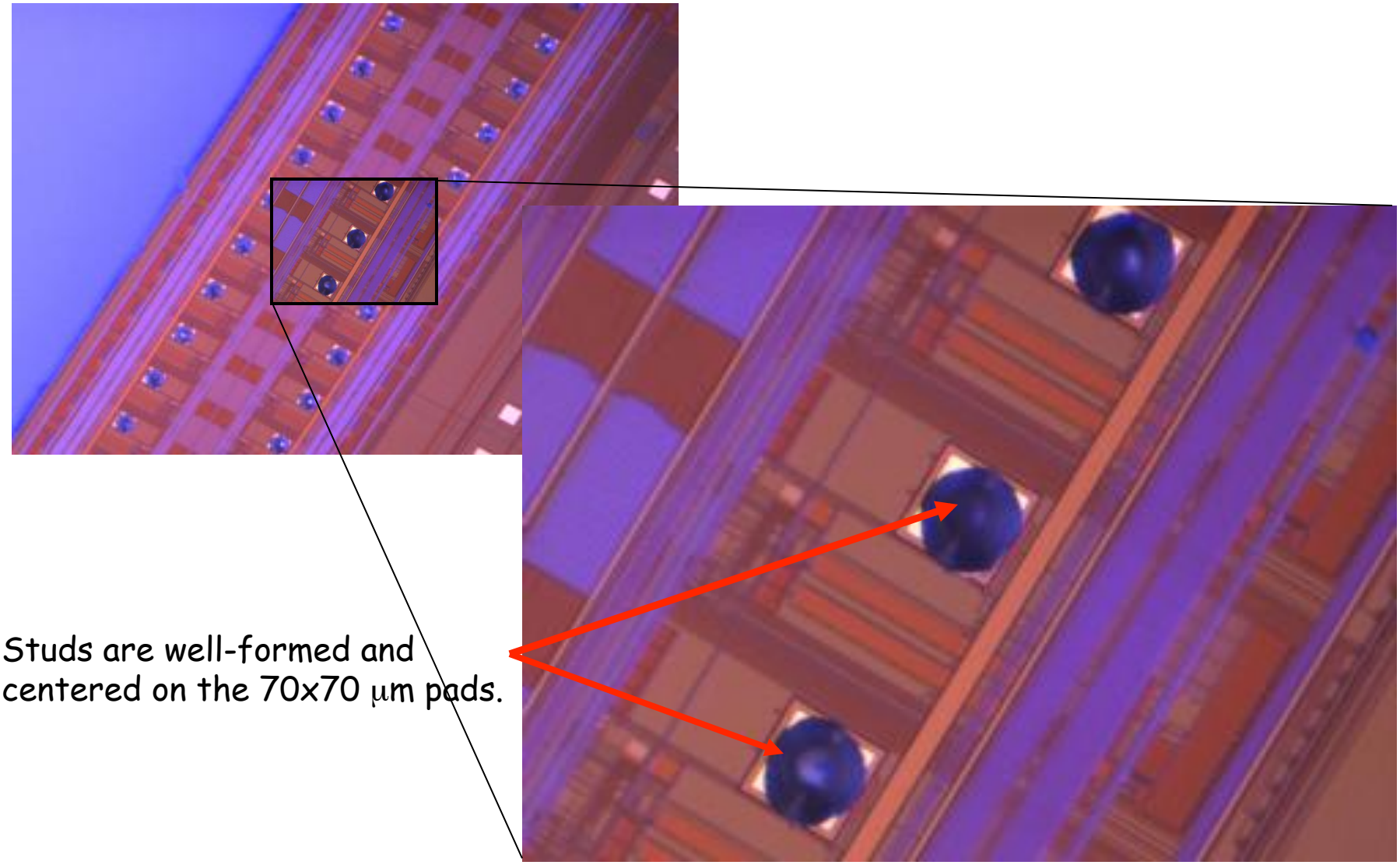
Sensors and Readout

- **Module is hybrid-less design with 3 components:**
- **Silicon Sensor**
  - **93.5 x 93.5 mm^2 sensor from 6" wafer with 1840 (3679) readout (total) strips**
  - **Routing of signals through 2nd metal layer, optimized for strip geometry**
    - Minimize capacitance and balance with trace resistance for S/N goal of 25
  - **Power and clock signals also routed over the sensor**
- **kPix readout ASIC**
  - **Sensor read out with two kPix chips bonded to the sensor**
  - **kPiX-8 with 256 channels in hand**
- **Flexible readout cable**
  - **2-layer, ¼ oz. Cu on 50µm Kapton**
  - **2 power + ground pairs**
  - **8 control/ro lines**
  - **Provides sensor HV bias**



Gold Stud Bonding

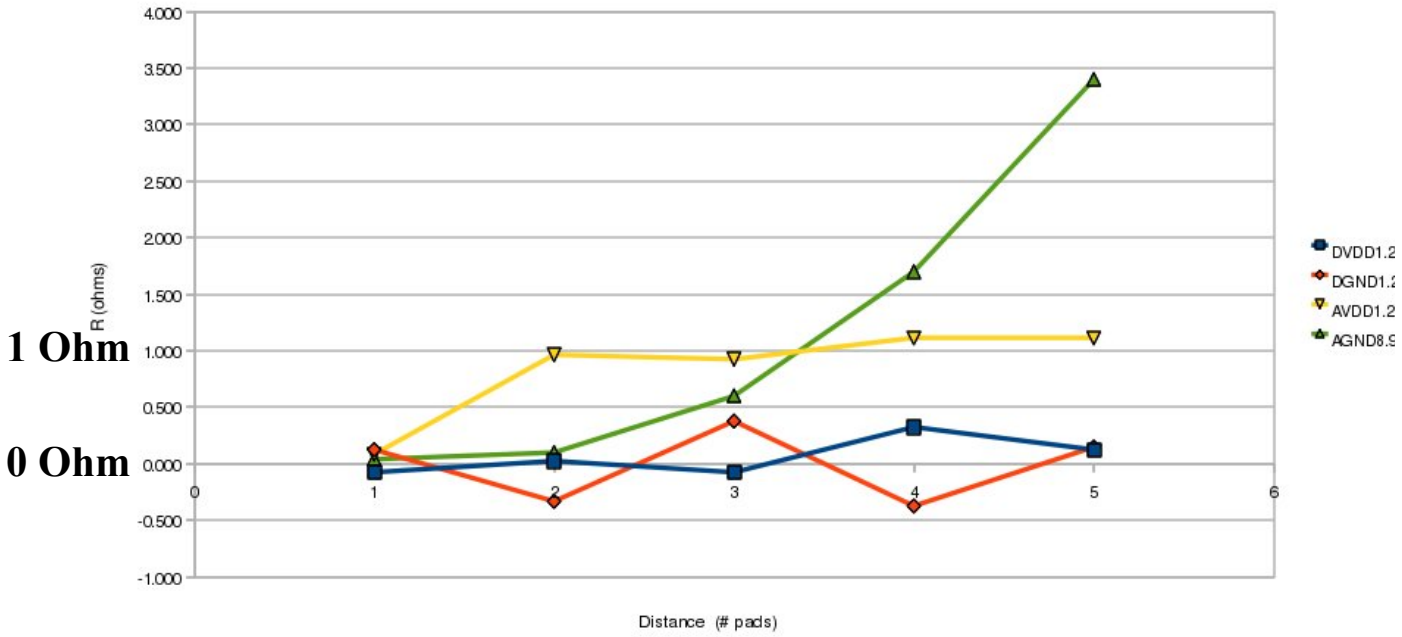
- **Gold Stud bonding carried out at UC Davis**



Studs are well-formed and centered on the 70x70 μm pads.

Gold Stud Bonding

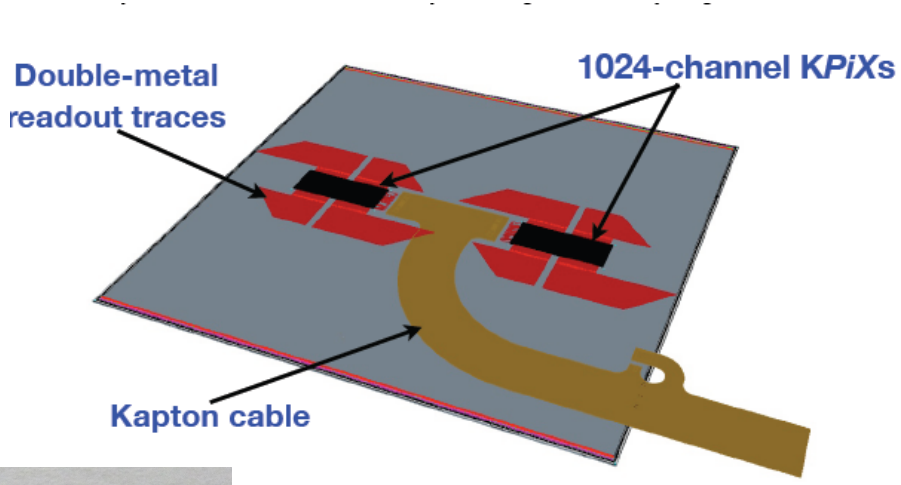
- Gold stud attachment through thermo-compression. Typically, high temperature and pressure: 300-350 ^{0}C and 150-200 g/bump. Machine limit ~100-200 kg → Limits total number of bumps

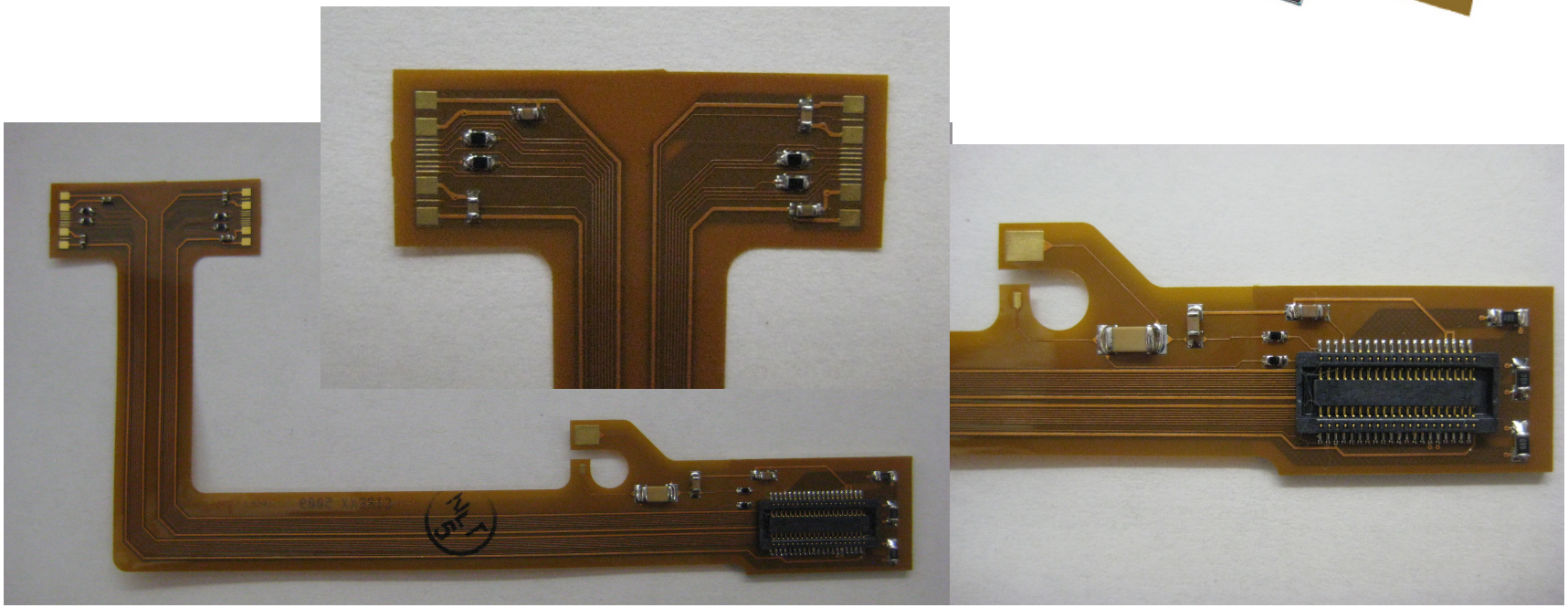


- 160 g/bump provides acceptable resistances for all bumps
- 100 g/bump was insufficient: 4 of 20 bumps were ~open
- Further studies:
  - Explore pressures greater than 160 g/bump
  - Study systematics with position, uniformity, reproducibility

Readout Cable

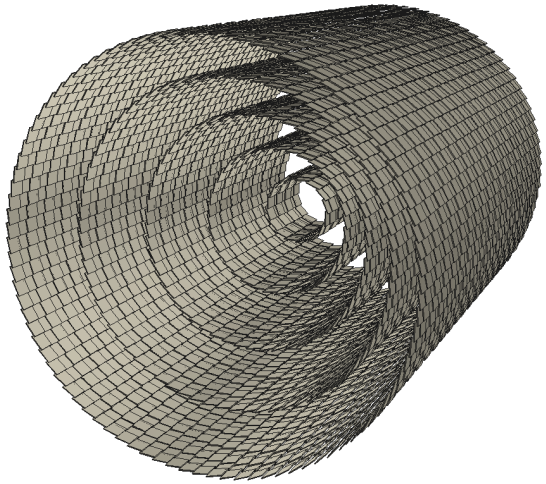
- Cables for DM-SiD sensors produced (New Mexico/Fermilab)
  - Being characterized at NM
- All components in hand to develop full KPiX/Double-Metal prototype assembly for performance studies
  - Plan calls for studies with test structures first



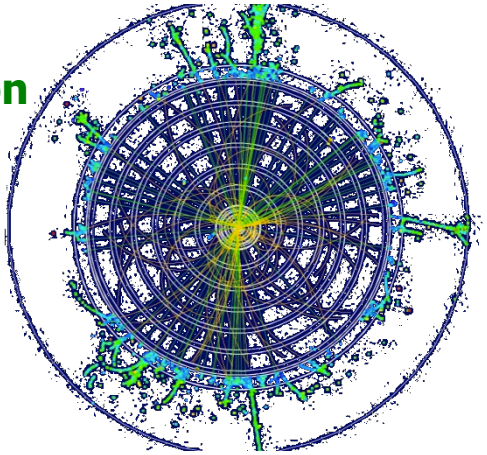


Detector Modeling

- **Geometry**
  - **Complete barrel and disk geometry available with dead material**
    - Virtual segmentation used for studies presented here
      - Barrel sensors have been approximated by thin cylinders, while the disk sensors have been approximated by planar disks perpendicular to the beamline.
    - Poly-hydra geometry definition
      - Fully segmented detector with individual sensors, overlap and dead material. Allows for detailed tracking and alignment studies



  - **Output is a "hit"**
    - Individual pixels and strips not included in the GEANT4 simulation
- **Digitization**
  - **Charge deposition is calculated from energy deposition generated by Geant4**
  - **Hits are put at center of detector with no smearing to improve speed**
  - **Full ghosting in stereo layers**



Track Finding Strategy

- **Track finding is guided by a set of user defined 'Strategies', which define which layers to be used, their roles, and constraints**

- **Strategies used to date:**
  - **Use three 'Seed Layers', which can be anywhere in the detector**
  - **At least 7 hits on the track**
    - Only 1 hit per layer
    - Special barrel only strategy with 6 hits used to pick up low-p_T particles in the central region
  - **$p_T > 0.2$ GeV**
  - **r - ϕ and s - z impact parameter cuts $|d_0| < 1$ cm and $|z_0| < 1$ cm**
  - **$\chi^2 < 50$ ($\chi^2 < 25$ for 6-hit barrel only strategy)**

- **'Strategy Builder' used to find optimized sets of seed and confirmation layers used for efficient track finding**

- **Nearly all pattern recognition code is agnostic as to the type of hit**
  - **No differentiation between pixel or strip, barrel or forward sensors**

Track Finding Algorithm

- **Track finding begins by forming all possible 3 hit track seeds in three "Seed Layers" specified by the user**
  - **Loops over all viable combinations of 3 hits in the 3 seed layers**
    - Reduce the combinatorics by eliminating hit combinations inconsistent with p_T and impact parameter constraints
- **Track finding then requires the presence of a hit in a "Confirmation Layer"**
  - **Significantly reduces the number of candidate tracks to be investigated**
- **Hits are then added to the candidate track using "Extension Layers"**
- **Upon each attempt to add a hit to a track candidate, a helix fit is performed and a global χ^2 is used to determine if the new track candidate is viable**
  - **All decisions based on χ^2 from fits and constraints (p_T>x)**
- **Final track selection**
  - **Discard track candidates with fewer than 7 hits (6 hits for barrel only tracks)**
  - **If two track candidates share more than one hit, best candidate is selected**

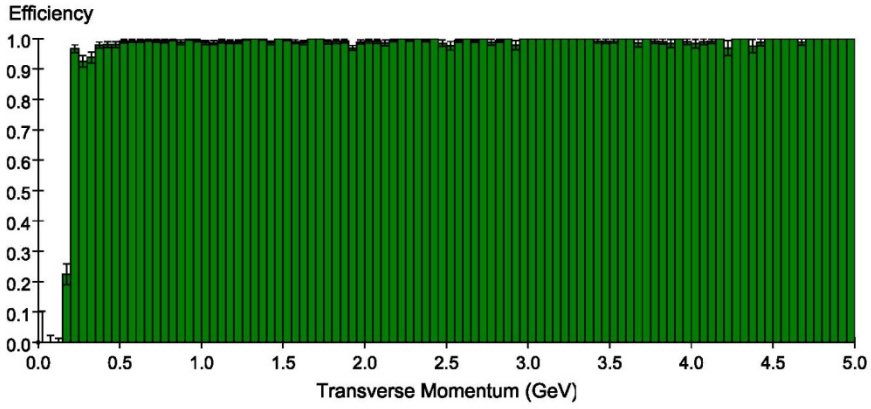
System Performance

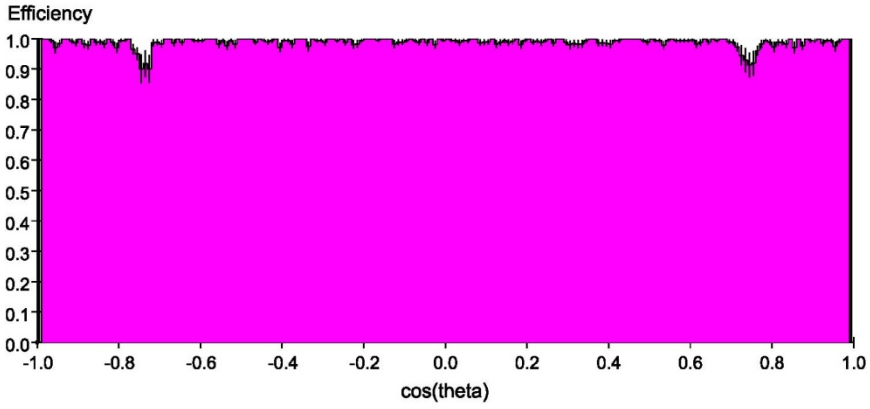
- **Overall track finding efficiency for findable tracks in $e^+e^- \rightarrow$ ttbar ($\sqrt{s}$ = 500 GeV) is 99.3% on findable tracks**

- **Fraction of findable tracks is about 84% of total number of tracks**

- **Efficiency is uniform in p_T and angle**

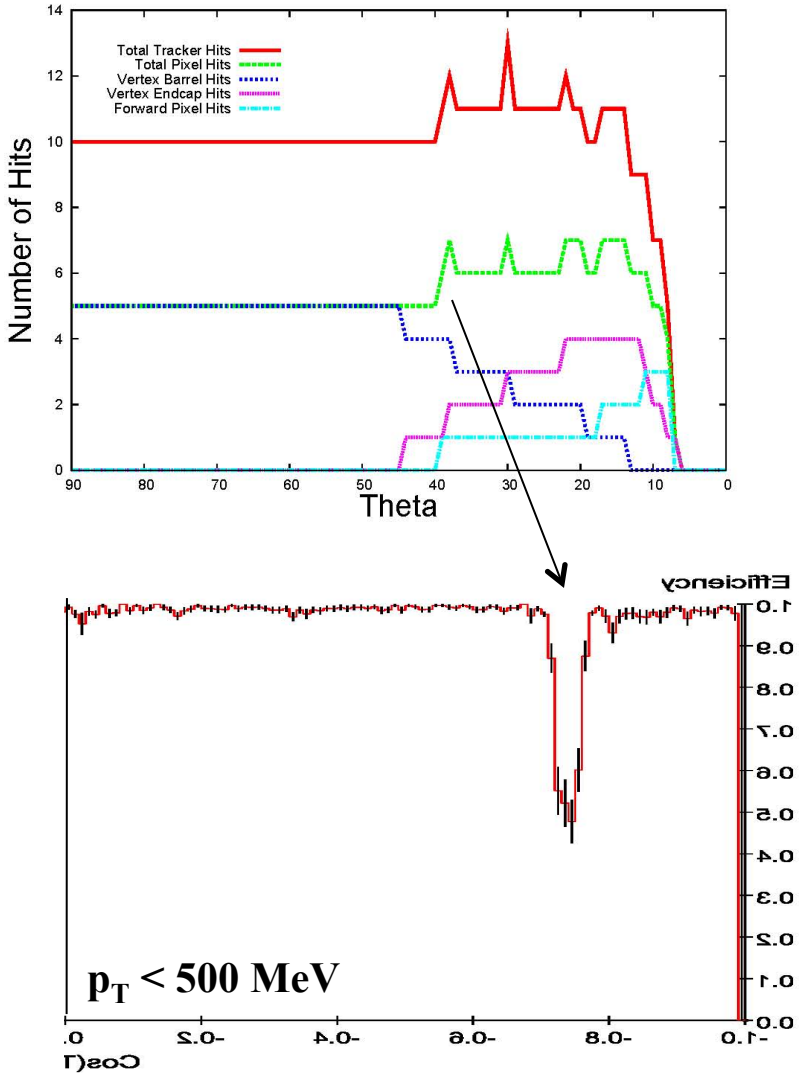
Selection	Selection Efficiency	Cumulative Efficiency
All Tracks	-	100%
$p_T \geq 0.2$ GeV	$(93.54 \pm 0.11)\%$	$(93.54 \pm 0.11)\%$
$N_{hit} \geq 6$	$(90.91 \pm 0.13)\%$	$(85.04 \pm 0.16)\%$
Seed Hits Present	$(99.78 \pm 0.02)\%$	$(84.85 \pm 0.17)\%$
Confirm Hit Present	$(99.95 \pm 0.01)\%$	$(84.84 \pm 0.17)\%$
$\lvert d_0 \rvert \leq 1$ cm	$(99.80 \pm 0.02)\%$	$(84.65 \pm 0.17)\%$
$\lvert z_0 \rvert \leq 1$ cm	$(99.69 \pm 0.03)\%$	$(84.39 \pm 0.17)\%$
Track Reconstruction	$(99.32 \pm 0.04)\%$	$(83.81 \pm 0.17)\%$





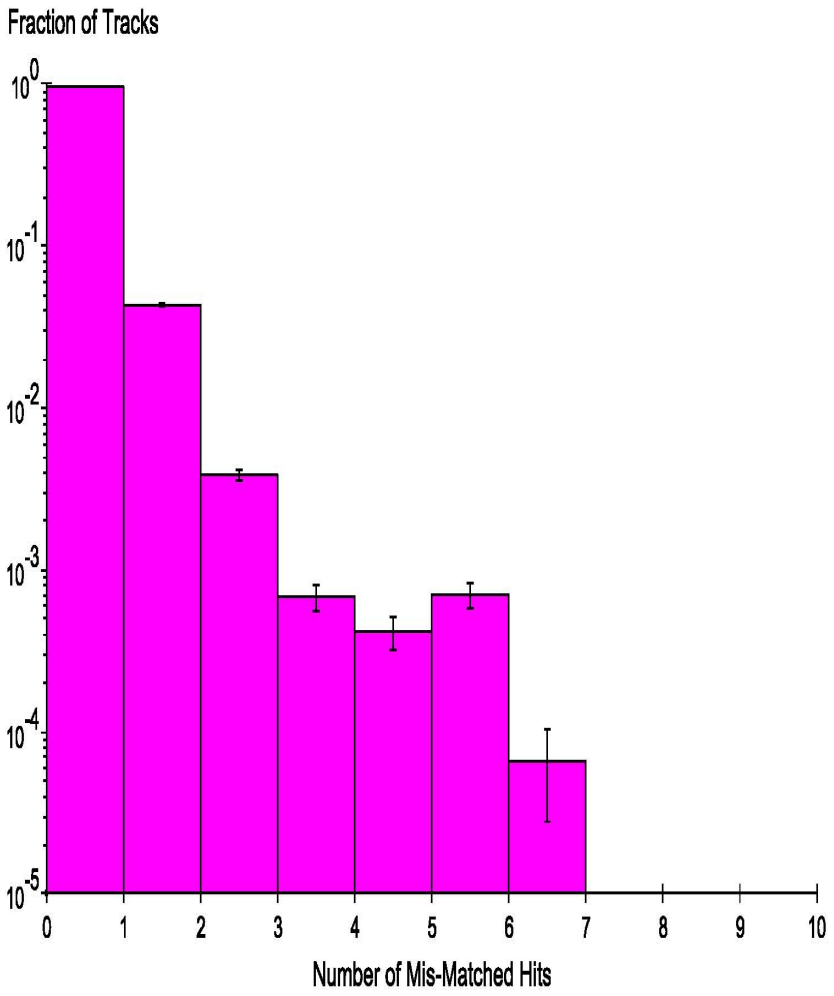
Tracking Efficiency

- **Why is the track finding efficiency not 100% for findable tracks?**
- **All the inefficiency is due to low momentum tracks (p_T < 500 MeV) in the transition region between barrels and disks**
  - **Efficiency is uniform in cos(θ) for p_T > 500 MeV**
- **It is thought that the inefficiency is due to tracks just beyond the pixel barrel acceptance that curl by more than 180 degrees before they get to the seed layers that cover this acceptance region**
- **This may be an artifact of the current tracking algorithm and could be improved upon**



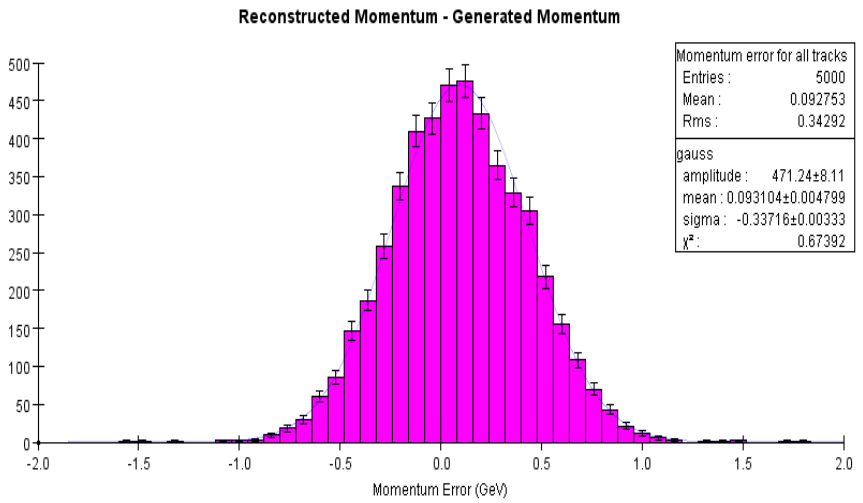
Track Quality

- A measure of the track quality is the number of mis-assigned hits on a track
  - These are hits generated by a different MC particle than the one with the majority of hits on the track
- More than 99% of tracks have at most one wrong hit on the track
- In these events (ttbar at √s = 500 GeV) fake tracks make up only 0.07% of the tracks found



Momentum Resolution

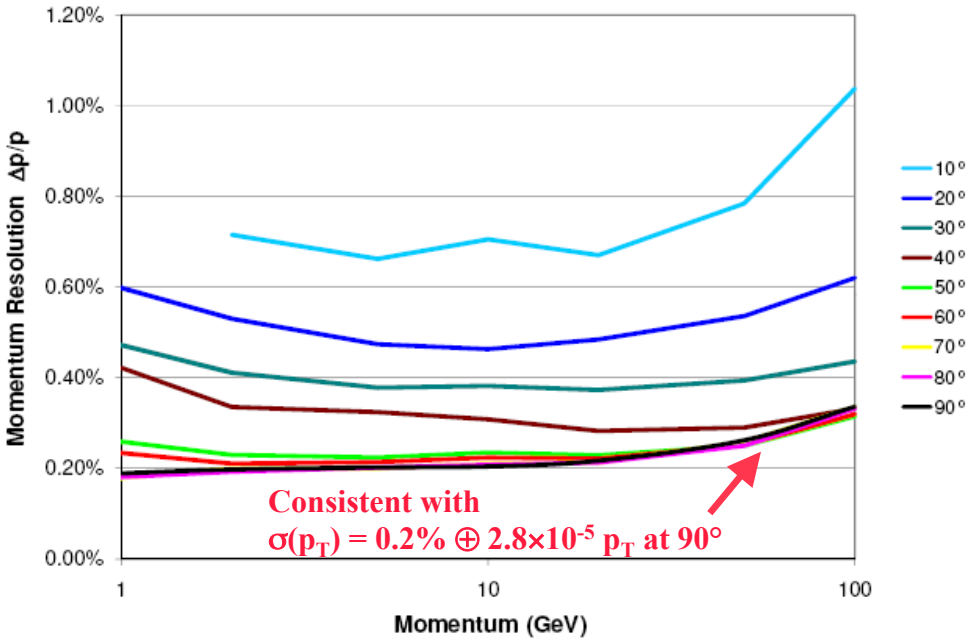
- **Momentum resolution for 100 GeV single muons at 90⁰**
  - σ_p = 0.34 GeV
- **Momentum resolution determined in $e^+e^- \rightarrow$ ttbar ($\sqrt{s}$ = 500 GeV) events**
- **Momentum resolution of 0.2% (0.3%) at 10 (100) GeV at large angles**
  - **Slightly better than "design goal" at high momenta**
  - **Slightly worse than "design goal" at low momenta**



$$\frac{\sigma(p_T)}{p_T^2} = 2.8\cdot 10^{-5} \oplus \frac{2\cdot 10^{-3}}{p_T \sin(\vartheta)} \quad (GeV^{-1})$$

$$\frac{\sigma(p_T)}{p_T^2} = 2\cdot 10^{-5} \oplus \frac{1\cdot 10^{-3}}{p_T \sin(\vartheta)} \quad (GeV^{-1})$$

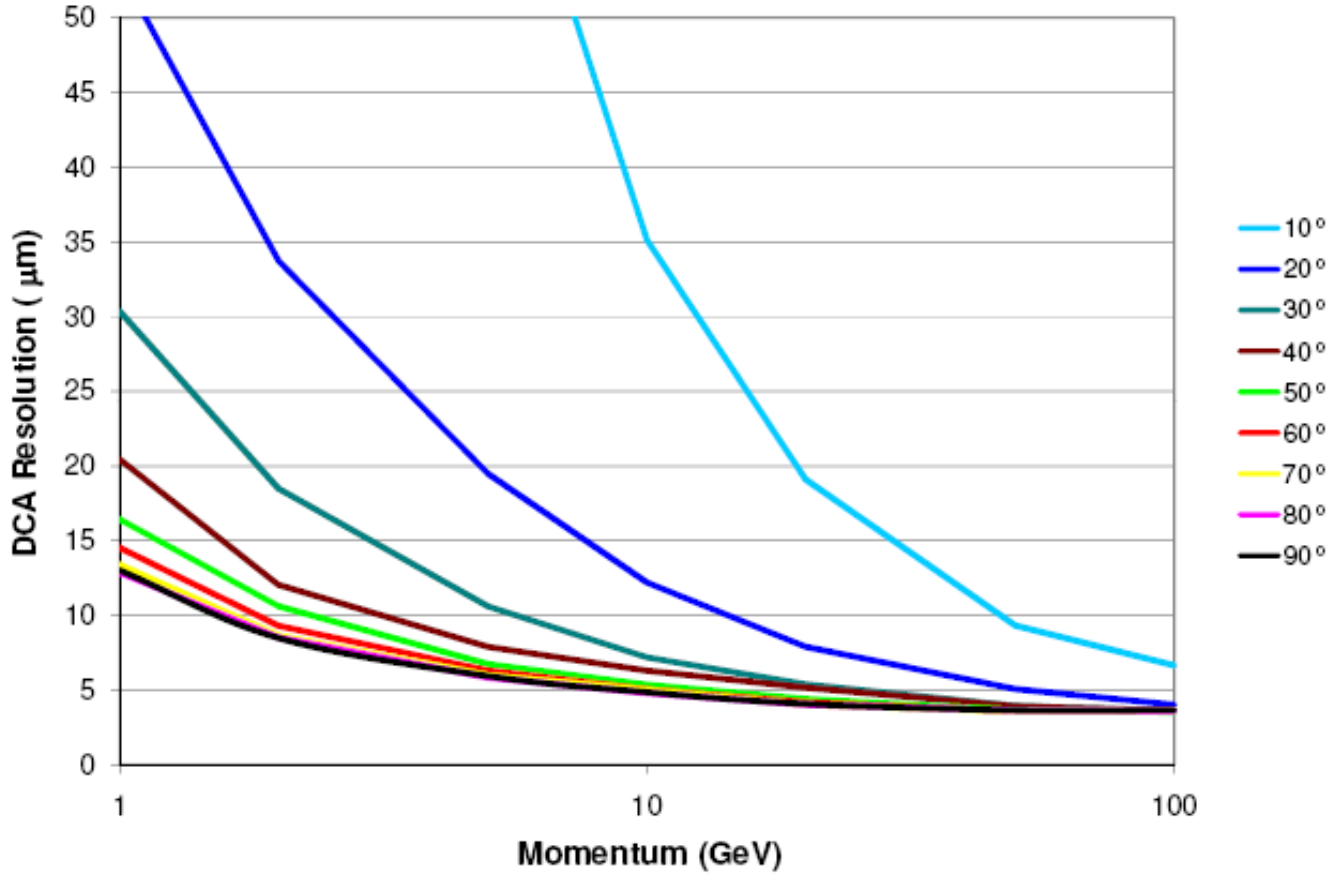
Design goal



DCA Resolution

- **Resolution on (x,y) distance of closest approach in $e^+e^- \rightarrow$ ttbar ($\sqrt{s}$ = 500 GeV) events and single muons, 100 GeV between $1^0 < \theta < 179^0$**

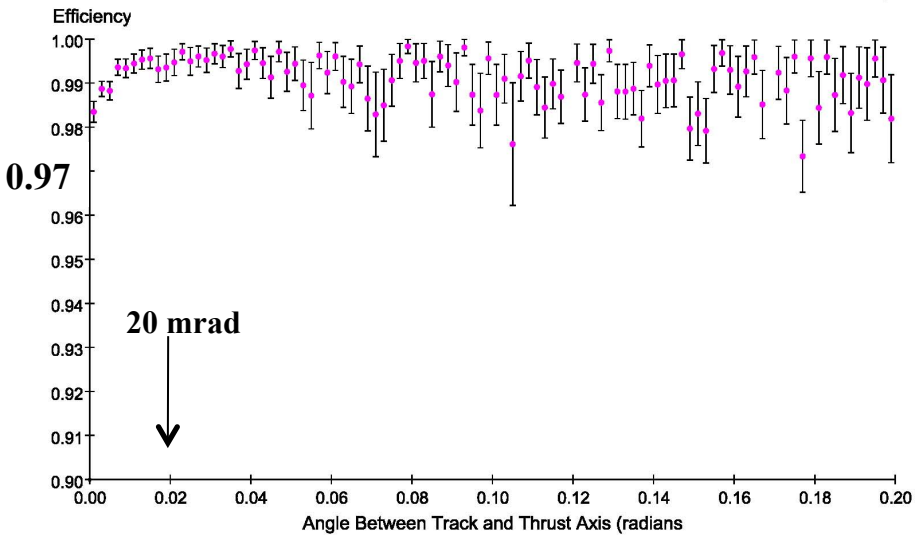
- **An asymptotic value of 4 μm is achieved for perpendicular tracks**

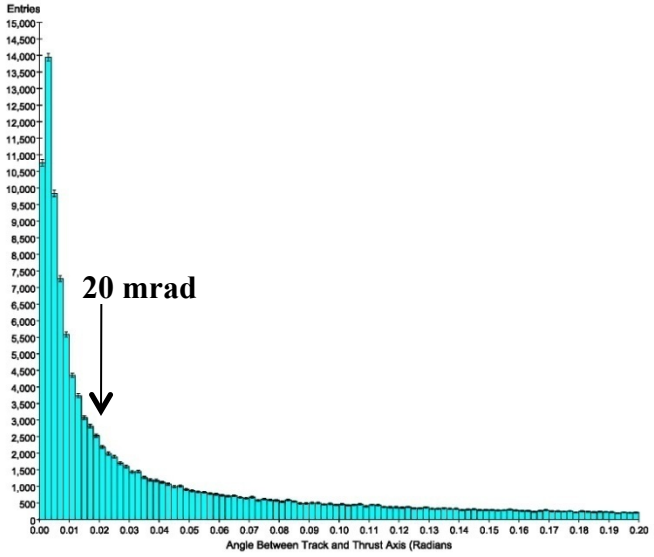


Robustness of Tracking

- The robustness of the SiD tracker has been evaluated under different experimental conditions

- Tracking in the environment of dense jets
  - $e^+e^- \rightarrow$ qqbar at $\sqrt{s}$ = 1 TeV
- Efficiency as function of track angle with respect to Thrust axis
  - Efficiency drops by ~1% from nominal within 2 mrad (first bin) of jet core
  - Note that the jet energies are 500 GeV



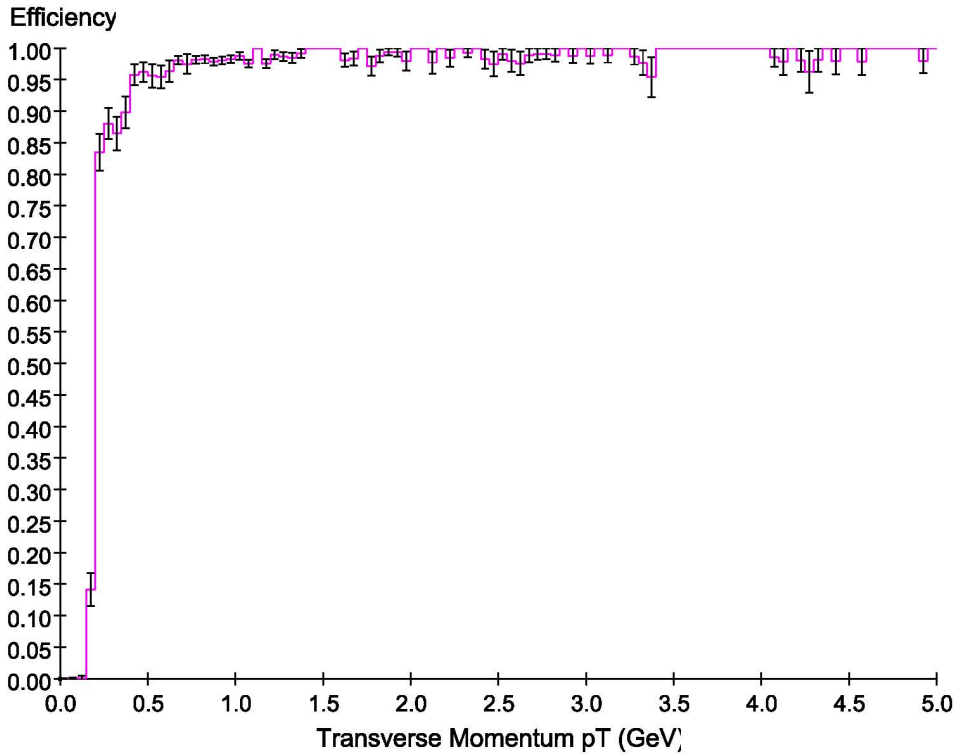


Robustness of Tracking

- The robustness of the SiD tracker has also been evaluated with the background from 10 bunch crossings overlaid
  - $e^+e^- \rightarrow$ bbbar at $\sqrt{s}$ = 500 GeV
- In this study the effect of accumulating beam backgrounds over 10 crossings has been mimicked by adding these hits to all pixel devices in the detector. Hits in the silicon strip tracker were added only for a single bunch crossing, in-time with the physics event.

- A small loss in efficiency at low pT is observed

- Also the fake track rate is slightly higher, about 0.6%. Most of the fake tracks seem to be due to combinatorics.



Concluding Remarks

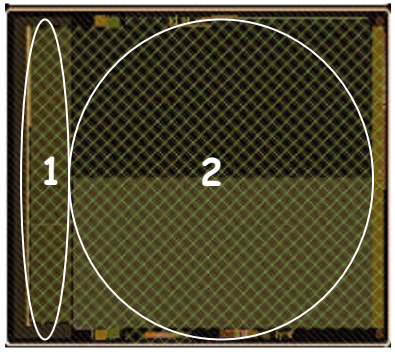
- **Major milestone of first 3D MPW submission achieved with a variety of technologies that could be used for ILC vertex detectors. Parts are in production at the foundry, and should be available late May.**
  Exciting times and a lot of work ahead.

- **Studies of overall tracking system show that an all silicon tracker is robust and achieves the performance parameters required by the physics at an ILC**

- **It is our intent to continue the optimization studies with limited resources to improve upon the existing design**

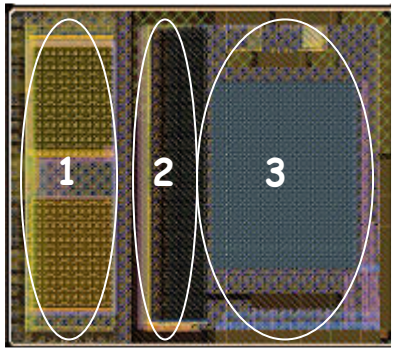
- **Continuing progress on the R&D front with kPiX, Si sensors and readout. Hope to have results of kPiX readout with sensor and cable at the next meeting.**

Sub-reticules A & B

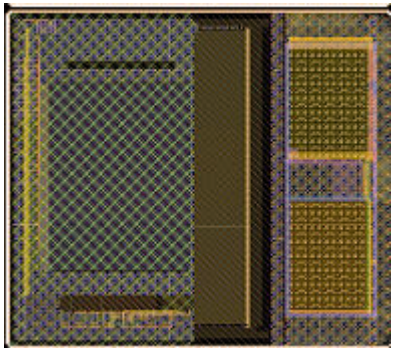


A Left

A Right



B Left

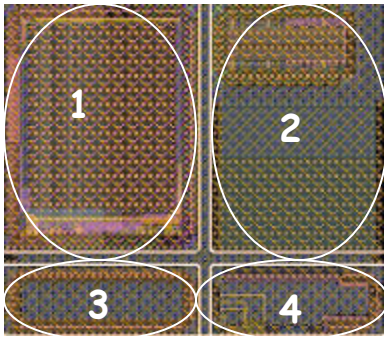


B Right

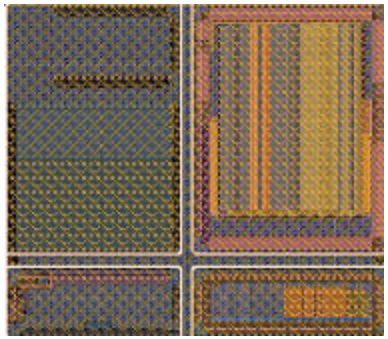
- **Sub-reticule A: Two sub-circuits intended to be bonded to sensors from XFAB (0.35 um with high res. Epi)**
  1. **ILC (Strasbourg, Saclay)**
     - Rolling shutter, low power tracker, 34x240 array, 20x20 um^2 pitch pixels
  2. **ILC (Strasbourg, Bergamo, Pavia)**
     - Self triggering pixel tracker, 245 x 245 array, 20x20 um^2 pitch with fast X-Y projection readout

- **Sub-reticule B – Three sub-circuits**
  1. **Two separate memory cores (CMP)**
  2. **MAPS for ILC (Strasbourg, Saclay)**
     - 42x240 array, 20x20 um^2 pixel MAPS operating in rolling shutter mode, 80 ns/ row
  3. **MAPS for ILC (Strasbourg)**
     - 128 x192 array, 12x24 um^2 pixel MAPS with 5 bit time stamp, 2nd hit marker, full serial readout
     - Future goal: to use separate sensor tier and to reduce the pixel size to 12x12 um^2

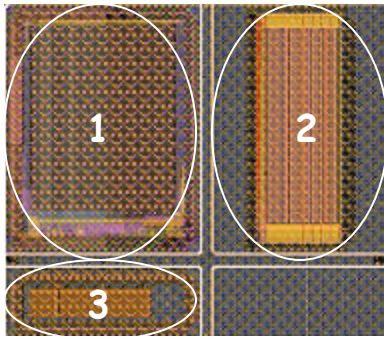
Sub-reticules C & D



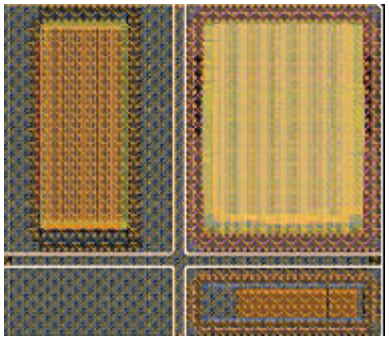
C Left



C Right



D Left

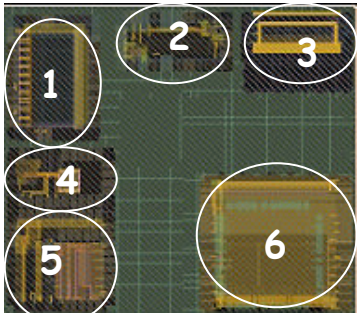


D Right

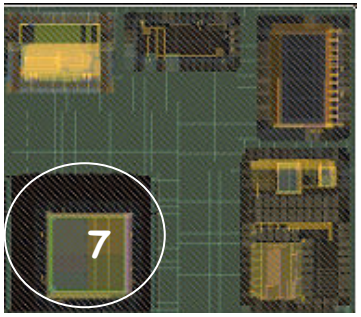
- **Sub-reticule C: 4 sub-circuits**
  1. **ATLAS 2D pixel design based on IBM 0.13 um FEI4 (CPPM/Bonn)**
     - Left (analog) side - 14 col, 60 rows, 50x166 um pixels with simple readout
     - Mating right side comprised of counter and "noisy" cells to study coupling to the left tier with different shielding ideas.
  2. **SEU resistant register and TSV-bond interface daisy chain to measure TSV and bond yield (CPPM)**
  3. **Test structures to evaluate transistor performance with TSVs in close proximity (CPPM)**
  4. **Test structures for robustness of circuits under wire bond pads (CPPM)**

- **SUB-RETICULE D: 3 SUB-RETICULES**
  1. **ATLAS 3D PIXEL DESIGN FOR ATLAS UPGRADE (CPPM/BONN)**
     - Left (analog) side - 14 col, 60 rows, 50x166 um pixels (same as sub-reticule C)
     - Mating right side contains special features such as time stamp, time over threshold, and four pixel grouping
  2. **SMALL PIXEL ARRAY FOR SLHC (LAL)**
     - 24x64 array of 50x50um^2 pixels
     - Threshold adjustment DAC/pixel
  3. **TSV CAPACITANCE TEST CIRCUITS (CPPM)**

Sub-reticule E



E Left

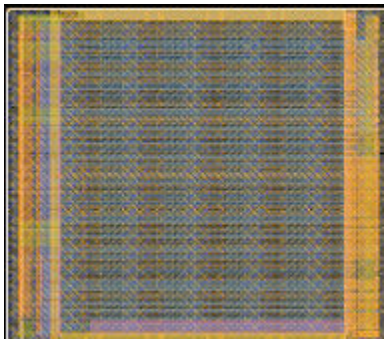


E Right

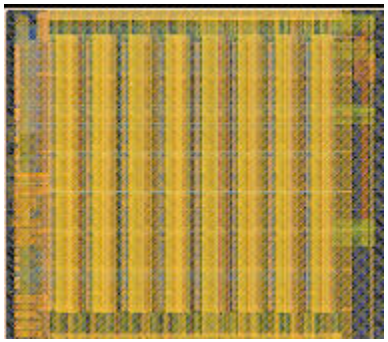
- **Sub-reticule E: 7 sub-circuits**

1. **3D MAPS with 32x64 array of 25x25 um² pixels with DCS, discriminator, auto-zeroing. Control logic in digital tier (Roma)**
2. **3D MAPS test structures - Two 3x3 40x40 um² pitch arrays. One with shaper-less preamplifiers (Pavia/ Bergamo/Pisa)**
3. **3D MAPS test structure with 8x32 array of 40x40 um² pixels, DNW sensors, data push architecture (Pavia/Bergamo/Pisa/Bologna)**
4. **Two test structures for the sub-reticule F DNW MAPS device (Pavia/ Bergamo)**
   - 16x16 array of 20x20 um² pixels with inter-train sparsified readout
   - 8x8 array of 20x20 um² pixels with selectable analog readout of each pixel
5. **Two 3D test structures**
   - 3x3 array of 20x20 um² pixels and 4 single channels for DNW MAPS (Pavia/Bergamo)
   - 5x5 and 16x16 3T pixel matrices with small and large detecting diodes (Perugia)
6. **2D version of 3D MAPS device in sub-reticule F, 64x64 array of 28x28 um² pixels (Pavia/Bergamo)**
7. **2D sub-matrices with 10x10 and 20x20 um² pixels to test signal to noise performance of MAPS in the Chartered process (Roma)**

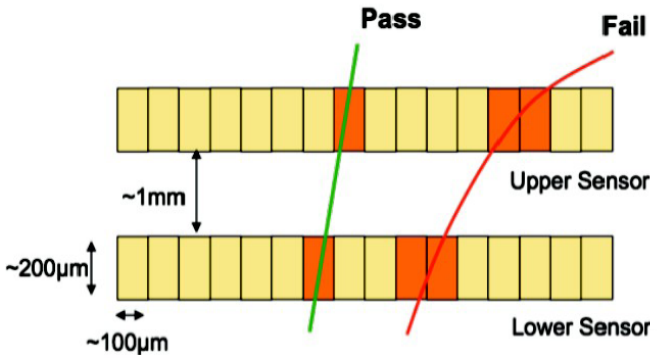
Sub-reticule H



H Left



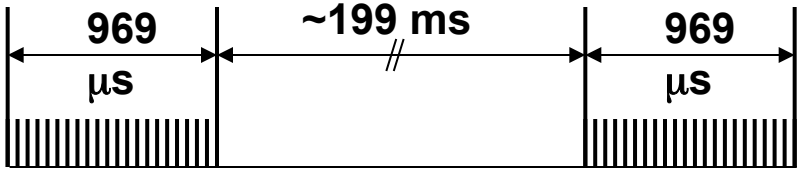
H Right



- **Sub-reticule H: VICTR Vertically Integrated CMS TRigger chip (FNAL/CPPM/LBNL)**
  - Processes signals from two closely spaced parallel Si sensors to form a track p_T trigger
  - Top tier: long phi strips Bottom tier: short z strips
  - Top tier looks for hits from long phi strips and bottom tier looks for coincidence between the phi strips and the hits from short z-strips connected to the bottom tier, to form p_T trigger
  - Serial readout of all top and bottom strips along with coincidence information
  - Downloadable hit patterns
  - Fast OR outputs
  - Circuit to be thinned to 24 microns and connections made to both the top and bottom of the chip
  - Designed for 80 micron pitch sensors
  - Sensors developed separately

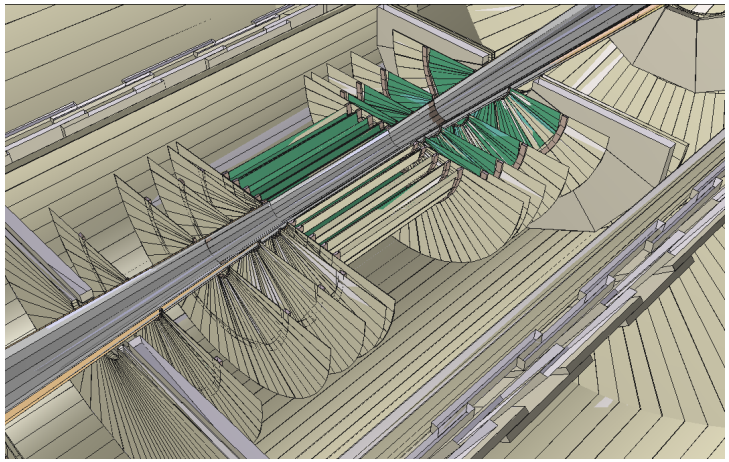
Pixel Detector

- The physics program at the ILC emphasizes excellent impact parameter and momentum resolution over the full angular region



ILC Beam structure:
Five trains of 2625 bunches/sec
Bunch separation of 369.2 ns

- Pixel detector requirements
  - Transparency: 0.1% X_0 per layer (equivalent of 100 μm of Si)
  - Low power consumption (~50 W for 1 Giga pixels)
  - High resolution thus small pixel size
    - Excellent point resolution (< 4 μm)
    - Superb impact parameter resolution (5μm ⊕ 10μm/(p $\sin^{3/2}\theta$))
  - Good angular coverage; robust pattern recognition (track finding in vtx alone)
  - Modest radiation tolerance for ILC applications
  - EMI immunity

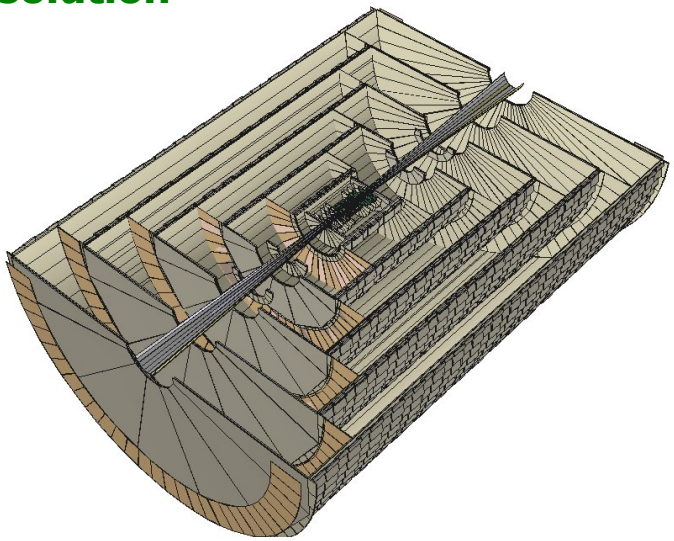


- Combination of small pixels, short integration time, low power required for ILC is difficult to achieve
  - Small pixels tend to limit the amount of circuitry that can be integrated in a pixel
  - Small pixels also mean that the power/pixel must be kept low

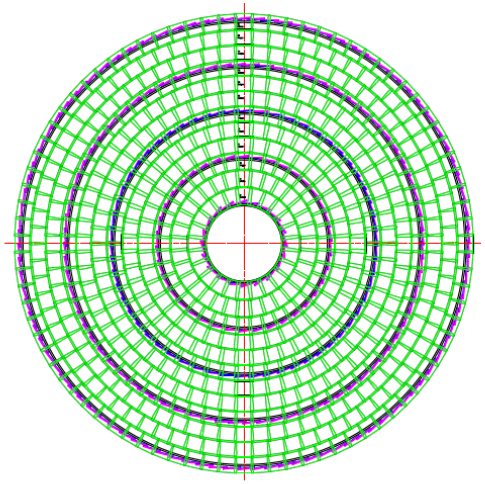
- A candidate technology is the 3D silicon technology

Tracking Detector

- **Tracking detector requirements**
  - **Transparency: 0.8% X_0 per layer average over full fiducial volume**
  - **Superb point resolution and momentum resolution**
    - Strip pitch of 25 μm
    - $\sigma(1/p) = 2\ 10^{-5}$ (GeV^{-1}) at 90 degrees
  - **Good angular coverage; robust pattern recognition**
    - Single bunch timing
    - Very high tracking efficiency for PFA
  - **Robust against aging and beam accidents**
  - **Modest radiation tolerance**



- **Silicon technology chosen**
  - **Mature technology which allows emphasis on phi resolution**
    - Superior asymptotic p_T resolution
  - **Allows for flexibility in minimizing material distribution through fiducial volume**



Track Finding Algorithm

- **Fit a helix to 3 seed hits**
  - **First fit without MS errors; determination of the helix parameters $\omega \equiv 1/R$, d_0, ϕ_0, z_0, and $\tan(\lambda)$**
  - **Calculate the MS errors for each hit using this helix**
  - **Perform a second helix fit including MS errors**

- **Calculate χ^2 from fit and constraints (p_T>x) if necessary**
  - **Calculate a constrained χ^2 to estimate the increase in χ^2 needed to pull into compliance with the constraint**
    - Constraints: $p_T > p_T^{min}$, $|d_0| < d_0^{max}$, $|z_0| < z_0^{max}$
    - Example: if ($|z_0| > z_0^{max}$) $\chi^2 = \chi^2 + (|z0| - z_0^{max})^2 / \sigma^2(z_0)$

- **Reject seeds that fail the χ^2 cut**

- **Confirm the seed by adding additional hit(s) from confirmation layer(s)**
  - **Perform a helix fit on the new seeds and those that fail the χ^2 cut are eliminated**
  - **Typically, it is found that good performance is achieved with one confirmation layer**

Track Finding Algorithm

- Extend the seed to include hits in additional tracking layers
  - Typically include all additional layers track might traverse
  - Each time a new hit is considered, a helix fit is performed and the hit is discarded if it fails the χ^2 cut
  - A minimum of 7 hits on a track is required for track candidates
- Merge track seeds through a merge algorithm
  - Two track candidates are allowed to share a single hit, but if a track candidate shares more than one hit with another candidate, an arbitration scheme is used to select the better candidate. Precedence is given to the candidate with the greatest number of hits, while the candidate with smaller χ^2 cut is selected when the number of hits is equal