

DEPFET Vertex Detectors

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Status and Plans

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for the DEPFET Collaboration

Linear Collider Workshop 2010
Beijing, March 2010



Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

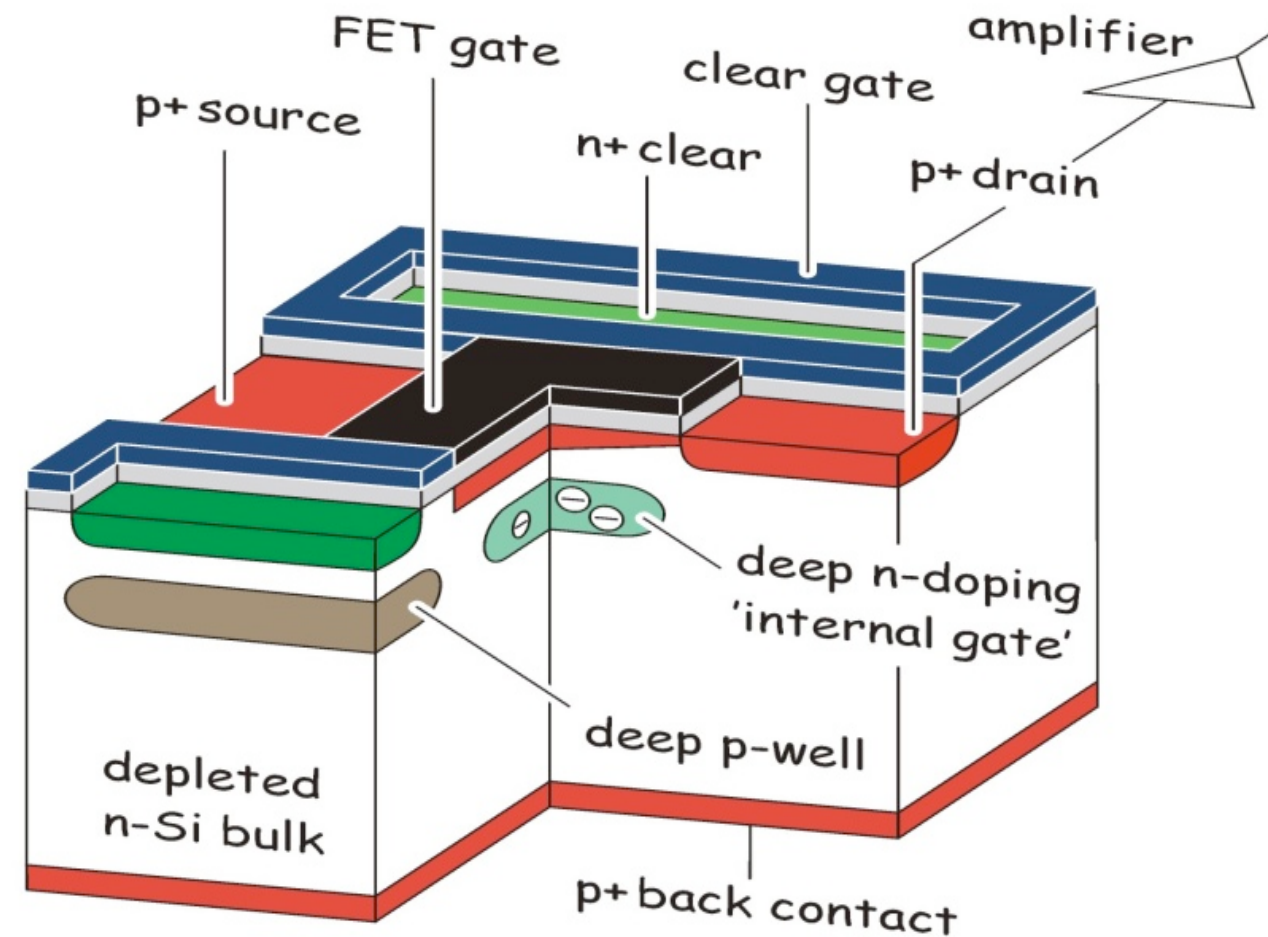


Overview

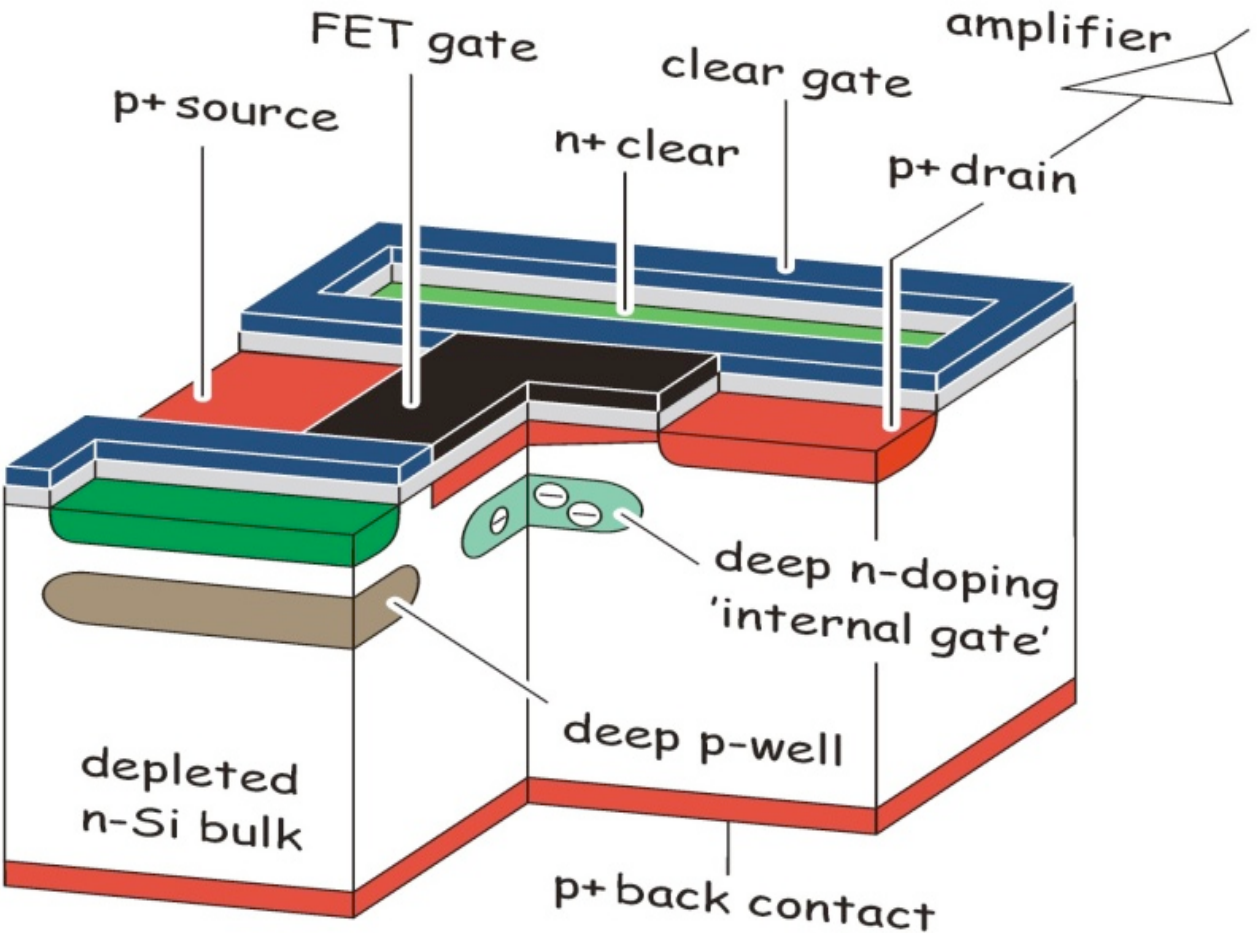
- DEPFET Technology
- Test Beam Results
- DEPFET Pixel Vertex Tracker for Belle-II
- The Road Ahead

DEPFET Basics: The Technology

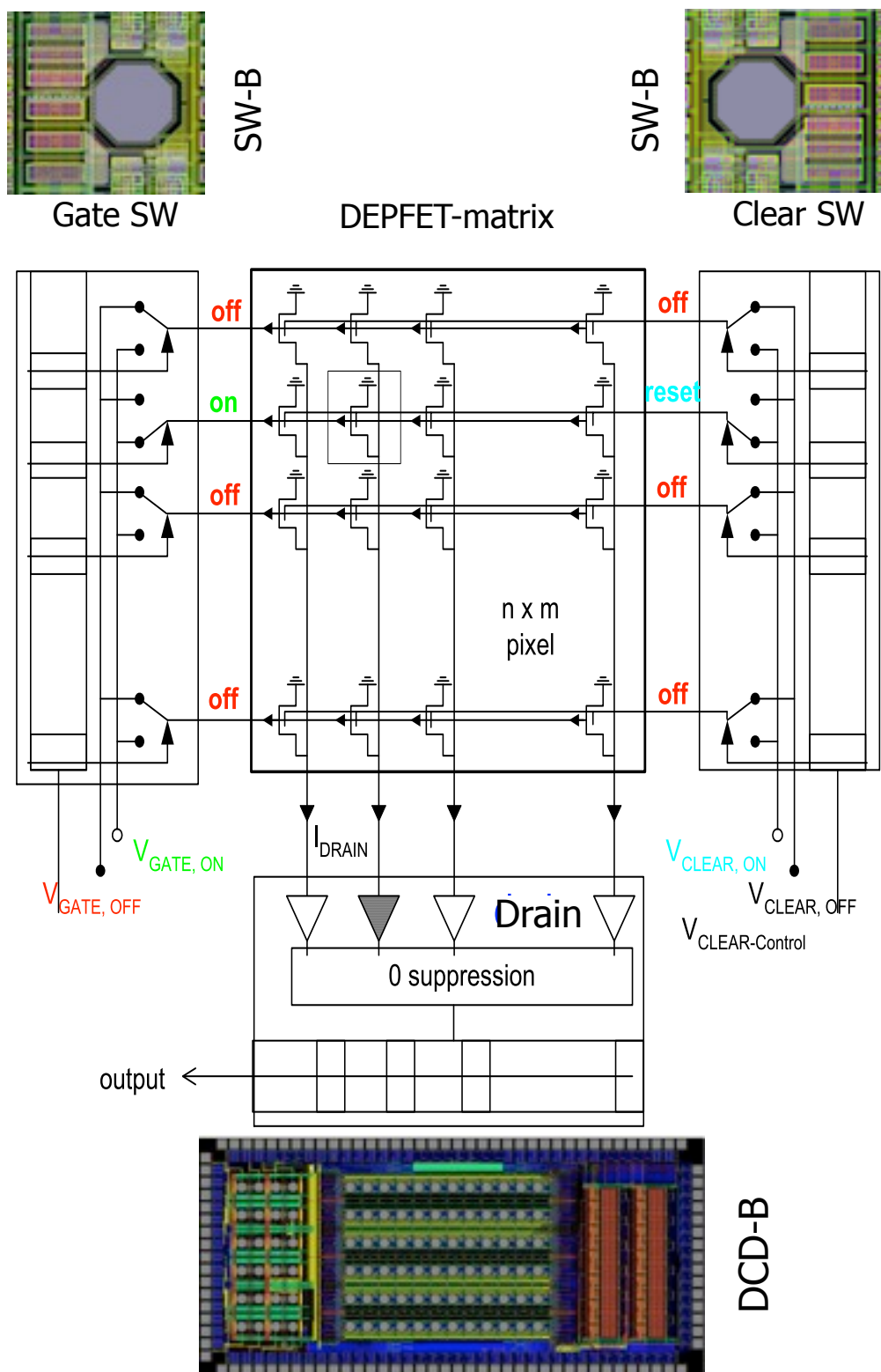
- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)
 - ▶ Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 400 \text{ pA/e-}$)
⇒ Internal amplification!
 - ▶ Low power consumption: Readout on demand, but: Constantly active for charge collection



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- 
- Small pixels possible
 - Small intrinsic noise due to small capacitance : $\sim 40 \text{ e}^-$ at high bandwidth readout
 - In-pixel amplification: Excellent signal to noise, thin detectors possible!

DEPFET Basics: Readout



Row wise r/o (Rolling Shutter):

- Select row with external gate, read current, clear DEPFET, read current again The difference is the signal
- Low power consumption: Only one row active at a time; Readout on demand (Sensitive all the time, even in OFF state)
- 100 ns readout time per pixel
- Two different auxiliary chips needed: Switchers for gate and clear
- Limited frame rate, but still: 50 kHz readout for 500 kPixel modules

DEPFET Basics: Thinning Technology



1. implant backside
on sensor wafer



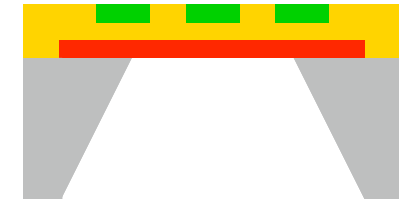
2. bond sensor wafer
to handle wafer



3. thin sensor side
to desired thickness

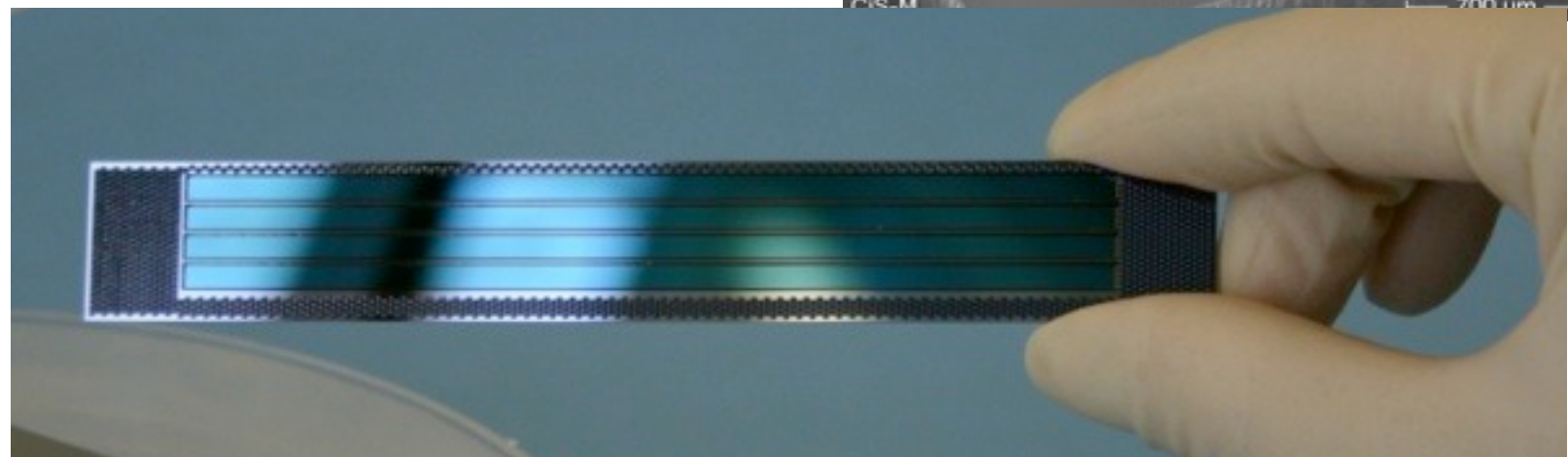
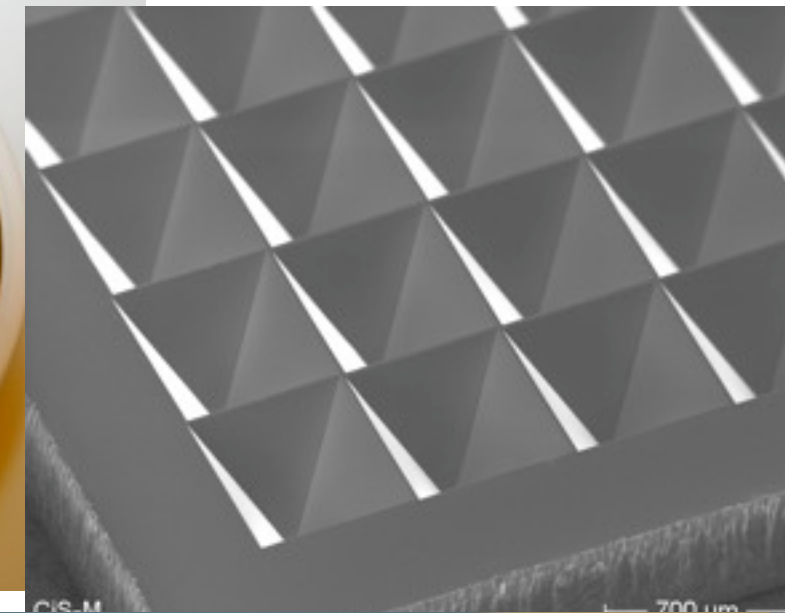
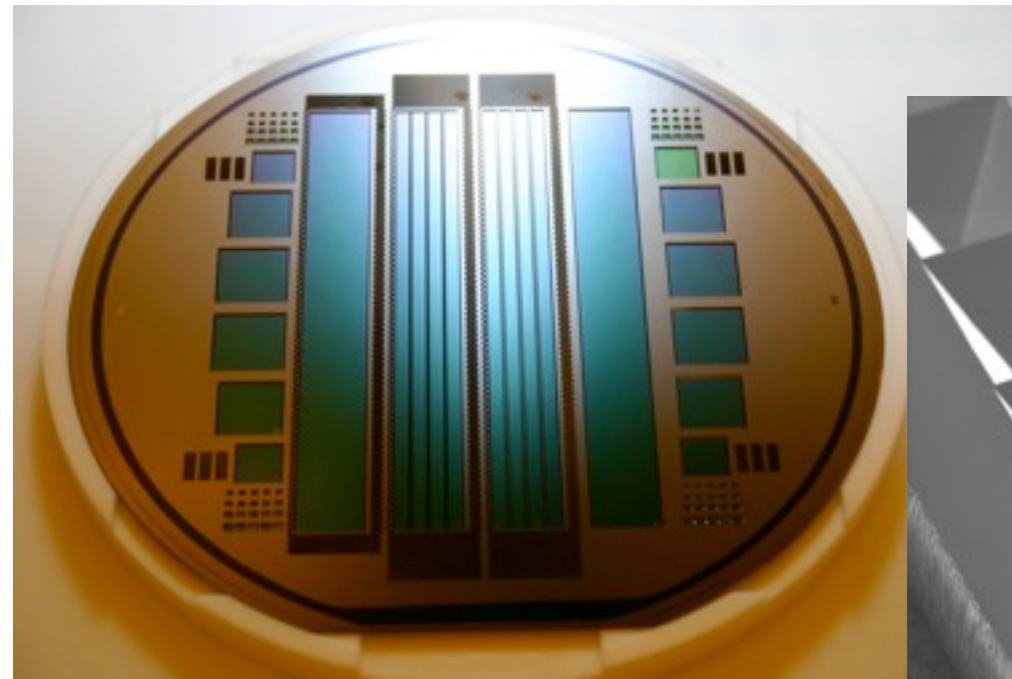


4. process DEPFETs
on top side



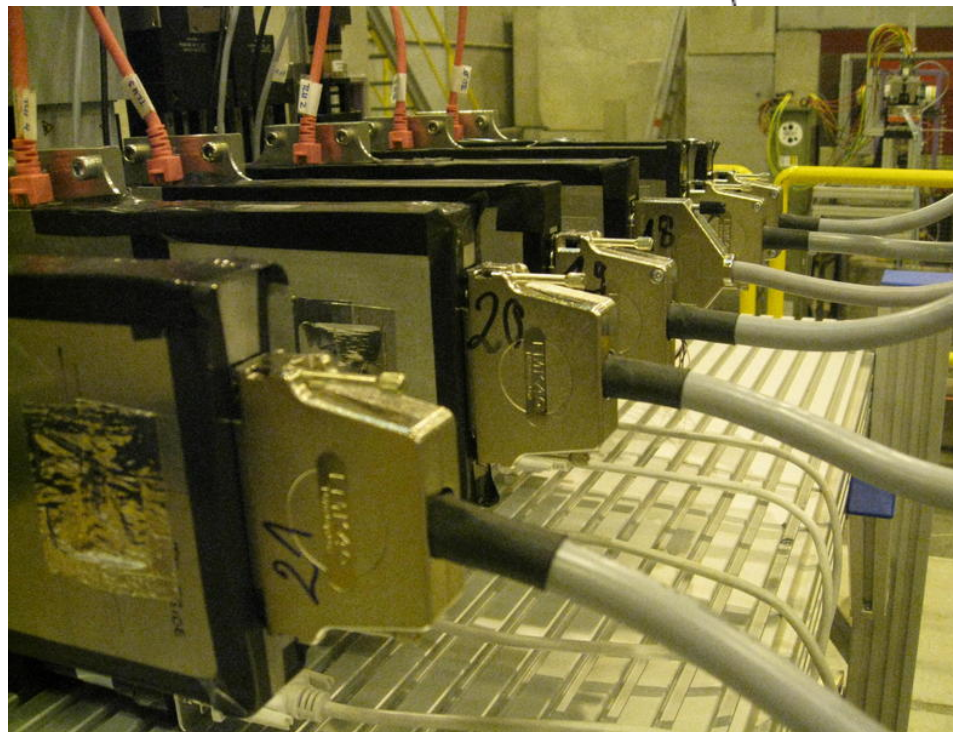
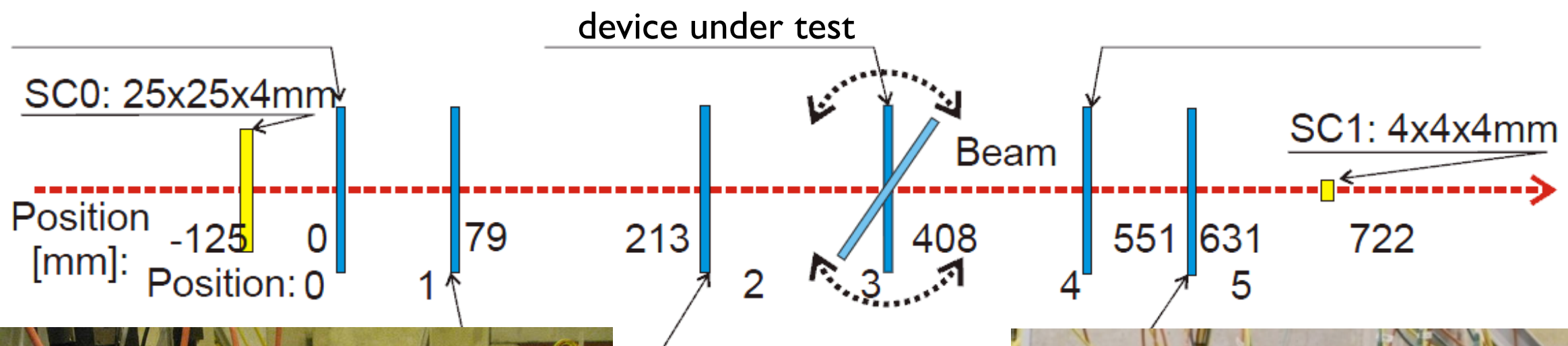
5. structure resist,
etch backside up
to oxide/implant

- Multi-step process
- Allows processing of both sides of sensor
- Mechanical support given by silicon structures produced in last etching step

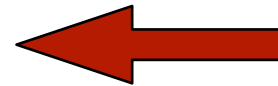


Test Beam Campaign

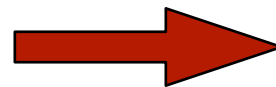
- Extensive test beam campaign at the CERN SPS 2008 and 2009
 - Test of “ILC” pixel structures: Small pixels, for optimum spatial resolution
 - Un-thinned silicon: 450 μm thick



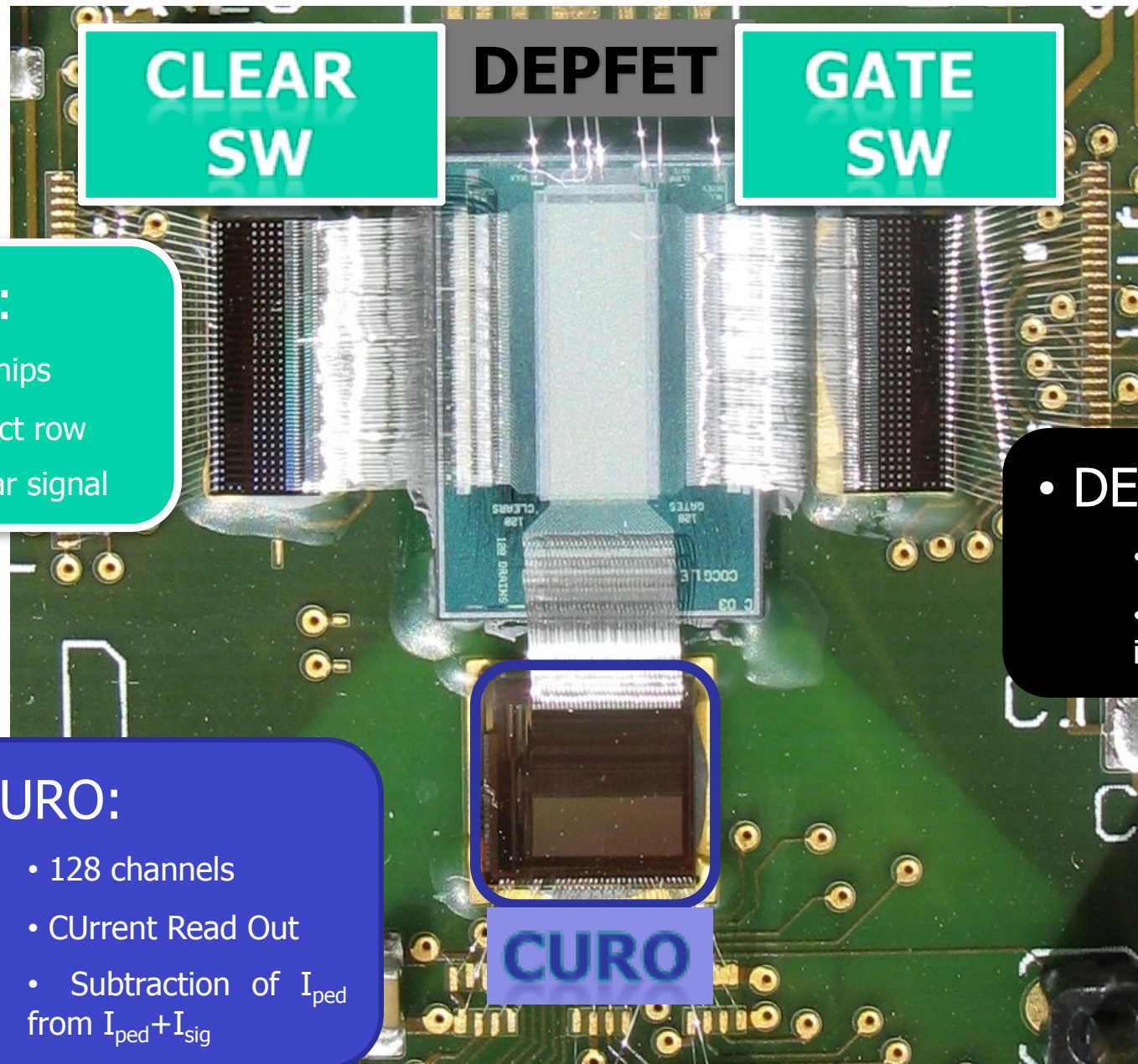
standalone tests:
DEPFET telescope



tests with EUDET
telescope



The Test Devices



- PXD5 chips tested in 2009

- **Switchers:**

- Steering chips
- Gate: Select row
- Clear: Clear signal

- **DEPFET Matrix**

- 64x256 pixels
- Several pixel sizes, implants, geometries

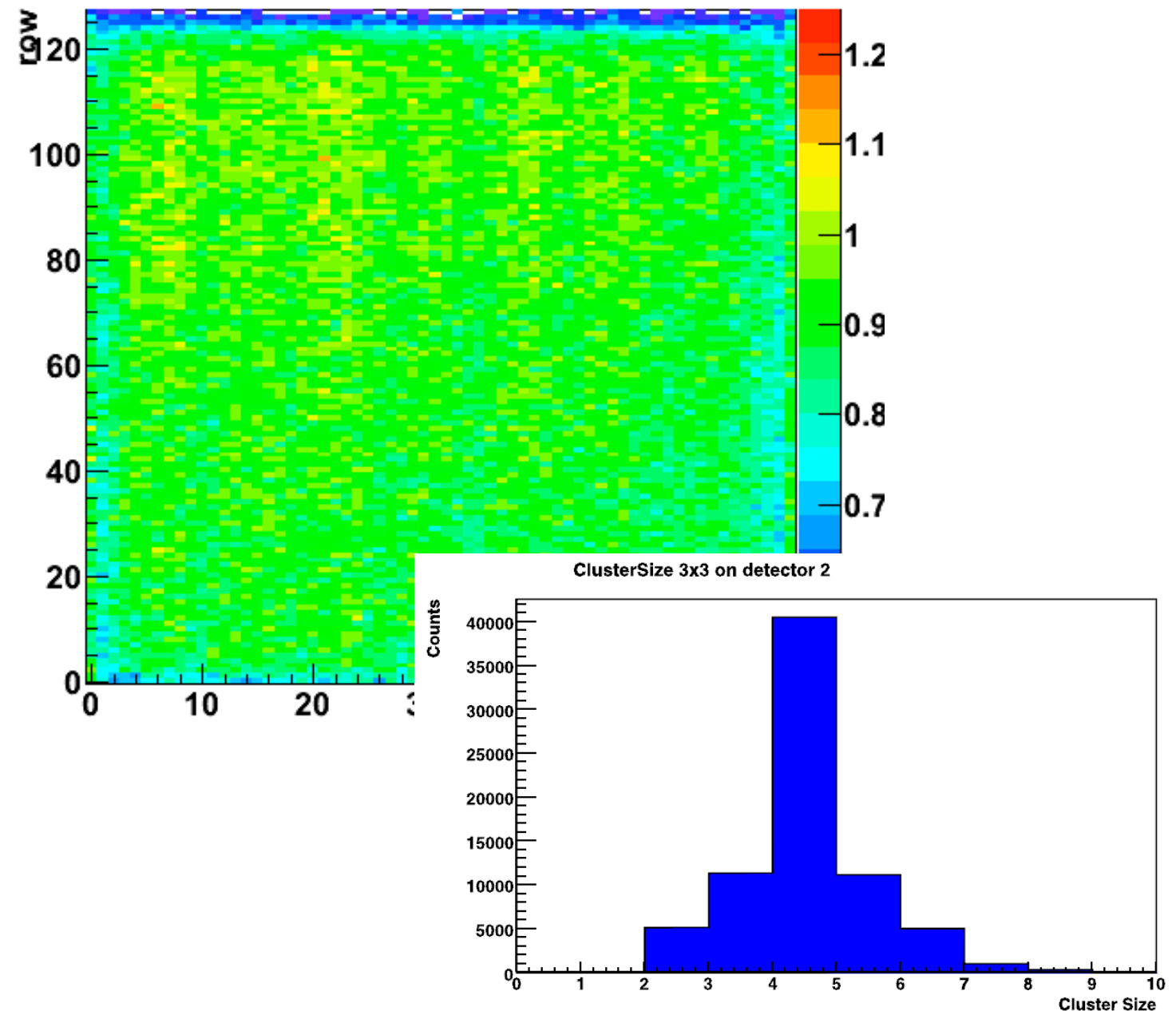
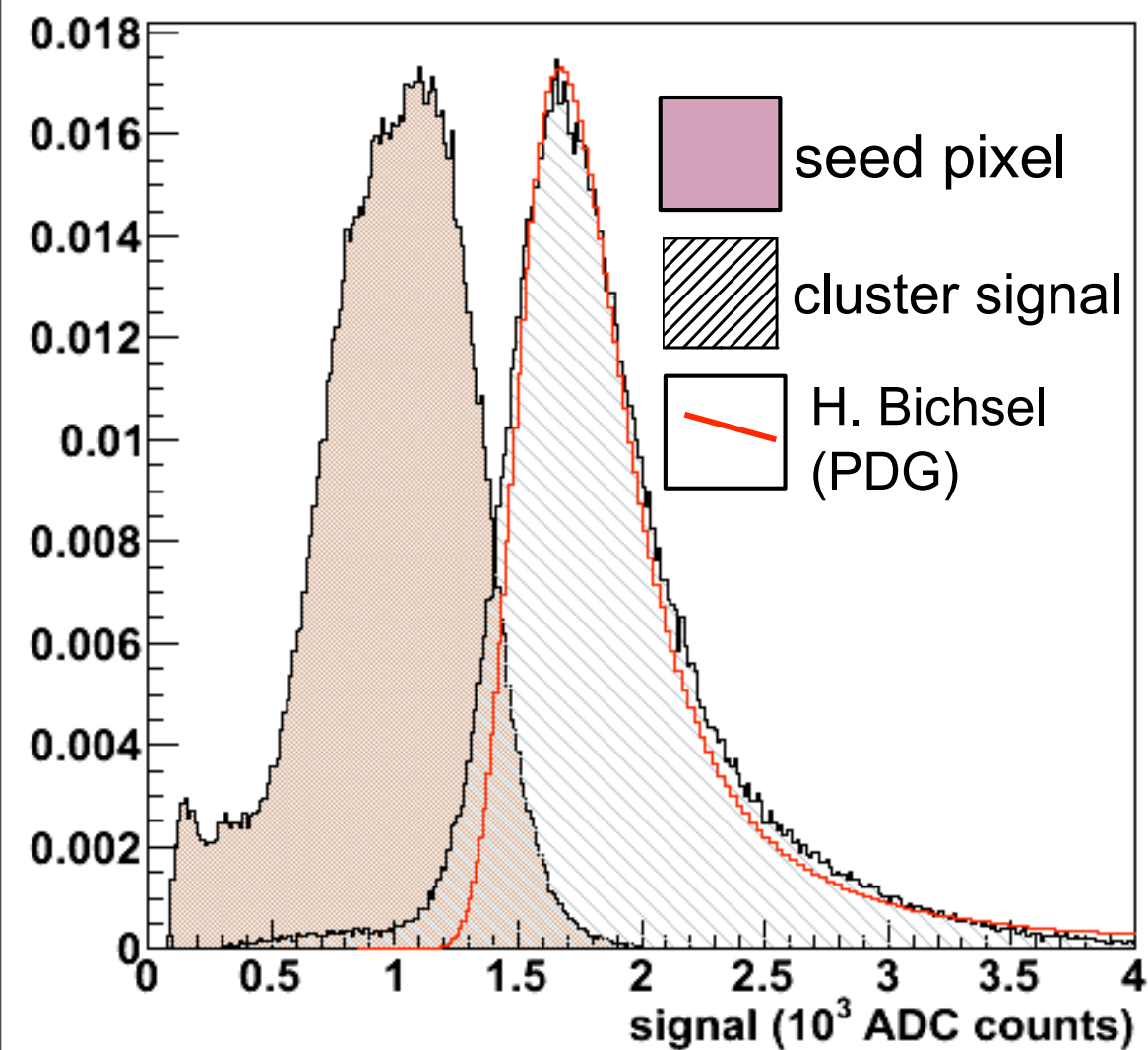
- **CURO:**

- 128 channels
- CUrrent Read Out
- Subtraction of I_{ped} from $I_{ped} + I_{sig}$

- unthinned devices: Silicon thickness 450 μm
- Production of thinned sensors (thickness 50 μm) in progress: PXD6

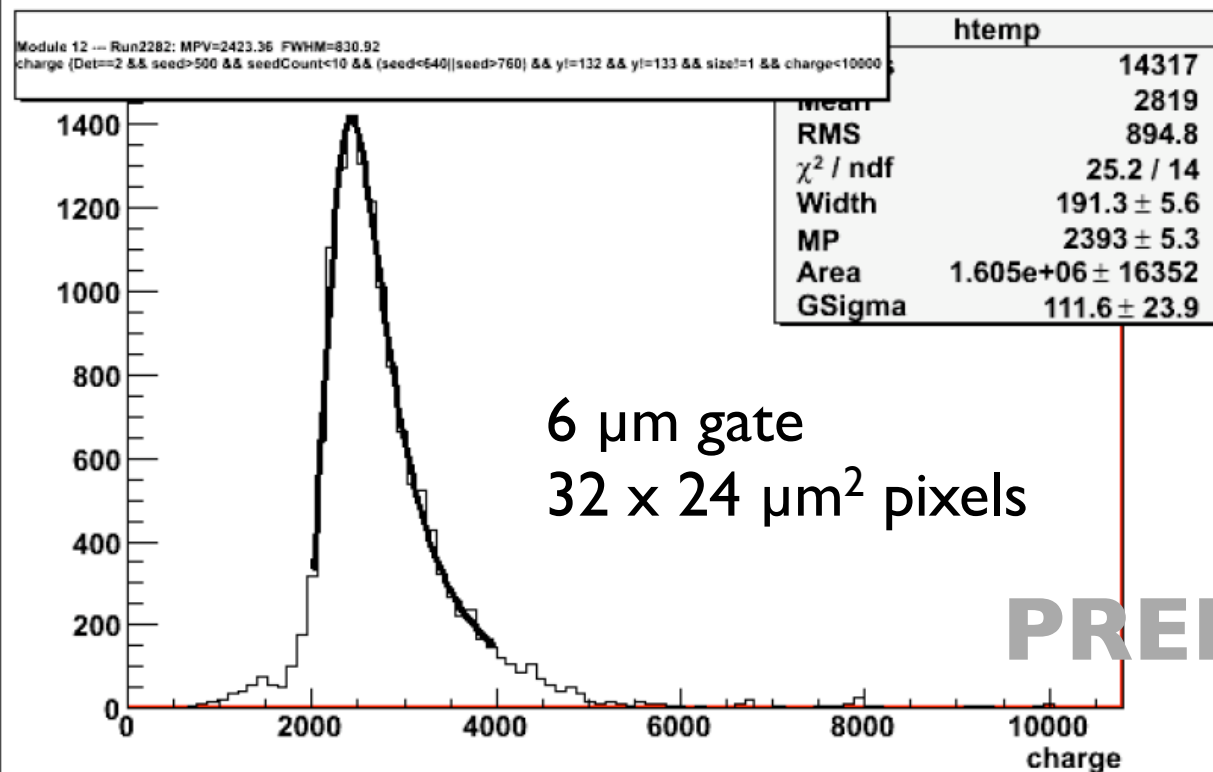
Results: Test Beam 2008

- Excellent performance observed: Clear detection of minimum ionizing particles, uniform response over the active area

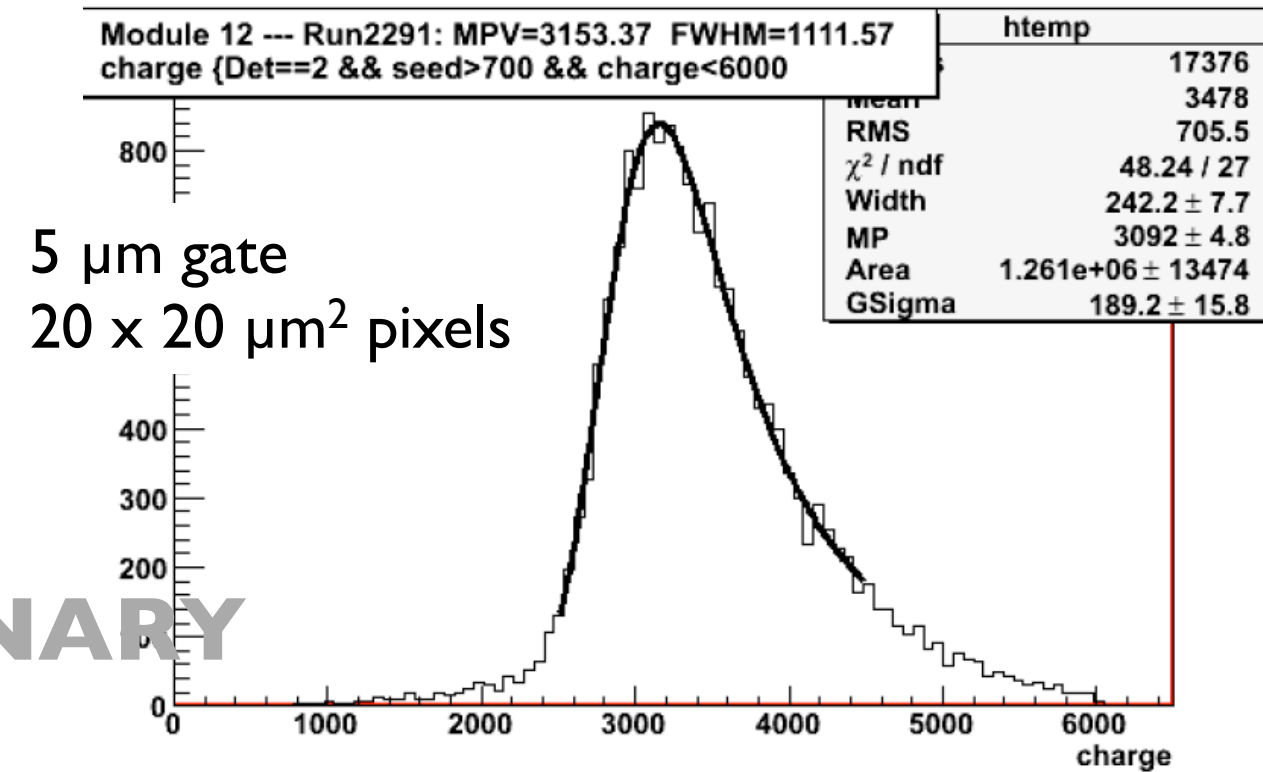


Further Improvement: Test Beam 2009

- Improved clearing through capacitatively coupled clear gate
- Study of different lengths for the gate (shorter gate $\Rightarrow$ higher gain)



S/N $\sim$ 160

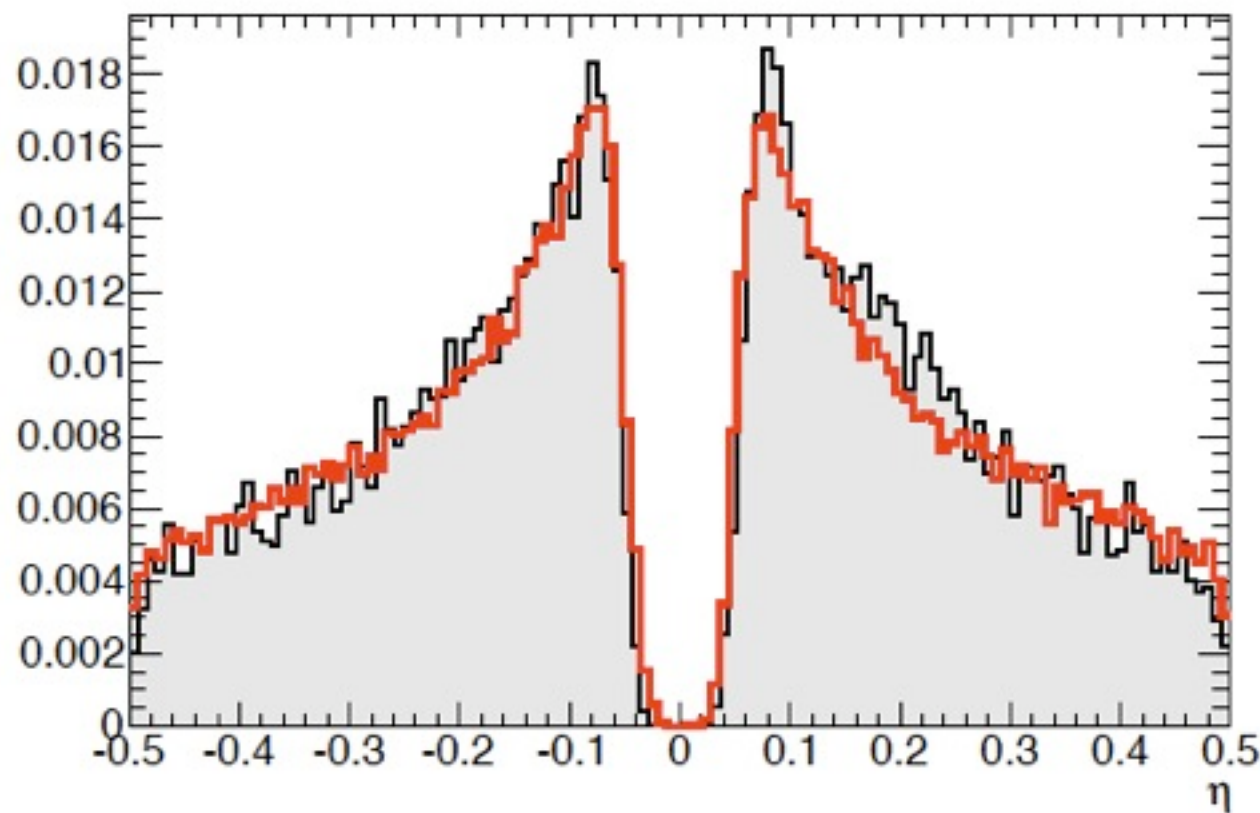


S/N $\sim$ 200

Excellent signal to noise ratio for thick sensors: Internal amplification in the DEPFET sensor!

Test Beam Results: Resolution & MC Validation

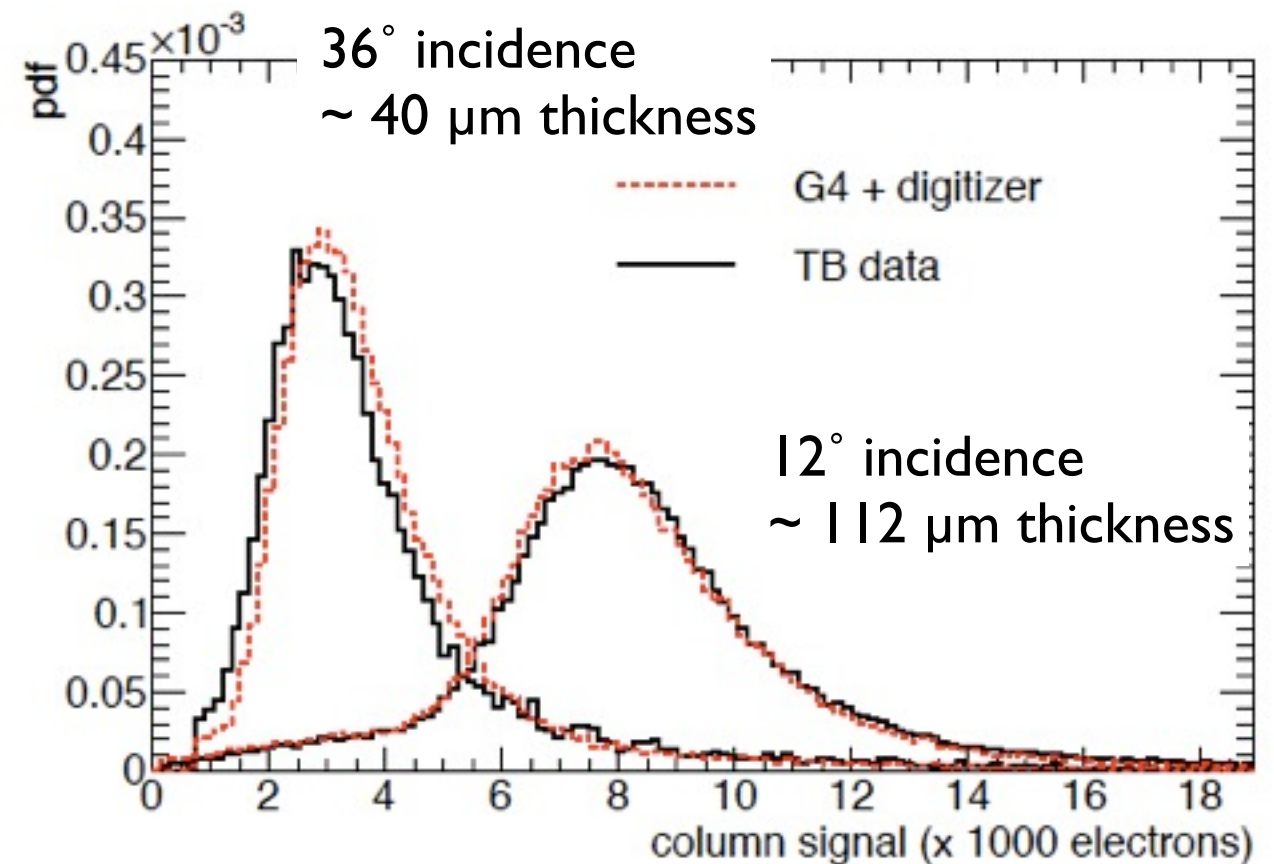
- High spatial resolution for $24 \times 24 \mu\text{m}^2$ pixels:
 $\sigma_x = 1.3 \pm 0.2 \mu\text{m}$, $\sigma_y = 1.2 \pm 0.1 \mu\text{m}$
- Simulation of detector response in good shape:



$$\eta = \pm \frac{S_N}{S_N + S_S}$$

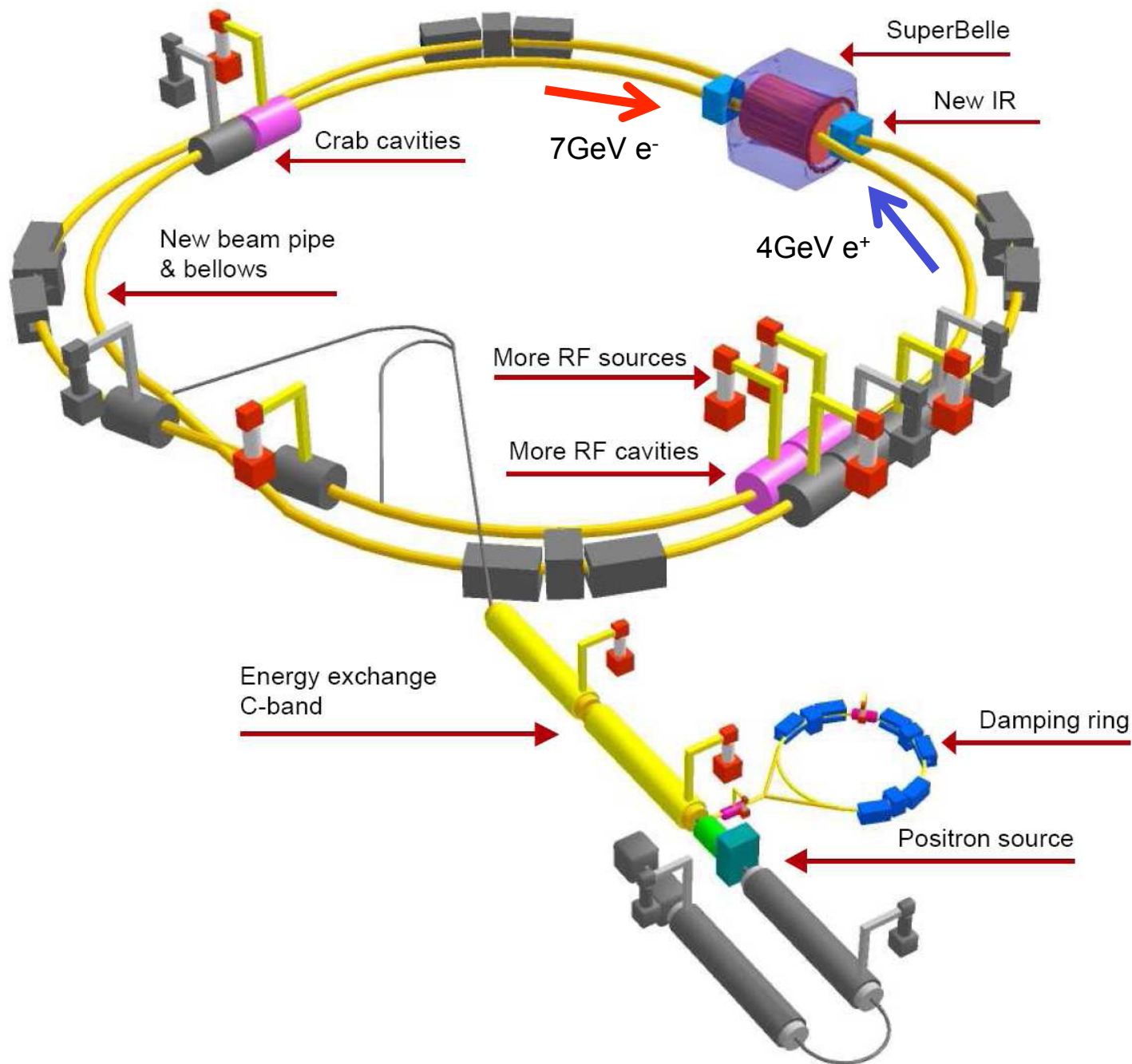
S_S : Seed amplitude

S_N : Amplitude of highest neighbor



From Prototypes to a Real Detector

- A DEPFET vertex detector now baseline for Belle-II



Upgrade of the KEK-B Flavor Factory

- Luminosity increase by x 40
final goal: $8 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$
aiming for an $\int L = 50 \text{ ab}^{-1}$
by 2020 (present data set x 50)
- Luminosity achieved by focusing:
“nano beams” and moderate
increase in current
- Increase in backgrounds: Both
Machine and QED background
- Still under investigation!

From ILC to Belle-II

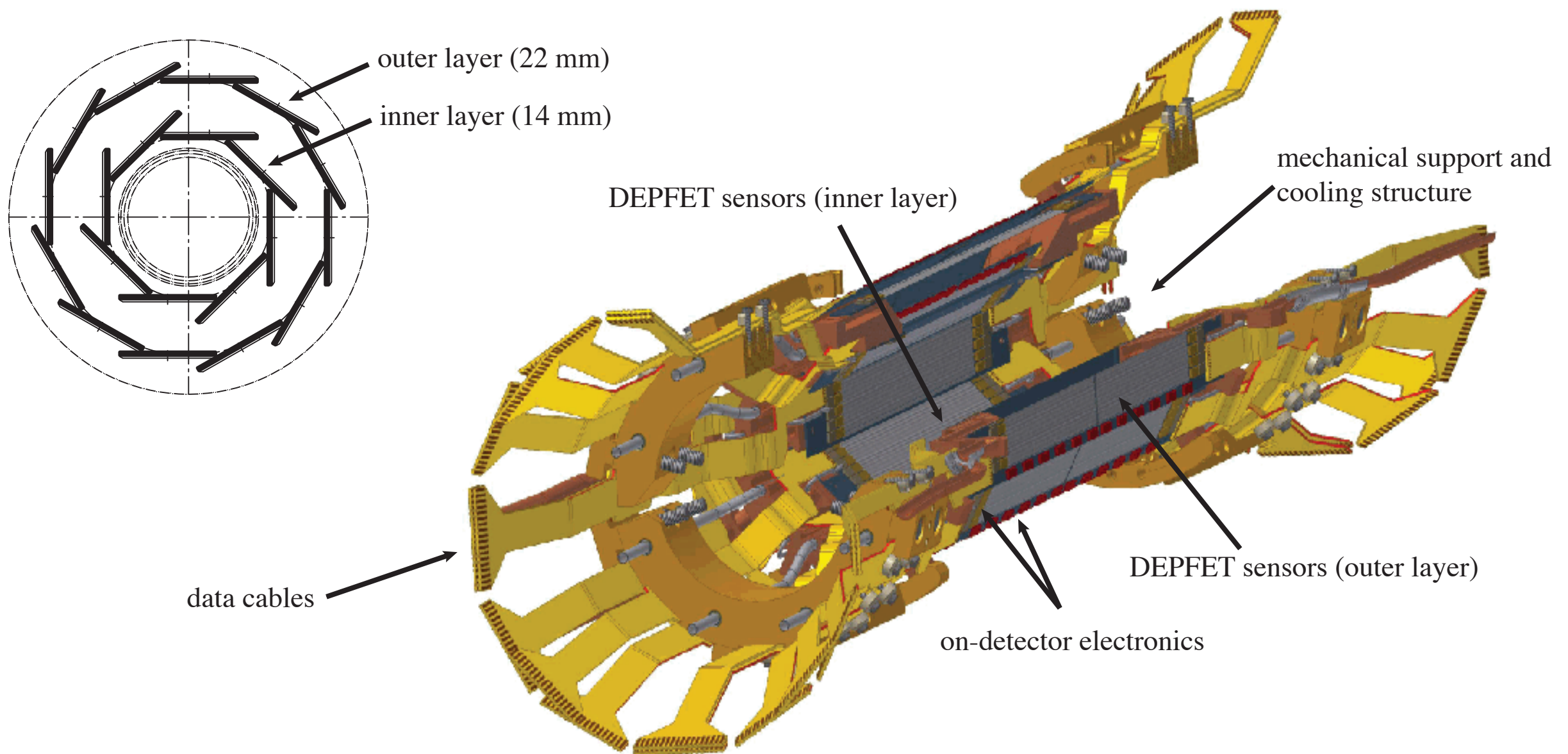
- The vertex detector at Belle-II brings with it its own set of challenges, compared to ILC:
 - Occupancy potentially up to 2%, machine & QED background (still under study)
 - Radiation dose > 1 Mrad / year $\Rightarrow$ Significant radiation hardness needed
 - Continuous readout $\Rightarrow$ Power and cooling becomes an issue
 - Frame rate $20 \mu\text{s}$
- On the physics side
 - ILC needs very large coverage, tracks of all momenta (focus on higher p_T)
 - Belle has a restricted coverage ($17^\circ - 150^\circ$), focus on low momentum tracks, even down to < 100 MeV

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- ▶ For the Belle-II PXD:
 - ▶ Moderate spatial resolution: 10 μ m (ILC: 2 μ m) $\Rightarrow$ larger pixels 50 x 50 μ m², 50 x 75 μ m²
 - ▶ Low material budget: 0.15% X_0 /layer (comparable to ILC goal)

The Belle-II PXD

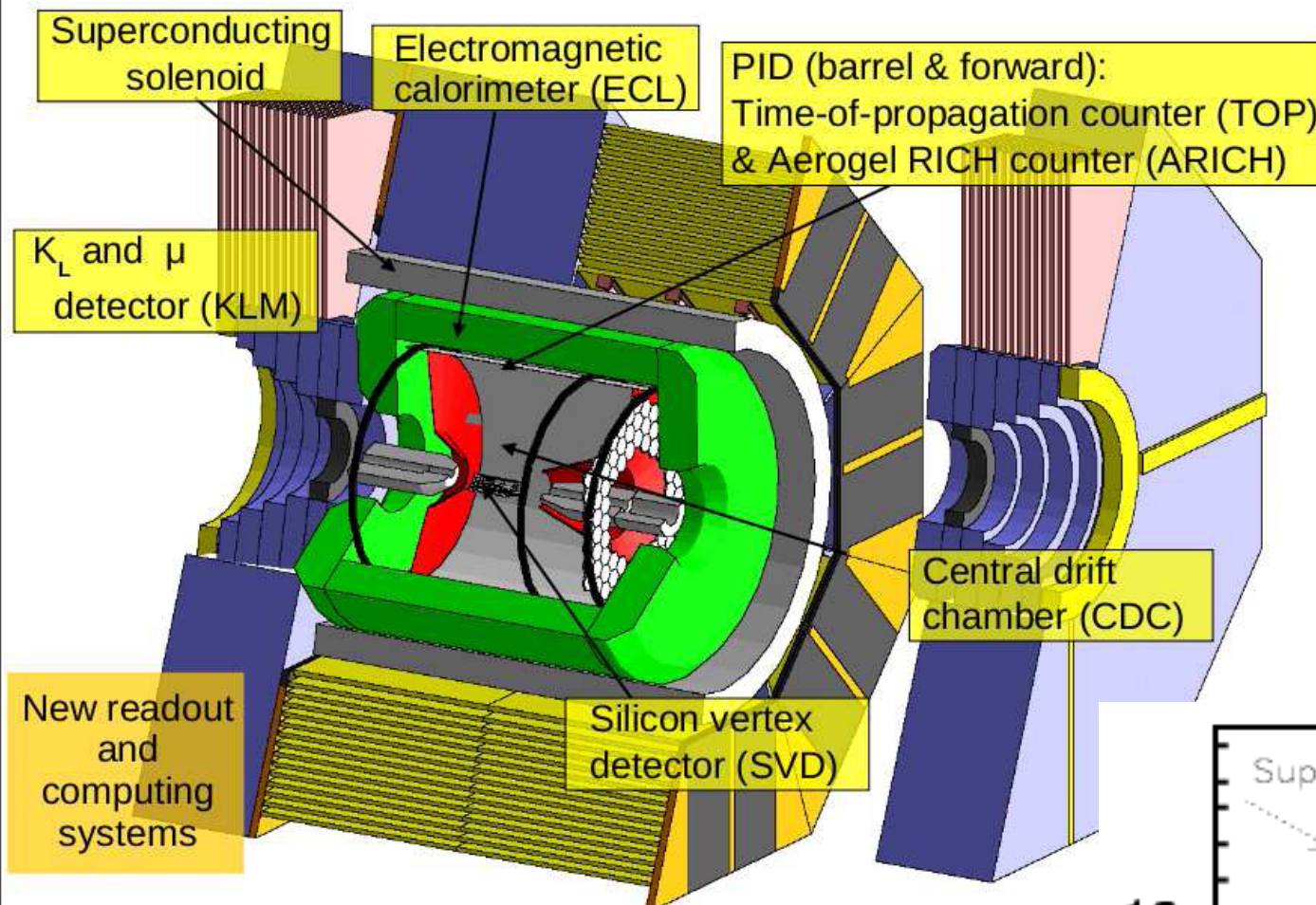
- 2 layer pixel vertex tracker
 - inner layer at a radius of 14 mm, outer layer at 22 mm
(beam pipe inner radius 10 mm, outer radius 12 mm $\Rightarrow$ getting as close as we can!)



A Sense of Scale



The PXD within Belle-II

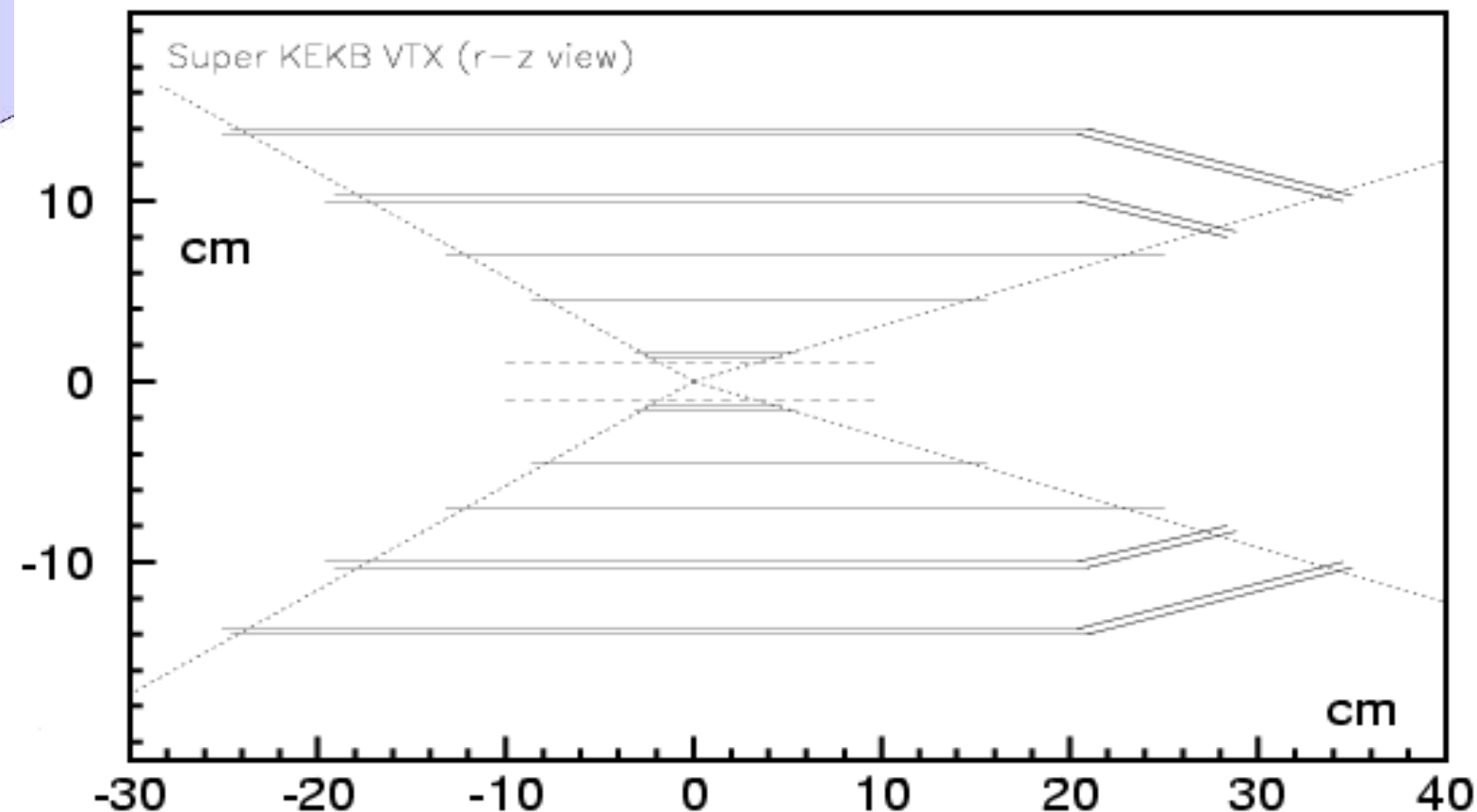


• Belle-II Tracking:

- Large volume tracker:
Central Drift Chamber
- Inner tracking:
Silicon Vertex Detector & Pixel Detector

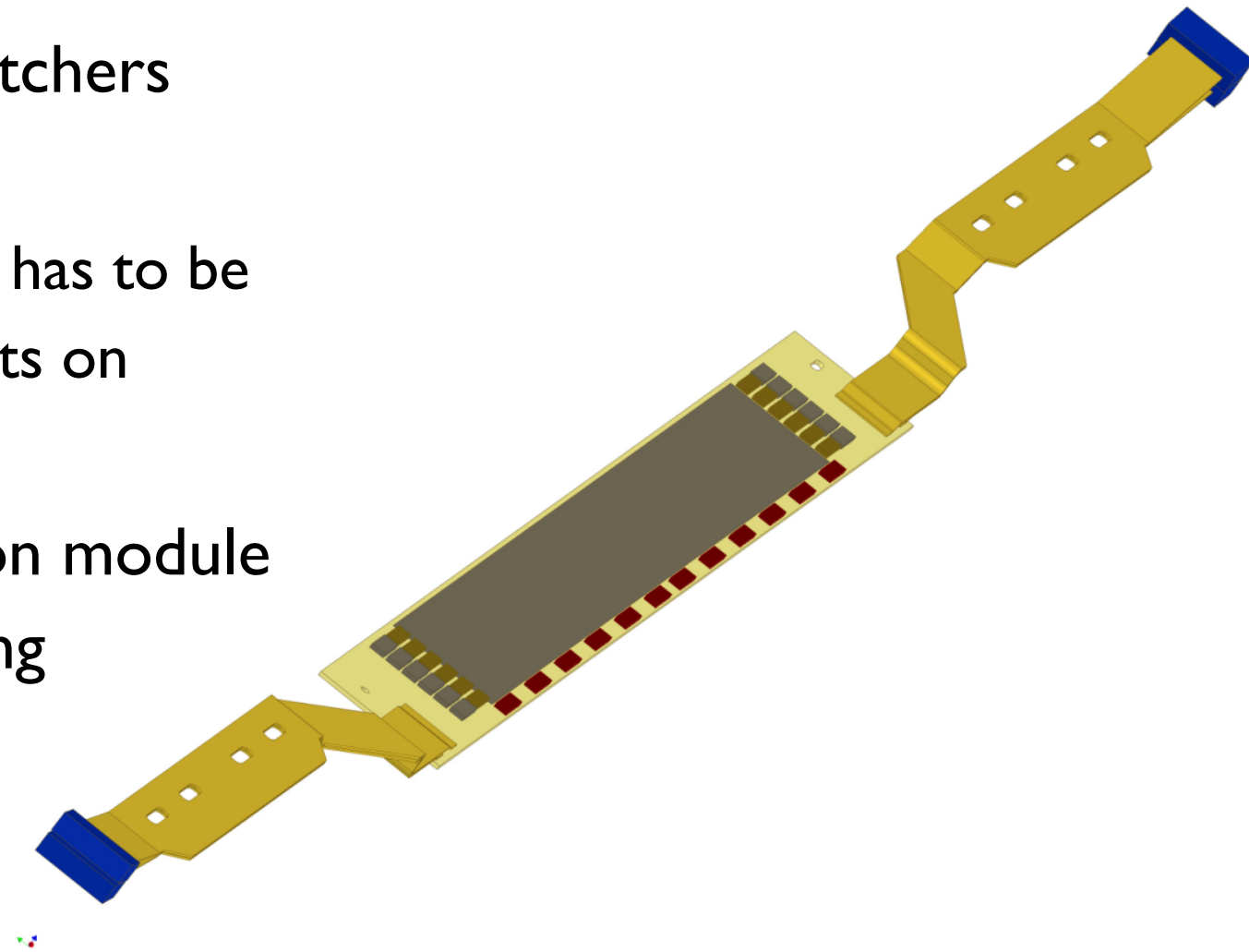
• Inner Tracking:

- 4 layer SVD, slanted modules in forward region of outer modules
- 2 inner layers
DEPFET-based PXD

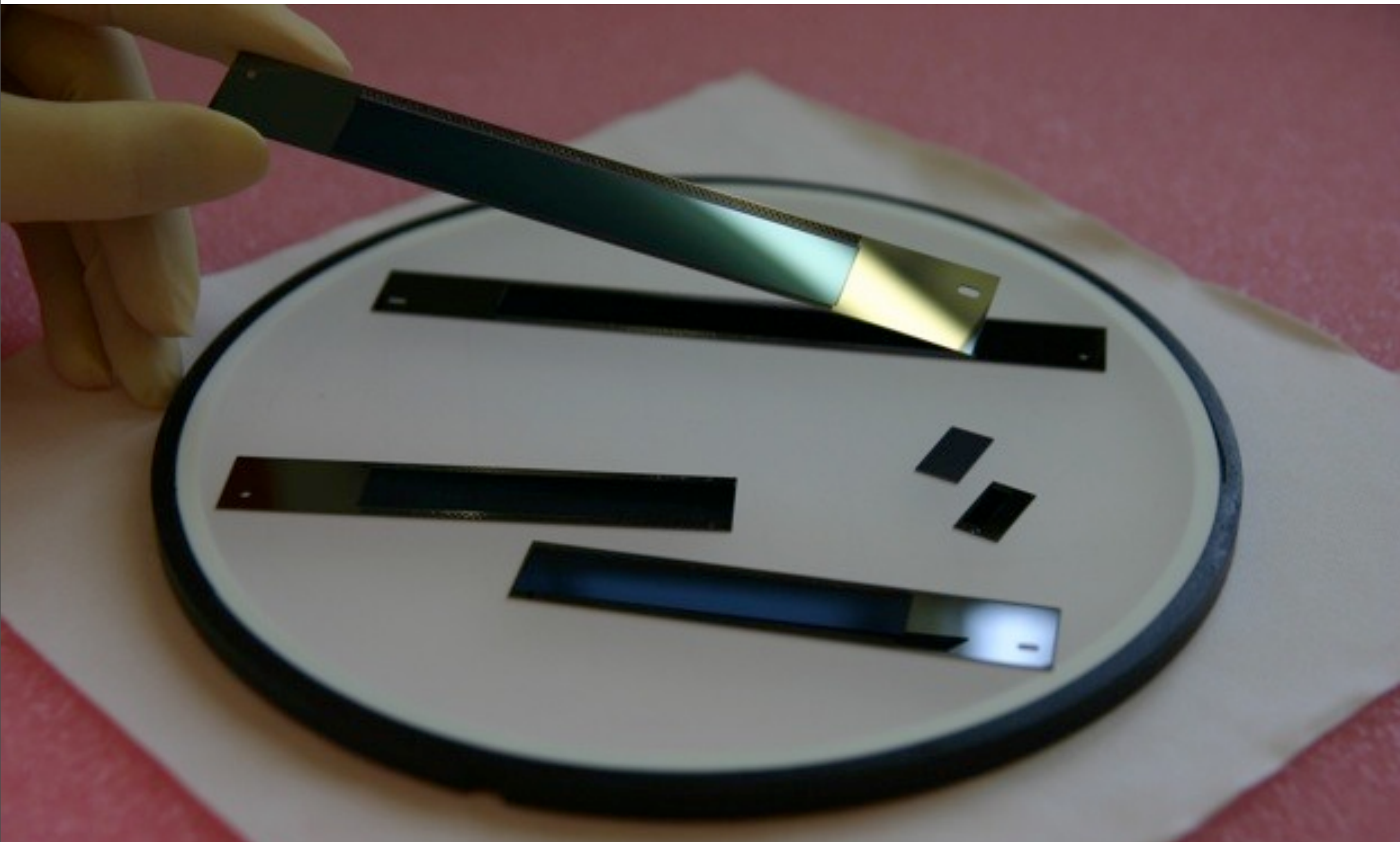


The PXD Modules

- All-silicon modules, with electronics (switchers and digitizers) bump-bonded on
 - inner layer can be monolithic, outer layer has to be split in the middle due to space constraints on wafer
- Kapton cable for data and power glued on module at both ends, connections by wire bonding
- 250 x 800 pixels per half-ladder
- 12 outer and 8 inner modules
- ▶ Total number of pixels 8 M

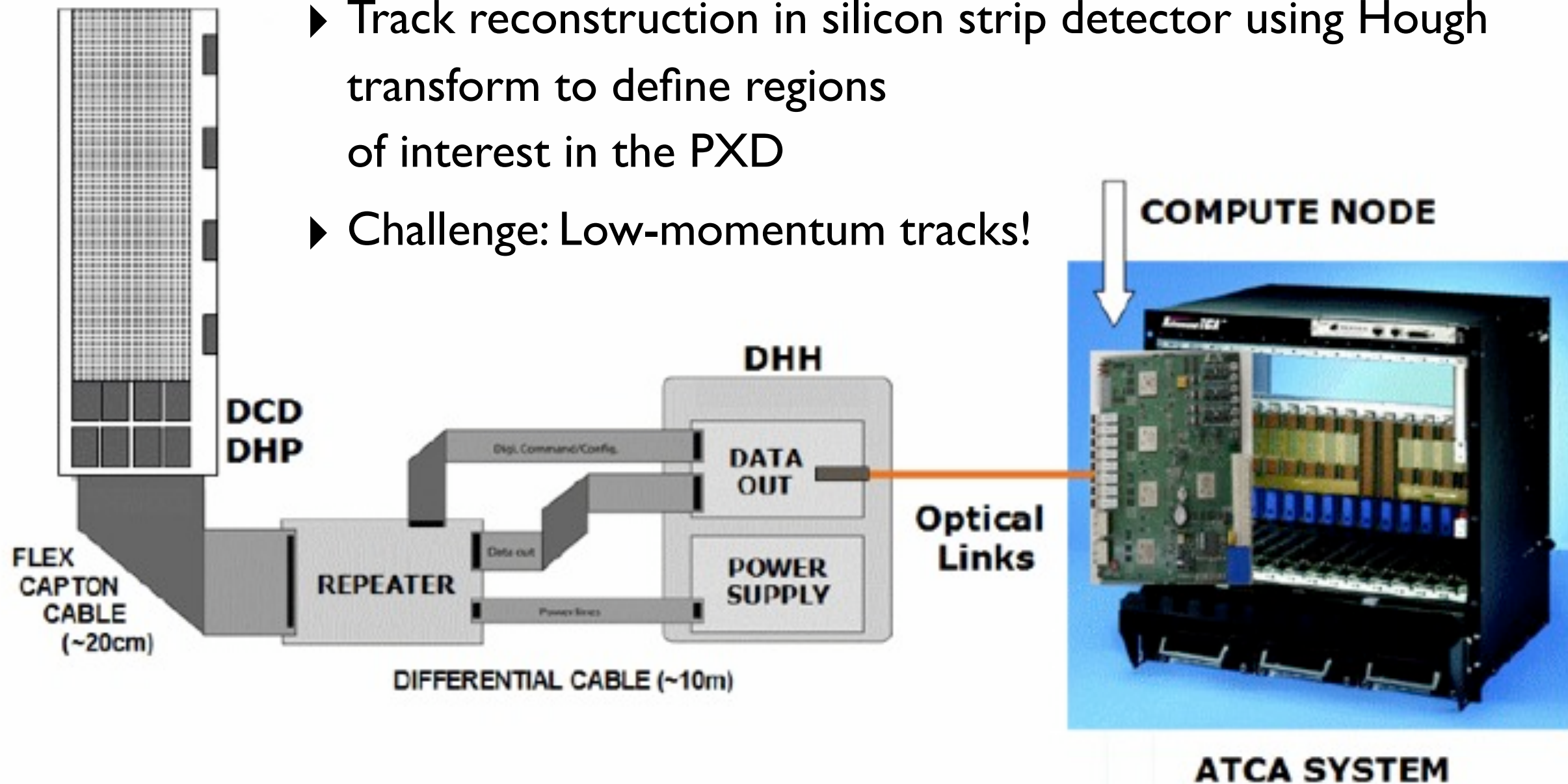


Mechanical Dummies: Thinned Silicon



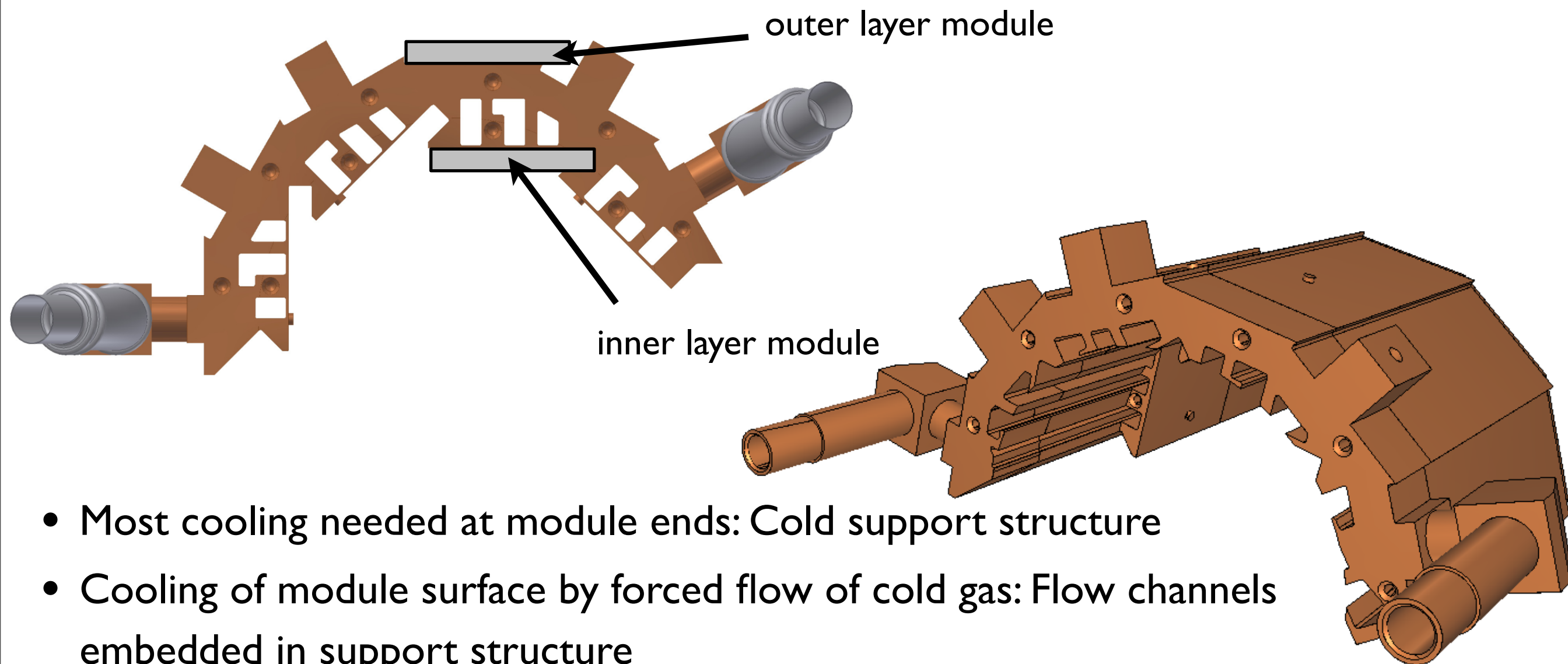
DAQ Concept

- Extreme data volume: The PXD generates up to 10 GB/s of data
 - ▶ Data transfer with high-speed optical links to DAQ system
 - ▶ Fast online reduction of data volume needed:
 - ▶ Track reconstruction in silicon strip detector using Hough transform to define regions of interest in the PXD
 - ▶ Challenge: Low-momentum tracks!



Cooling: The Challenge of Constant Readout

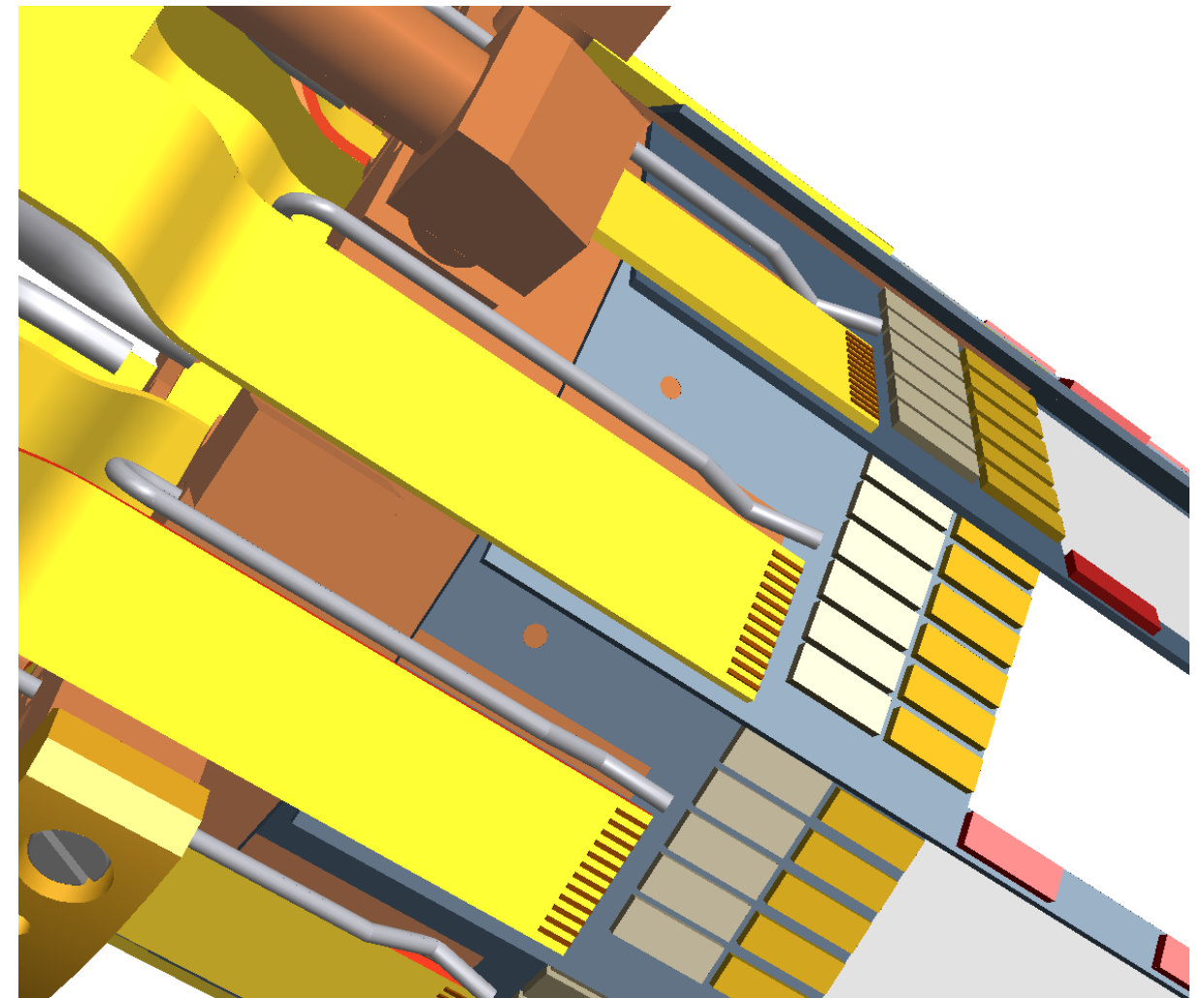
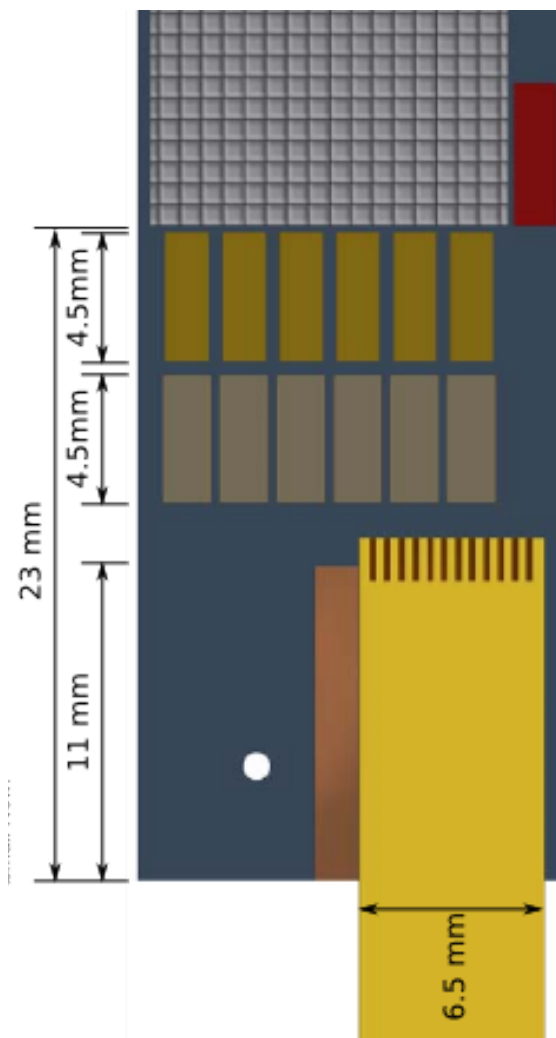
- Power consumption ~ 8 W per module end in constant readout mode, 1 W in addition over the active area including switcher chips
- ▶ ~ 180 W per detector side: Active cooling needed!
 - ▶ Evaporative cooling using CO_2 , other options still being considered



- Most cooling needed at module ends: Cold support structure
- Cooling of module surface by forced flow of cold gas: Flow channels embedded in support structure

Putting it together: Fixation of Modules

- Fixation of modules has to allow for thermal movement to avoid stress and deformation
 - Current design: All module ends fixed on support rings, one ring is allowed to slide along the beam direction
 - Initial idea: Allow individual module ends to slide on support: Fixation by springs



The Road Ahead

- DEPFET technology matches Belle-II requirements
 - excellent signal to noise, low material budget for thin detectors, high resolution
- TDR for Belle-II in preparation: Submission in April
- Final DEPFET prototype production currently ongoing: Test devices in fall
 - Fully thinned modules: 50 μm thick silicon
 - Large size matrices, also ILC-type pixel geometry (small pixels)
 - ▶ Final production starting early 2011
- Foreseen start of Belle-II data taking in 2014

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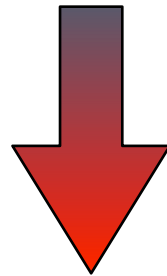
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- Foreseen start of Belle-II data taking in 2014
- Design for Belle-II PXD being finalized
 - Mechanical support with integrated cooling structure
 - Performance and background studies under way
 - DAQ System being developed

What does this mean for DEPFET @ ILC?

- DEPFET pixel sensors now part of a construction project
- ⇒ Accelerated development of the technology
- ⇒ Design and construction of a complete detector system
 - complete readout chain: front-end ASICs, data transmission, DAQ
 - mechanical support and detector integration

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The DEPFET technology is not just generic R&D anymore

Technology now ready for use in collider experiments,
complete system ready to go in the very near future!

Backup

The DEPFET Collaboration

