Advances in 3D Silicon Technology

Status Report

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Fermilab

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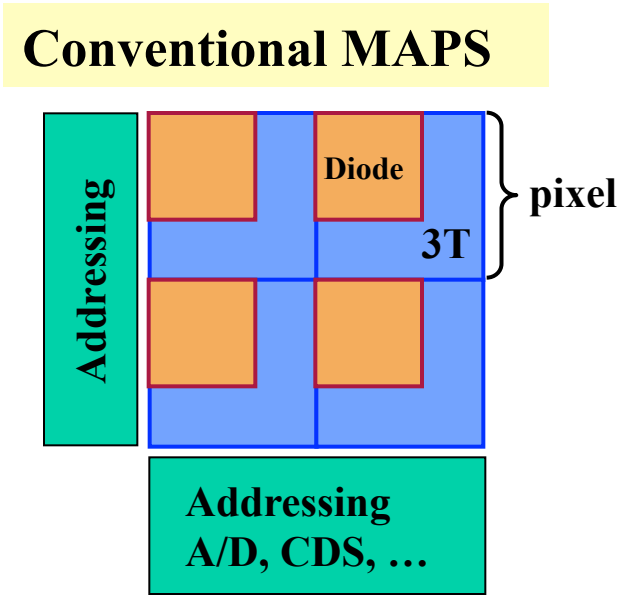
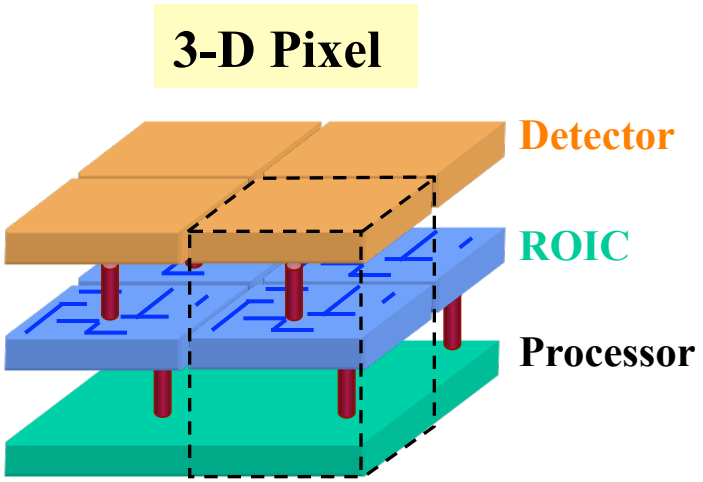
Vertical Integrated Circuits – 3D

- "Conventional MAPS"
  - Pixel electronics and detectors share area
  - Fill factor loss
  - Co-optimized fabrication
  - Control and support electronics placed outside of imaging area

- 3D Vertical Integrated System
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
  - Fabrication optimized by layer function
  - Local data processing
  - Increased circuit density due to multiple tiers of electronics
  - 4-side abuttable

- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

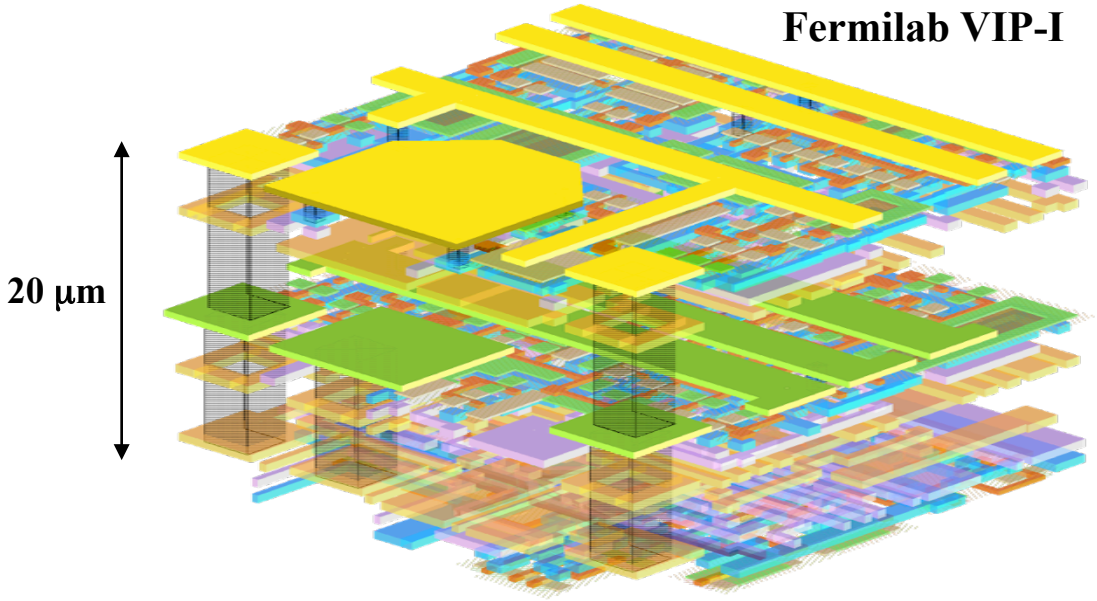




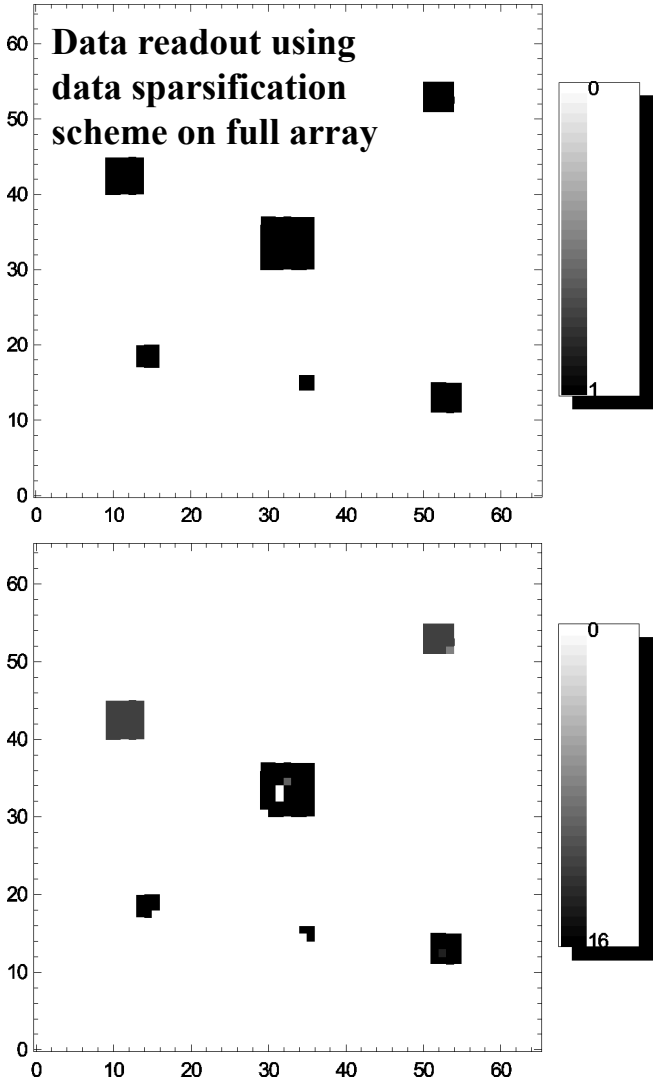
VIP Chip

- Fermilab started to actively pursue the 3D technology, initially with MIT Lincoln Laboratories (MIT-LL), who had developed the technology that enables 3D integration
- MIT-LL offers DARPA funded 3-tier multi-project run, 180nm SOI process

- Designed Vertical Integrated Pixel (VIP) chip for ILC pixel detector
  - Pixel array 64x64, 20x20 μm^2 pixels; design for 1000 x 1000 array
  - Provides analog and binary readout information
  - 5-bit Time stamping of pixel hit
  - Token passing readout scheme
  - Sparse readout
- Chip divided into 3 tiers
  - ~ 7 μm / tier
  - 175 transistors / pixel
- No integrated sensor



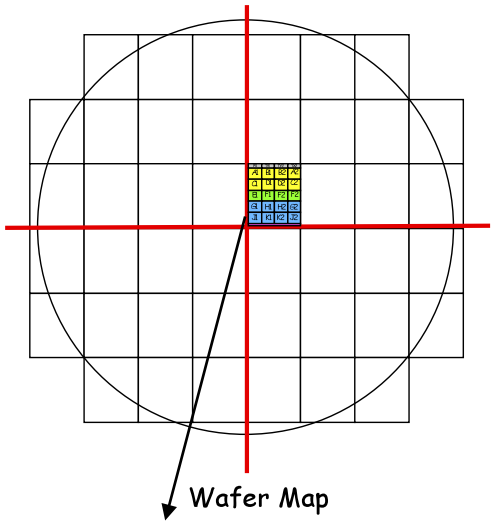
VIP-1 and VIP-2a

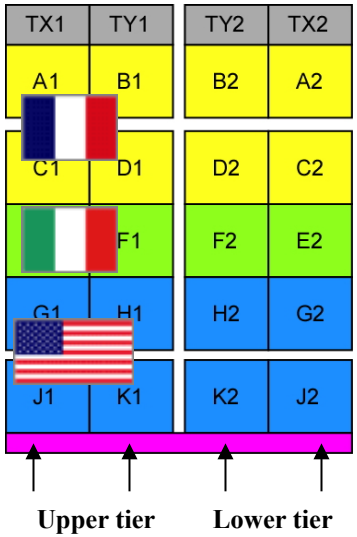


- VIP-1 chip submitted Oct. 2006; ~20 devices delivered late 2007; chip works !
- Major breakthrough in the development of advanced ASICs and integrated detector systems
- An improved version of VIP-1 has been submitted to MIT-LL on October 13, 2008 (150nm, SOI, 3 tiers): VIP-2a
  - Different power and grounding layout;
  - Redundant vias and larger traces in critical paths
  - Added diagnostics
  - Slightly larger pixels
- 3D technology driven by industry; started an initiative with one of the leaders in 3D technology, Tezzaron (Naperville), willing to accept MPW runs

Preselected Injection (top) and Readout (bottom) pattern of pixels reported as hit using data sparsification

Fermilab 3D Multi-Project Run





Reticle Layout

- **Fermilab formed a 3D consortium and hosted a 3D multi project run with Tezzaron**
  - **Two layers of electronics fabricated in the Chartered 130 nm process, useful reticule size is 16x24 mm**
  - **Wafers will be bonded face to face**
  - **Submission closed September 2009**

- **17 Participating institutions in the MPW run**

Fermilab, Batavia	CPPM, Marseilles	AGH University, Krakow
University at Bergamo	IPHC, Strasbourg	Brookhaven
University at Pavia	IRFU Saclay	LBNL
University at Perugia	LAL, Orsay	
INFN Bologna	LPNHE, Paris	
INFN at Pisa	CMP, Grenoble	
INFN at Rome	University of Bonn	

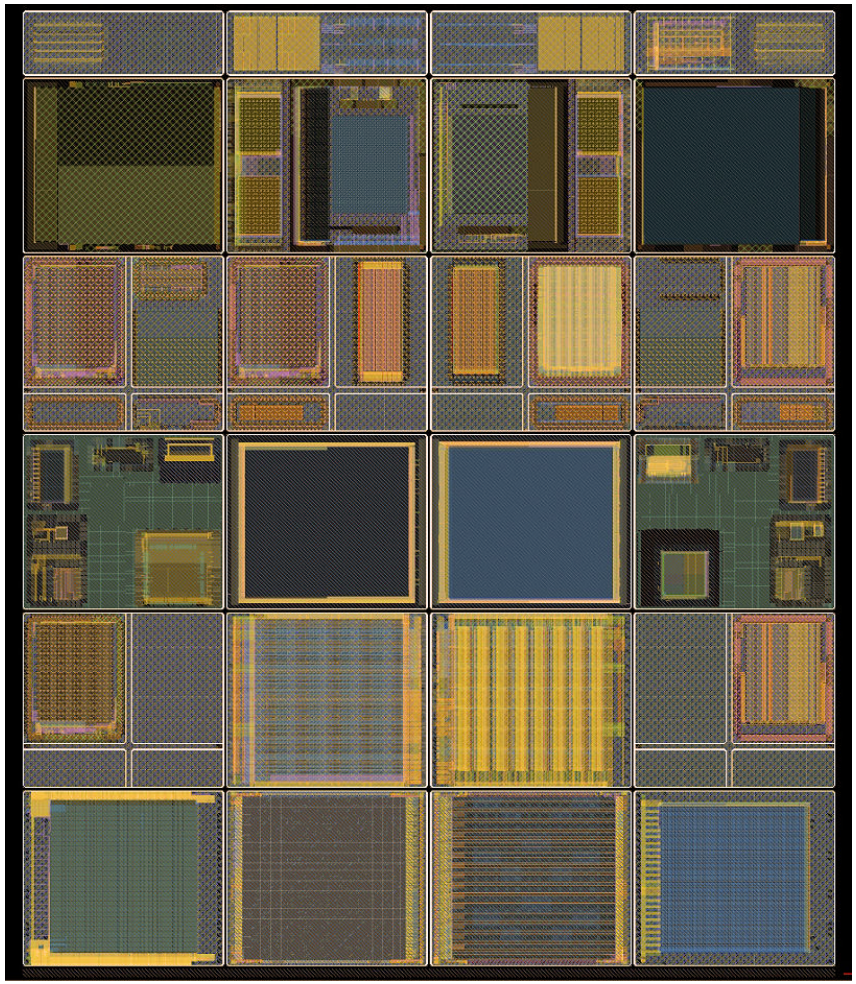
- **Frame divided into 12 sub-reticules for consortium members**

- **More than 25 two-tier designs (circuits and test devices)**

MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

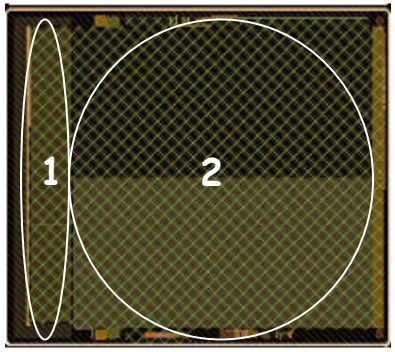
Subreticules:
A, B, C, D,
E, F, G, H, I, J
5.5 x 6.3 mm



Notice
Symmetry
about vertical
center line

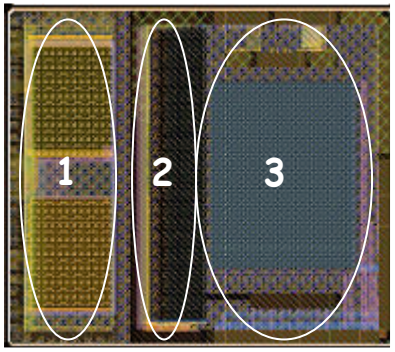
← Top tiers → ← Bottom Tiers →

Sub-reticules A & B

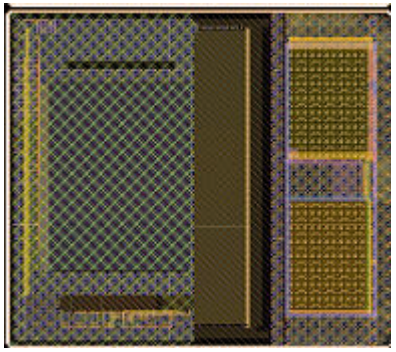


A Left

A Right



B Left

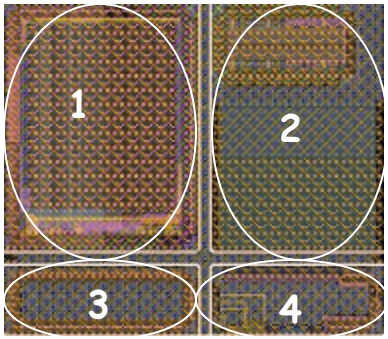


B Right

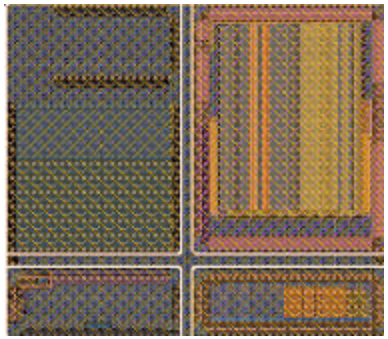
- **Sub-reticule A: Two sub-circuits intended to be bonded to sensors from XFAB (0.35 um with high res. Epi)**
  1. **ILC (Strasbourg, Saclay)**
     - Rolling shutter, low power tracker, 34x240 array, 20x20 um^2 pitch pixels
  2. **ILC (Strasbourg, Bergamo, Pavia)**
     - Self triggering pixel tracker, 245 x 245 array, 20x20 um^2 pitch with fast X-Y projection readout

- **Sub-reticule B – Three sub-circuits**
  1. **Two separate memory cores (CMP)**
  2. **MAPS for ILC (Strasbourg, Saclay)**
     - 42x240 array, 20x20 um^2 pixel MAPS operating in rolling shutter mode, 80 ns/ row
  3. **MAPS for ILC (Strasbourg)**
     - 128 x192 array, 12x24 um^2 pixel MAPS with 5 bit time stamp, 2nd hit marker, full serial readout
     - Future goal: to use separate sensor tier and to reduce the pixel size to 12x12 um^2

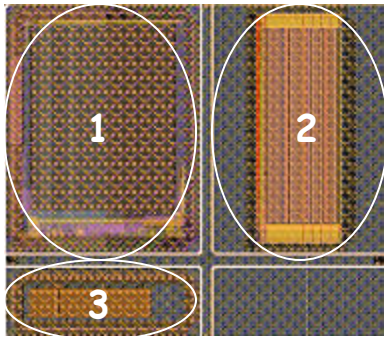
Sub-reticules C & D



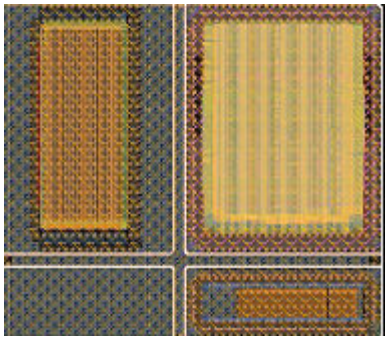
C Left



C Right



D Left

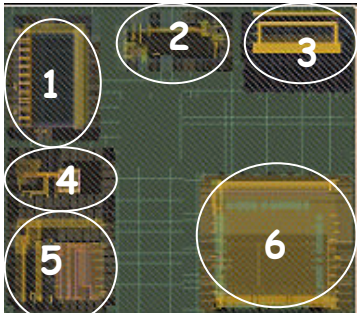


D Right

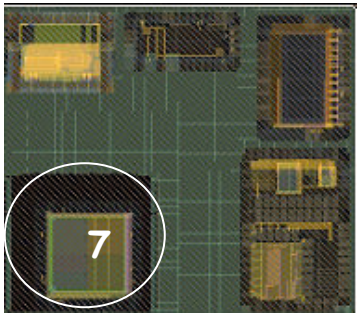
- **Sub-reticule C: 4 sub-circuits**
  1. **ATLAS 2D pixel design based on IBM 0.13 um FEI4 (CPPM/Bonn)**
     - Left (analog) side - 14 col, 60 rows, 50x166 um pixels with simple readout
     - Mating right side comprised of counter and "noisy" cells to study coupling to the left tier with different shielding ideas.
  2. **SEU resistant register and TSV-bond interface daisy chain to measure TSV and bond yield (CPPM)**
  3. **Test structures to evaluate transistor performance with TSVs in close proximity (CPPM)**
  4. **Test structures for robustness of circuits under wire bond pads (CPPM)**

- **SUB-RETICULE D: 3 SUB-RETICULES**
  1. **ATLAS 3D PIXEL DESIGN FOR ATLAS UPGRADE (CPPM/BONN)**
     - Left (analog) side - 14 col, 60 rows, 50x166 um pixels (same as sub-reticule C)
     - Mating right side contains special features such as time stamp, time over threshold, and four pixel grouping
  2. **SMALL PIXEL ARRAY FOR SLHC (LAL)**
     - 24x64 array of 50x50um^2 pixels
     - Threshold adjustment DAC/pixel
  3. **TSV CAPACITANCE TEST CIRCUITS (CPPM)**

Sub-reticule E



E Left



E Right

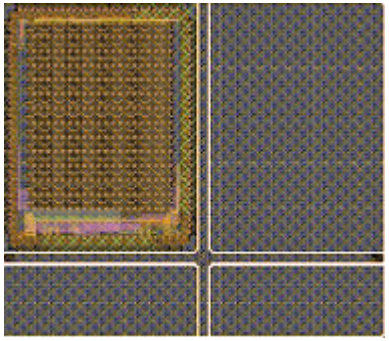
- **Sub-reticule E: 7 sub-circuits**

1. **3D MAPS with 32x64 array of 25x25 um² pixels with DCS, discriminator, auto-zeroing. Control logic in digital tier (Roma)**
2. **3D MAPS test structures - Two 3x3 40x40 um² pitch arrays. One with shaper-less preamplifiers (Pavia/ Bergamo/Pisa)**
3. **3D MAPS test structure with 8x32 array of 40x40 um² pixels, DNW sensors, data push architecture (Pavia/Bergamo/Pisa/Bologna)**
4. **Two test structures for the sub-reticule F DNW MAPS device (Pavia/ Bergamo)**
   - 16x16 array of 20x20 um² pixels with inter-train sparsified readout
   - 8x8 array of 20x20 um² pixels with selectable analog readout of each pixel
5. **Two 3D test structures**
   - 3x3 array of 20x20 um² pixels and 4 single channels for DNW MAPS (Pavia/Bergamo)
   - 5x5 and 16x16 3T pixel matrices with small and large detecting diodes (Perugia)
6. **2D version of 3D MAPS device in sub-reticule F, 64x64 array of 28x28 um² pixels (Pavia/Bergamo)**
7. **2D sub-matrices with 10x10 and 20x20 um² pixels to test signal to noise performance of MAPS in the Chartered process (Roma)**

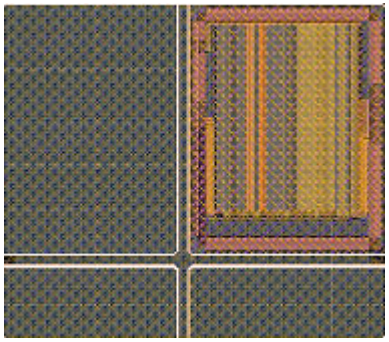
Sub-reticules F & G

F Left

F Right



G Left

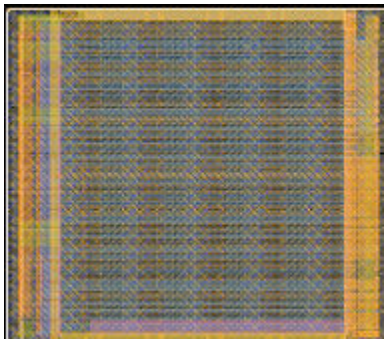


G Right

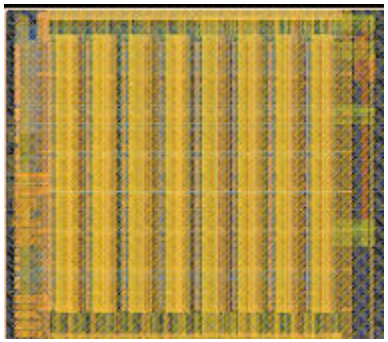
- **Sub-reticule F: 3D MAPS (Pavia, Bergamo)**
  - **3D MAPS device with 256x240 array of 20x20 um^2 pixels with Deep N-Well sensors and sparsification for ILC**

- **Sub-reticule G: ATLAS Pixel FE (Orsay/LBNL)**
  - **ATLAS 2D pixel design based on FEI4 design in IBM 130 nm**
    - Left (analog) side – 14x60 array of 50x166 um^2 pixels with simple readout
    - Analog tier designed for opposite polarity input from circuits in sub-reticules C and D.
    - Mating side comprised of counter to study coupling with the left tier with different shielding ideas.

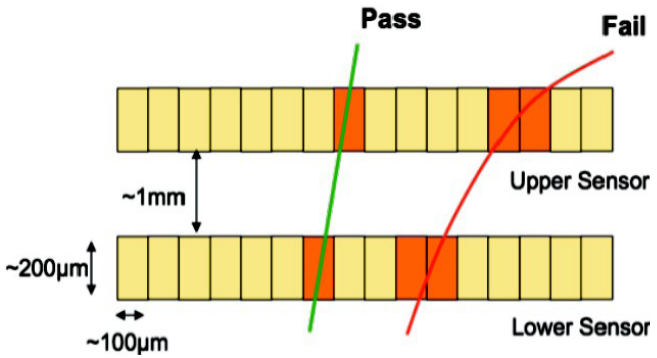
Sub-reticule H



H Left

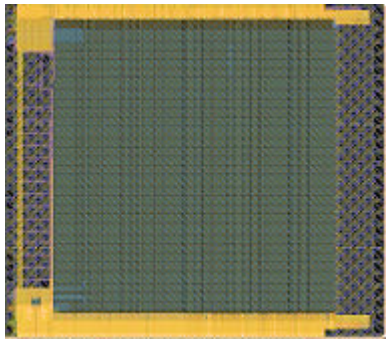


H Right

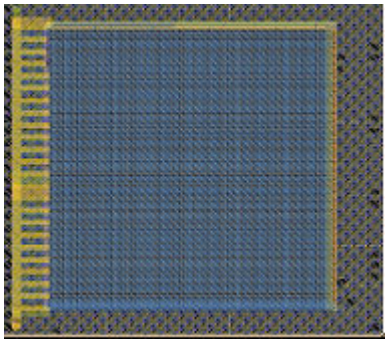


- **Sub-reticule H: VICTR Vertically Integrated CMS TRigger chip (FNAL/CPPM/LBNL)**
  - Processes signals from two closely spaced parallel Si sensors to form a track p_T trigger
  - Top tier: long phi strips Bottom tier: short z strips
  - Top tier looks for hits from long phi strips and bottom tier looks for coincidence between the phi strips and the hits from short z-strips connected to the bottom tier, to form p_T trigger
  - Serial readout of all top and bottom strips along with coincidence information
  - Downloadable hit patterns
  - Fast OR outputs
  - Circuit to be thinned to 24 microns and connections made to both the top and bottom of the chip
  - Designed for 80 micron pitch sensors
  - Sensors developed separately

Sub-reticules I & J



I Left



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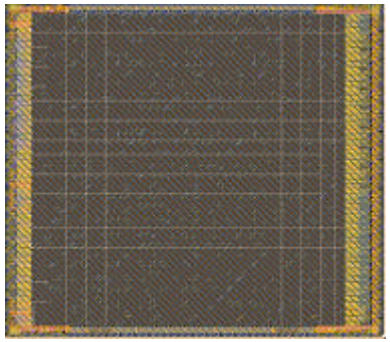
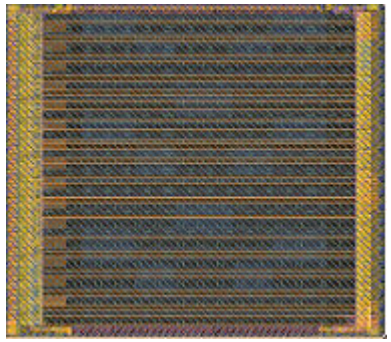


J Left



J Right

- **Sub-reticule I: VIP2b 3D demonstrator chip for ILC vertex detector with separate bonded sensor (FNAL)**
  - **Adapted from earlier MIT LL designs in SOI technology**
    - 192 x 192 array of 24x24 um^2 pixels
    - 8 bit digital time stamp
    - Data sparsification
    - DCS analog signal info output
    - Separate test input for every pixel cell
    - Serial output bus

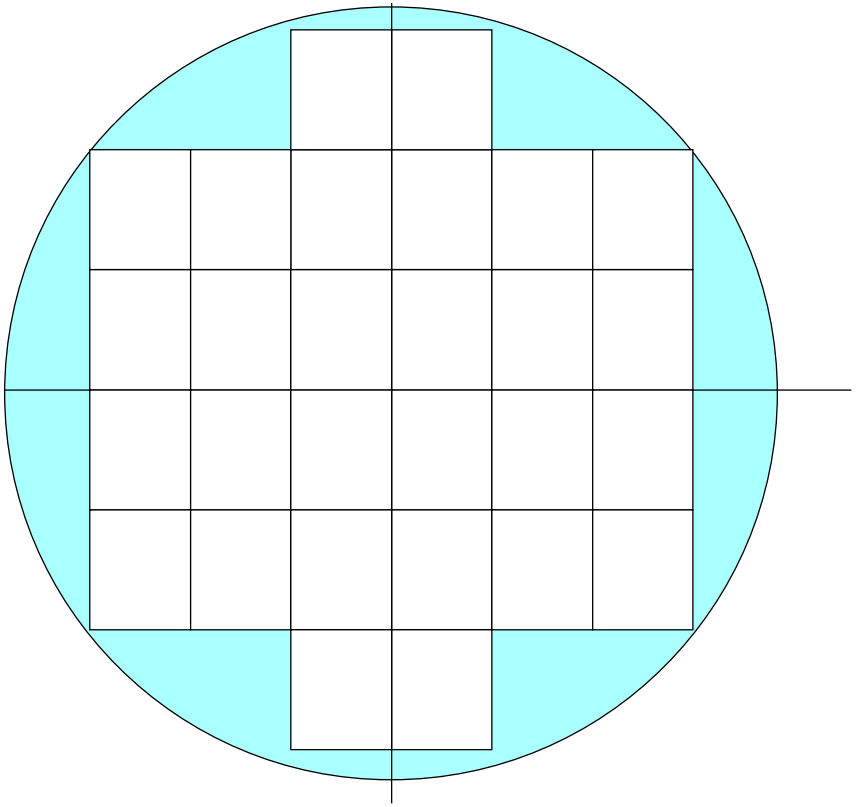
- **Sub-reticule J: VIPIC 3D demonstrator chip for X-ray Photon Correlation Spectroscopy (FNAL/AGH-UST/BNL)**
  - **Characteristics:**
    - 64 x 64 array of 80x80 um^2 pixels
    - Separate analog and digital tiers
    - Sparsified, binary readout
    - High speed frame readout
    - Trigger-less operation
    - 16 Parallel serial output lines
    - Two 5 bit counters/pixel for dead timeless recording of multiple hits per time slice
    - Innovative binary tree pixel addressing scheme

Timeline and Schedule

- **All designs were received by Fermilab in May 2009**
- **June 2009 – March 2010 spent preparing and reviewing the submission(s)**
  - **Note, this was the first time for Fermilab and Tezzaron to organize a MPW run and there were a large number of 'growing pains'**
  - **A large number of problems were discovered**
    - Frame and street definitions
    - Design kit incompatibilities, software bugs
    - TSV issues: protection, spacing, bond interface
- **March 6, 2010: Fabrication started**
- **At the end of April: 2D wafers expected out of foundry**
  - **3 wafers to be diced and parts sent to designers**
- **May – June 2010: 3D wafers expected to be completed**
- **June 2010: 3D characterization to start**
- **July 2010 or so: wafers prepared for bonding to sensors**

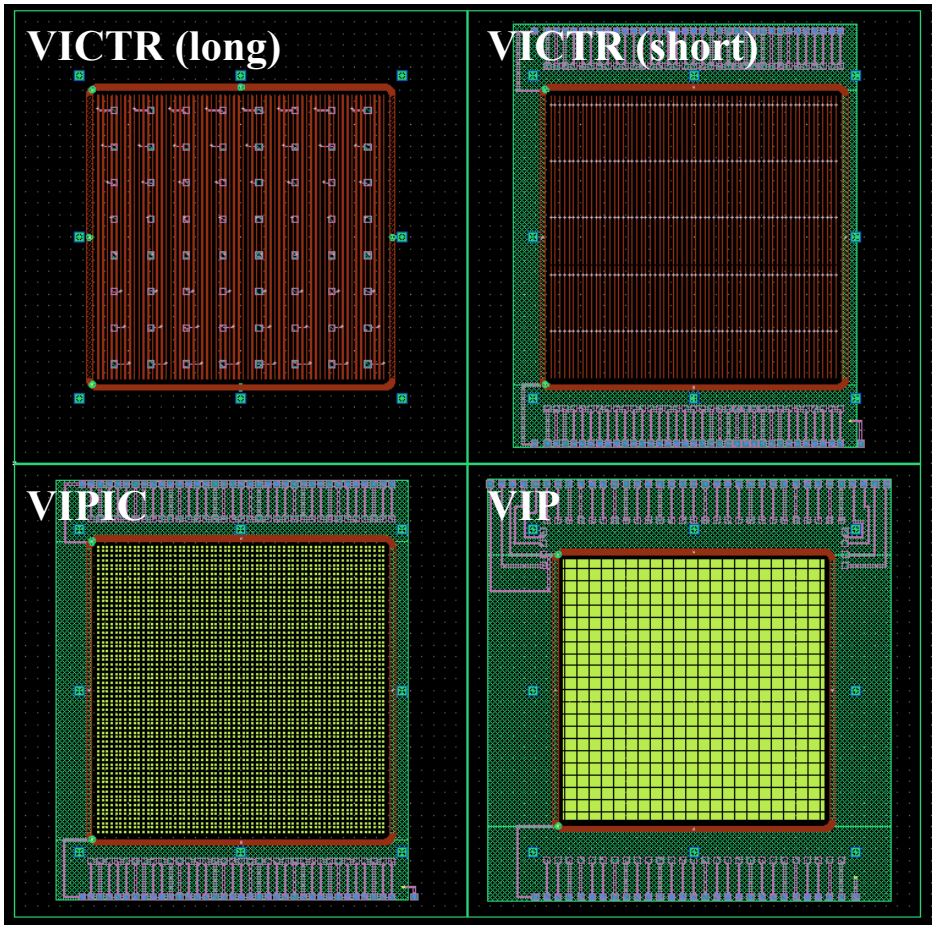
Production and Parts Count

- Procured one lot of 31 wafers, with 28 full reticules per wafer
- Partition of wafers:
  - 3 wafers will be used for 2D wafer testing
- Available for 3D bonding 28 wafers, which yields 14 3D wafers
- There are 14 3D assemblies per wafer
- If one assumes a yield of 50%, seven working 3D wafers available
  - 98 assemblies of each sub-reticule
- A lot of work ahead !



Sensor Design

- **Sensors need to be developed to be mated to the 3D circuits**
  - **Will allow for complete testing of technology**
    - 3D circuits and bonded devices
    - Integrated devices with interposer
    - Test beam characterization
- **Four sensors designed to be fabricated at BNL**
  - **CMS short strips**
  - **CMS long strips (not DBI bonded)**
  - **VIP**
  - **Imaging sensor**
- **Exploring sensor fabrication at XFAB**

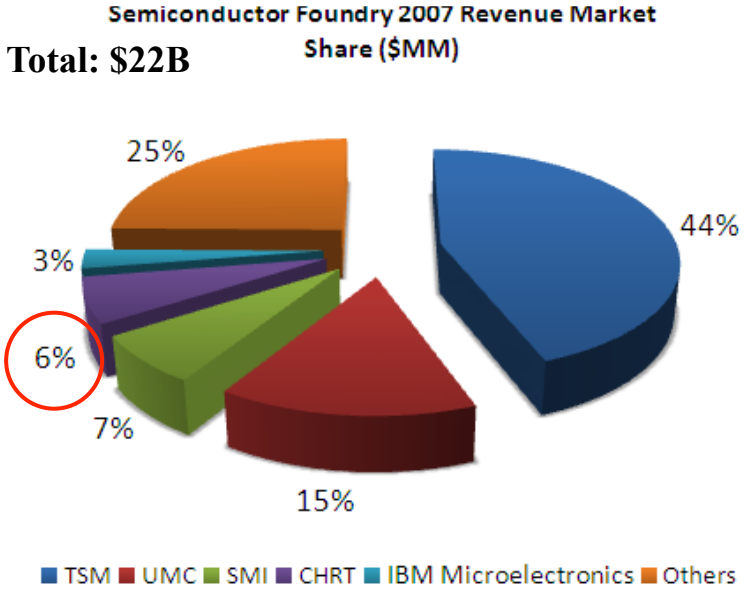


Concluding Remarks

- **Major milestone of first 3D MPW submission achieved with a variety of technologies that could be used for ILC vertex detectors.**
- **Parts are in production at the foundry, and should be available late May.**
- **Sensors designed to be mated with 3D electronics designs**
- **Various bonding techniques explored and verified, such as DBI-bonding**
- **Exciting times and a lot of work ahead!**

Collaboration with Industry

- 3D technology driven by industry; MIT-LL is a research facility. We started an initiative with local vendor, Tezzaron, willing to accept MPW runs
- Tezzaron, located in Illinois (Naperville):
  - One of the leaders in developing 3D technology
  - Wafers are fabricated by Chartered in Singapore
  - 3D assembly is completed by Tezzaron in Singapore



Source: EE-Times, TechInsights, April 2008

- Advantages:
  - Existing rules for vias and bonding
  - Relatively fast turn around
  - One stop shopping for wafer fabrication, via formation, thinning, bonding
  - Process is available to all customers
  - Low cost