# Impact of open source CPU on feature online systems

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#### Outline

- RISC-V story
- Pros and Cons

- Open Source
- RISC-V in China
- RISC-V in High Energy Physics

### RISC-V background

## Intel Failed to acquire SiFive at \$2Billion

#### Intel's Attempt to Acquire SiFive for \$2 Billion Fell Apart, Report Claims

By Anton Shilov 19 days ago

\$2 billion is not enough.











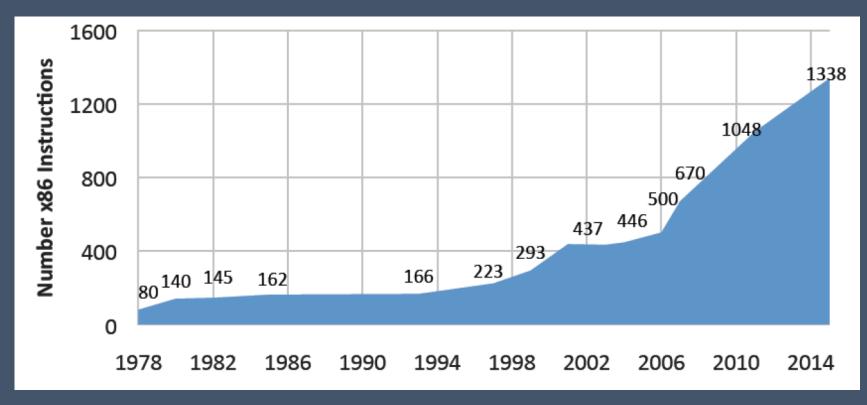
**(1)** ○ ◎ **(2)** ○ **(2)** Comments (11)



2020	Rivet Network	By:Chunjie Wang	
2019	Barefoot Network		
2019	Habana	\$2B	
2017	Mobileye	\$15.3B	
2016	Nervana	\$350M	
2016	Movidius	\$400M	
2015	Altera	\$16.7B	

From: https://www.tomshardware.com/news/intel-failed-to-buysifive

## Why RISC-V?



[Rodgers and Uhlig 2017]

- 1. 4 instructions/day for the past 3 decades
- 2. forward compatibility

## RISC-V Story

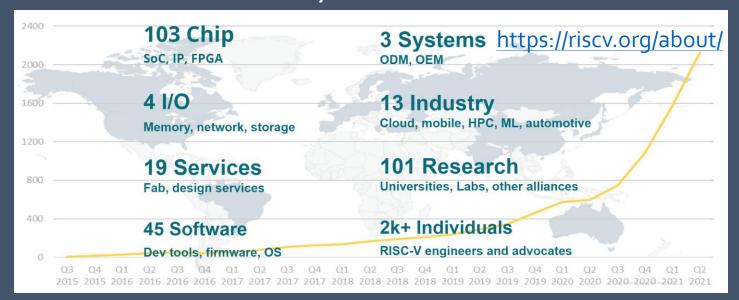
- Kick off in 2010 at UC Berkeley as "3-month project" guided by David Pattern (Turning Award in 2017)
  - Target a pure and simple ISA
  - Commercial ISAs were too complicated, and had legal issues burden
- What is RISC-V (Fifth generation of RISC-based research project)
  - A high-quality, license-free and open RISC ISA
  - Available freely under a permissive license
  - Just open ISA, not open CPU implementation



#### RISC-V Foundation

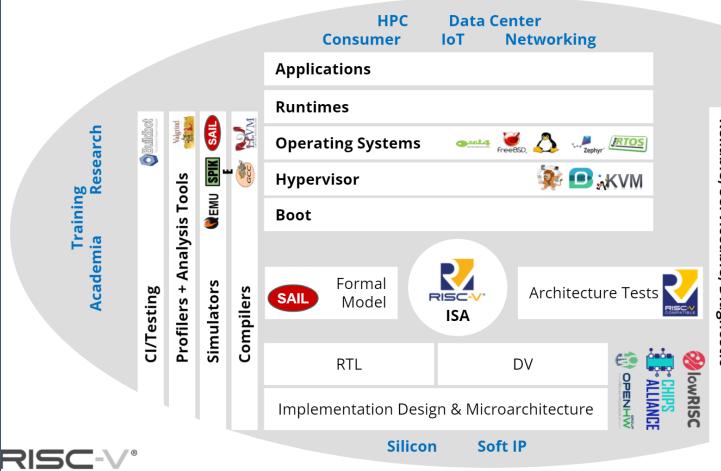


- A non-profit organization formed in August 2015 to publicly govern the ISA
  - Direct future development of ISA
  - Promotion of ISA
- > 2K members in more than 70 countries



## RISC-V Eco-system

RISC-V is everywhere



Security

GLOBALPLATFORM

Performance

Reliable, Serviceable, Diagnostic

RISC-V -> Linux ?

https://riscv.org/about/

## RISC-V Eco-system(2019)



https://www.zdnet.com/article/risc-v-opens-up-processor-design/

#### RISC-V: ISA

31 30 25	24 21 20	19 1	5 14 12	2 11 8 7	6 0	
funct7	rs2	rs1	funct3	rd	opcode	R-type
imm[1	1:0]	rs1	funct3	rd	opcode	I-type
imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode	S-type
						1
$[imm[12] \mid imm[10:5]$	rs2	rs1	funct3	imm[4:1]   imm[11]	opcode	B-type
				1		1
	imm[31:12]			rd	opcode	U-type
		_		<u>-</u>		1 _
[imm[20]] $[imm[1]$	$0:1]$ $ \operatorname{imm}[11]$	imm[	19:12]	rd	opcode	J-type

Base Instruction Formats (RISC-V User-Level ISA V2.2)

#### RISC-V Modular Instruction Sets

Basic Instruction	No. of Instruction sets	Description
RV <sub>3</sub> 2I	47	Base integer instruction set; 32-bit address space; 32 General-purpose registers
RV <sub>32</sub> E	47	Part of RV32, only 16 general-purpose registers
RV64I	59	64-bit address space; 64-bit general-purpose registers
RV128I	71	128-bit address space

M: Integer Multiplication

A: Atomic Instructions

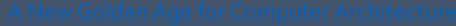
F: single-precision floating-point

D: Double-precision floating-point

Refer to: The RISC-V Instruction Set Manual V2.2.

## Free & open

	Free & open design	Licensable Design	Closed design
Free & Open Spec	Rocket Chip, CVA6, BOOM, PicoRV32	SiFive, Andes, Bluespec, Codasip	RISC-V in Nvidia
Licensable Spec(ARM)		Cortex-A <sub>7</sub> 6	Apple processor
Closed Spec (X86)			Intel & AMD







#### Pros and Cons

#### RISC-V: Pros and Cons

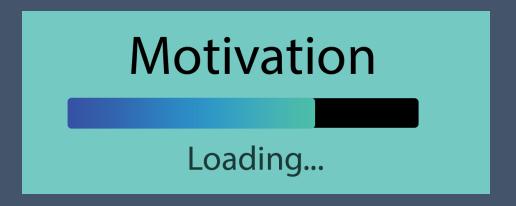
- Meanings of Open ISA
  - Everyone can design a CPU. No need to pay for IP if you implement it
  - Benefit from the RISC-V ecosystem, such as open compilers, develop tools & software dev environment (IDE)
  - Domain-specific application
- Challenges
  - RISC-V ISA fragments: different RISC-V ISAs
  - Motivation to develop software stack

### RISC-V: Pros and Cons

Barriers	https://riscv.org/about/ Legacy ISA	RISC-V ISA
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	\$\$\$ – Limited	Free – Unlimited
License and Royalty fees	\$\$\$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions, open & proprietary cores
Software ecosystem	Extensive	Growing rapidly

## RISC-V: Software Stack (Open Source)

- Compilers
  - GCC/llvm
- Library
  - Newlib: use with proxy kernel
  - Glibc: use with riscv-linux
- RISC-V simulation
  - Spike/QEMU
- Debug
  - GDB



https://github.com/riscvarchive/riscv-software-list

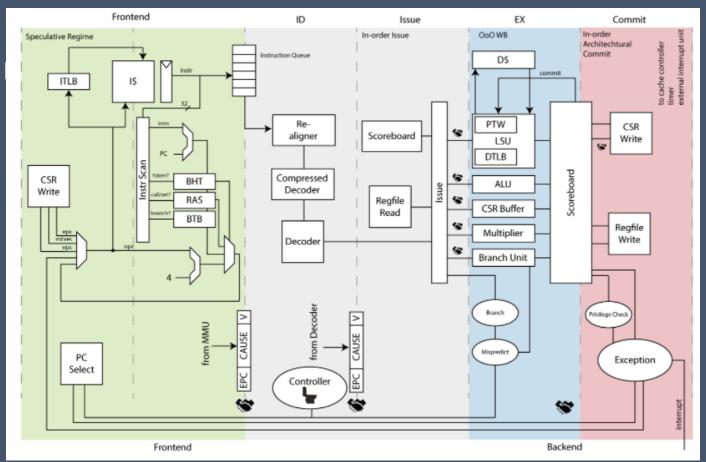
#### Open Source

## RISC-V Open Source

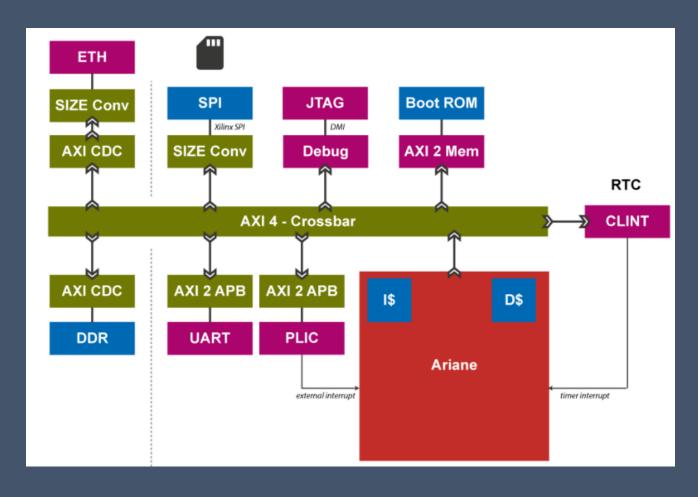
Project	Github	Star	Arch	Language	Linux- supported
CVA6	https://github.com/openhw group/cva6	1.3K	RV64	System-Verilog	Yes
Rocket Chip	https://github.com/chipsalli ance/rocket-chip	2K	RV64	Chisel	Yes
LowRISC	https://github.com/lowRISC	514	RV <sub>3</sub> 2	Verilog	Yes
Hummingbird E200	https://github.com/SI- RISCV/e200_opensource	1.9K	RV <sub>3</sub> 2	Verilog	No
Picorv32	https://github.com/clifford wolf/picorv32	1.8K	RV <sub>3</sub> 2	Verilog	No
	Impact of open	cource CDL	on teature online systems		18

#### RISC-V: CVA-6

- Github: https://github.com/openhwg oup/cva6
- Genesys 2 (kintex-7 FPGA)
- Boot Linux

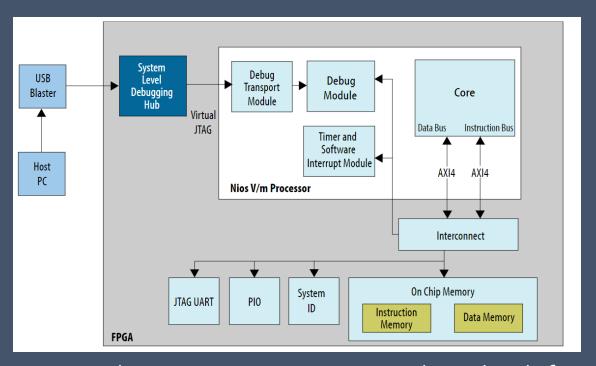


## RISC-V: CVA-6 (Ariane)



#### RISC-V: Intel FPGA IP

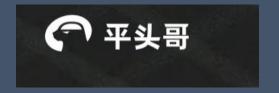
- Intel FPGA(Quartus Prime Pro 21.3)
- Nios V processor
  - RV32IA: atomic extension
  - 5-stage pipeline
  - AXI interface
  - uC/OS-II support



https://www.intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html

#### • RISC-V in China

#### RISC-V in China























## Design your RISC-V chip

- Buy RISC-V IP and build a SoC (system on chip) by yourself
  - Verification is quite heavy
  - Interconnect all kinds of IP, such as DDR controller, Ethernet PHY
- Custom chip from the providers

### RISC-V in High Energy Physics

## RISC-V in High Energy Physics

 Used as CPU implemented in FPGA. Use C code in RISC-V instead of Verilog

Implement the Open-source RISC-V in ASIC to work as the CPU.
 Open and Cheap compared to the legacy CPU

Custom the RISC-V ISA to speed up specific algorithms

## Voice From High Energy Physics

#### Important Technical Developments

"Off & On" Detector synergistic planning will result in orders of magnitude performance improvement: Lower Power/data transfer rates

On-Detector Processing for Low-Power, High-Performance Sensor Readout

Significant gains in data reduction are possible utilizing reconfigurable logic as witnessed by the high growth of FPGA processing.

- ► Implementing open source RISC-V processors in next Generation ASICs
  - Allows reconfigurable processing using C code instead of Verilog code. More familiar to the physics community.
  - Likely result is more abstracted information from the front end
  - Large savings per channel in power and off detector bandwidth.
- PRD Develop & share a RISC-V instruction set to enable to reach down into the detector. This can Leading to a huge reduction of power and bandwidth per channel.

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BRN ASICs & Readout 2019 presentatic

https://indico.cern.ch/event/870453/contributions/3671193/attachments/1960641/3258991/BRN\_DC\_ASICsre adout-2.pdf



## Thank you

#### RISC-V outside China







Western Digital.

#### Industrial Market

- Low performance
  - IoT
- Middle performance
  - Storage
- High performance
  - Computation

