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PFA electromagnetic calorimetry prototypes: R&D Status and Highlights

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https://indico.ihep.ac.cn/event/14938/

Introduction: Particle Flow Detectors

- Particle flow paradigm: for precision measurement of jets
 - Measurements of individual particles
 - Maximal exploitation of precise tracking
- General concepts
 - Choose sub-detector best suited for each particle type
 - Separate showers of close-by particles in the calorimeters
 - Need to minimize the confusion term
- High-granularity (imaging) calorimeters: PFA-oriented
 - Emphasis on tracking capabilities of calorimeters
 - Hardware: readout channels on the order of 1~10 million
 - Compact: all calorimeters inside magnet coil
 - Hermetic: minimum gaps

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• Limited space for instrumentation





PFA-ECAL options at future lepton colliders

- Tungsten as absorber material
 - Narrow shower profiles
 - Compact design
 - Good separation of EM and hadronic showers
 - $X_0 = 3.5$ mm, $R_M = 9.3$ mm, $\lambda_I = 99.5$ mm
- Active materials for detection
 - Silicon sensors
 - Compact layout, capable of pixelization, intrinsic stability
 - Scintillator + SiPMs
 - Mature technology, cost effective
- Both two options are being investigated in CALICE
 - Developments of technological prototypes







PFA-ECAL: Silicon-Tungsten option





Silicon sensor (pixelized)







- Sensitive layers: stringent requirement on space
 - Silicon sensors: 0.32~1.0 mm thick
 - PCB + ASICs: 1.8 mm thick (challenging)
 - COB 1.2mm thick demonstrated: ASICs wire-bonded
- Technology application in the CMS-HGCAL project
 - Major focus on radiation hardness and active cooling
 - (-35 degrees with dual-phase CO2)
 - Challenges due to complicated geometry in endcap regions
 - Invited talk by David Barney in the same session: stay tuned





Overview: SiW ECAL prototype developments

Physics prototype

Proof of principle 2003 - 2011



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No. channels: 9720 Pixel size: 1x1 cm2 Effective $R_M = 1.5$ cm Weight: 200 kg

Technological prototype

Addressing engineering challenges: since 2010



No. channels: 45k Pixel size: 0.55x0.55 cm2 Effective $R_M = 1.5$ cm Weight: ~ 700 kg







Sensors: silicon wafers with PIN diodes

ILD design: **low cost**, ~2000 m2 Minimized number of manufacturing steps Target: 2.5 EUR/cm2 Now : 10 EUR/cm2 (in Japan)



IV and CV characterizations

- Breakdown voltage >500V
- Current leakage <4 nA/pixel (DC coupled with chip)
- Full depletion at <100 V
 - ~40 V with 320 um, ~70 V with 500um



256 PIN diodes, 0.25 cm2/diode, 9 x 9 cm2 total area







- Wafers are glued to PCB (robot at LPNHE & Kyushu U.)
 - Segmented guard-rings layout as an option
- Silicon sensor bias via a copper/Kapton sheet





Front-end electronics for silicon sensors

• SKIROC ASIC: full integrated electronics

- 64 channels, SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm
- Variable-gain charge amplifier
- 12-bit Wilkinson ADC (also for TDC ramp)
- Digital logic: acquisition, conversion, SCAs and I/O
- Large dynamic range
 - High and low gain modes: 0.1~ 2500 MIPS
- Auto-trigger at typically ~0.5 MIP

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- Low power: 25µW/ch featuring with power pulsing
- SKIROC ASIC: core ingredient in SiW ECAL prototypes
 - ECAL layout: evolution with PCB and chip packaging
- Note: SKIROC is not designed for circular colliders
 - The successor chip "HGCROC" developed for HL-LHC CMS-HGCAL project can be a better reference for continuous operation mode







S Callier et al 2011 JINST 6 C12040



SiW-ECAL: towards system integration

> Very dense PCBs aka FEV with 1024 readout channels (with digital, analogue, clock signals) in a 18x18 cm board

FEV10-12



ASICs in BGA Package

- Incremental modifications
- From v10 -> v12
- Main "Working horses" since 2014

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FEV_COB



- ASICs wirebonded in cavities
- COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

FEV13



- Also based oin BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Taken from A. Irles' talk at LCSW2021: "Status of the technological prototype of the CALICE SiW-ECAL"



SiW-ECAL: long slab prototypes

- Daisy chain of 8 ASUs (extendable to 12)
 - Corresponding to typical barrel ECAL length
 - Based on FEV12 ASU (& SMBv4)
 - No ILC geometrical constraint (thickness)
 - Baby-wafer 4x4 pixels on each ASU
- Goals
 - To validate the electrical behavior of a long slab: clocks, data integrity, noise level on length







SiW-ECAL: address challenges from space constraints







- Module assembly chain established
- Ultra thin PCB: Chip On Board (COB)

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- ILD constraints: total space for ASICs and PCB 1.8mm
 - Very thin board: 1.2mm 9-layer PCB, good planarity (issue for gluing)
- PCBs with naked ASICs placed in carved cavities and wire-bonded
- Investigating alternative options of encapsulating

Zoom into ASIC cavities







After application of epoxy



SiW ECA: ready for the 2021 test beam campaign



Beam test 4 layers in 2019



Intermediate slots for Tungsten plates

15 layers in 2020: 15000 cells in readout





First cosmic (Adrian Irles)



Over 15 layers ready for beam test (FEV10, 11, 12, 13 and COB)

- Rapid development of compact readout electronics
- For the first time all components at hand that could be installed in a lepton-collider detector
- Beam test at DESY is ongoing: Nov. 1-15, 2021

"Live" from the DESY Beam Test

Fresh results (Nov. 8) from Roman Pöschl (IJCLab)

Detector Setup



Detector in beam position



Hit maps of all 15 layers



• DESY Beam Test 1/11/21 - 15/11/21

- Successful operation of the prototype composed of 15 layers (15360 cells)
- Smooth data taking as we speak
- Exciting and important results can be expected



SiW-ECAL: ultra compact DAQ

- Core Mother-Daughter system
 - Able to control and read up to 30 SLboards
- SL-Board
 - The sole interface for the ~10k channels of a slab
- The new DAQ fits tight space requirements







Detector Interface

For signal buffering and power regulation



Before 2019

Since 2019



SiW-ECAL: new developments in front-end electronics

- Design new front-end board (FEV2.0)
 - Updates for LV power distribution, buffer for slow control
 - Change HV distribution for wafer: add HV filter per wafer, FEV drive HV instead of Kapton
 - New HV Kapton: 1 per FEV instead of 1 per slab
- New packager for SKIROC2A (NCAP in China)
 - 390 chips packaged, first results look good; will fully evaluate performance with test stand



FEV2.0: 180x180mm

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SiW-ECAL: new developments in front-end electronics

- New design of HV Kapton
 - New design: 1 Kapton per front end board -> easier to insert/replace in long slab
 - Better wafer protection (handling) HV propagate through FEV connector + filter to wafers
 - Old design: 1 Kapton for 10 boards (difficult and expensive solution)
 - Glue 40 wafers on single Kapton, incompatible with FEV interconnection connector



- "Fake" front-end board and long slab: leak current
 - Mockup to study HV distribution and mechanical assembly







PFA-ECAL: Scintillator-Tungsten option





- Sensitive layers: challenges from space
 - Scintillator strips: 2mm thick
 - PCB + ASICs: considerably thicker than 1.2 mm in design specs (quite challenging)

CEPC ScW ECAL prototype constructed

- Over 6700 channels, 32 layers, air cooling
- Commissioning with cosmic and beam particles
- Close collaboration between Chinese and Japanese groups within CALICE



Overview: ScW ECAL prototype developments

Physics prototype

Sc-WECAL 26~30 layers, 1x4.5 cm² cells



interview in the second se





- Technological prototype
 - 32 layers with ~6700 channels (SPIROC2 chips)

Technological prototype

- Scintillator strip directly coupled with SiPM
- Tested at USTC and IHEP (BEPC-II E3 beam line) with cosmic muons and hadrons
- Not able to perform DESY beam tests due to Covid



- 30 layers with 2160 channels
- Scintillator strip + WLS fiber + SiPM
- Tested at DESY and FNAL with electrons during 2007 and 2009





ScW ECAL prototype construction: reminder

- Scintillator strip: directly coupled with SMD-SiPM
 - Response uniformity scan along strip length direction
- Multiple ECAL readout boards: commissioning tests with DAQ







5.5mm 3.82mm SiPM SiPM SiPM SipM Sipm Scintillator

SPIROC2E chip on EBU



FELIX-based DAQ board



Multi-layer boards: ageing tests in a cabinet





ScW ECAL prototype construction: reminder

- Scintillator strips: individually wrapped, QA/QC (visual and dimension check)
- Prototype with 16 "super-layers"
 - Each "super-layer": 2 sensitive layers and 2 CuW plates fixed onto one frame





Size measurement



assembling















ScW ECAL prototype: first beam test at IHEP

- BEPC-II E3 beam line at IHEP campus
 - Secondary particle beam
- Mixed particles with protons and pions
 - Protons dominated

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- Momentum : 300MeV-1.2GeV
- Low event rate: less than 100 per minute
- Rehearsal for future beam tests at DESY/CERN
 - Successful assembly and data taking (12k events)





1GeV proton candidate







1400

1200 1000 800

- Long-term tests with cosmic muons
 - Pedestals, SiPM noises



Pedestals of one channel: 10um vs 15um SiPMs h1 Chip-1 Channel-1 Entries 12273 h1_Chip-1_Channel-1 410.7 Entries 11139 3.53 Std Dev 411.5 Mean Std Dev 5.046 SiPM with 15um SiPM with 10um pixel pitch pixel pitch 380 400 Pedestal width of all channels

Sigma of pedestal [ADC]

35

30

25 20 15 Number of channel

10

5

0 0



20

180

160

140

120

100

Number of chip

80

60

40

- Long-term tests with cosmic muons
 - Pedestals, SiPM noises
 - Calibration with all SiPMs
 - SiPM gain: single photon spectrum
 - MIP response

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- Tracking performance extracted with cosmics
 - Better than 2mm positioning resolution achieved



Tracking precision in each layer

ADC



Response uniformity with muons





- Long-term tests with cosmic muons
 - MIP response and temperature impacts
- Scintillator strip: two different designs
 - Chinese group: 45mm strip (equipped 30 ECAL layers)
 - Japanese group: 90mm long strip (equipped 2 layers)
 - Coupled with two SiPMs (15um pixel pitch)





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Higher S/N ratio achieved; can use lower trigger threshold



- Long-term tests with cosmic muons
 - Calibration with all ASICs (SPIROC2E)
 - High gain vs low gain: inter-calibration
 - With LED, charge injection and cosmics
 - MIP response and temperature impacts

Long-term temperature monitoring



ASIC HG/LG inter-calibration





Data with cosmic rays show similar HG/LG curve: ongoing studies

Detection efficiency



Detection efficiency is generally stable; but also observed that it gradually dropped for 10-um SiPMs



ScW ECAL prototype: time measurements

- Data of cosmic muons: timing performance
 - Based on the time calibration with pulse generator: TDC tics -> ns
 - to calibrate the "TDC offset" per chip and per channel
 - TDC differences of channels measured by the two chips





muon

Hit time

Hit time

EBU1

chip1

EBU2

ScW ECAL prototype: shower studies using cosmic-rays

- Development of shower finding algorithm
- Further exploit the cosmic data, comparison with simulation



Naoki Tsuji's talk at CALICE Meeting Sep. 2021



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Summary:

- Steady progress made on PFA ECAL prototypes within CALICE
- SiW ECAL option
 - Address challenges from technical requirements
 - Ultra Compact DAQ
 - In parallel to the workshop, testing a SiW ECAL prototype with 15k-channels (combined tests with other CALICE calorimeters foreseen for 2022)
 - Intense R&D activities ongoing

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- Ultra thin PCB, optimization of powering/HV in a long slab
- Long slab: from an electronics prototype to a technological prototype
- ScW ECAL option
 - Successfully constructed a technological prototype with 32 layers (6700 channels)
 - Commissioning with long-term cosmic ray tests: demonstrate good performance
 - A first beam test was successfully done at BEPC-II E3-line in IHEP campus
 - Ready for beam tests at DESY/CERN in 2022/23 (with other CALICE prototypes)







Thank you!

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Ongoing studies: scintillator-SiPM response

- Scintillator-SiPM stability: long-term monitoring
- Groups in China and Japan both observed drops of scintillator-SiPM response
 - Shinshu University: setup with a Sr-90 source
 - USTC: setup with LED and scintillator test bench



