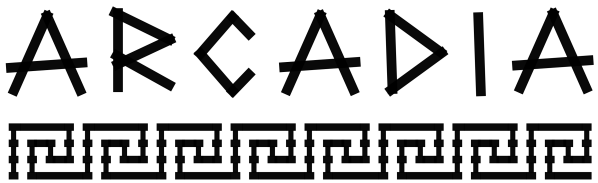
ARCADIA

A novel platform for the implementation of innovative CMOS monolithic sensors

International Workshop on the CEPC
November 8th - 12th, 2021

Istituto Nazionale di Fisica Nucleare



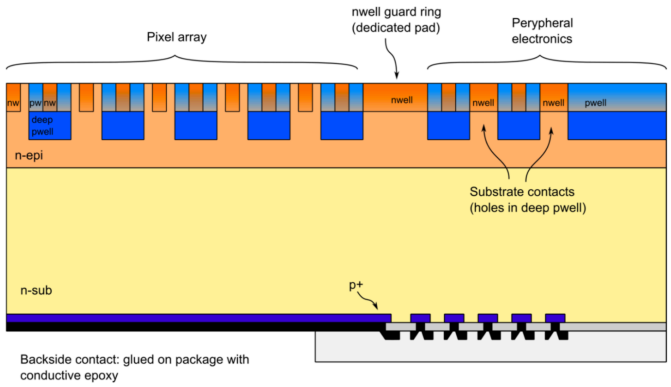
Manuel Rolo (INFN),
on behalf of the ARCADIA Collaboration

ARCADIA (INFN CSNV Call Project)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Creation of a novel platform for the implementation of innovative monolithic sensors compatible with standard CMOS fabrication processes

- Challenge: deployment of large-area system-grade CMOS sensors implementing scalable readout architectures with ultra-low power capability (O(10 mW/cm2))
- Technology: LFoundry 110nm CMOS node, quad-well, high-resistivity bulk
- Active sensor thickness in the range 50 µm to 500 µm
- Operation in full depletion with fast charge collection only by drift
- Small charge collecting electrode for optimal signal-to-noise ratio

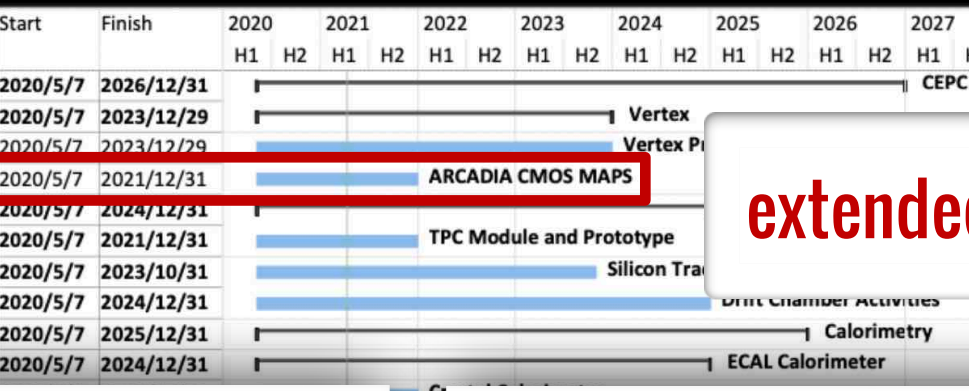


ARCADIA CMOS DMAPS at CEPC

https://indico.ihep.ac.cn/event/15229/session/6/contribution/3/material/slides/3.pdf

Projects overview: R&D schedule

PBS	Task Name	Start	Finish
	CEPC Detector R&D Project	2020/5/7	2026/12/31
1	Vertex	2020/5/7	2023/12/29
1.1	Vertex Prototype	2020/5/7	2023/12/29
1.2	ARCADIA CMOS MAPS	2020/5/7	2021/12/31
2	Tracker	2020/5/7	2024/12/31
2.1	TPC Module and Prototype	2020/5/7	2021/12/31
2.2	Silicon Tracker Prototype	2020/5/7	2023/10/31
2.3	Drift Chamber Activities	2020/5/7	2024/12/31
3	Calorimetry	2020/5/7	2025/12/31
3.1	ECAL Calorimeter	2020/5/7	2024/12/31



extended 12/2022

CEPC detector R&D Project for preliminary evaluation by the CEPC International Detector R&D Committee

https://indico.ihep.ac.cn/event/15229/session/6/contribution/3/material/slides/4.pdf

1.2 ARCADIA CMOS MAPS

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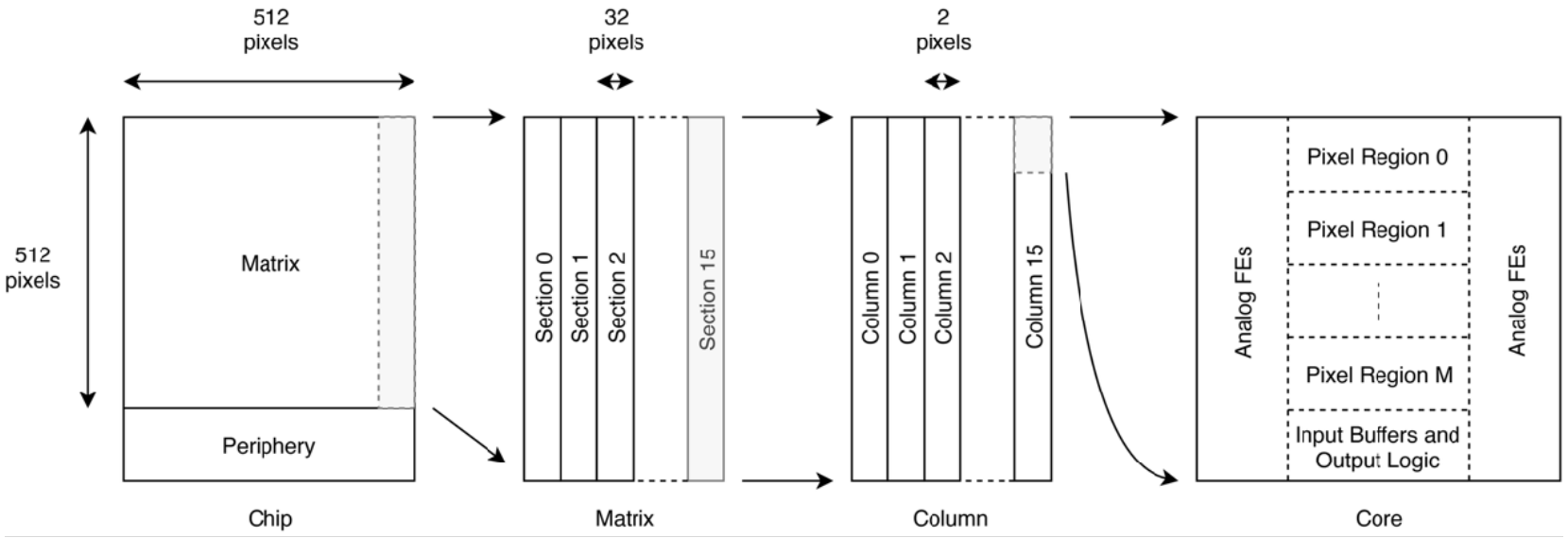
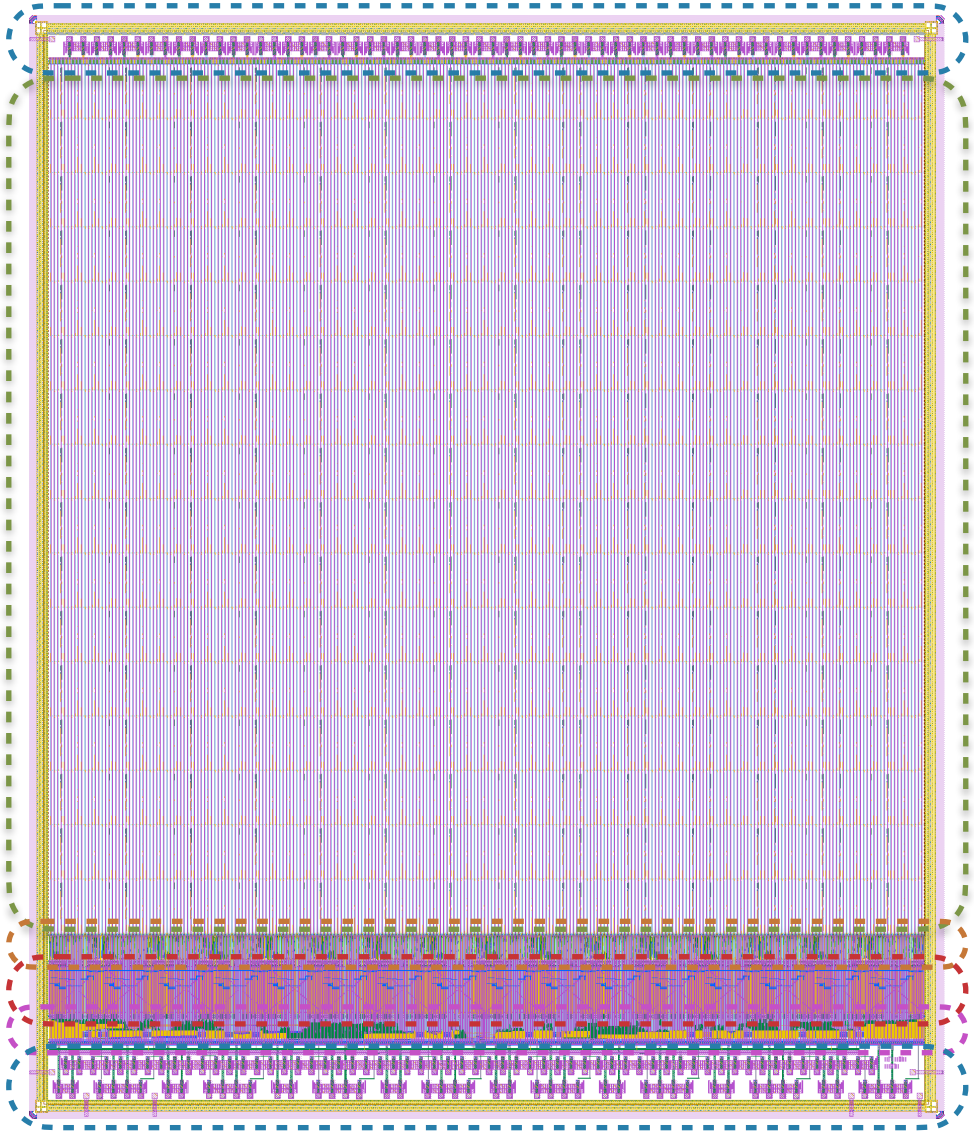
"**The main goal of the project**, started in 2019 with a timescale of 3 years, is the design, production and commissioning of an array of 512x512 pixels with a pitch of 25 x 25 μm2 (total matrix area 1.28x1.28 cm2), embedded electronics performing sparsified readout and power consumption at the level of 20 mW/cm^2. This test vehicle is expected the be a **viable prototype for** applications at the **next generation lepton colliders**."

ARCADIA-MD1: Main Demonstrator Chip



- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm^2 silicon active area, "side-abuttable"
- Triggerless binary data readout, event rate up to 100 MHz/cm^2
- **First Engineering Run** (SPW) takeout 11/2020, **silicon being tested**
- **2nd full CMOS maskset** mid-2021, fab out expected January 2022
- **3rd SPW mid-2022** with design fixes, explorative sensor and CMOS designs, new architectures with higher data throughput, full chip demonstrator for fast timing (R&D on sensors and electronics already started with 2nd SPW)

ARCADIA-MD1 - Floorplan



Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

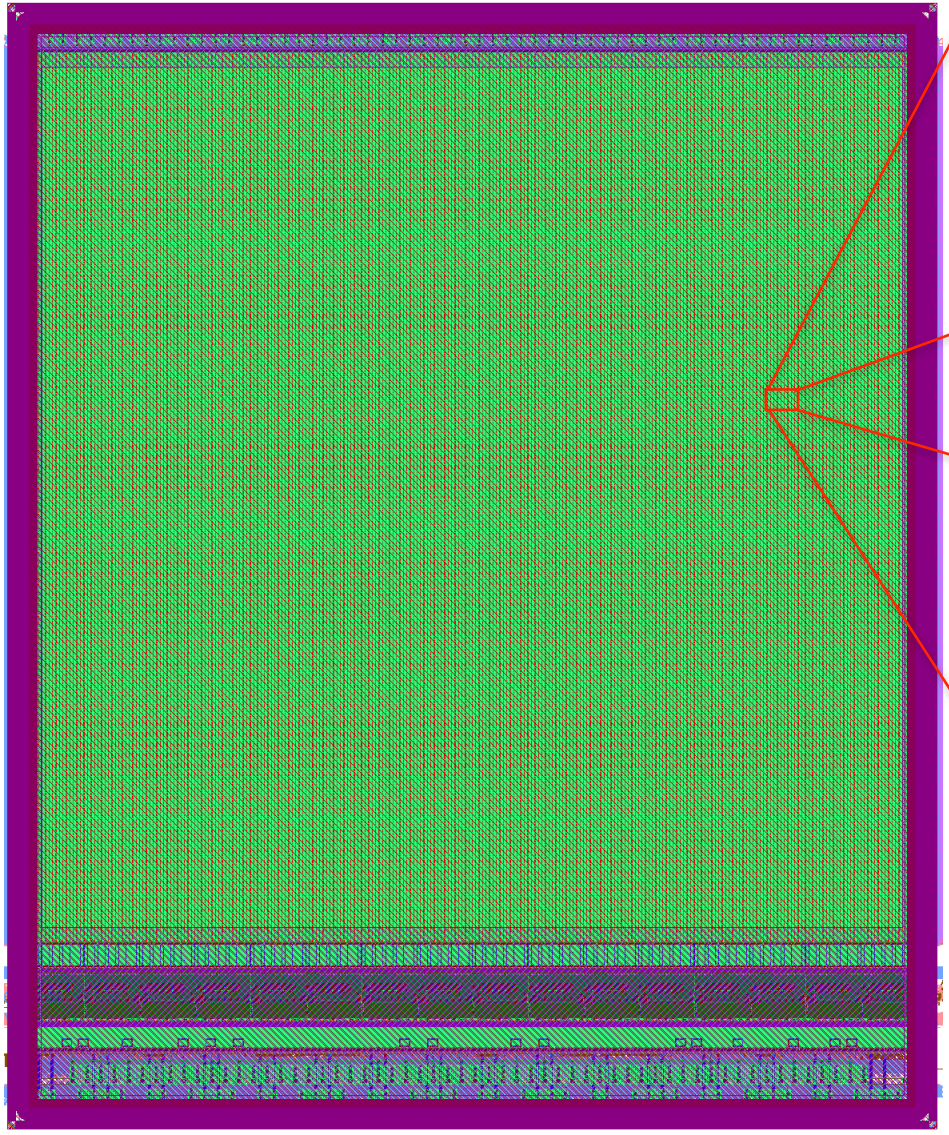
Periphery

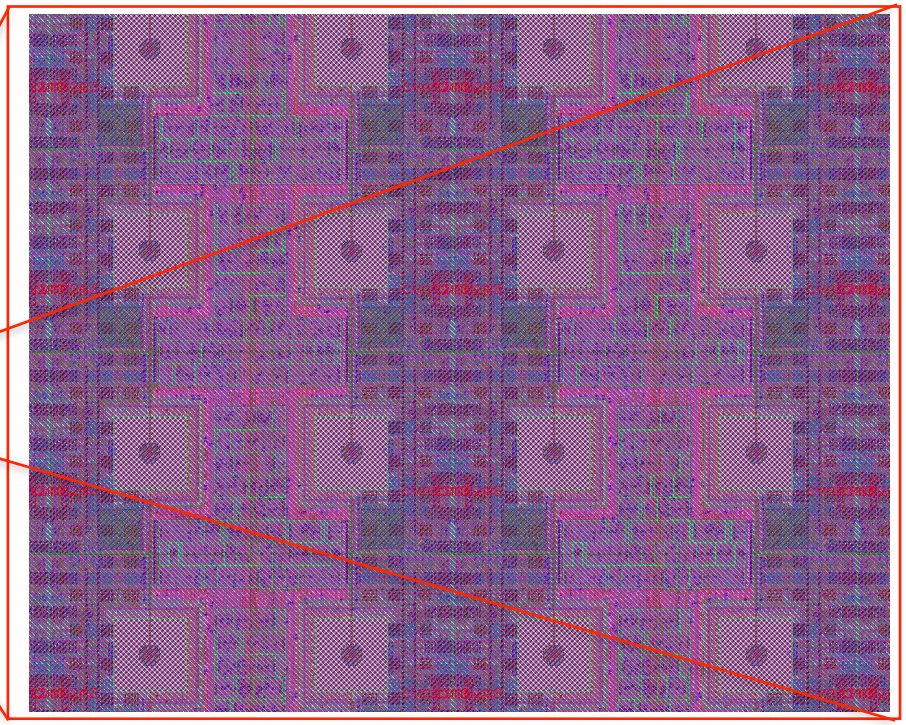
SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe

Stacked Power and Signal pads

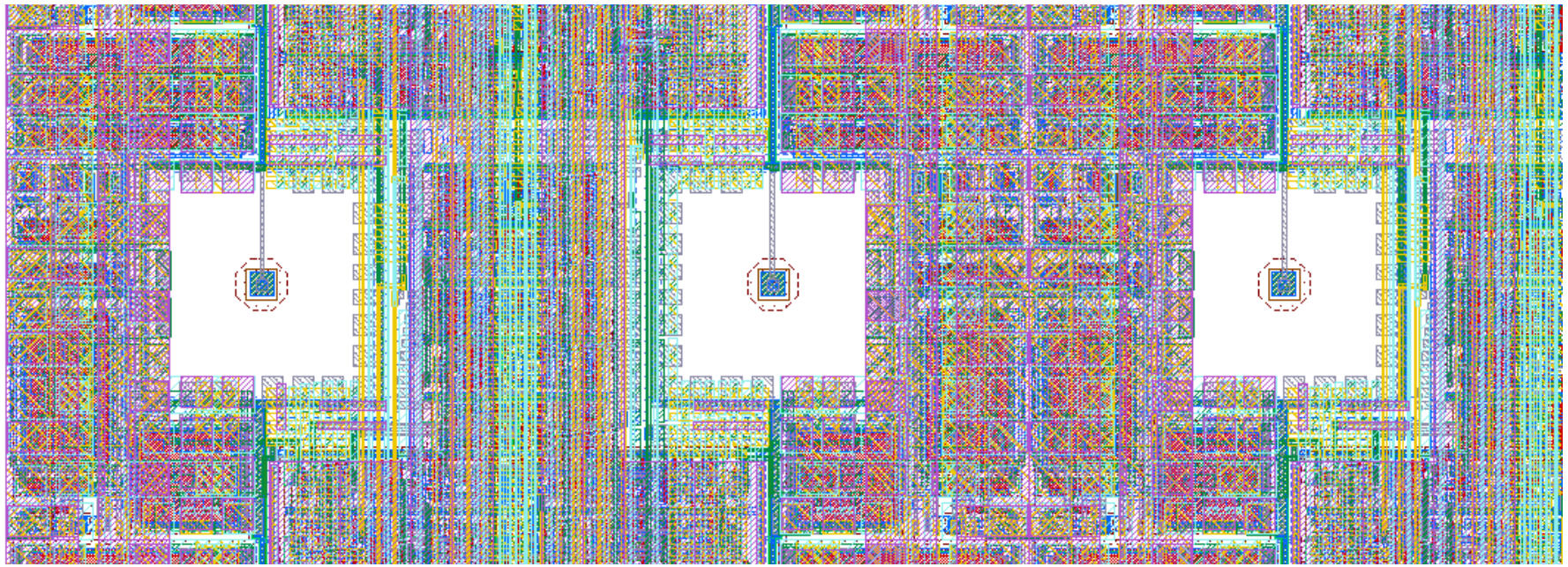
ARCADIA - Main Demonstrator Chip





- Digital-on-top integration, ICC2 flow developed by the Collaboration
- Each 2x512 Column is composed of 2x32-pixel Cores (the minimum synthesisable entity)
- ALPIDE/BULKDRIVEN front-ends on MD1a and MD1b
- Clock-less matrix integrated on a power-oriented flow

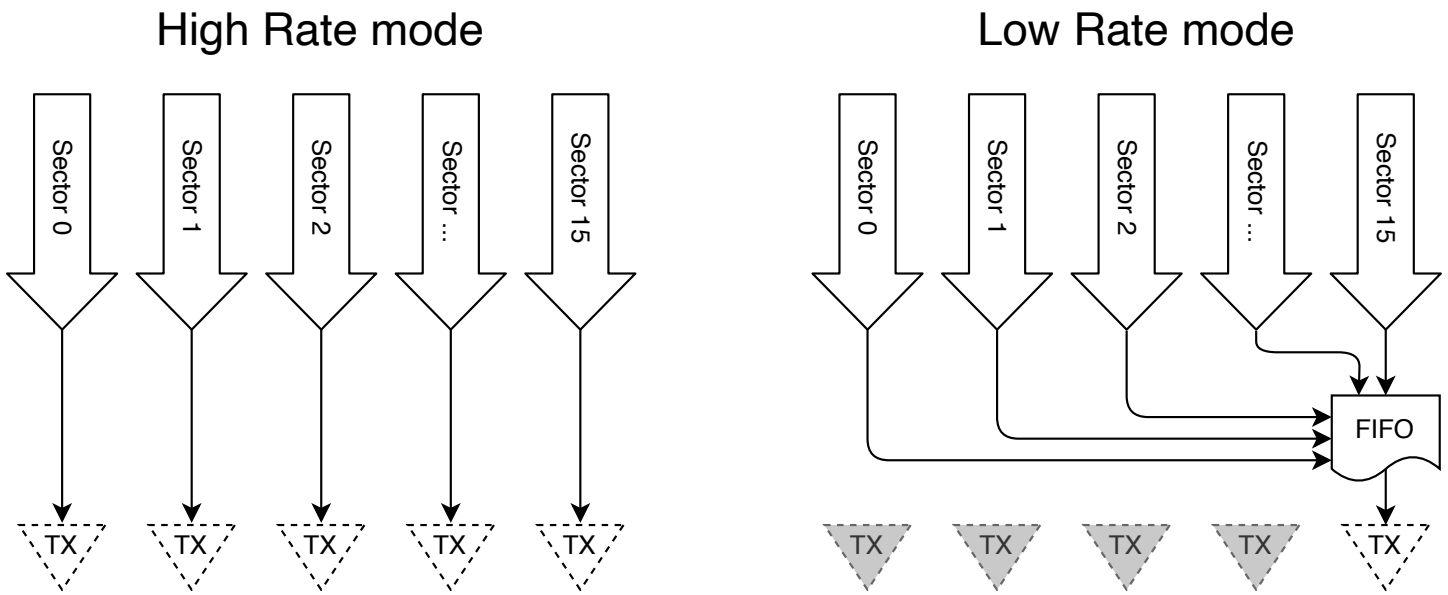
ARCADIA-MD1 - Pixels



- The pixel's area is occupied by the collection diode (16%), analog and digital circuitry
- 2-bit pixel configuration for masking and injection enabling
- Digital injection capability for readout chain testing, bypassing FEs
- Custom power distribution scheme to maximize metal occupancy

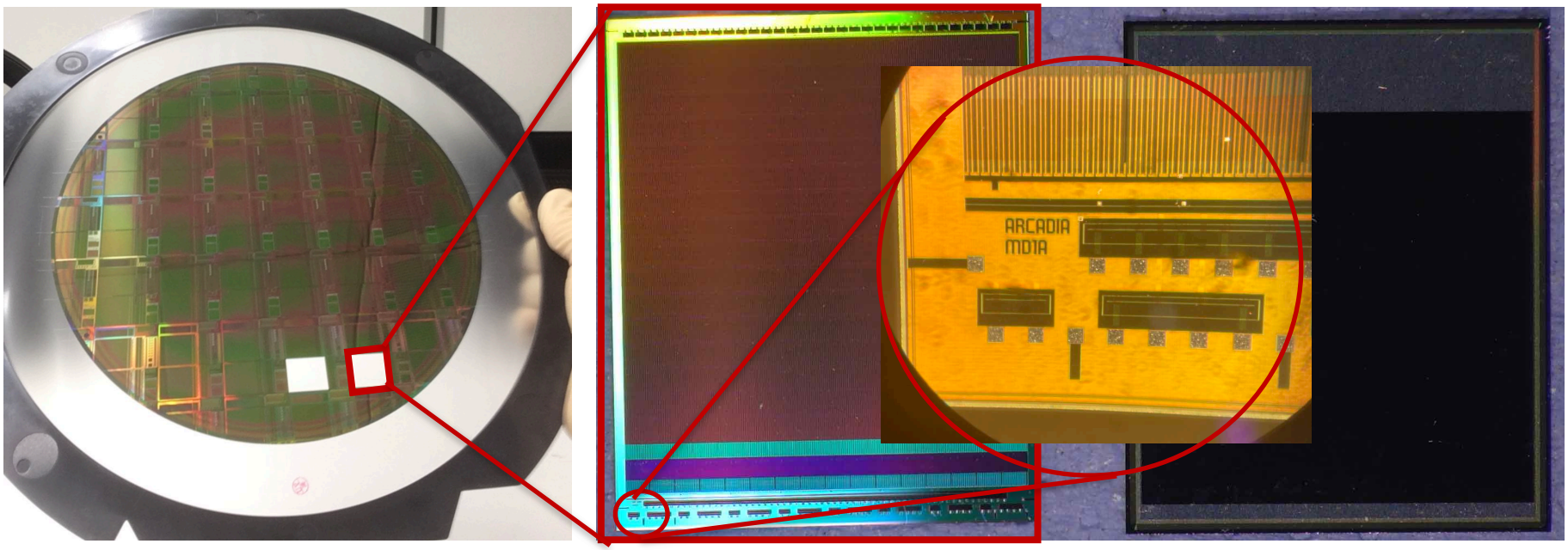
ARCADIA-MD1 - Peripheral Dataflow

- Each Column (32x512 pixels) has a readout BW of 443Mbps
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

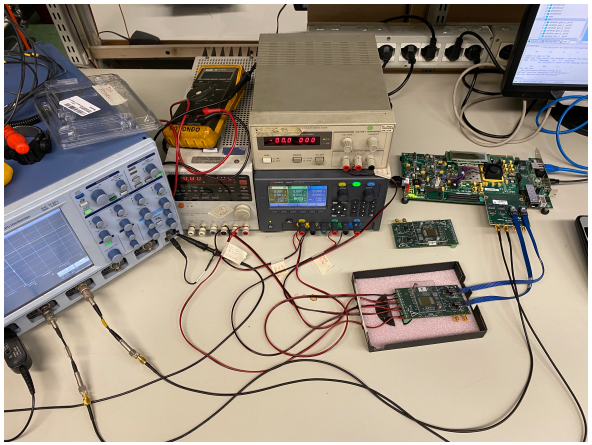


* "A 2 Gbps custom LVDS transceiver for the ARCADIA project", talk at IEEE NSS-MIC 2021

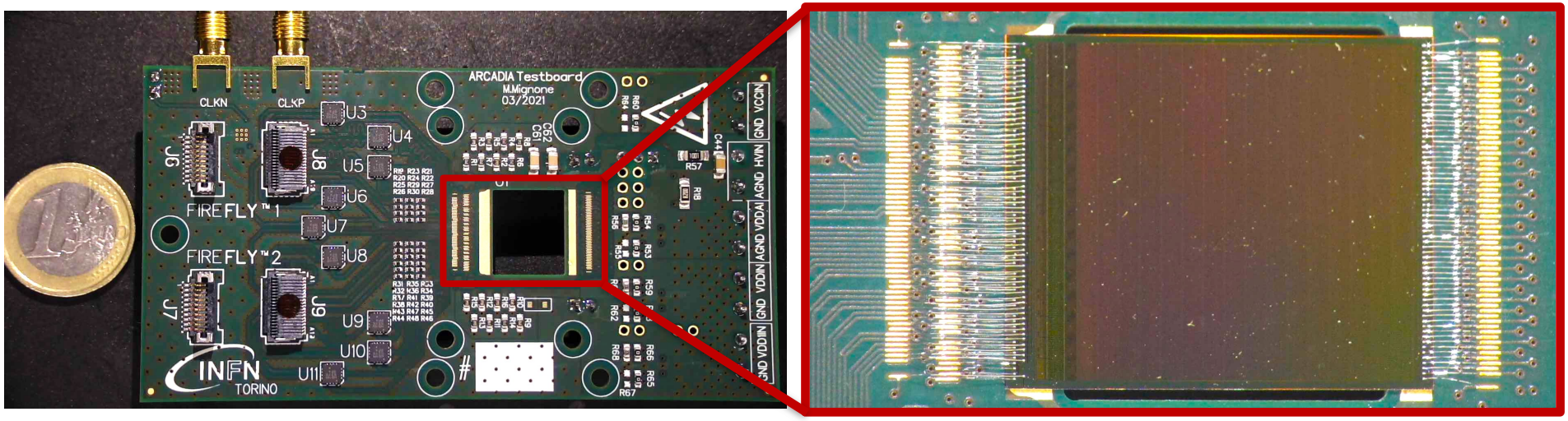
Silicon from 1st Eng. Run - MD1

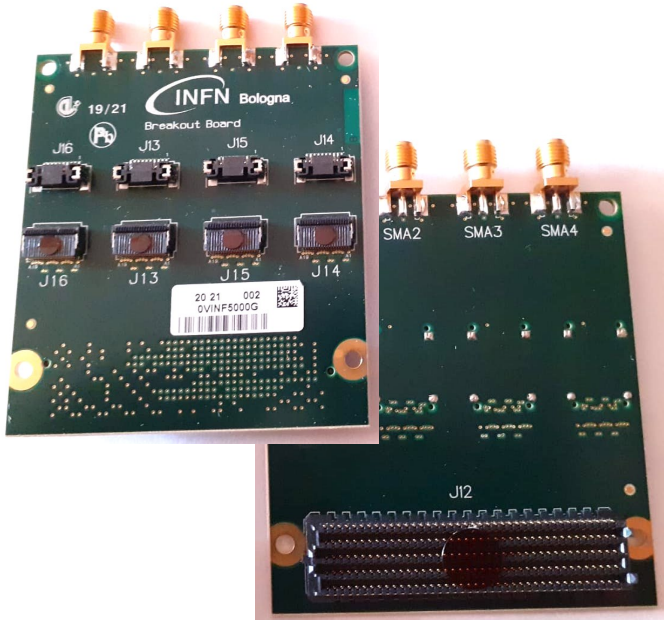


- First samples of **ARCADIA-MD1 powered-on** this summer
- Later-than-tapeout simulations identified bug on pad frame connections, simple to solve with FIB
- First data looks good & sensor depletion OK



Front-end FEB-MD1 and breakout boards

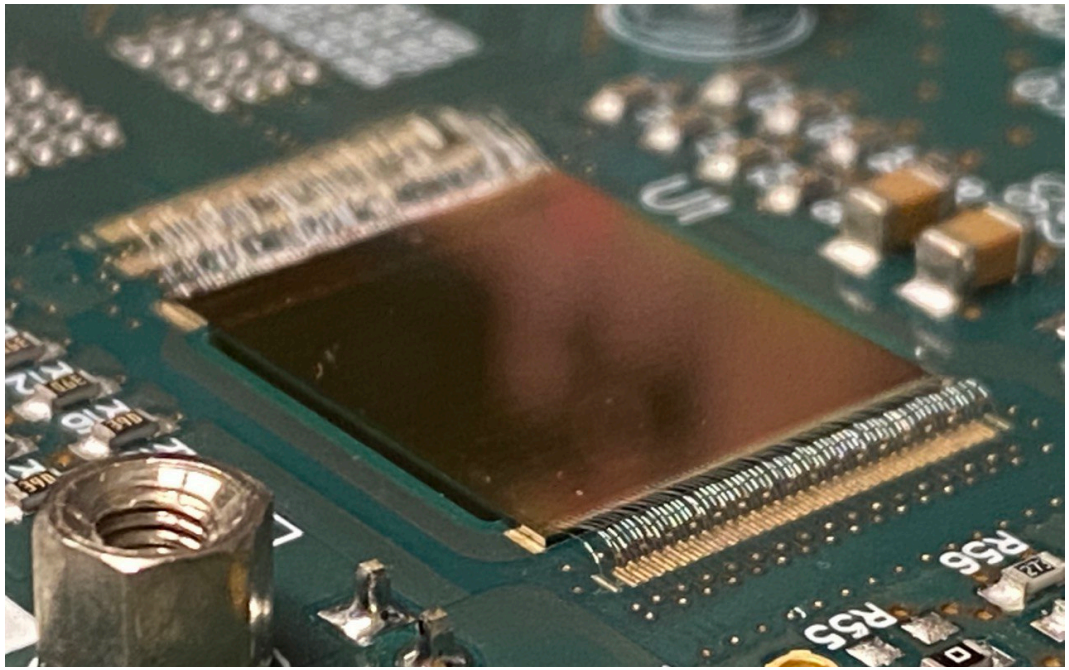




- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Connection to external low jitter Clock (via SMA connectors)
- High voltage to the DMAPS backside or (wirebonded) to pads on top
- Independent LDOs for IO Buffers, Analog Core, Digital Core
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board

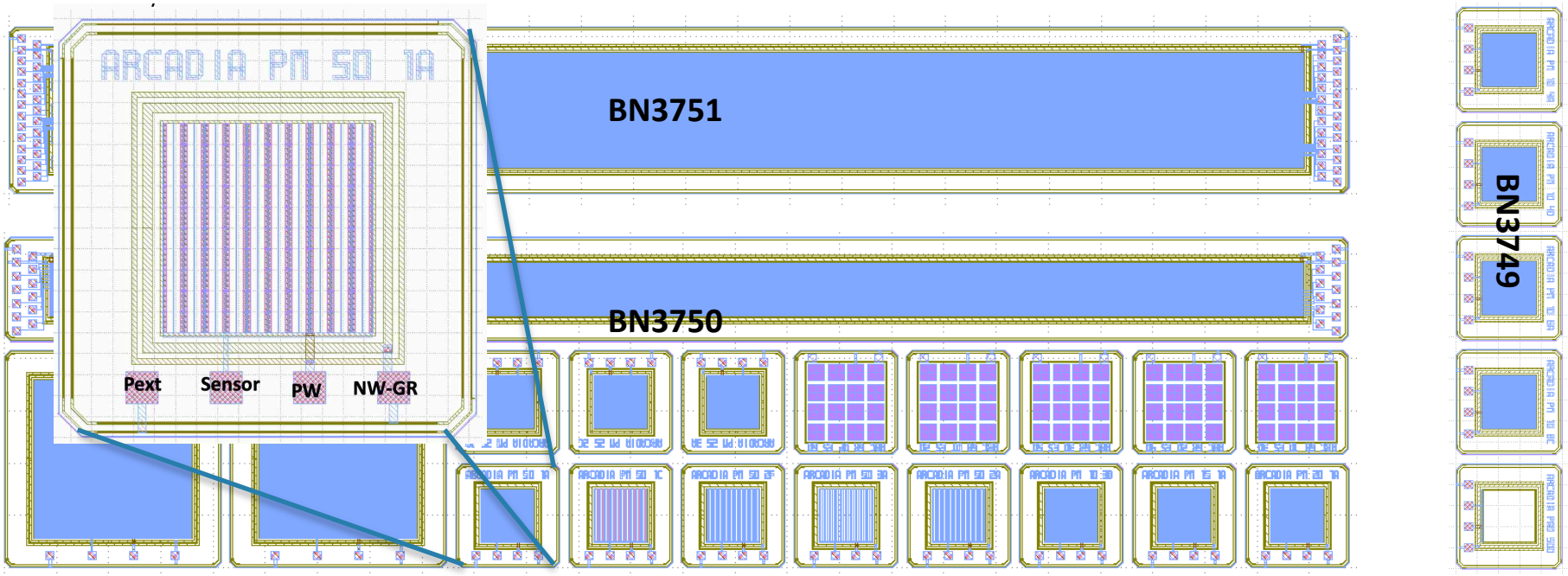
MD1: check-list from electrical tests

- ☑ Chip configuration write/readback
- ☑ Space Mode enable/disable
- ☑ Clock Gating and Clock Dividers
- ☑ Digital Injection
- ☑ LVDS SER1-15 enable/disable
- ☑ Test Pulse connectivity
- ☑ Analog FE bias and threshold scan
- ☑ Soft (SPI-enabled) and Hard (through Ext pin) Resets



- **tests with analogue front-end ongoing:**
  - test pulse charge injection with FE, s-curves, FE baseline map, noise measurements, depletion studies
  - next: characterisation with radioactive sources and laser

Pixel/Strip Test Structures



- **strips come in different flavours:**
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]
- **and pixels as well:**
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - 10 μm (6 variants)

Status of silicon testing - 1st SPW

- Measurements on bonded test structures (first non-irradiated and then irradiated with x-rays and neutrons), front-side and back side

now

- **IV curves with temperature, extraction of depletion, punch-through voltages, dark current and capacitance, first laser tests**

11/21

- Charge collection with focused pulsed laser (back-side). On pixels: only signal evolution with time and position of the laser spot. On strips: charge sharing is also possible.
- Lab. sources. (top-side and back-side)

- Characterisation of the ARCADIA-MD1

now

- **functional and electrical characterisation (basic functionalities with on-chip test pulse and hit injection, s-curves, threshold calibration, rate assessment)**

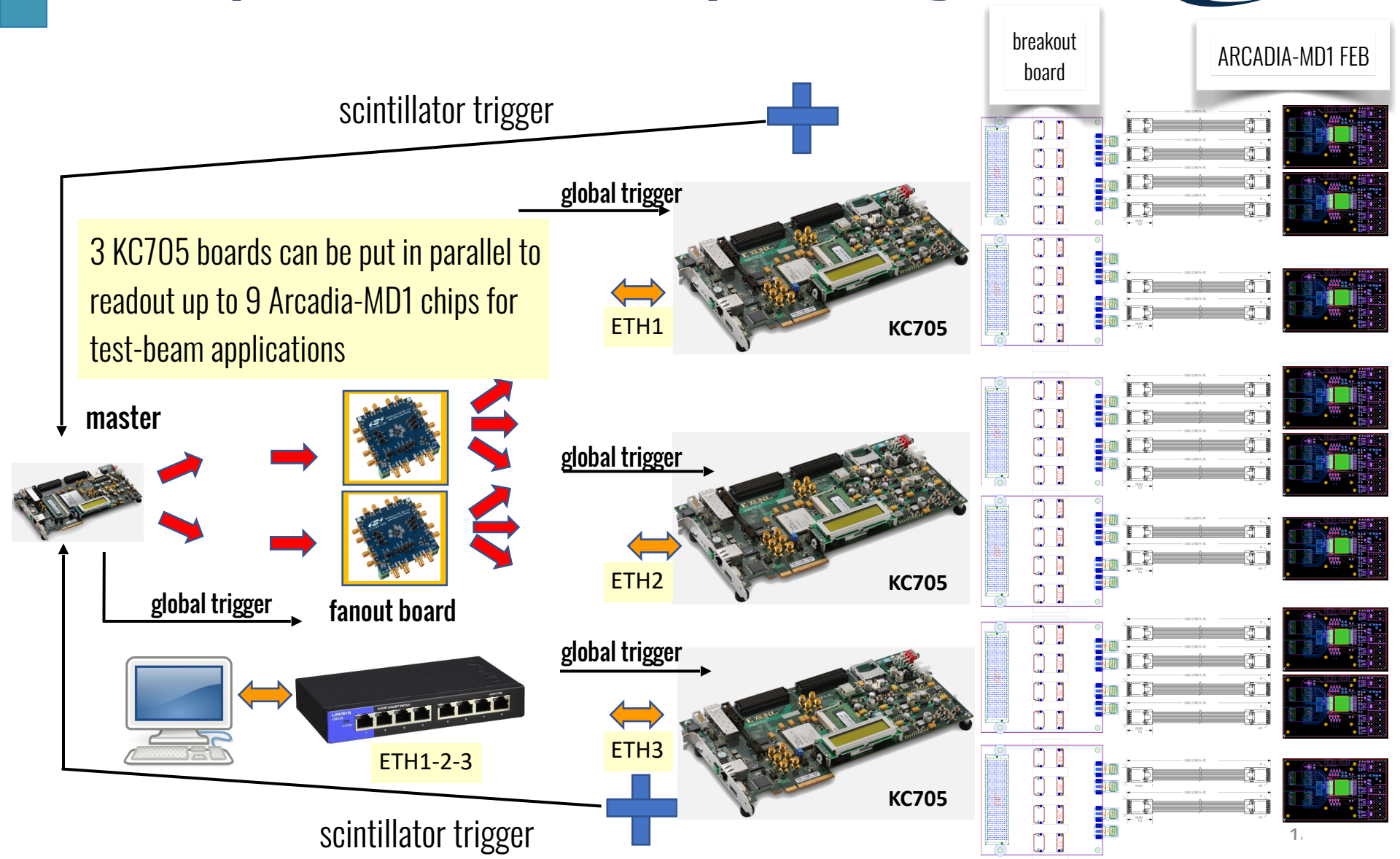
12/21

- laser scans with red and IR light (CCE vs bias voltage, uniformity, clustering and resolution)
- tests with x-ray and radioactive sources (55Fe, 241Am, 90Sr)

mid-22

- cosmic ray stand (sync and event building, efficiency, resolution) and beam tests with MD1 telescopes

Multi-plane MD1 Telescope Configuration



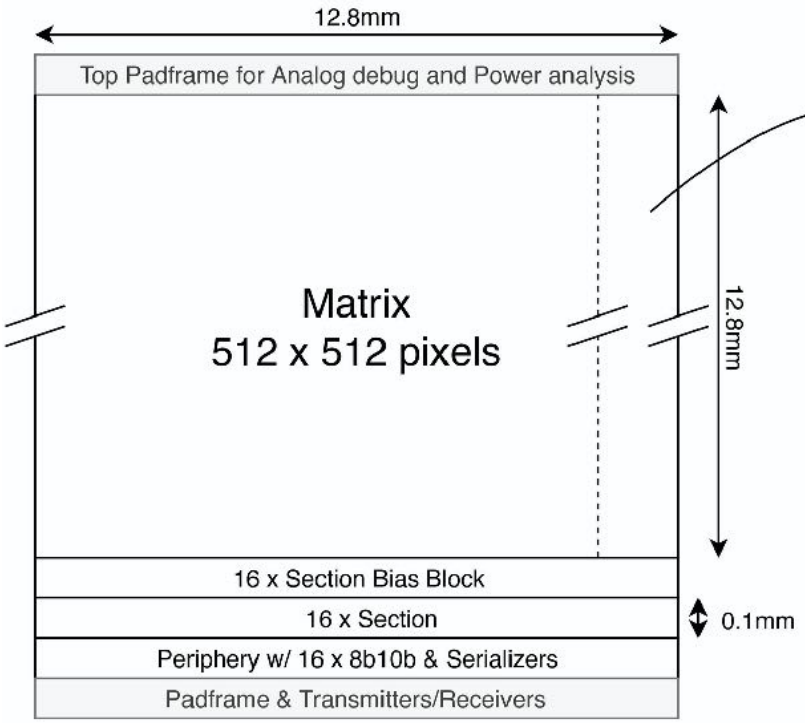
ARCADIA-MD2

A second main demonstrator (codename ARCADIA-MD2) has been submitted in Summer 2021, featuring design and architecture improvements targeting power reduction, scalability.

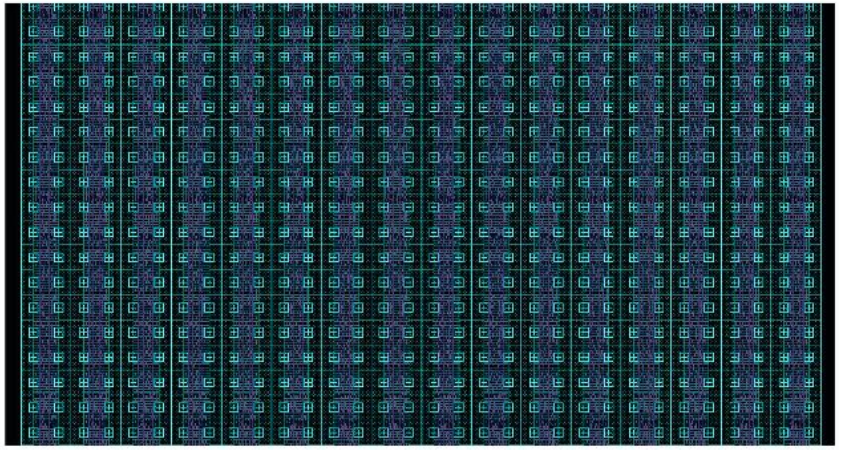
- 16x2 pixel Cores, 8 Cores in the Matrix
- Logic and buffering optimization -> Acknowledge signal propagates 7 times faster!
  - Simulations validated matrices up to 8192 pixels high
- Power optimization in the periphery
- 1 GHz DDR serializer -> 2Gbps bandwidth!
- Now in foundry, expected dies in January 2022.

Pixel Readout ASIC for photon-counting

in collaboration with the Division of Nuclear Technology and Applications at IHEP



Matrix (512x512 pixels)
Section (32x512 pixels)
Column (2x512)
Core (2x32)
Region (2x2) groups 4x 50 µm pixels



- Implementation of the sensor matrix for photon-counting ASIC using a 100 x 100 µm ARCADIA super-pixel
- Chip design and sensor simulations ongoing, silicon prototype production scheduled for 2022-Q2
- Final version should allow both a hybrid assembly of a CdTe detector and a fully-depleted silicon sensor

CMOS Embedded Si-strip and readout

- Design and Production of continuous and “pixelised” strips, range 10 - 100µm pitch
- Proof-of-concept: **CMOS monolithic strip block and readout electronics**

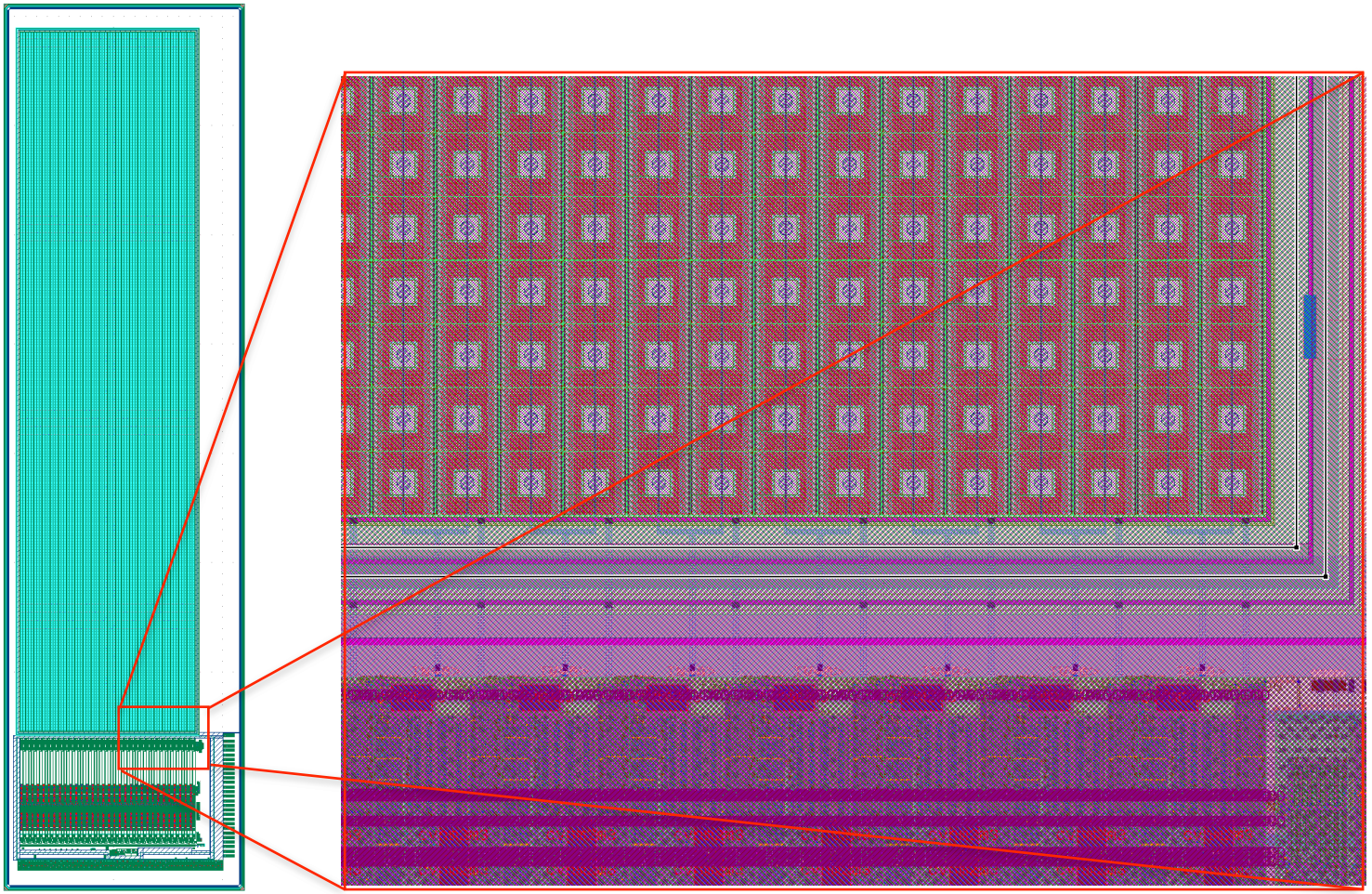


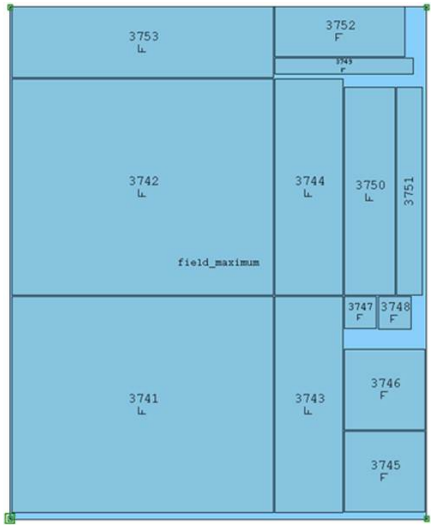
Figure: CAD Layout of 2x32x50µm pixelised strips

Figure: (top) detail of 2x32x50µm pixelised strips and (bottom) 32-channel custom readout

Summary and Outlook

- **ARCADIA** has now secured a total budget of 1.4 M€ with several groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space Instruments

- **Schedule for 2021-2022**
  - ARCADIA-MD1 submitted in October 2020, first dies in June 2021
  - 1st SPW run included 800 mm2 of innovative DMAPS, sensor and CMOS technology (tests on sensors are ok, tests on all digital and analog features confirmed the expected functionality)
  - 2nd run mid-2021: in foundry, 3rd run scheduled for mid-2022;



Thank you for your time!