# Vertex detector at Belle II: present & future

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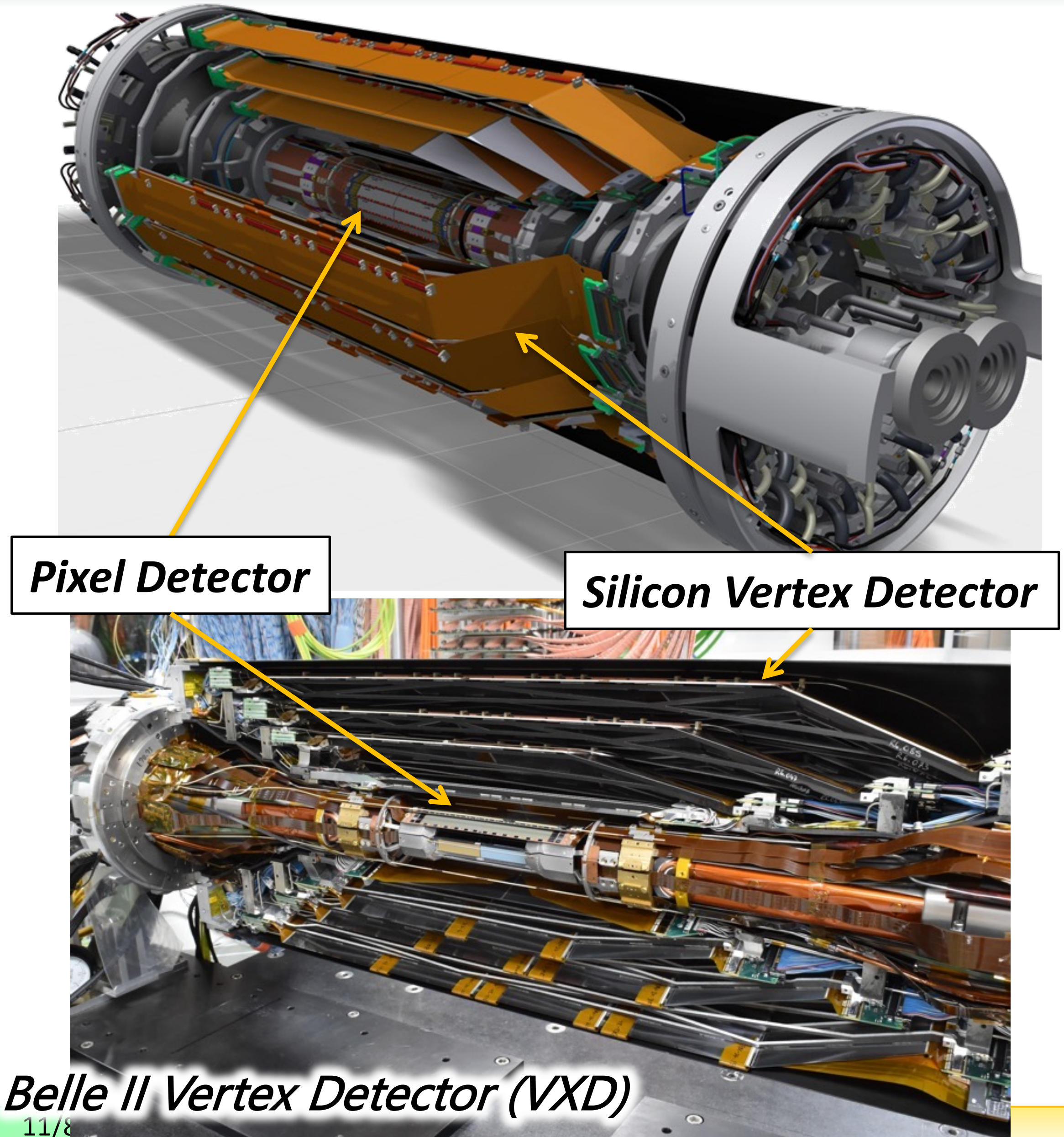
2021 International Workshop on the High Energy Circular Electron Positron Collider

# Present Vertex Detector in Belle II: Pixel detector (PXD) and Strip detector (SVD)

# Vertex Detector at Belle II Experiment




- **Belle II experiment at SuperKEKB collider**
  - Luminosity-frontier experiment, exploring new physics beyond the standard model
  - Asymmetric $e^+$-$e^-$ collisions at $\sqrt{s}$ = 10.58 GeV
    - Target integrated luminosity: 50 $ab^{-1}$
    - Target instantaneous luminosity: L ~ 6 x $10^{35}$ $cm^{-2}s^{-1}$
  - Operated with the vertex detector since 2019

Vertex detector (VXD) in Belle II

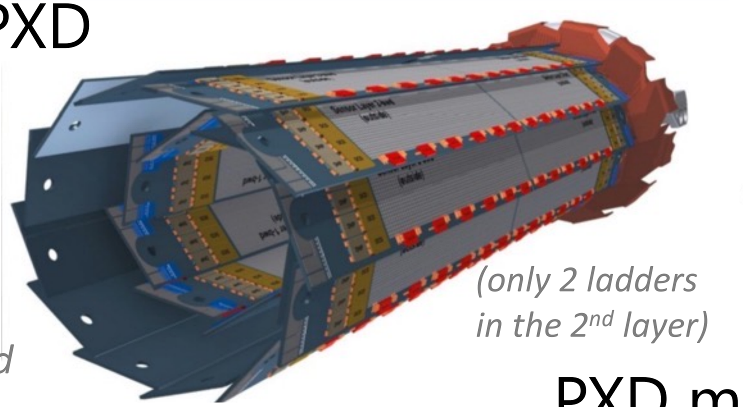
- **Inner 2 layers: PiXel Detector (PXD)**
  - DEPFET sensor
- **Outer 4 layers: Silicon Vertex Detector (SVD)**
  - Double-sided silicon strip (DSSD) sensor
- Roles of VXD
  - Determine the vertex position
  - Standalone tracking
  - PID using SVD $dE/dx$ for low $p_T$ tracks

# PXD: Detector Structure and Specification

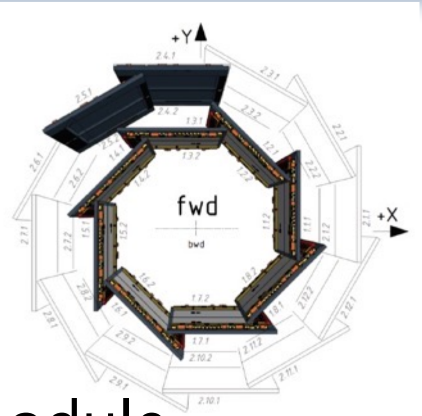
- **2 layers of DEPFET sensors**
  - 1st layer: 8 ladders at **R=14mm**
  - 2nd layer: 12 ladders at R=22mm, but only 2 ladders installed now
  - $7.7\times10^6$ pixels in total
  - about **0.21% $X_0$** per layer
- **PXD readout**
  - Rolling shutter readout mode
  - Full integration time: about 20 μs
- **PXD modules and ladders**
  - Module: DEPFET sensors + ASICSs
    - 6× switchers: row control, 4 rows per channel
    - 4× DCD: 256 channels 8-bit ADC
    - 4× DHP: data processing, trigger, and timing
  - Ladder: Two modules glued to one ladder

*Short distance from IP, and small material budget*
*→ Excellent vertex resolution*

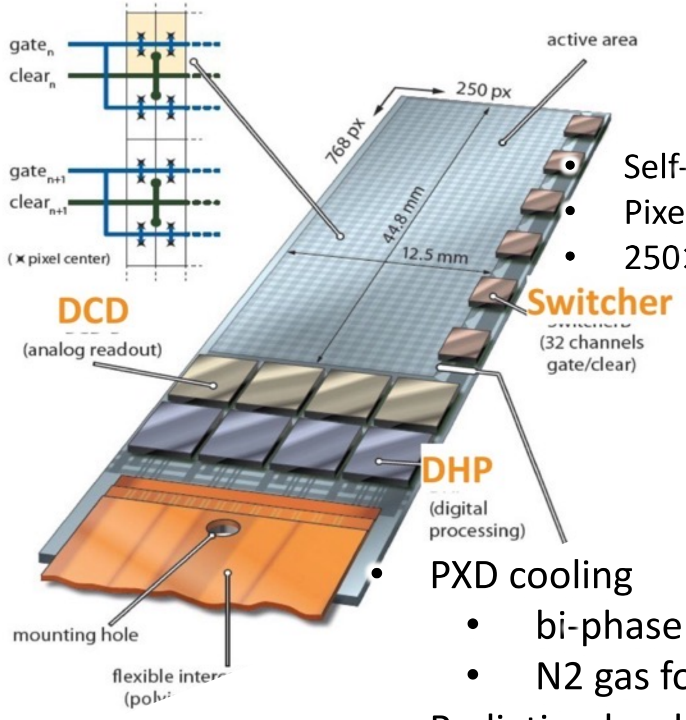
PXD



*(only 2 ladders in the 2nd layer)*




PXD module



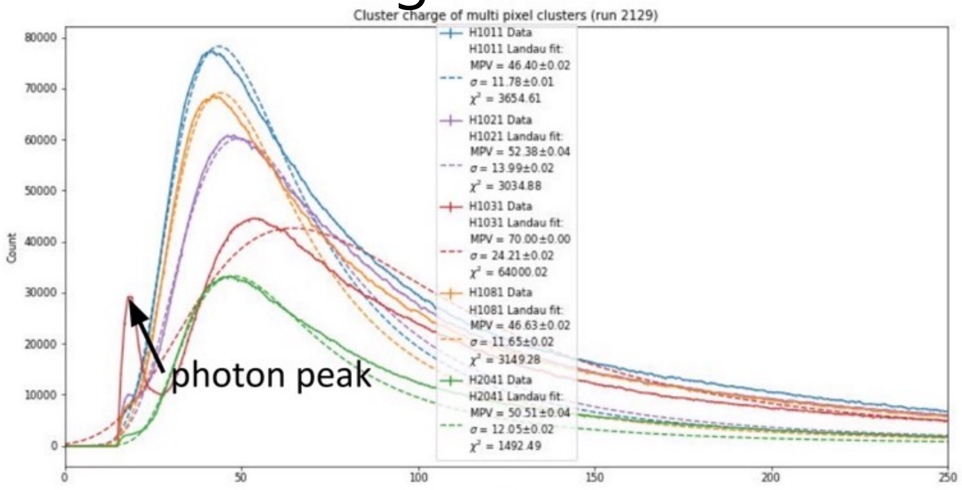

- Self-supporting 75 μm thickness
- Pixel size: 50×(55-85) $\mu m^2$
- 250×768 pixels per sensor

- PXD cooling
  - bi-phase -20 °C $CO_2$ for DCD/DHP
  - N2 gas for sensor and switchers
- Radiation hardness of sensor and ASIC
  - confirmed up to 266kGy

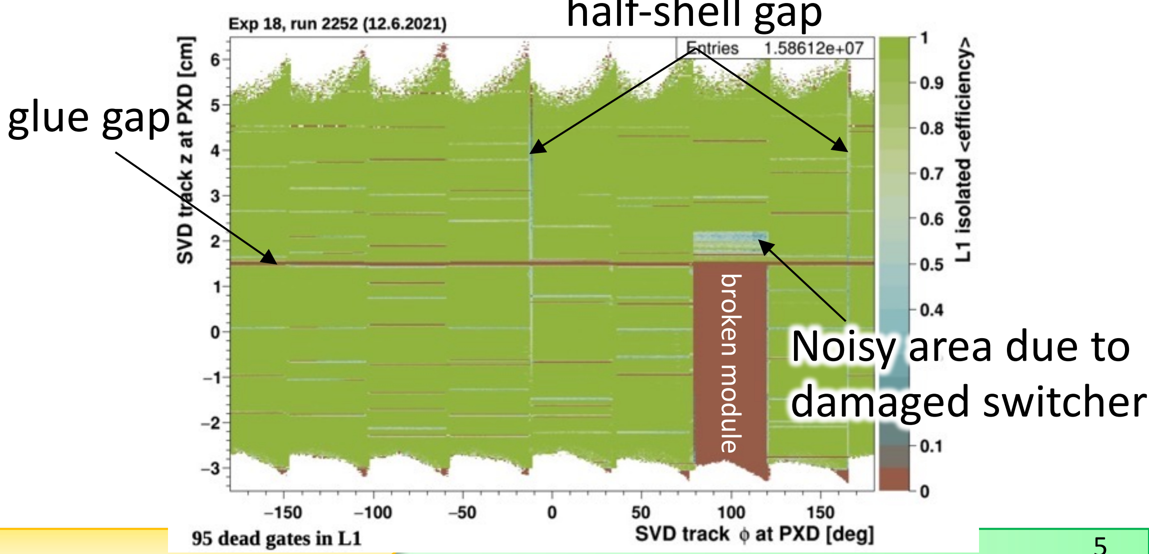
# PXD: Performance

- **Signal and Noise**
  - Most Probable Values (MPV) of cluster charge uniform in each module
  - Low noise < 1 ADU ~ 200 $e^-$: homogeneous in each module
  - Signal-to-Noise Ratio (SNR) ranges from 30 to 50
- **Hit efficiency**
  - About 99% in good regions
  - Bad switcher channels mostly due to large beam losses
    - They degrade overall hit efficiency by about 3%.
    - One damaged switcher since May 10, 2021 also due to large beam loss.
  - One module broken from the beginning
    - The acceptance covered by the 2nd layer

Cluster charge distribution

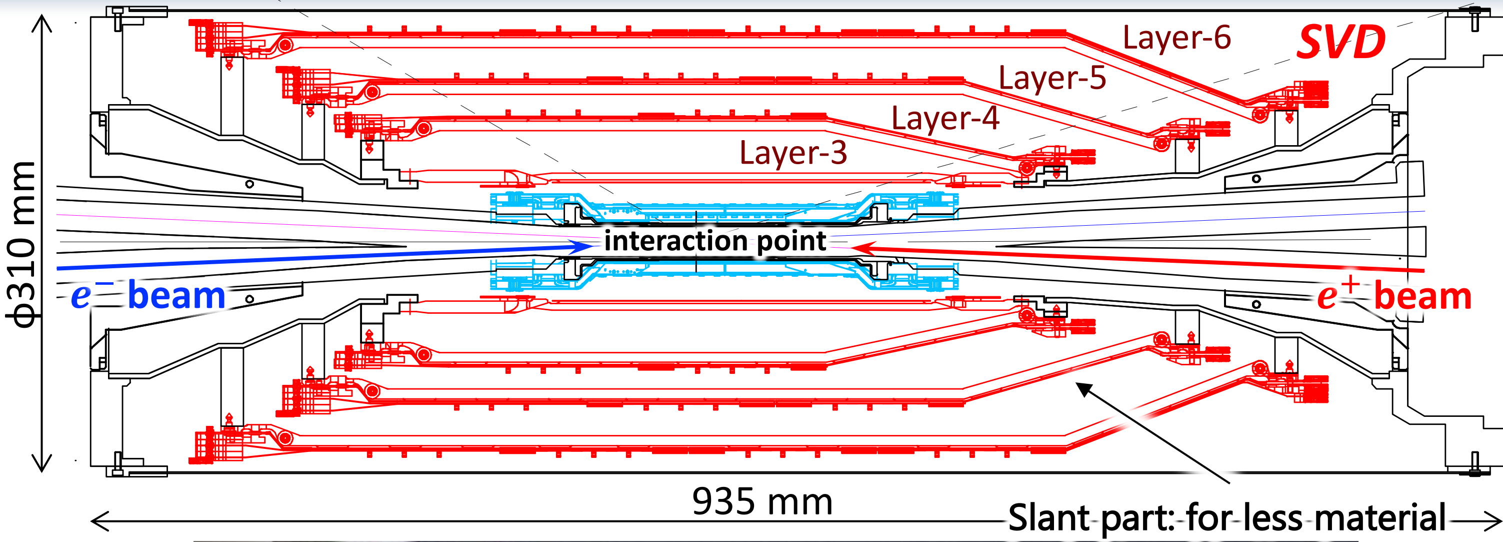



Hit efficiency map in 1st layer

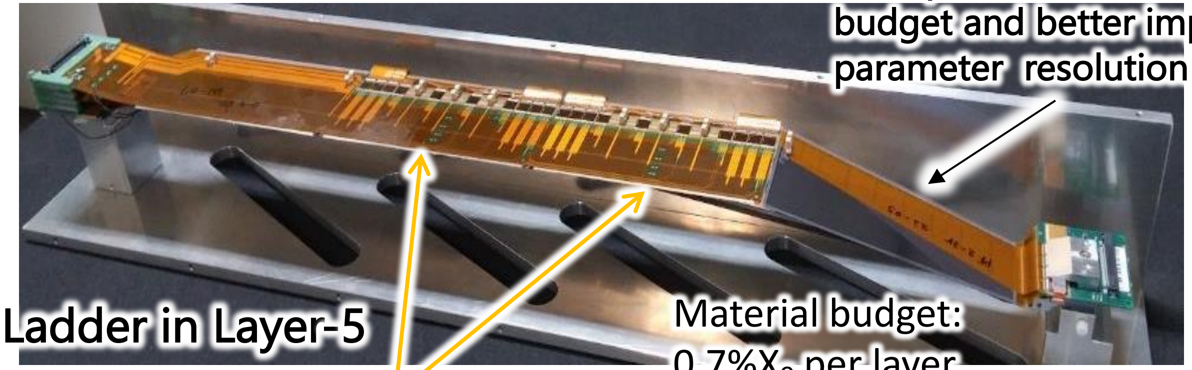


# SVD: Detector Concept

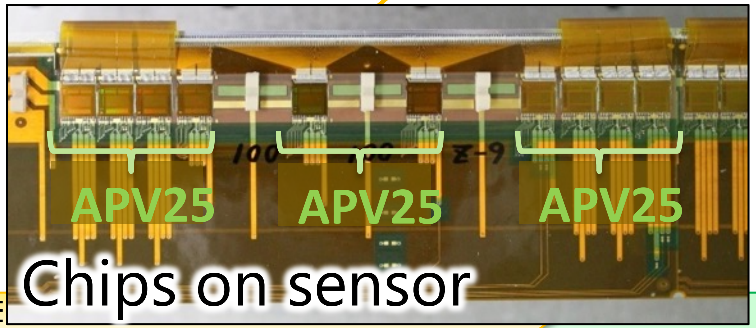
- **DSSD sensors** *pitches of barrel sensors*
  - Readout strip pitch (P/N): 50µm/160µm for Layer-3, 75µm/240µm for Layer-4,5,6
    - floating strips between two adjacent readout strips
  - Thickness: 300-320µm
  - In total: 172 sensors, 1.2m$^2$ sensor area, and 224k readout strips
- **Front-end ASIC: APV25 chip**
  - Originally developed for CMS Si tracker
  - Fast: 50 ns shaping time
  - Radiation hardness: > 1 MGy
  - 128 channel inputs
  - Power consumption: 0.4 W/chip → 700W in total (1748 chips)
- **Chip-on-sensor concept**
  - Shorter signal propagation length → smaller capacitance and noise
  - Thinned to 100 µm thickness to reduce material budget
  - Cooling on-side with bi-phase -20 ℃ $CO_2$



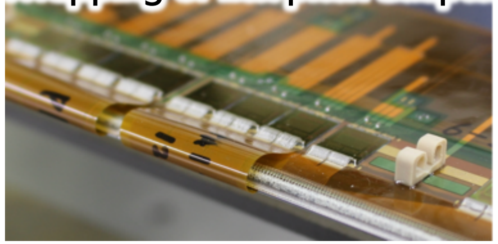

Slant part: for less material budget and better impact parameter resolution




Material budget: 0.7%$X_0$ per layer

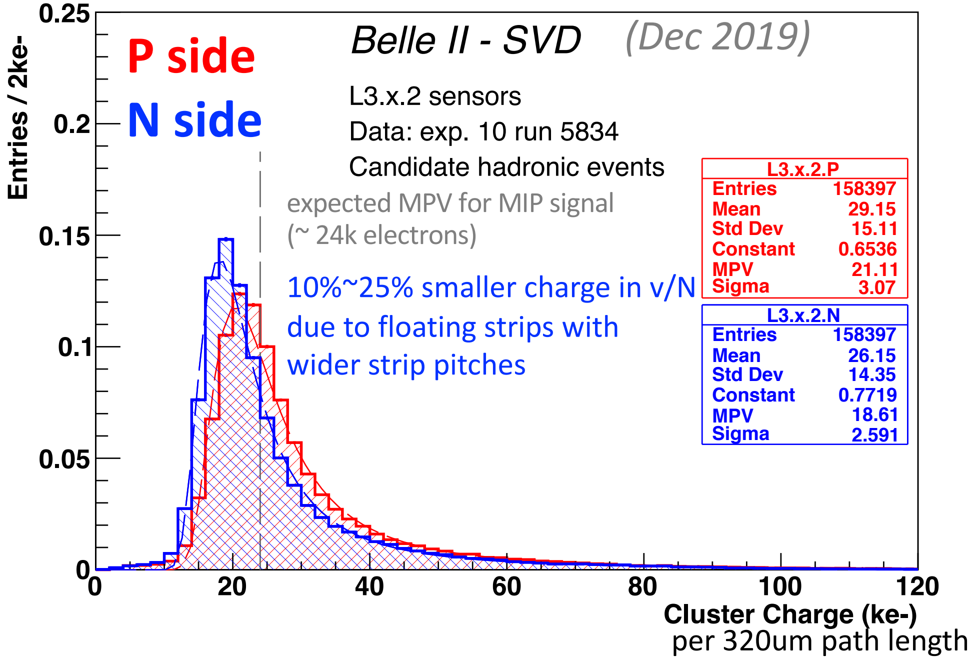


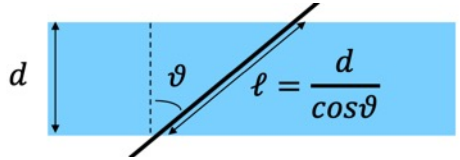

Wrapping of flex pitch adapter



# SVD: Signal and Noise

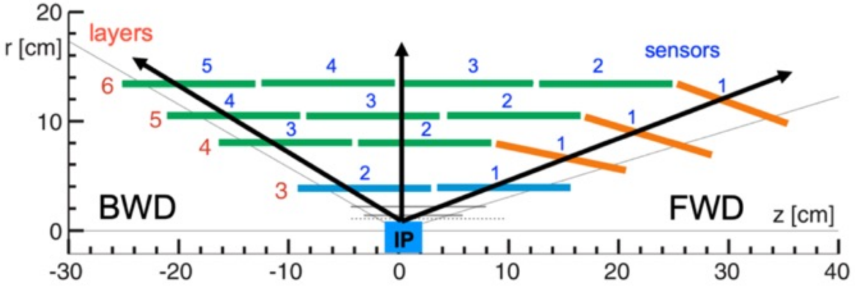
## Cluster Charge (normalized by path length)



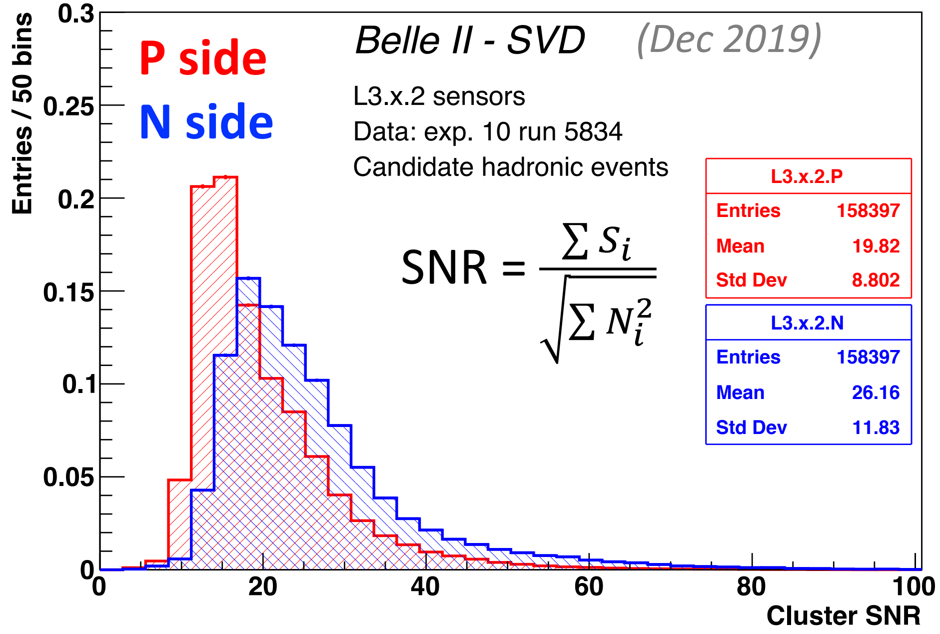




$d = 320 - 300\mu m$

$E \simeq \frac{d}{\cos\vartheta} \cdot 75\ \frac{e^-}{\mu m}$




## Cluster Signal-to-Noise Ratio (SNR)




$$\mathrm{SNR} = \frac{\sum S_i}{\sqrt{\sum N_i^2}}$$

**All 172 sensor have good SNR with MPV between 13 and 30.**

## Equivalent Noise Charge (ENC) *(before irradiation)*

| Sensor position/type | u/P side ENC ($e^-$) | v/N side ENC ($e^-$) |
|---|---|---|
| Layer 3 (HPK small) | 930 | 630 |
| Layer 4/5/6 Origami (HPK large) | 958 | 510 |
| Layer 4/5/6 BWD (HPK large) | 790 | 680 |
| Layer 4/5/6 FWD (Micron wedge) | 740 | 640 |

Larger noise in u/P due to longer strip length = larger interstrip capacitance.

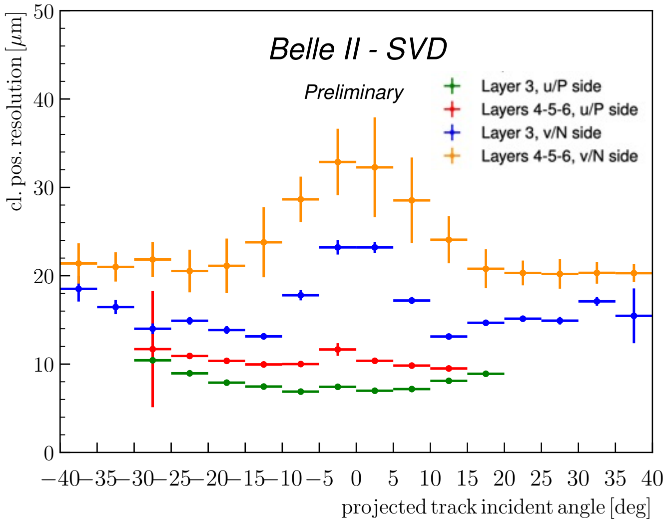
# SVD: Particle Detection Performance

## Hit efficiency (averaged in each layer)

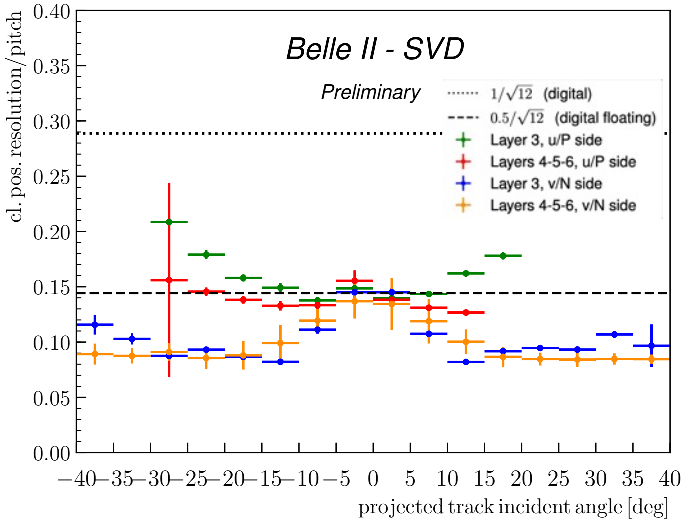
| layer | $\varepsilon(u/P)(\%)$ | $\varepsilon(v/N)(\%)$ |
|---|---|---|
| 3 | $99.83 \pm 0.01$ | $99.48 \pm 0.03$ |
| 4 | $99.69 \pm 0.03$ | $99.68 \pm 0.03$ |
| 5 | $99.66 \pm 0.03$ | $99.77 \pm 0.04$ |
| 6 | $99.31 \pm 0.08$ | $99.58 \pm 0.06$ |

**Excellent performance confirmed from experiment data.**

## Cluster position resolution (vs. track incident angle)

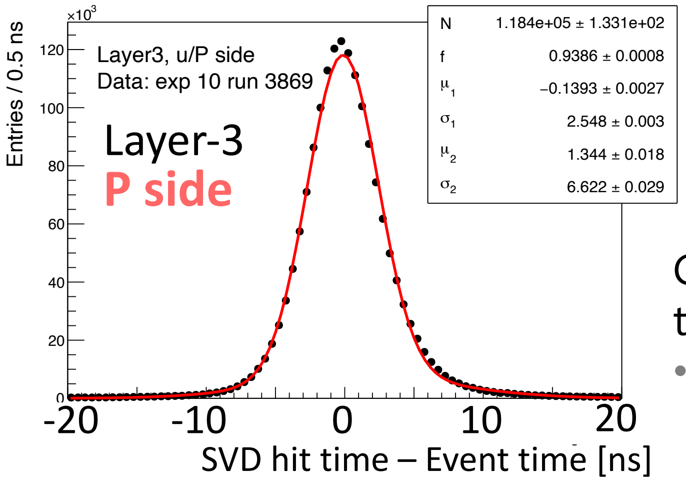



normalized with readout pitches




Excellent position resolution in agreement with the expectation form strip pitch
Still room for improvement for the P side

## Hit time resolution




Resolution in Layer-3 (RMS)

**P side**: **2.9 ns**

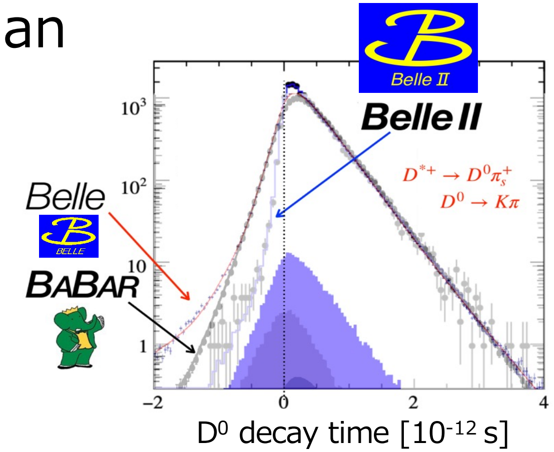
**N side**: **2.4 ns**

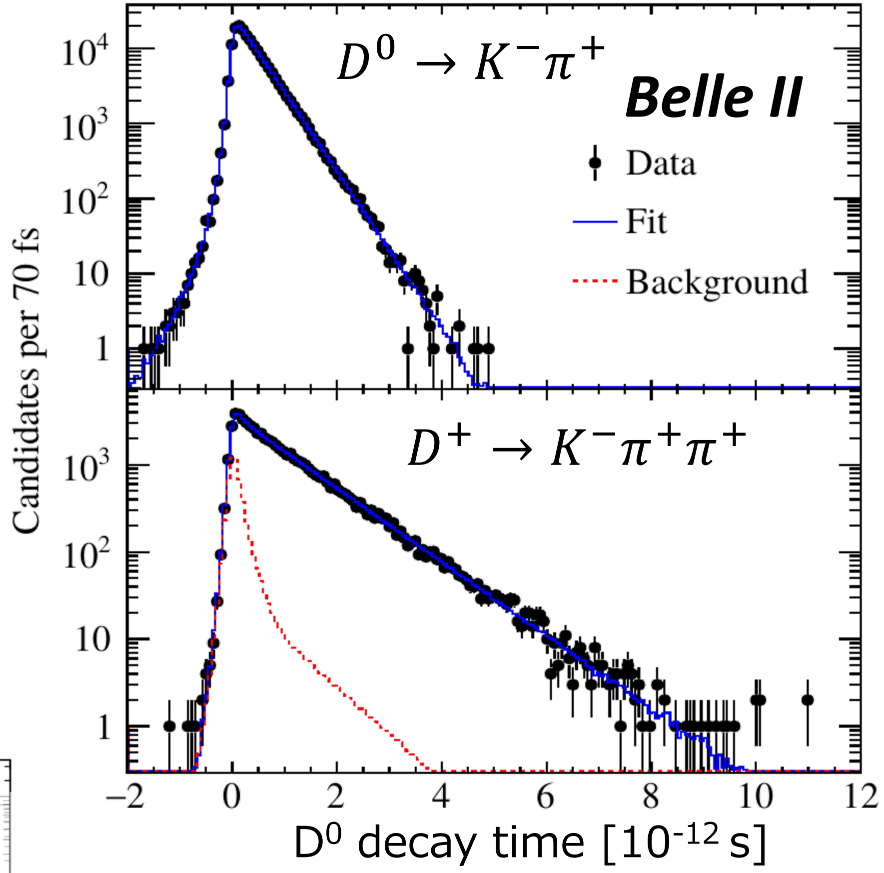
Cluster time information will be used to reject off-time beam BG hits in future.

- mitigate the deterioration of the tracking performance due to beam BG.

# Vertex Detector Resolution

- Excellent vertex resolution
  - Measured d0/z0 resolution of about 12μm/15μm
    - by beam profile measurement using Bhabha events
    - Good agreement with MC expectation
- D lifetime measurement arXiv:2108.03216
  - Vertex determination plays a key role in the lifetime measurement
  - Belle II time resolution better than Belle/BaBar by factor about 2
  - World's most precise D lifetime measurements




$$\tau(D^0) = \quad 410.5 \pm 1.1\,(\text{stat}) \pm 0.8\,(\text{syst})\text{ fs}$$

$$\tau(D^+) = 1030.4 \pm 4.7\,(\text{stat}) \pm 3.1\,(\text{syst})\text{ fs}$$

c.f. the world average before this work:

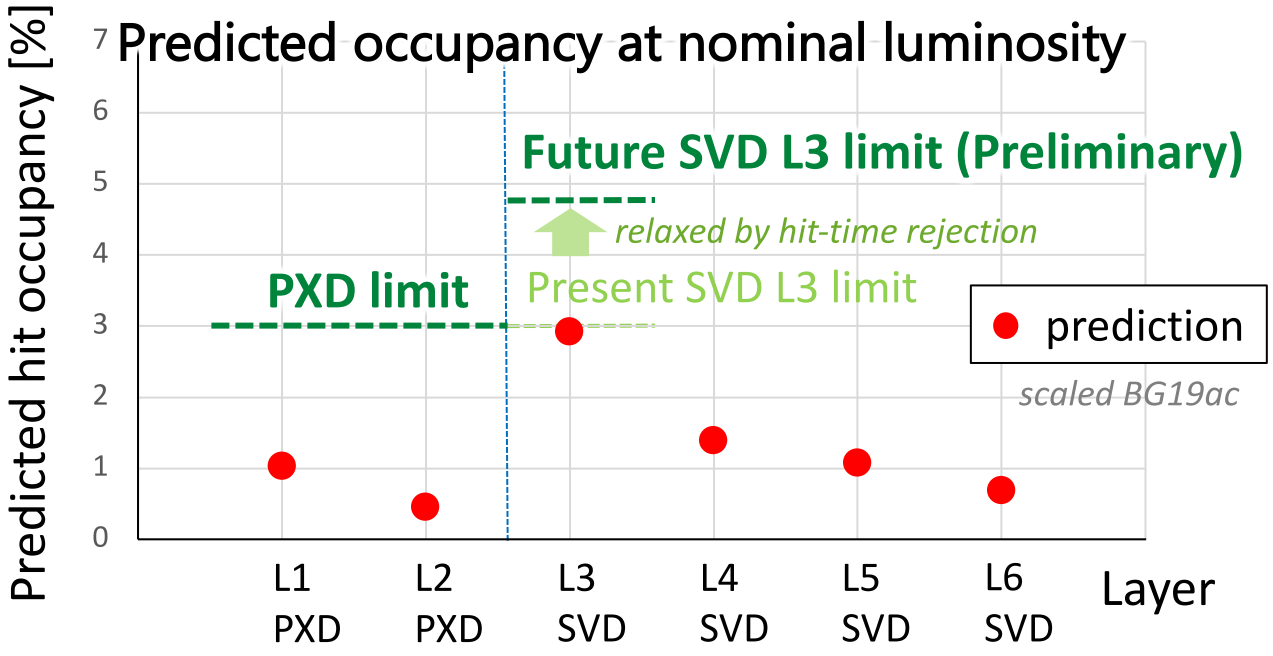
$\tau(D^0) = \quad 410.1 \pm 1.5$ fs

$\tau(D^+) = 1040 \pm 7$ fs

# Future Vertex Detector in Belle II: VXD Upgrade Project

# Limits on current VXD and VXD upgrade

## Tolerance for beam-induced background (BG)




- Difficulty of accurate prediction for injection BG and collimator condition at design luminosity ☹
- Drastic change in beam optics for design luminosity → large uncertainty ☹ ($\beta_y^*$ = 1.0mm → 0.3mm)

**Predicted BG within limits, BUT without enough safety margin**

## Tracking and vertexing performance

- Tracking performance in low-$p_t$ limited by material budget
- Room to improve vertex resolution with better hit position resolution
- Improvement in $K_S$ vertexing desirable

**Improvement in tracking and vertexing performance highly desirable**

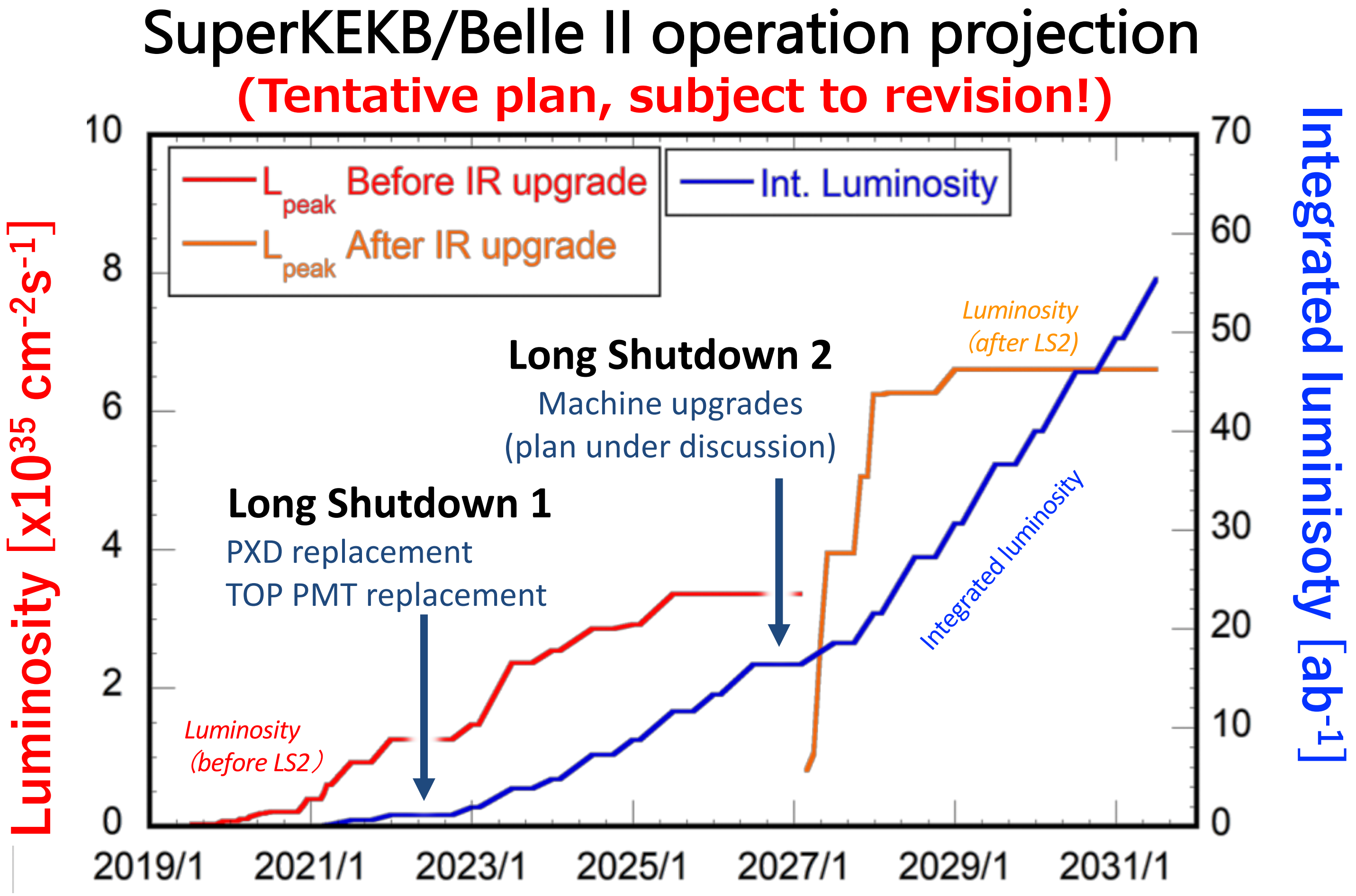
**→ Belle II VXD upgrade project formed**

**Several technology options under investigation by R&D subgroups**

- Thin DSSD sensor
- Upgraded DEPFET sensor
- SOI pixel sensor
- CMOS pixel sensor

# Timescale of the VXD upgrade project

- **Occasion of new VXD installation: 2nd long shutdown for SuperKEKB intermediate upgrade**
  - Timeframe expected to be 2026-2027, but still with uncertainty
    - Detailed SuperKEKB upgrade plans are under discussion with the international taskforce teams
  - Preparation to be done in several years → Currently available technologies preferable
- **R&D activities will access the options**
  - Which concepts bring best performance?
  - Which technology fit requirements?
  - Which technology fit timeframe of installation?
- **CDR to be prepared within ~1 year w/ full-scale prototype test and physics benchmarking**



# Upgrade R&D (1): Thin DSSD sensor

## Thin/fine-pitch SVD (TFP-SVD) concept

### Targets

- Outer layers
- Handle higher hit-rate
  - O(1MHz/cm²) R>4cm
- Improve tracking/$K_S$ vertexing performance

### Thin DSSD sensor (Micron)

**Thinner sensor**: 140um

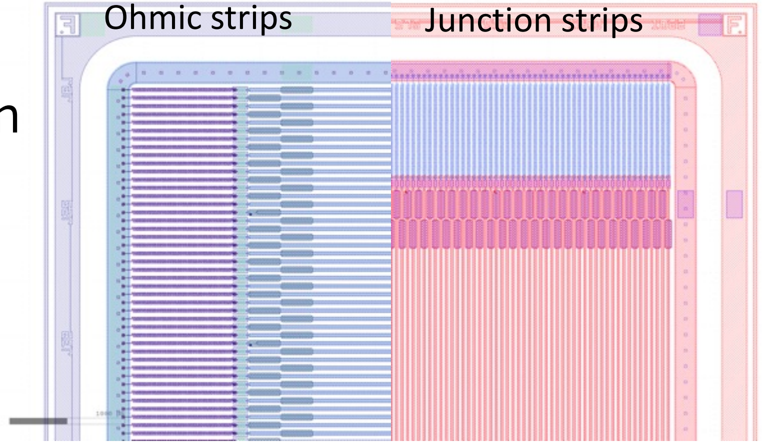
**Finer N-side strip pitches** than SVD: ~85um

### Develop new front-end ASIC (SNAP128A)

→ **R&D challenges in front-end**

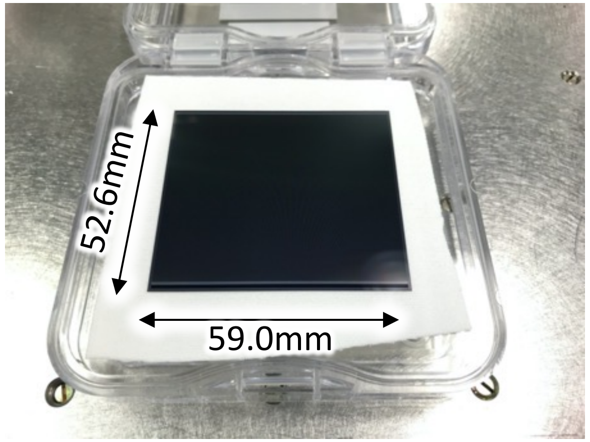
- Small noise : ~640e⁻ @ $C_{det}$=12pF (simulation)
- Small heat dissipation: ~330mW
- Short signal pulse width : ~60us

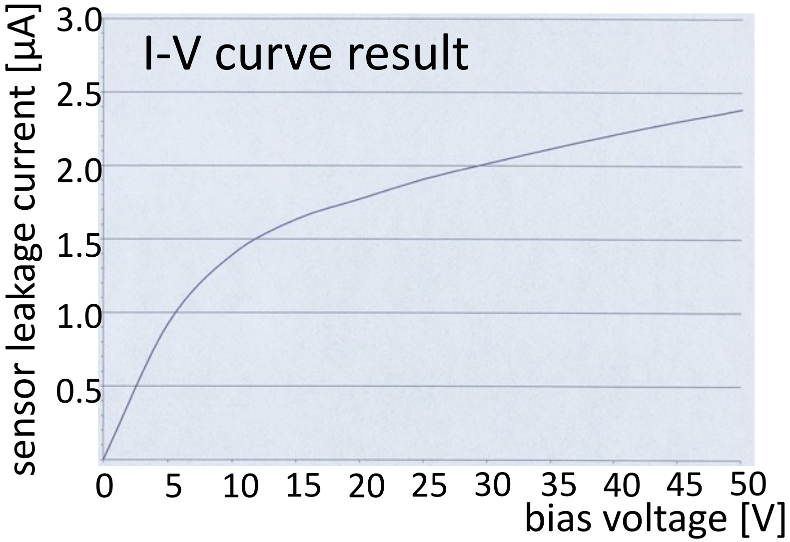
TFP-SVD DSSD layout




- Basic characterization of prototype sensors
  - Reasonable I-V and C-V curves
  - Thickness: 148±5um
  - Full depletion voltage: 14±1 V
- Performance evaluation of prototype ASIC on going

DSSD prototype

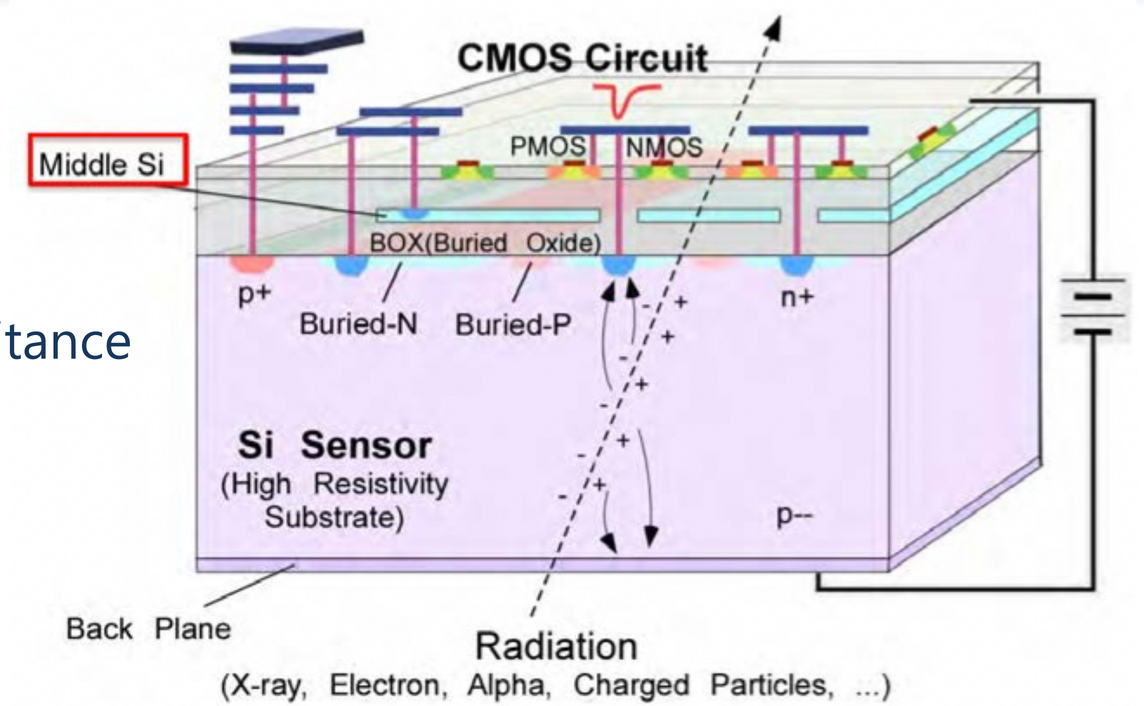


# Upgrade R&D (2): SOI pixel sensor

## Silicon-On-Insulator pixel (SOIPIX)

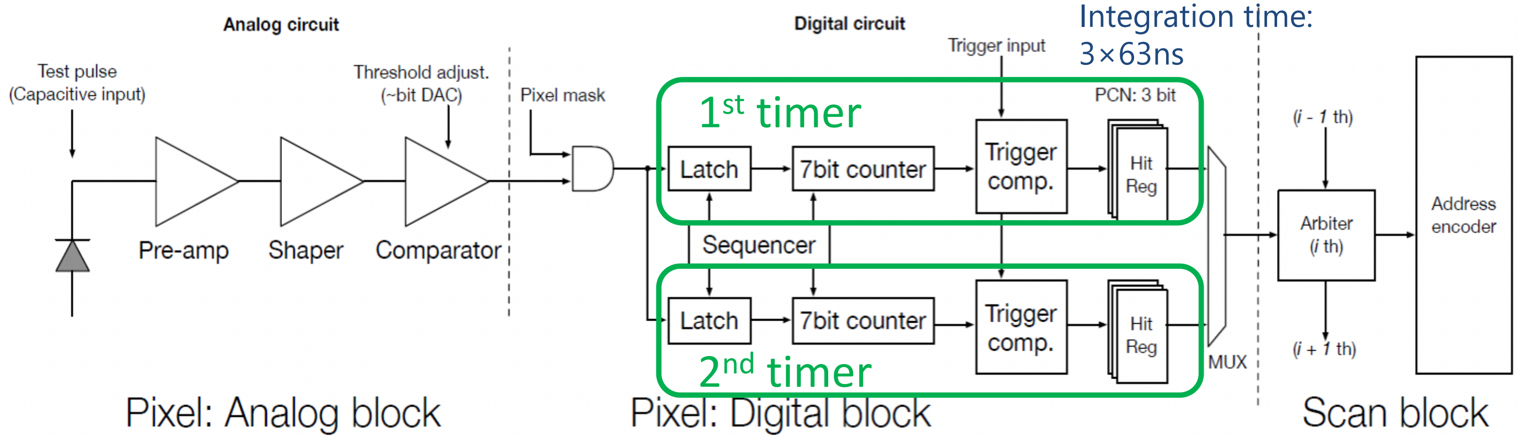
- CMOS circuit produced on silicon wafer isolated by a buried oxide (BOX) layer
  - Full depleted sensor: Fast signal, good S/N
  - Logics w/o well structure: High density, small capacitance
  - Complex circuit can be implemented in each pixel
- Produced by LAPIS semiconductor




## Dual Timer Pixel (DuTiP) concept

- Alternative operation of two timers allows the next hit before the trigger arrival for the previous hit.
  - Hit loss probability due to pile-up expected to be ~0.03% at 113MHz/cm$^2$ (assuming 8us trigger latency)

Rough estimation of final power consumption: about 0.1 W/cm$^2$



# Upgrade R&D (2): SOI pixel sensor

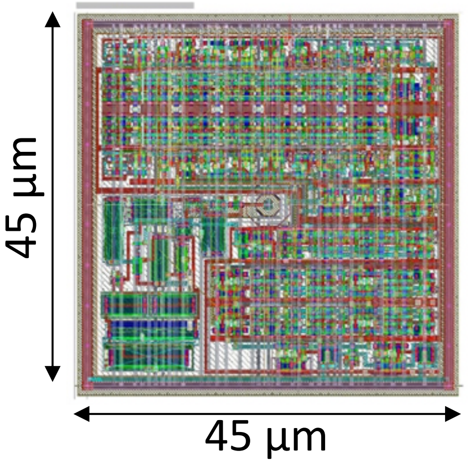
## DuTiP 1st prototype

| | |
|---|---|
| Chip size | 6x6 mm$^2$ |
| Pixel size | 45x45 μm$^2$ |
| Thickness | 50 μm$^{(*)}$ |
| Clock | 15.9 MHz (63ns) |
| Expected noise | about 86 e$^-$ |

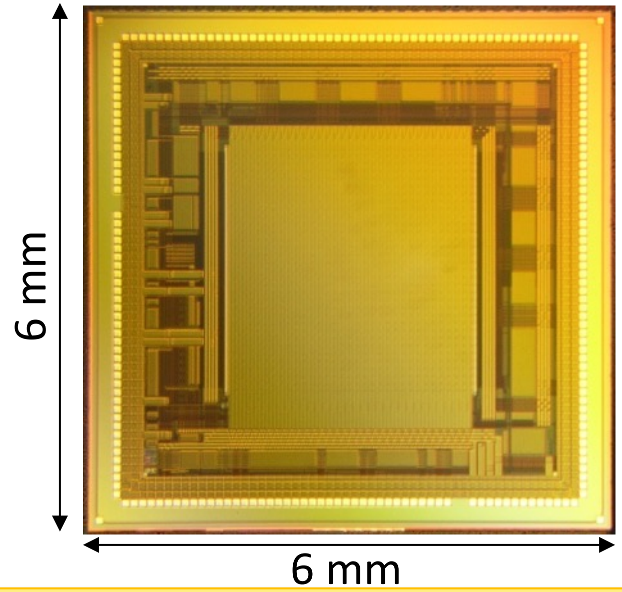
(*) chip to be thinned to 50um in future

- **Circuits already fabricated**
  - Modified ALPIDE (low power) analog circuit
  - Basic in-pixel digital circuit
- **Circuits still to be fabricated**
  - Sophisticated pixel scanning circuit

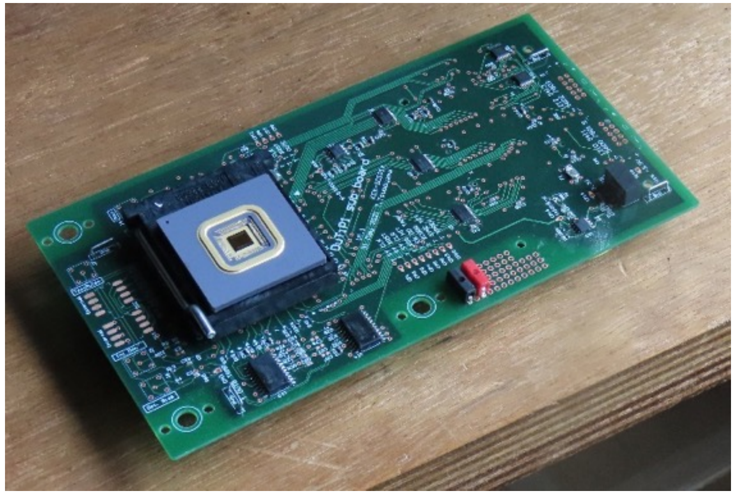
Pixel layout




DuTiP 1st prototype




## Sensor evaluation board



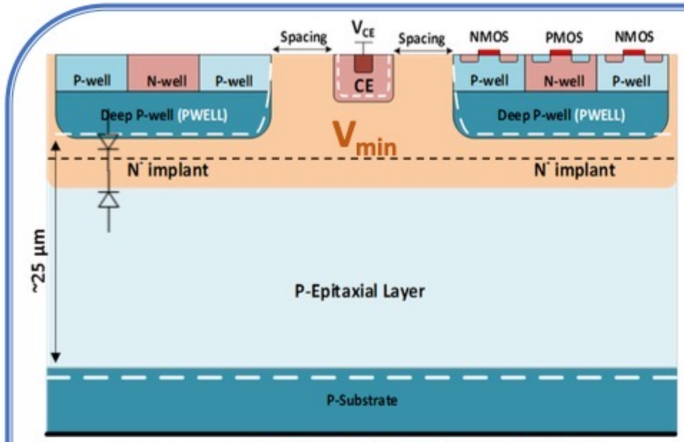
Prototype performance evaluation on-going
- digital part working as expected

Beam test to be performed

## DuTiP 2nd prototype plan

Plan to submit by the end of 2021 (depends on MPW schedule)
- Full functionality
- Semi-final chip size

# Upgrade R&D (3): CMOS pixel sensors




W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

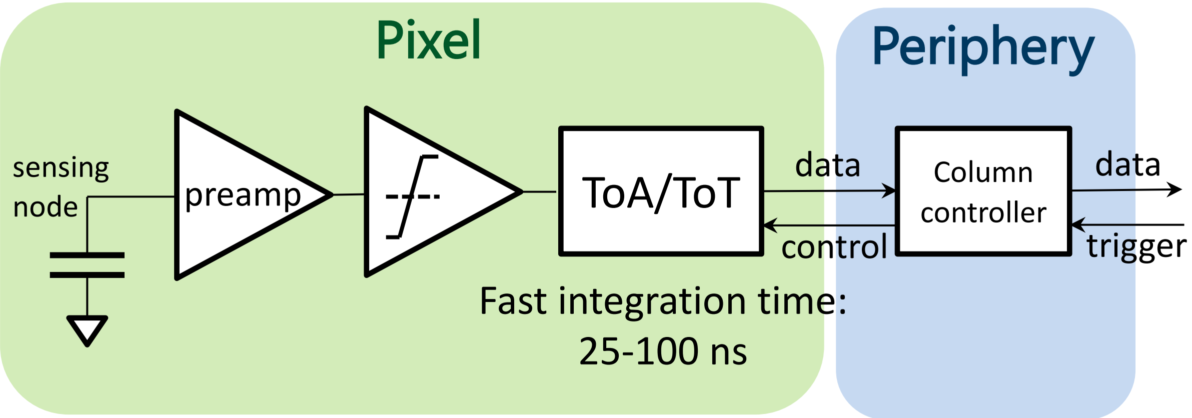
$C_d \leq 3fF$

$P \approx \frac{S}{N} \approx \frac{Q}{C_d}$

## DMAPS in TJ 180 nm: Concept

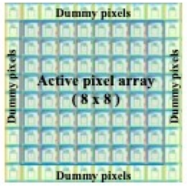
- Small sensor capacitance (Cd)
  - Key for low power/low noise
- Radiation tolerance challenges
  - Modified process
  - Small pixel size
- Design challenges
  - Compact, low power FE
  - Compact, efficient R/O

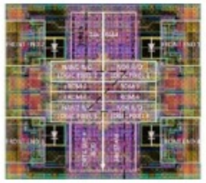
## TJ-Monopix readout scheme

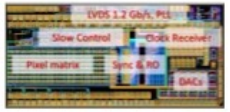


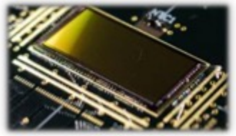

We are here now

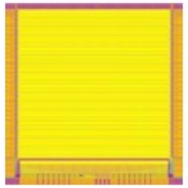
| TJ-Investigator characterization | TJ-Monopix1 & MALTA Design | TJ-Monopix1 & MALTA Submission | Mini-MALTA sub. with process fixes | TJ-Monopix1 resub. process fixes & Cz | TJ-Monopix2 & MALTA2 Design | TJ-Monopix2 & MALTA2 Submission | TJ-Monopix2 Characterization | "OBELIX" Design |
|---|---|---|---|---|---|---|---|---|
| Q2 2016 | Q4/2016 | Q3/2017 | Q3/2018 | Q2/2019 | Q2/2019 | Q3/2020 | Present | Future plans |

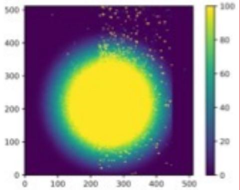








Full scale System-ready: LDO, CDR, memory etc.

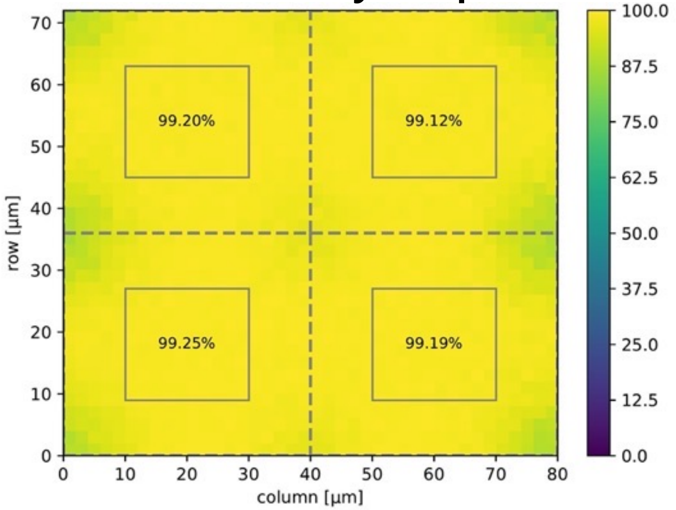
# Upgrade R&D (3): CMOS pixel sensors

## TJ-Monopix1

Characterization started in 2018

- Noise, threshold, gain, hit efficiency, and radiation hardness

### Efficiency map




300 μm Cz: 98.6% @ 490 $e^-$
(with $10^{15}$ $n_{eq}/cm^2$ irradiation)

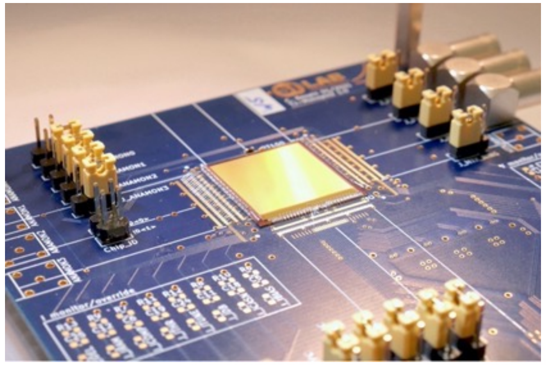
## TJ-Monopix2

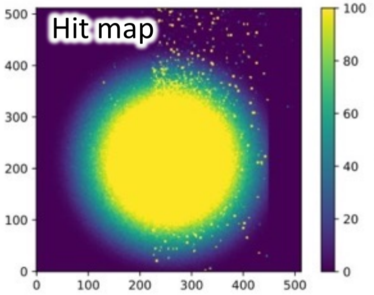
Chip size: 2x2 $cm^2$

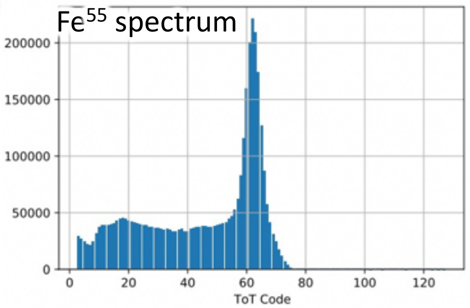
Chip is alive and working

- Synchronization, configuration, DACs
- Analog pixels respond to injection
- Chip detects radiation

Analysis of beam test data on-going






**Proof-of-principle prototype**

## Specification

| | TJ-Monopix2 |
|---|---|
| Chip Size | 2x2 $cm^2$ (512x512 pix) |
| Pixel size | 33.04 × 33.04 $\mu m^2$ |
| Total matrix power | 170 mW/$cm^2$ |
| Noise | < 8 $e^-$ (improved FE) |
| LE/TE time stamp | 7-bit |
| Threshold Dispersion | < 10 $e^-$ rms (improved FE + tuning) |
| Minimum threshold | < 200 $e^-$ |
| In-time threshold | < 250 - 300 $e^-$ |
| Efficiency at $10^{15}$ $n_{eq}/cm^2$, 30 μm epi | > 97 % |
| Efficiency at $10^{15}$ $n_{eq}/cm^2$, Cz | > 99 % |

(red) Expectations

# Summary and Outlook

## Present Vertex Detector in Belle II

- **Belle II VXD consists of PXD and SVD, and they are working well since 2019**
  - PXD: DEPFET pixel sensor
  - SVD: DSSD strip sensor
- **Excellent performance of VXD confirmed**

## Future Vertex Detector in Belle II

- **Upgrade of Belle II VXD is desirable**
- **Several technology R&D on-going to assess the performance and integration feasibility**
  - Thin DSSD sensor
  - Upgraded DEPFET pixel sensor
  - SOI pixel sensor
  - CMOS pixel sensor
- **Steady progress: prototype delivered and performance evaluation started**

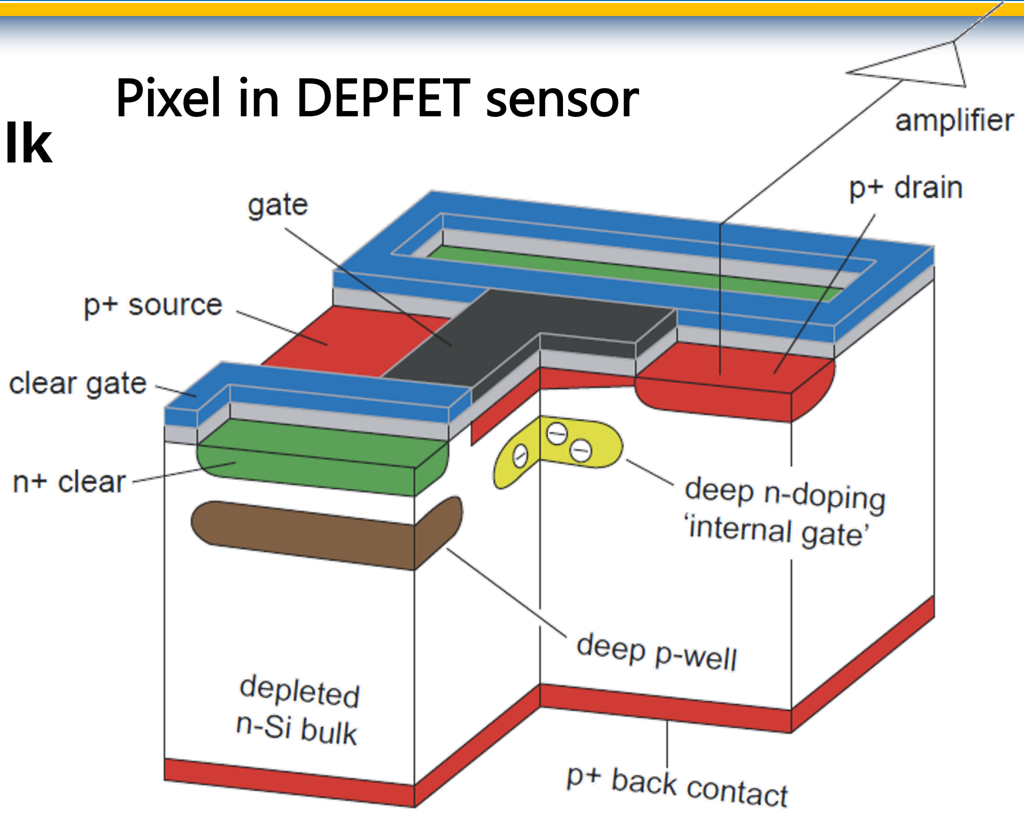
# Thank you for your attention

# backup

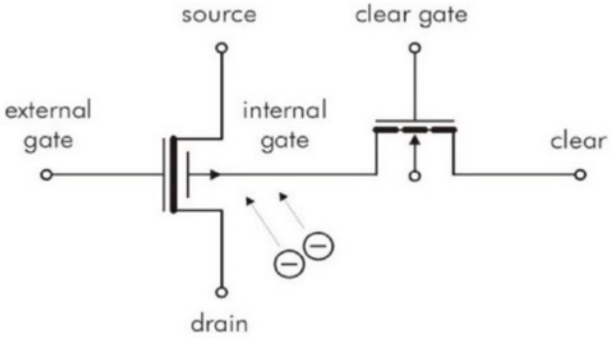
# PXD: DEPFET Sensor

- **Depleted P-channel Field Effect Transistor (DEPFET) on top of fully depleted silicon bulk**
  - Fast charge collection O(10ns)
  - Low power consumption
  - High signal-to-noise ratio
  - Thin sensors: 75μm in active region
- **Working principle**
  - Collecting charges in the "internal gate"
  - Drain current modulated by collected charges
  - Gate must be cleared after readout
- **Internal amplification gain:**
  - $g_q = \frac{\partial I}{\partial q} \approx 500$ pA/$e^-$
- **Sensor specification**
  - Self-supporting 75 μm thickness in active area
  - Pixel size: 50×(55-85) $\mu m^2$
  - 250×768 pixels per sensor

Pixel in DEPFET sensor

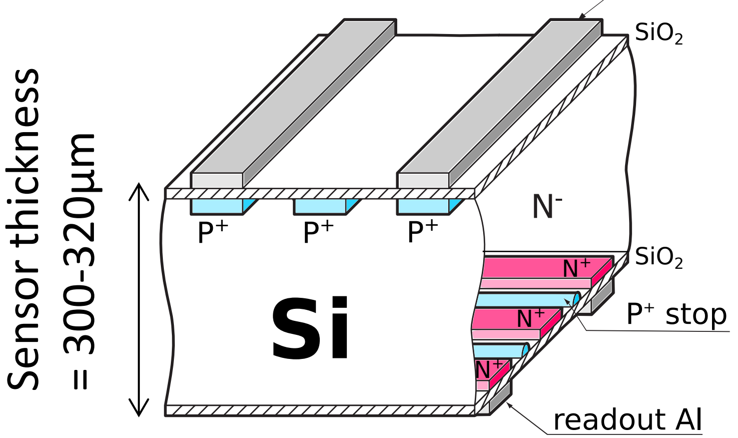



Equivalent circuit



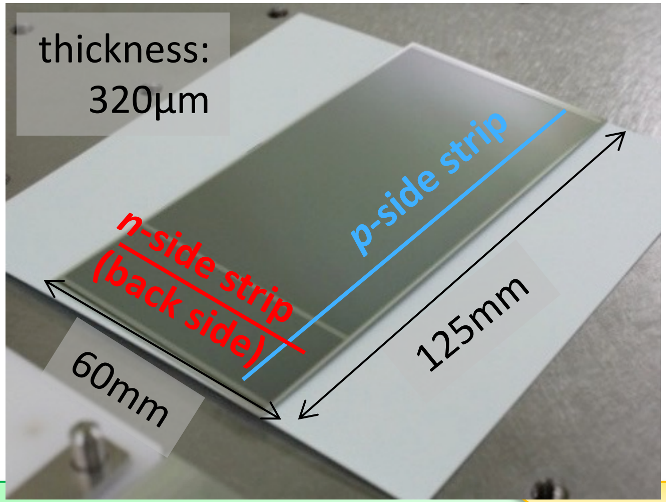
# SVD: Double-side Silicon Strip Detector

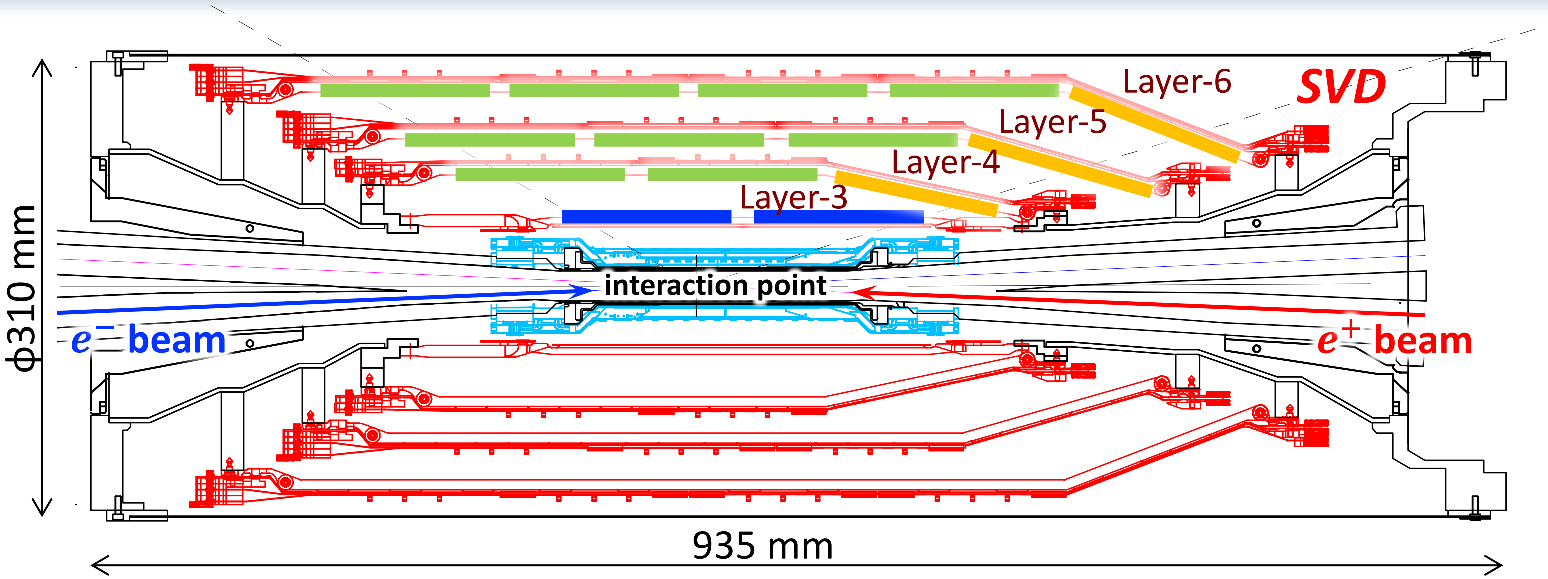
## *DSSD sensor*




AC-coupled strips on N-type substrate
Full depletion voltage: 20-60V
Operation voltage: 100V

### *Large Rectangular sensor*




## *SVD DSSD sensors*

| | Small sensors | Large sensors | Trapezoidal sensors |
|---|---|---|---|
| Readout strips *P*-side | 768 | 768 | 768 |
| Readout strips *N*-side | 768 | 512 | 512 |
| Readout pitch *P*-side (rϕ) | 50 $\mu$m | 75 $\mu$m | 50 – 75 $\mu$m |
| Readout pitch *N*-side (Z) | 160 $\mu$m | 240 $\mu$m | 240 $\mu$m |
| Sensor thickness | 320 $\mu$m | 320 $\mu$m | 300 $\mu$m |
| Manufacturer | Hamamatsu | Hamamatsu | Micron |

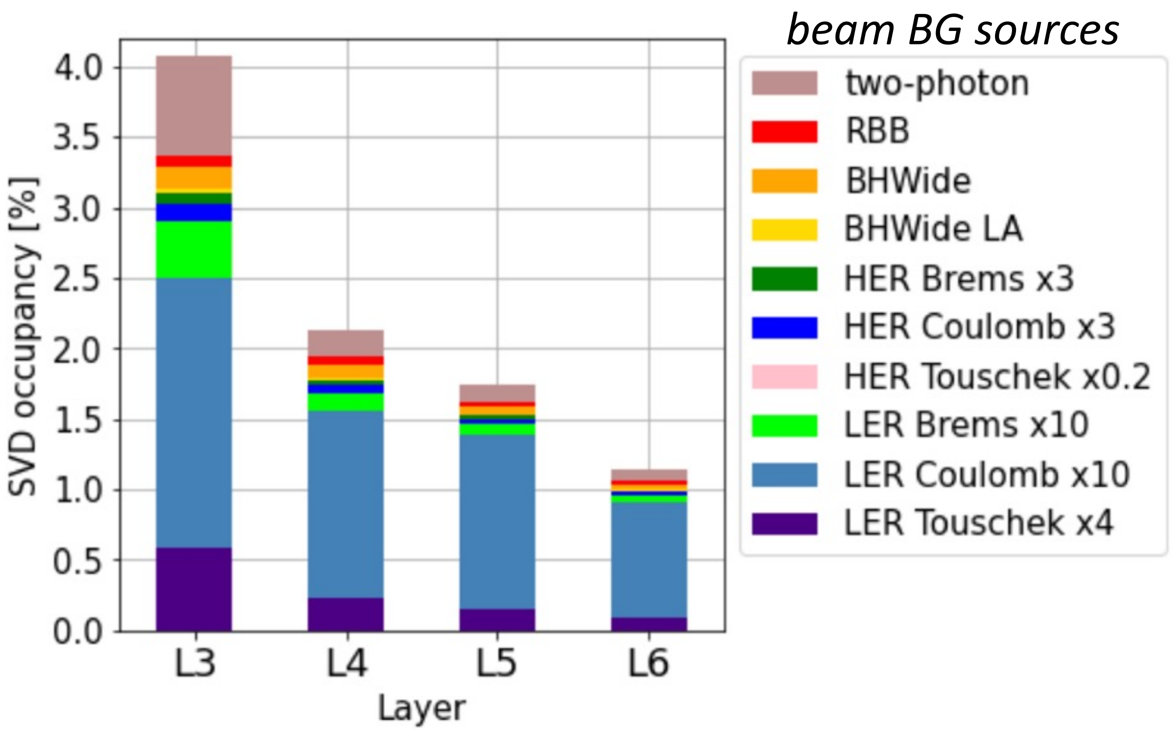
one intermediate floating strip between two readout strips

**In total: 172 sensors, 1.2m$^2$ sensor area, and 224k readout strips**

# Beam Background and SVD Hit Occupancy

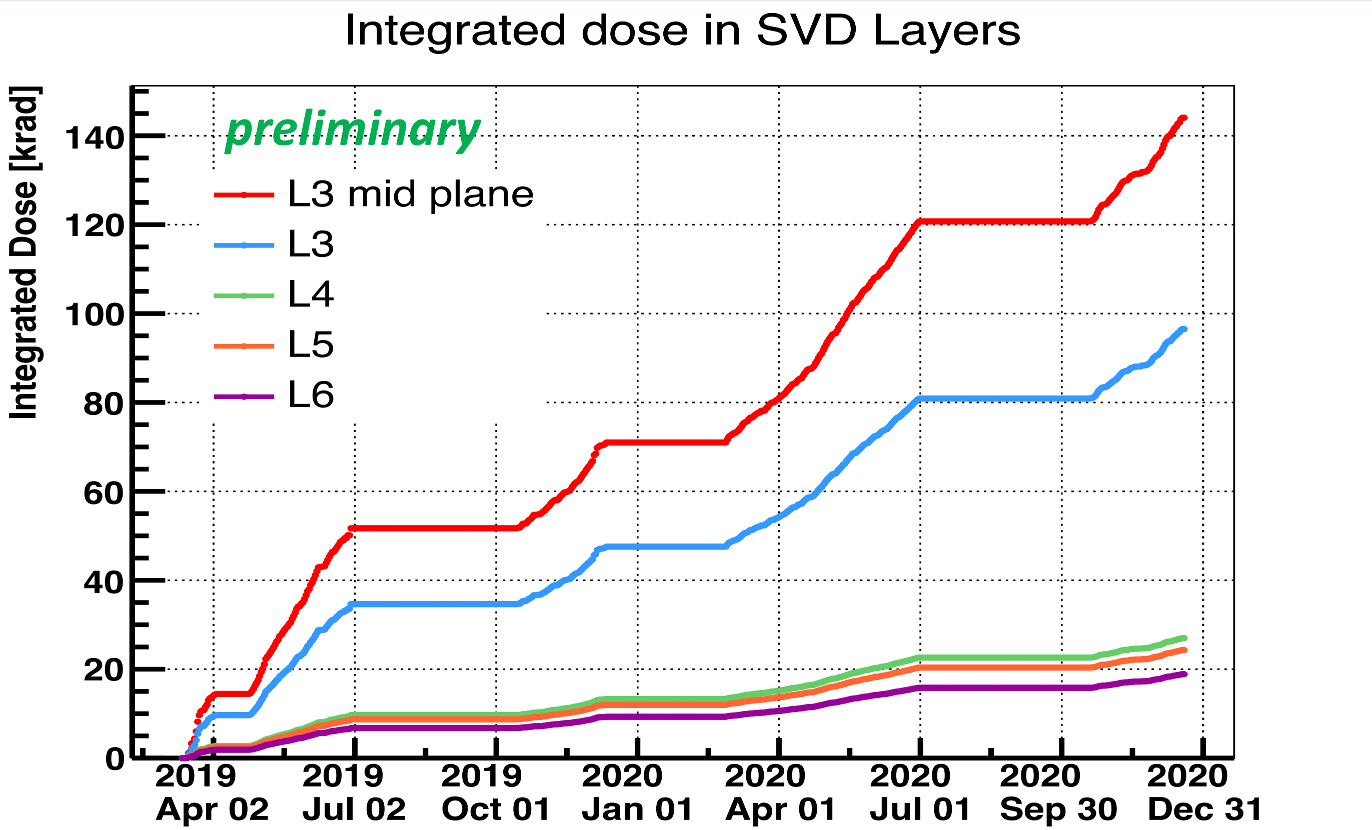
- **Beam BG and SVD hit occupancy**
  - Beam BG irradiating SVD increases hit occupancy
  - Large hit occupancy degrades SVD tracking performance. Present limit is 2-3% in layer-3.
  - With future BG rejection based on hit-timing cut, this limit can be relaxed by a factor of about 2.
- **Beam BG level during operation under control at present**
  - Averaged hit occupancy in layer-3 is < 0.5%
    - Very few exceptions with bad beam-injection BG which cannot be vetoed properly.
- **Projection of hit occupancy at L = 8.0 x $10^{35}$ $cm^{-2}s^{-1}$ is about 4% in layer-3.**
  - estimated by MC scaled with data/MC ratio
  - Corresponding to dose of ~300 krad/smy, and equiv. neutron fluence of ~$4.5 \times 10^{11}$ $n_{eq}/cm^2/smy$
    - smy: snow-mass-year = $10^7$ sec

SVD beam BG projection at L = 8.0 x $10^{35}$ $cm^{-2}s^{-1}$




*Effects from integrated dose on SVD are discussed in next slides.*

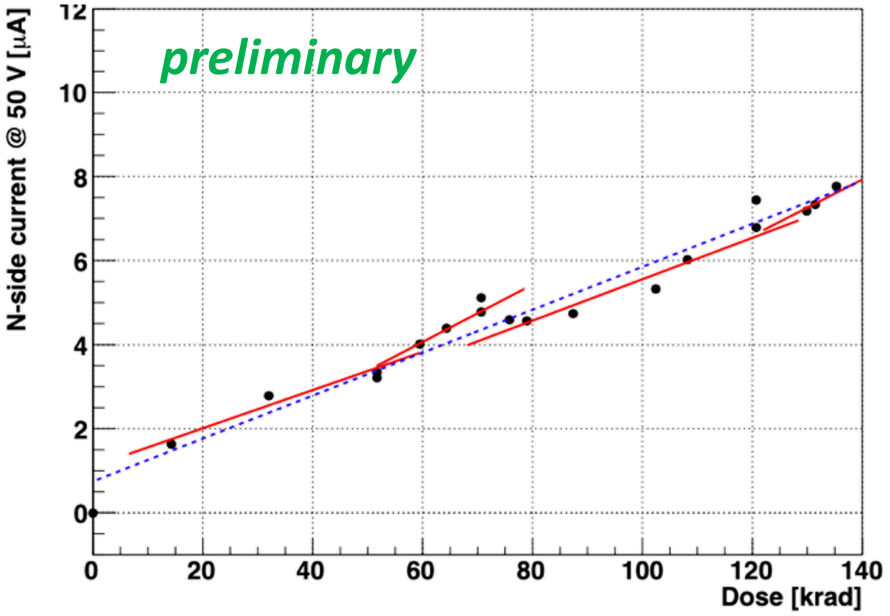
# SVD Integrated Dose



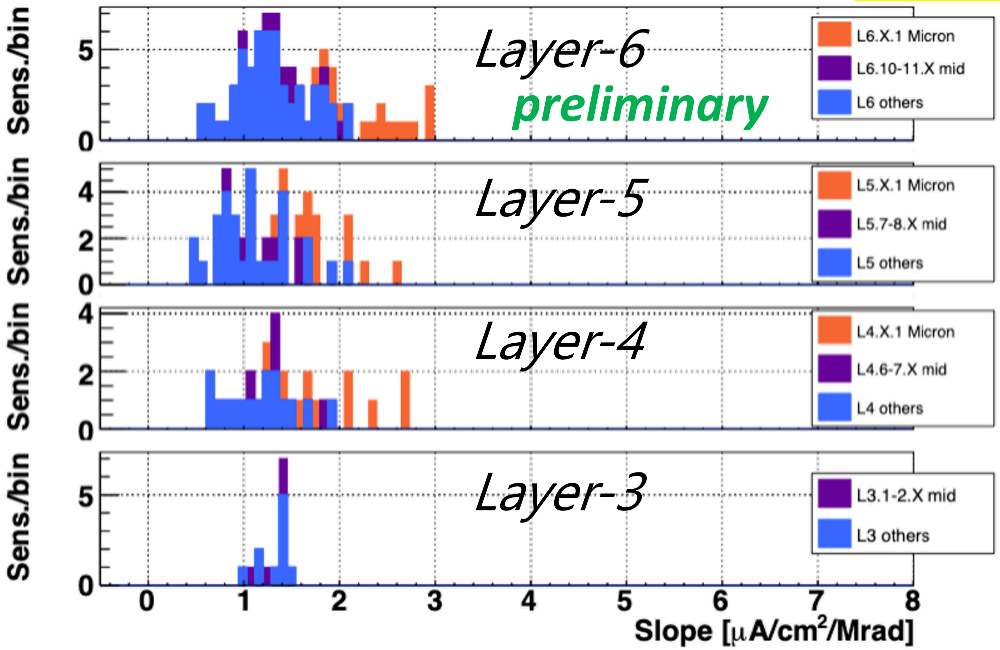

- **SVD dose estimated by dose on diamond sensors: 140krad in Layer-3 mid plane**
  - applying measured ratio between SVD and diamond doses,
  - large uncertainty: to be updated with new measurement of correlation to diamonds
- **1-MeV equivalent neutron fluence also evaluated: $2.1 \times 10^{11}$ $n_{eq}/cm^2$**
  - applying a ratio $n_{eq}$/dose obtained from MC, $1.5 \times 10^{12}$ $n_{eq}/cm^2$ / 1Mrad

# SVD Leakage Current Evolution

Leakage current vs. Dose (Layer-3 mid plane)




Extracted slopes in all sensors (Stacked histogram)




- **Good linear correlation between leakage current and estimated dose: nominal slope of about 1-2 μA/cm²/Mrad**
  - Results are same order of the BaBar measurement (~1 μA/cm$^2$/Mrad @ 20 ℃) *Nucl. Instrum. Meth. A* **729** (2013) 615
- **Width of the slope distributions due to temperature effects and dose spread among sensors in layer (avg. dose in layer used for all sensors)**
- **Even after 10Mrad irradiation, leakage current will not significantly affect strip noise.**
  - noise dominated by sensor capacitance because of short shaping time (50ns) in APV25

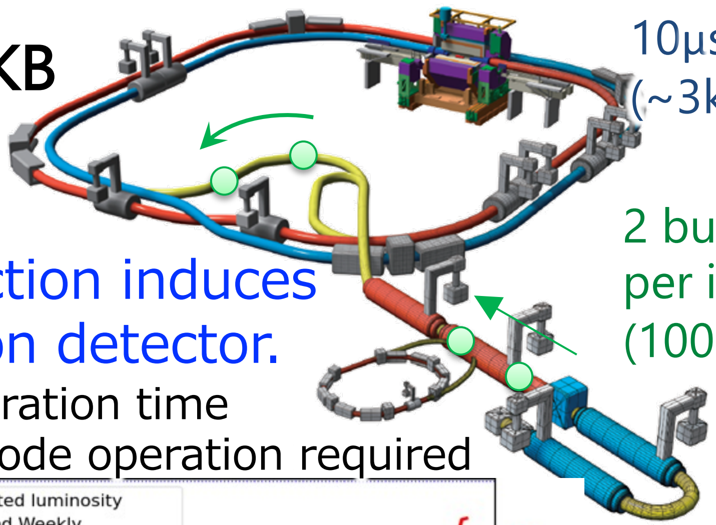
# VXD Operation in Belle II

## Successful VXD operation at present

under continuous beam injections

- to keep constant beam currents
- max.25Hz injection to each beam

SuperKEKB

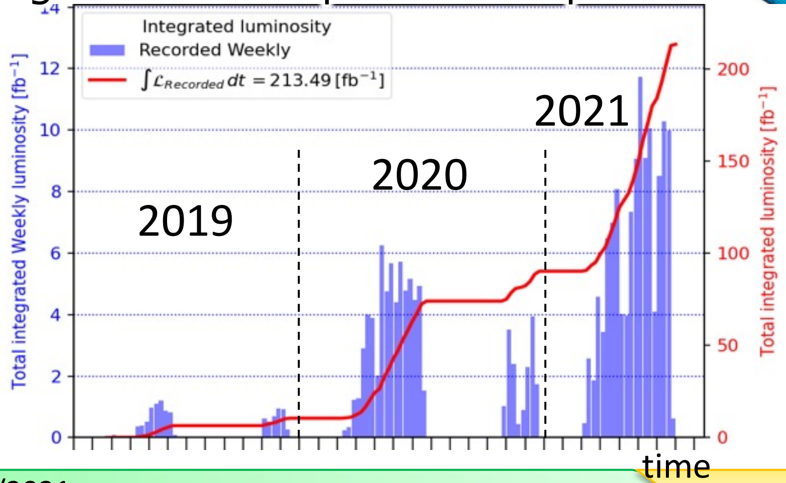


10μs revolution time (~3km circumference)

2 bunches per injection (100ns spacing)

Every injection induces beam BG on detector.

→ short integration time or gated-mode operation required

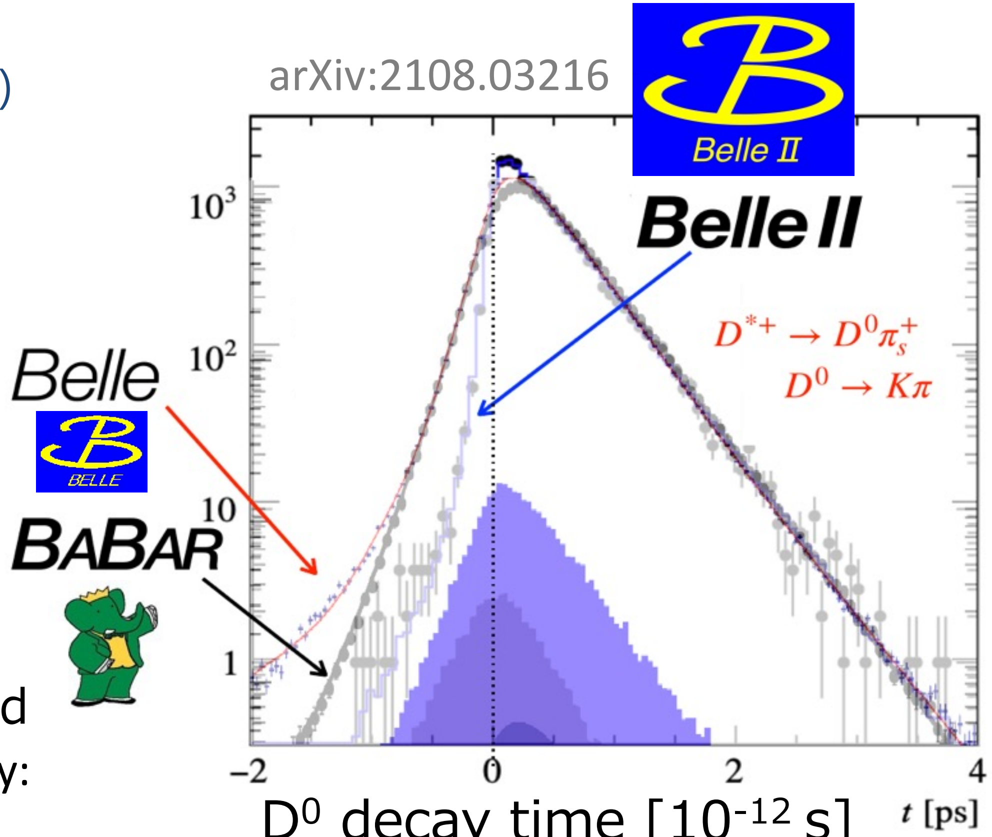



So far,
213 fb-1 accumulated
Recorded peak luminosity:
$3.12 \times 10^{34}\ cm^{-2}s^{-1}$

## Improved vertexing performance

- confirmed by D lifetime measurement
- Resulting time resolution in Belle II is better than Belle/BaBar by factor about 2

arXiv:2108.03216

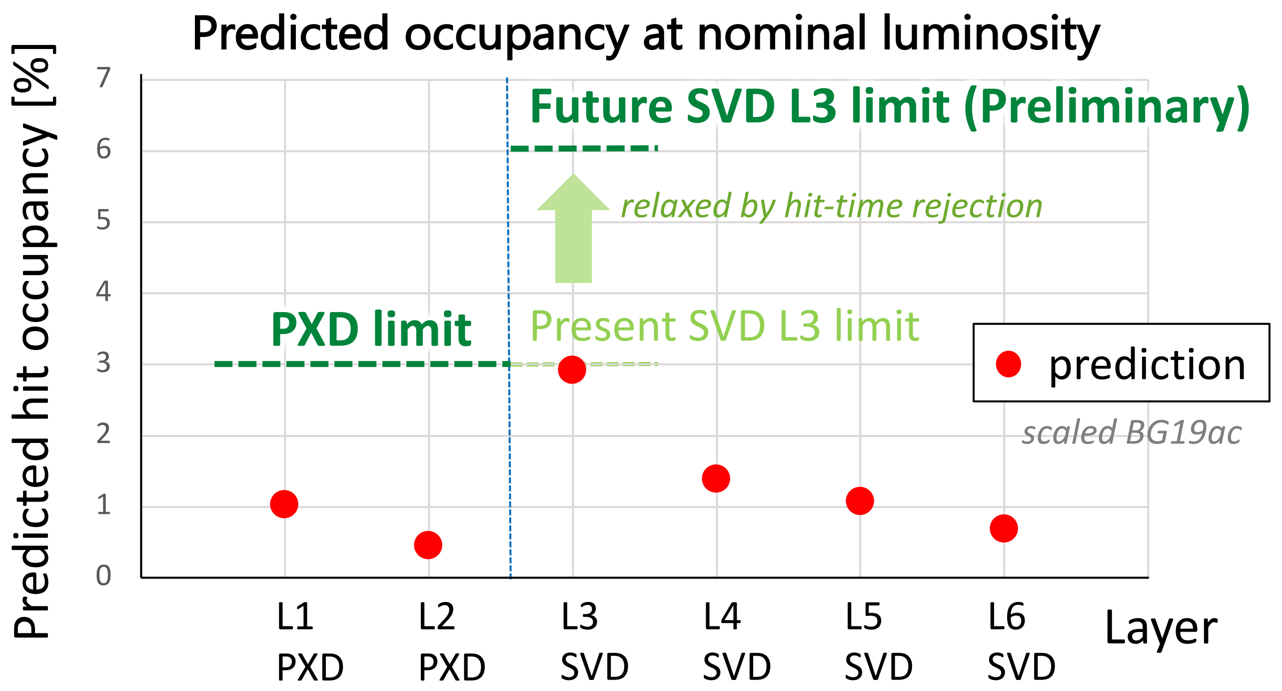



$D^0$ decay time $[10^{-12}\ s]$

World's most precise D lifetime measurements

# Limits on current VXD and VXD upgrade

## Tolerance for beam-induced background (BG)




- SVD limit will be relaxed by hit-time BG rejection ☺
- Difficulty of accurate prediction for injection BG and collimator condition at design luminosity ☹
- Drastic change in beam optics for design luminosity → large uncertainty ☹ ($\beta_y^*$ = 1.0mm → 0.3mm)

No big margin...

## Tracking and vertexing performance

- Tracking performance in low-$p_t$ limited by material budget
- Room to improve vertex resolution with better hit position resolution
- Improvement in $K_S$ vertexing desirable

## Latency of Level-1 trigger

- Belle II trigger latency is limited to 5.0μs by SVD (depth of APV25 ring-buffer)

So in summary,

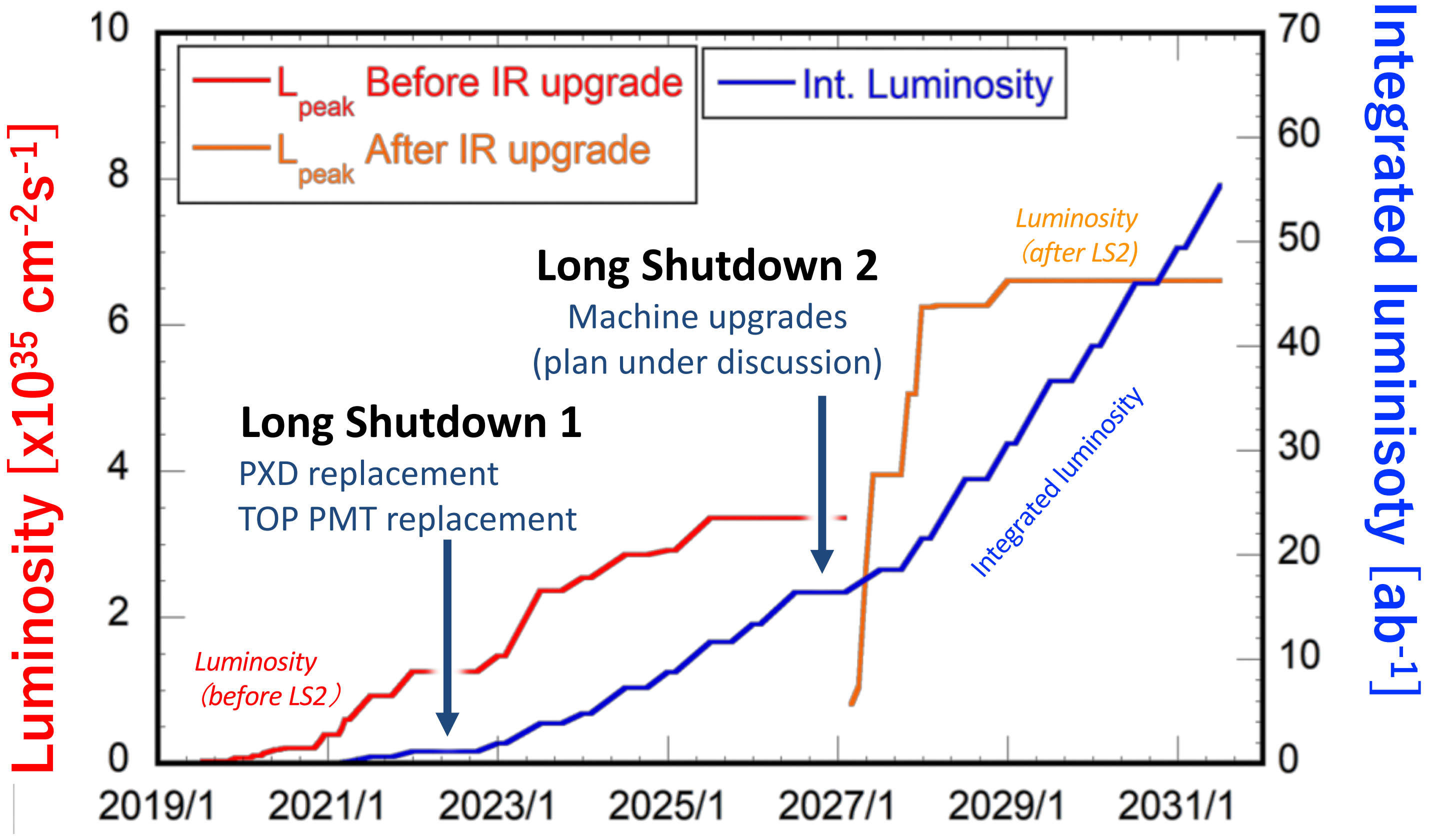
- **Predicted BG within limits, BUT without enough safety margin**
- **Also performance improvement highly desirable**

# Timescale of the VXD upgrade project

- **2nd long shutdown for SuperKEKB intermediate upgrade**
  - Timeframe expected to be 2026-2027, but still with uncertainty
    - Detailed SuperKEKB upgrade plans are under discussion with the international taskforce teams.
  - Opportunity for large upgrades of Belle II subdetectors
  - Preparation to be done in several years → Currently available technologies preferable

Target of on-going VXD upgrade project

SuperKEKB/Belle II operation projection



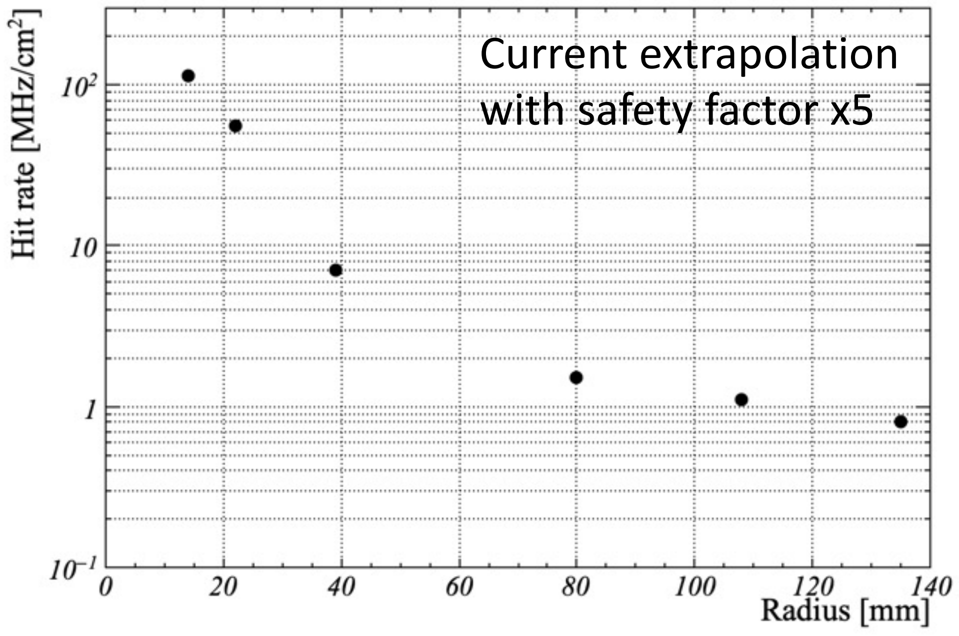
# Requirements for the VXD upgrade

## Requirements

| | |
|---|---|
| Radius range: R | 14 – 135 mm (**) |
| **Tracking & Vertexing performance** at least as good as current VXD | |
| Single point resolution(*) | < 15 um |
| Total material budget | < (2x 0.2% + 4x 0.7%) $X_0$ |
| **Robustness against radiation environment** current extrapolation with safety factor x5 | |
| Hit rate(*) | ~ 120 MHz/$cm^2$ |
| Total Ionizing Dose(*) | ~ 10 Mrad/year |
| NIEL fluence(*) | ~ $5.0 \times 10^{13}$ $n_{eq}/cm^2$/year |

(*) requirement for the innermost layer (R=14mm)
(**) Optionally, we may include also the CDC inner region (135<R<240mm)

## Required hit rate tolerance vs. Radius




## Possible other improvements by upgrade

- Impact parameter resolution
- Tracking performance for low-$p_T$ tracks
- Longer trigger latency
- Capability of Level-1 trigger creation

# Strategy of upgrade R&D

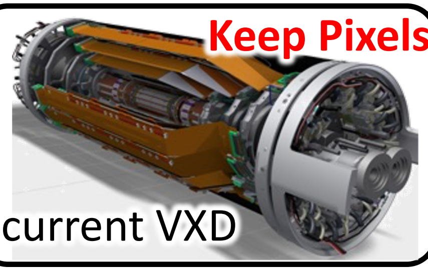
- **Several technology options under investigation by R&D subgroups**
- R&D activities will access the options
  - Which concepts bring best performance?
  - Which technology fit requirements?
  - Which technology fit timeframe of installation?
- CDR to be prepared within ~1 year w/ full-scale prototype test and physics benchmarking
  - and then TDR (w/ full technical description) as well

**Several technology R&D subgroups**

- Thin DSSD sensor
- DEPFET pixel sensor
- SOI pixel sensor
- CMOS pixel sensor

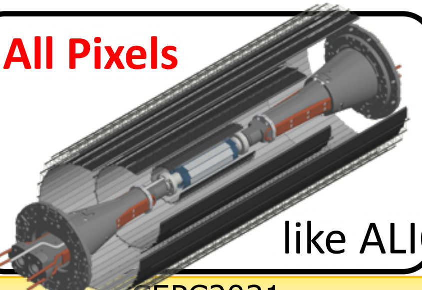
**Detector concept**

Keep Pixels+Strips



like current VXD

All Pixels



like ALICE ITS2 concept

**Performance evaluation**

**Common analysis framework**
w/ different geometries and digitizers
- For systematic performance study of multiple options
- For less development cost and resources

*under preparation*

# R&D subgroup (1): Thin DSSD sensor

## Thin/fine-pitch SVD (TFP-SVD) concept

### Targets

- Outer layers
- Handle higher hit-rate
  - O(1MHz/cm$^2$) R>4cm
- Improve tracking/$K_S$ vertexing performance

### Thin DSSD sensor

**Thinner sensor**: 140um

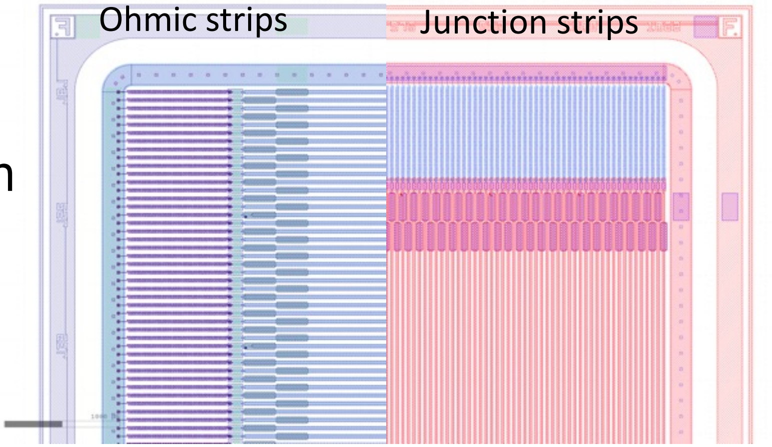
- Produced by Micron

**Finer N-side strip pitches** than SVD: ~85um

→ R&D challenges in front-end

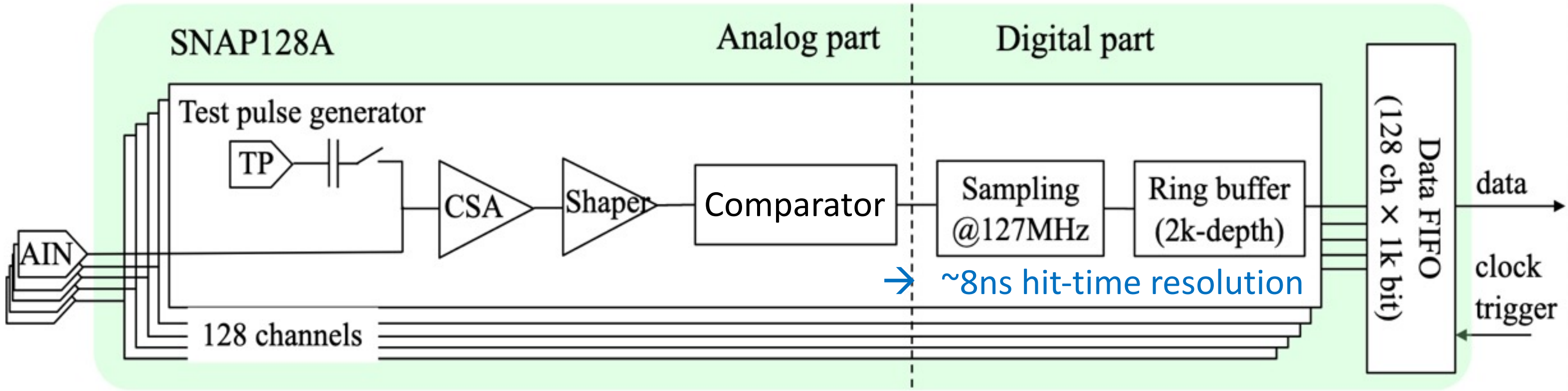
- Noise (smaller signal)
- Heat dissipation (larger # of channels)

TFP-SVD DSSD layout




## Dedicated front-end ASIC (SNAP128A)

- 180nm CMOS process by Silterra
- Short signal pulse width: ~55ns (simulation)
- Better noise characteristic and less power consumption than SVD
  - simulated noise: ~640e$^-$ @ $C_{det}$=12pF
- Binary hit readout
  - to reduce cables



# R&D subgroup (1): Thin DSSD sensor

## DSSD 1st prototype

- Three prototype sensors delivered

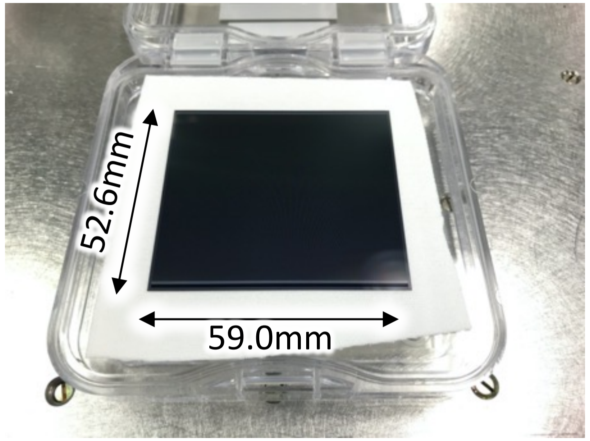
Basic characterization in Micron

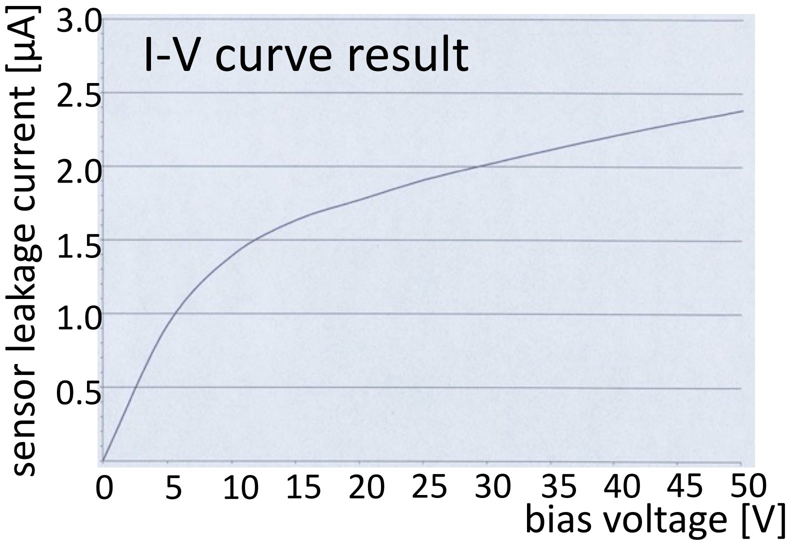
- Reasonable I-V and C-V results
- Thickness: 148±5um
- Full depletion voltage: 14±1 V

Specification of prototype ver.1

| | |
|---|---|
| Sensor dimension | 52.6 mm x 59.0 mm (rectangle) |
| Active area | 51.2 mm x 57.6 mm |
| Sensor thickness | 140 um ± 10um |
| Junction (P-side) strip | |
| P-side strip pitch | 50 um |
| P-side strip width | 14 um |
| P-side # of strips | 1024 |
| P-side floating string | no floating strip |
| Ohmic (N-side) strip | |
| N-side strip pitch | 75 um |
| N-side strip width | 14 um |
| N-side # of strips | 768 |
| N-side floating string | no floating strip |

DSSD prototype

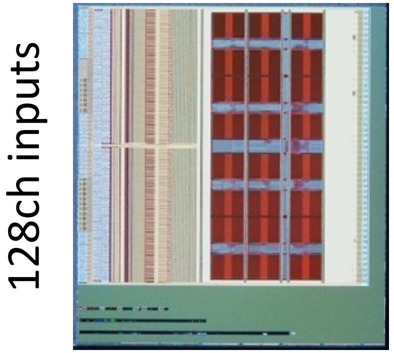



## SNAP128A: 1st prototype

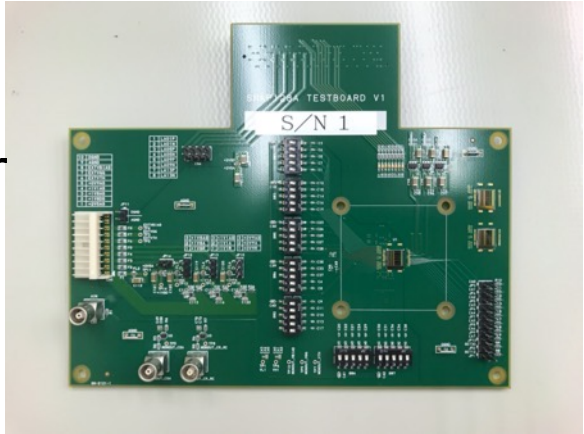
- All necessary functions both analog and digital integrated
- Being tested in KEK
  - Amp/shaping part and digital part working
  - Reasonable power consumption: 329mW

SNAP128A



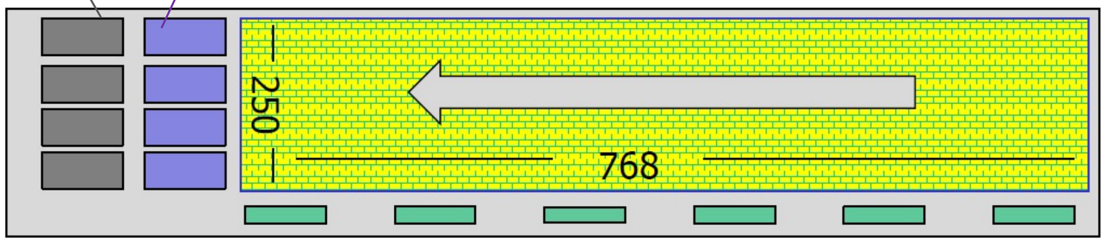

- To be assembled with DSSD to evaluate detector performance in early 2022

SNAP128A test board



# Upgrade R&D (2): DEPFET pixel sensor

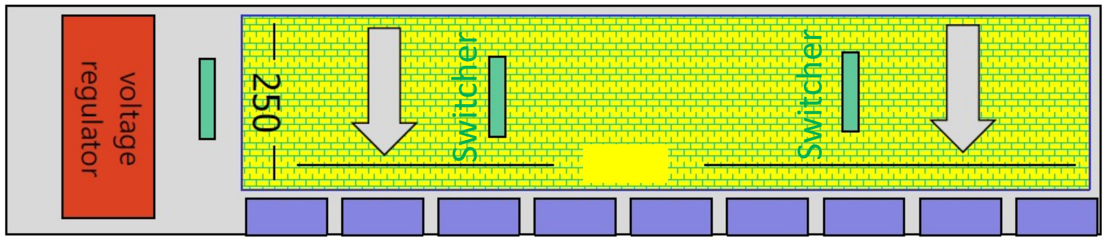
- **Current Belle II PXD**
  - First use of the technology in HEP experiment
  - Current integration time: 20 μs




- **Sensor R&D**
  - Gain increase with shorter FET length L
    - higher amplification in pixel → thinner oxide → improved radiation tolerance
  - Extend Cu interconnection layer into pixel array
    - improve the signal integrity of fast signals (e.g. "clear" and "gate")

$$g = \frac{dI_{drain}}{dQ} \propto \sqrt{\frac{t_{ox}}{L^3}}$$

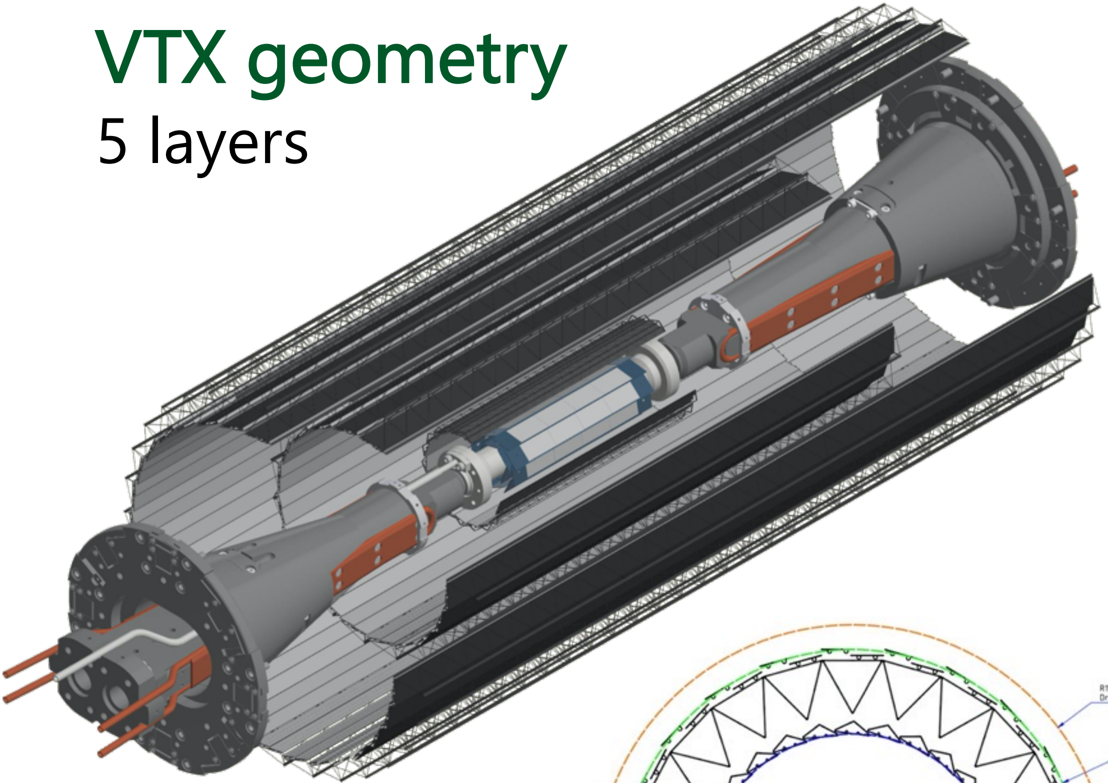
- **ASIC R&D**
  - Faster driving and readout circuit
    - Integration speed x2
- **More aggressive option**
  - Rotate readout direction of pixel array by 90°
    - Additional improve on integration speed x3

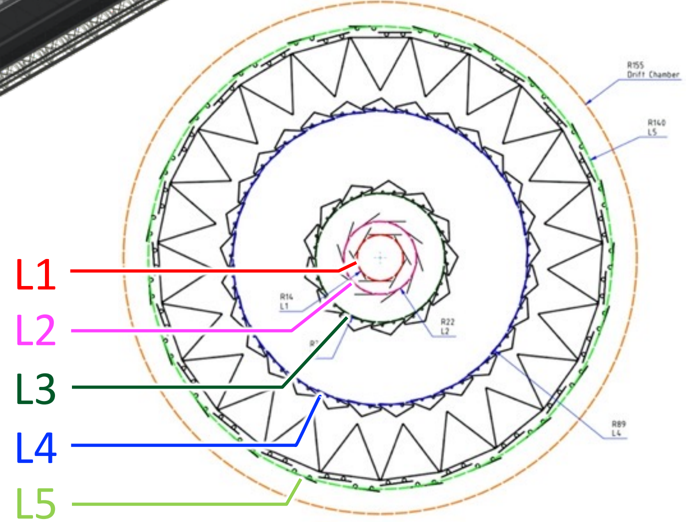


# VTX: An integrated design for fully pixelated option

## VTX geometry

5 layers

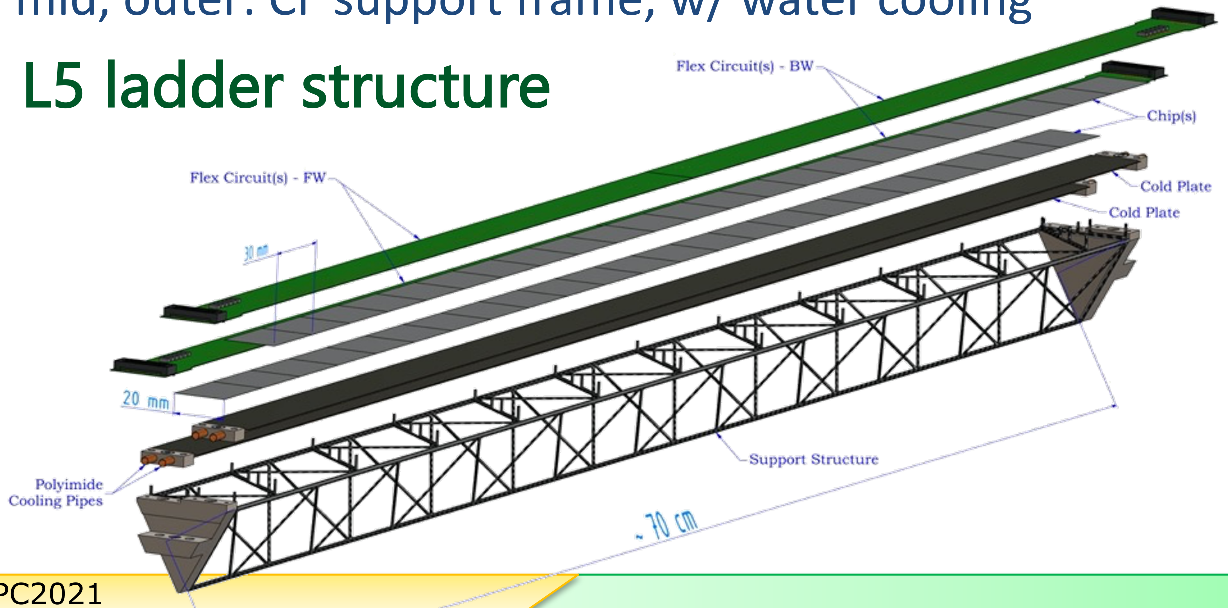





## General concept of VTX

- **Fully pixelated detector with CMOS sensors**
  - Chip size: 2x3 cm$^2$ (same chip in all layers)
- **Low material budget:**
  - sensor thickness ~50 µm
  - 0.1%$X_0$ (L1-2) / 0.3%$X_0$ (L3-4) / 0.8% $X_0$ (L5) per layer
- **Different integration among inner (L1-2), middle (L3-4), and outer (L5) layers**
  - inner: Self supportive silicon ladders, w/ air cooling
  - mid, outer: CF support frame, w/ water cooling

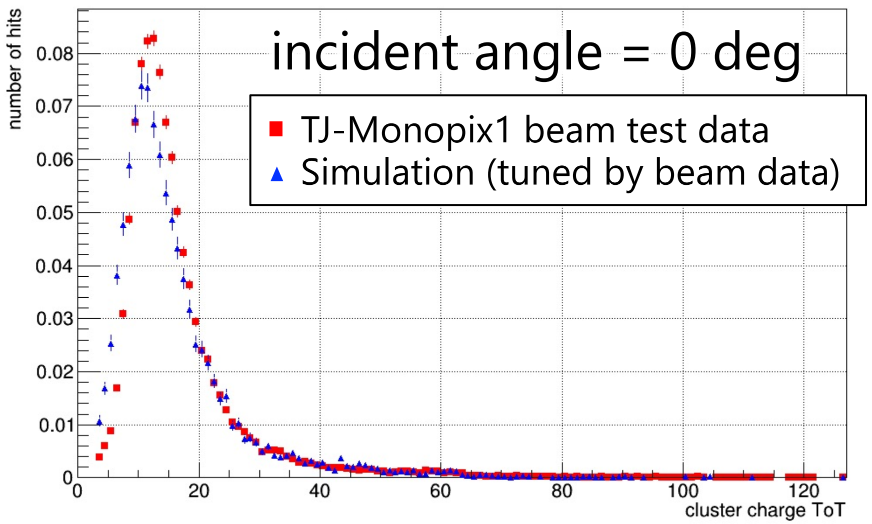
## L5 ladder structure



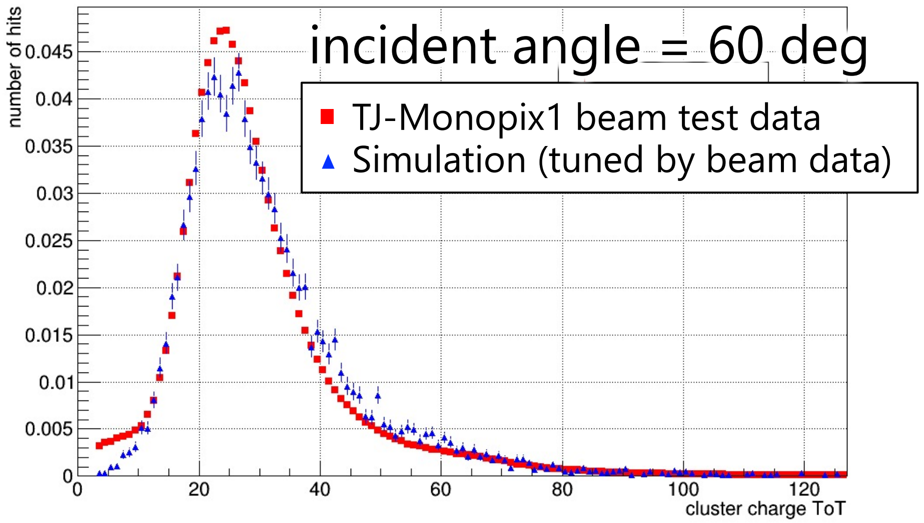
# Simulated VTX Performance

- **VTX performance simulation with Belle II analysis framework**
  - Connect to the existing outer-detector tracking
  - Realistic beam backgrounds with accurate Geant4 geometry
- **Realistic pixel sensor model implemented**
  - 30 μm depletion layer
  - 33x33 $\mu m^2$ pixels with 7-bit ToT
  - tuned with TJ-Monopix1 beam test data

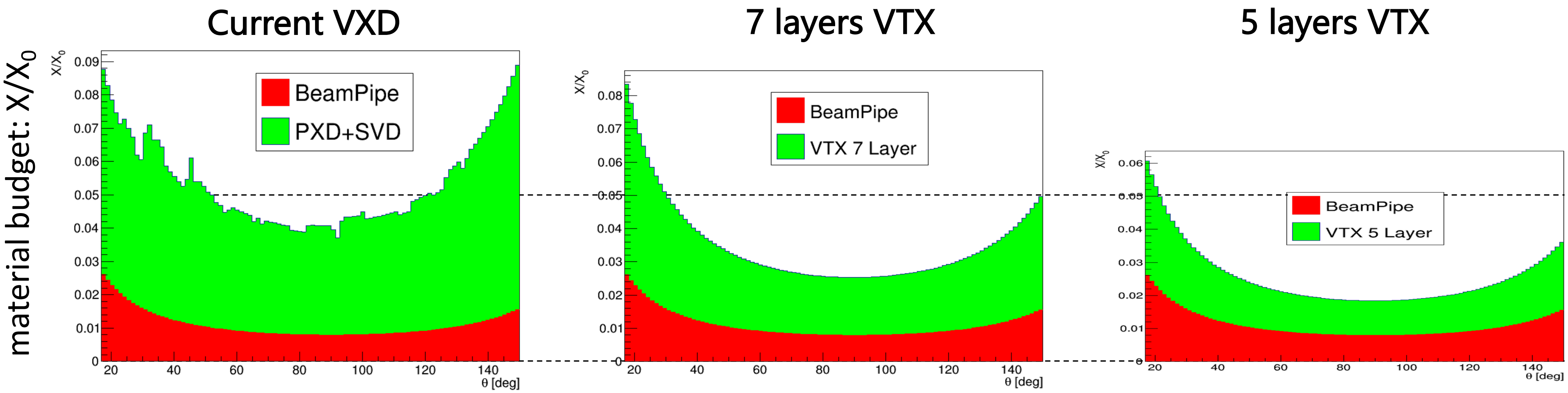
Cluster charge distribution




Cluster charge distribution



# Estimated material budget of VTX




- **Very simple detector design, but realistic material budget:**
  - 0.1% X0 (inner layers) + 0.3% X0 (outer layers)
    - 5 layers VTX: L1-2 inner + L3-5 outer, 7 layers VTX: L1-3 inner + L4-7 outer
- **Only barrel layers (no disk sensors in forward)**