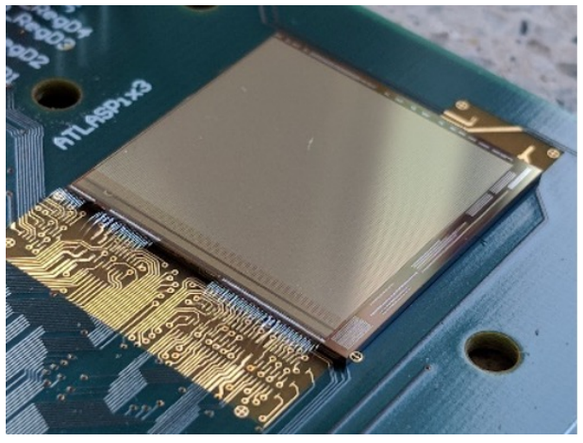
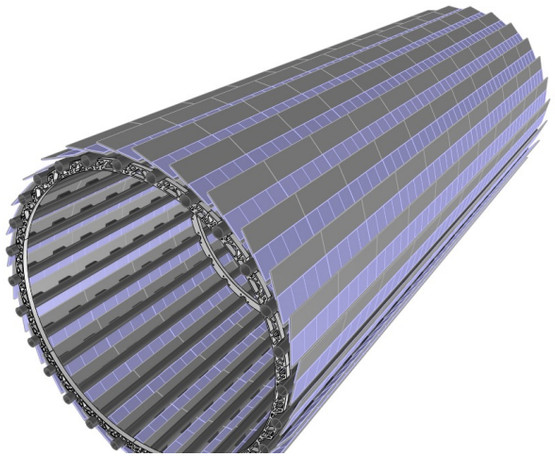




Update on HVCMOS based silicon tracker R&D

Yanyan Gao (University of Edinburgh)

On behalf of the CEPC silicon tracker community

The 2021 International Workshop on the High Energy Circular Electron Positron Collider

8-November-2021

Introduction - tracker layout and requirements

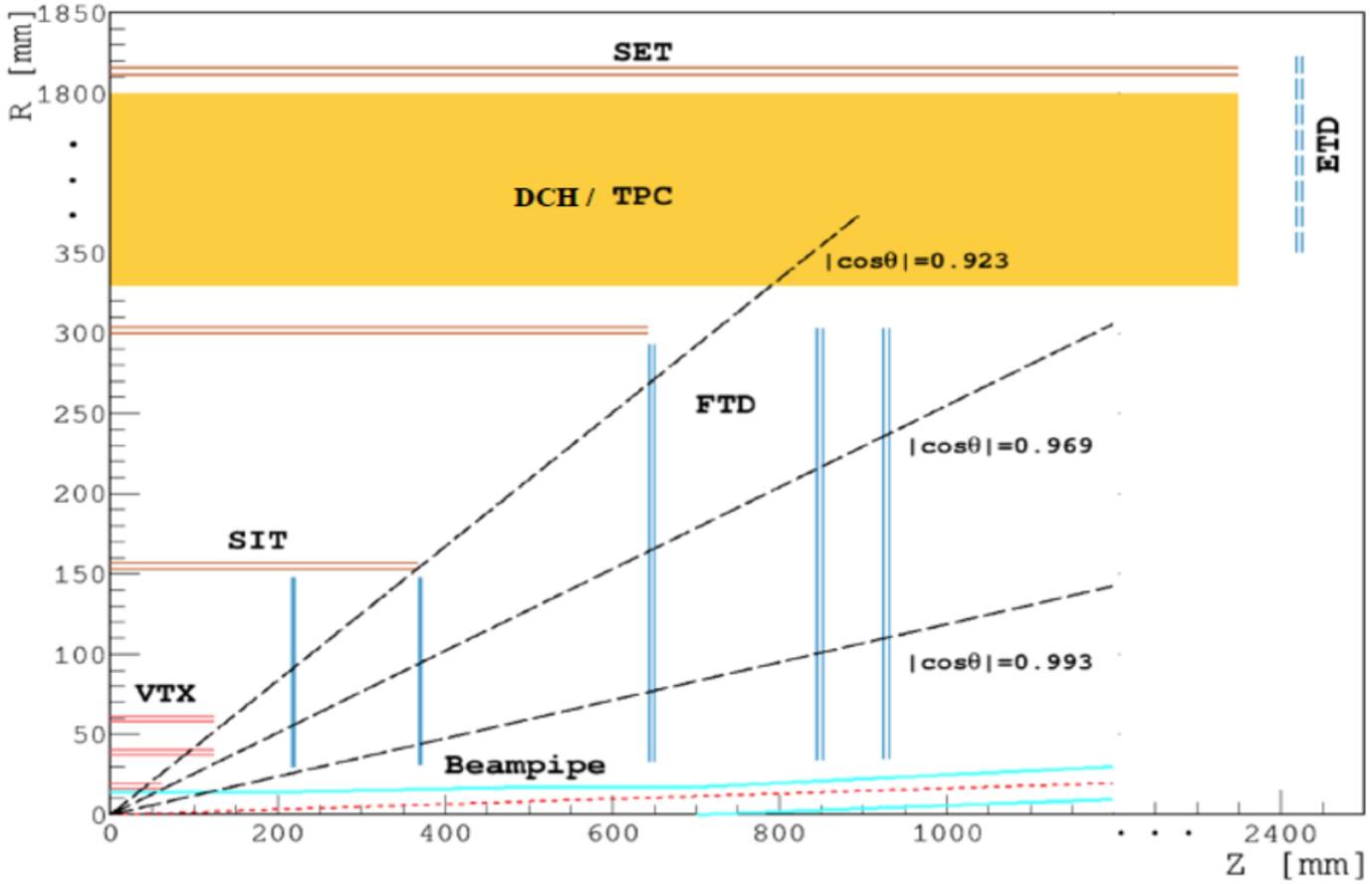
Physics | Lancaster University

CEPC tracker designs: TPC or DCH + Si

Baseline tracker design: TPC

and 3 layers / 5 disks of silicon sensors,

50 m² (33 w/o ETD) if built in CMOS pixels (strips default)



Detector		Radius R [mm]		$\pm z$ [mm]	Material budget [X_0]
SIT	Layer 1	153		371.3	0.65%
	Layer 2	300		664.9	0.65%
SET	Layer 3	1811		2350	0.65%
		R_{in}	R_{out}		
FTD	Disk 1	39	151.9	220	0.50%
	Disk 2	49.6	151.9	371.3	0.50%
	Disk 3	70.1	298.9	644.9	0.65%
	Disk 4	79.3	309	846	0.65%
	Disk 5	92.7	309	1057.5	0.65%
ETD	Disk	419.3	1822.7	2420	0.65%

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$

$\sigma_{r\phi} \approx 7\mu m$

List of institutes

- Australia
  - University of Adelaide
- China
  - Institute of High Energy Physics, CAS
  - Shang Dong University
  - Tsinghua University
  - University of Science and Technology of China
  - Northwestern Polytechnical University
  - T.D.Lee Institute-Shanghai Jiao Tong University
  - Harbin Institute of Technology
  - University of South China
- Germany
  - Karlsruhe Institut für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisae, Università di Pisa
  - INFN Sezione di Torino, Università degli Studi di Torino

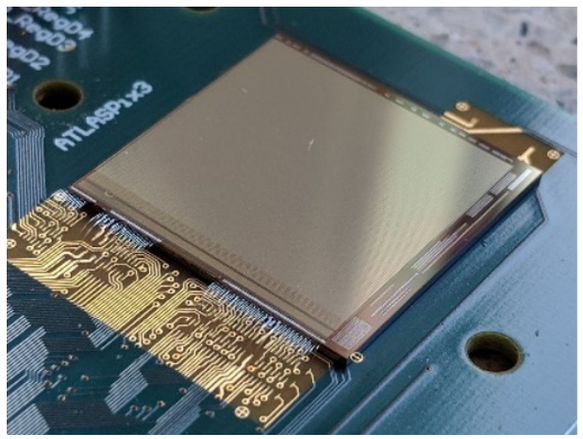
UK

- University of Bristol
- STFC-Daresbury Laboratory
- University of Edinburgh
- Lancaster University
- University of Liverpool
- Queen Mary University of London
- University of Oxford
- STFC-Rutherford Appleton Laboratory
- University of Sheffield
- University of Warwick

Convenor:
Harald Fox (Lancaster, UK)
Meng Wang (SDU, China)

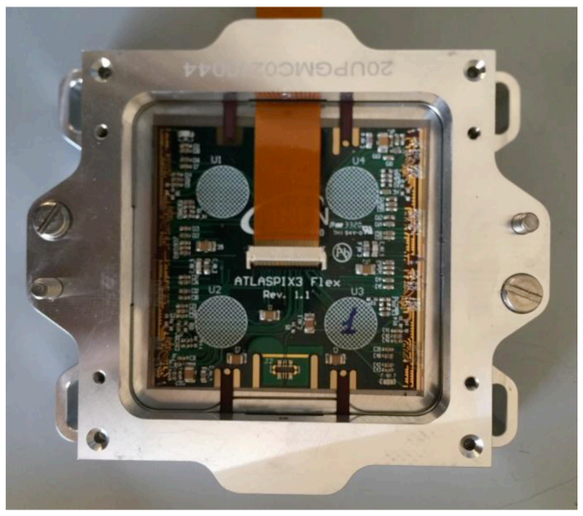
Tracker prototype overview

Single chip



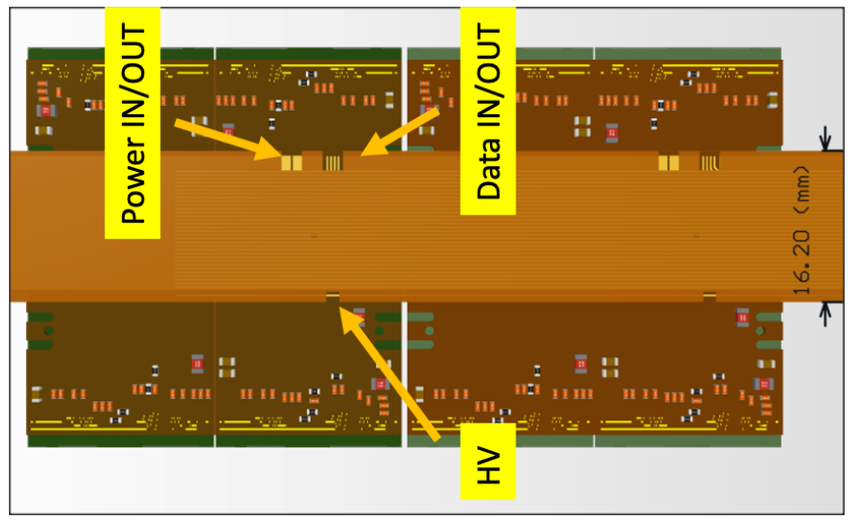
~2cm×2cm

Quad module



~4cm×4cm

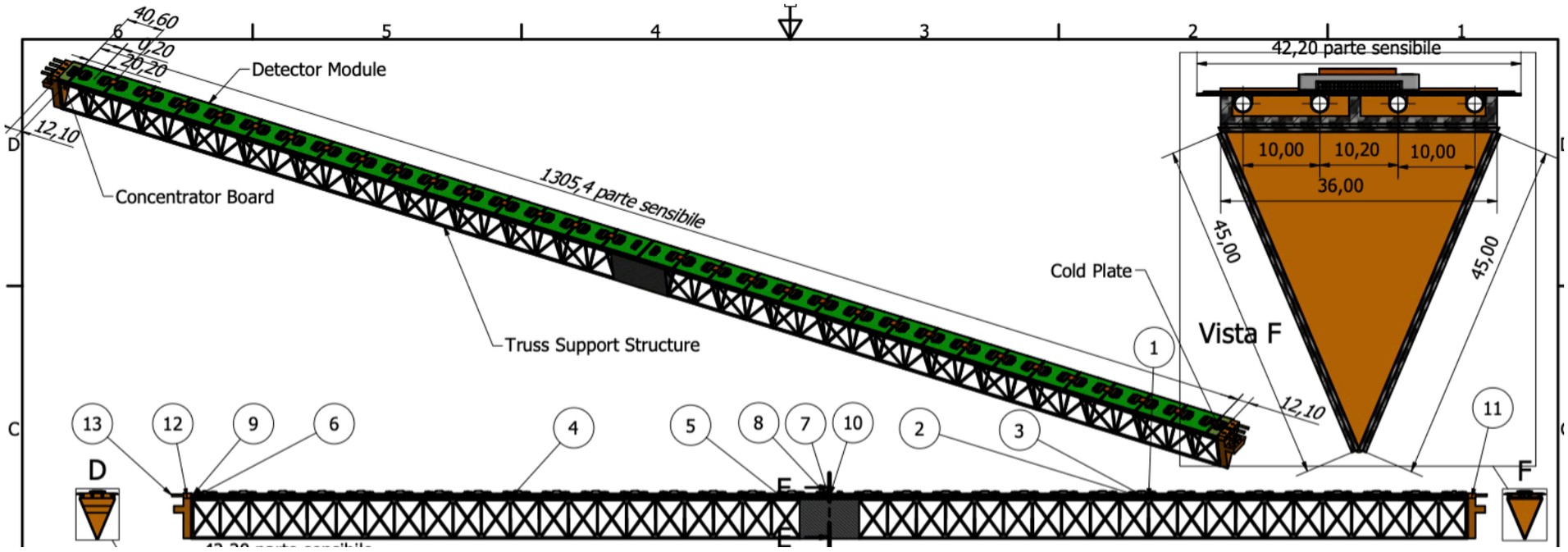
A serial powering chain (up to 16 quads)



~4cm×64cm

Long stave

~4cm×130cm

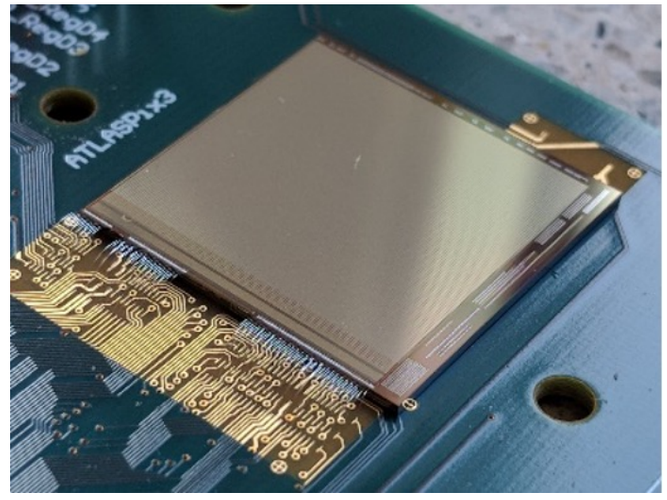


Update for today

- New ATLASPix3 measurements
- New HVCMOS designs and preliminary measurements
  - First 55nm technology with Chinese foundry HLMC
- Multi-chip, quad module, construction and first lab measurements
- Multi-module system design concepts “stave” and electrical bus
- Mechanical support structure design concepts and pre-prototyping
- Plans for the next steps

Brief reminder of ATLASPix3

- ATLASPIX3 sensor was originally developed for ATLAS, it is now used as technology demonstrator for HVCMOS, several sensors are based on ATLASPIX3 design
- Features pixels of 50µm x 150µm
- Pixels contain amplifiers and comparator with threshold tune circuit
- Chip size 2.2 cm x 2.0 cm
- Matrix size 132 x 372
- Comparator is NMOS only
- Data output 1.28 Gbit/s 64b/66b (triggered),or 1.6 Gbit/s 8b/10b (un-triggered)
- Serial powering
- Clock data recovery from command in
- Power consumption 140mW/cm²

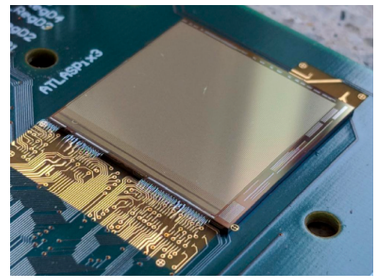


I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021
https://ieeexplore.ieee.org/document/9373986

Two versions:
1) ATLASPix3.0
2) ATLASPix3.1
- submitted in Dec 2020, delivered in Feb 2021
- selected improvements: VDDA/VDDD regulators

ATLASPix3.0 KIT-GECCO based single chip programme

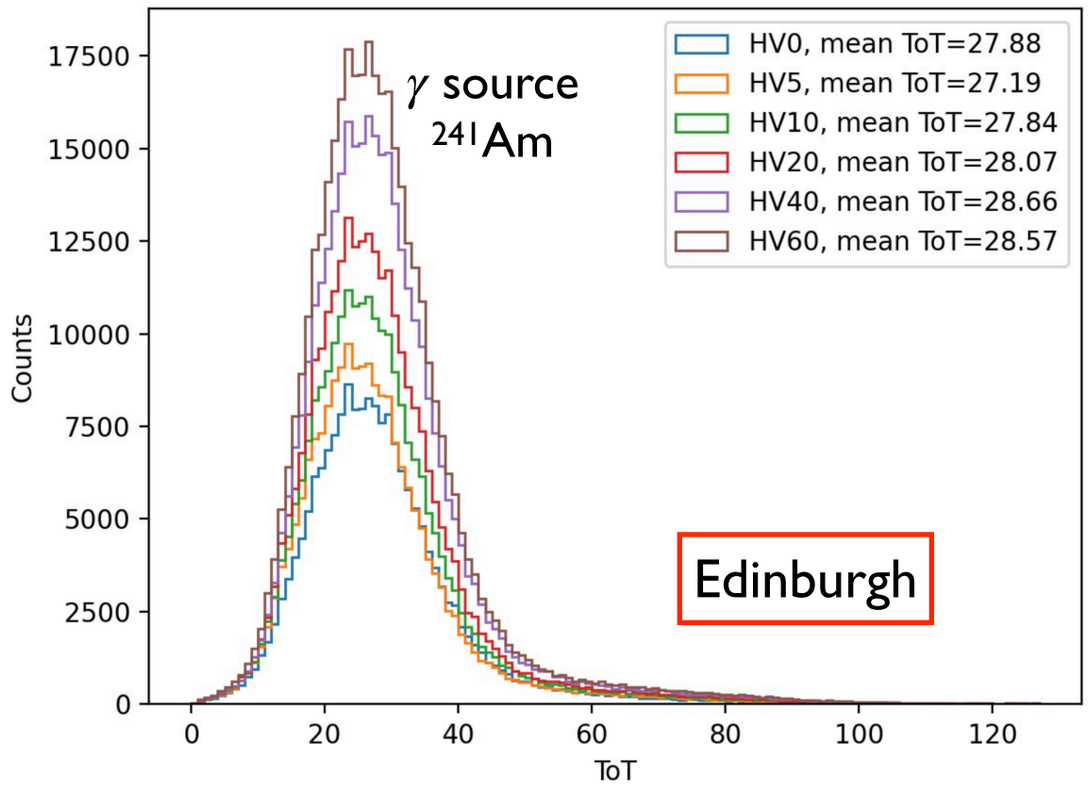
NexysVideo FPGA **GECCO board** **Single chip carrier**

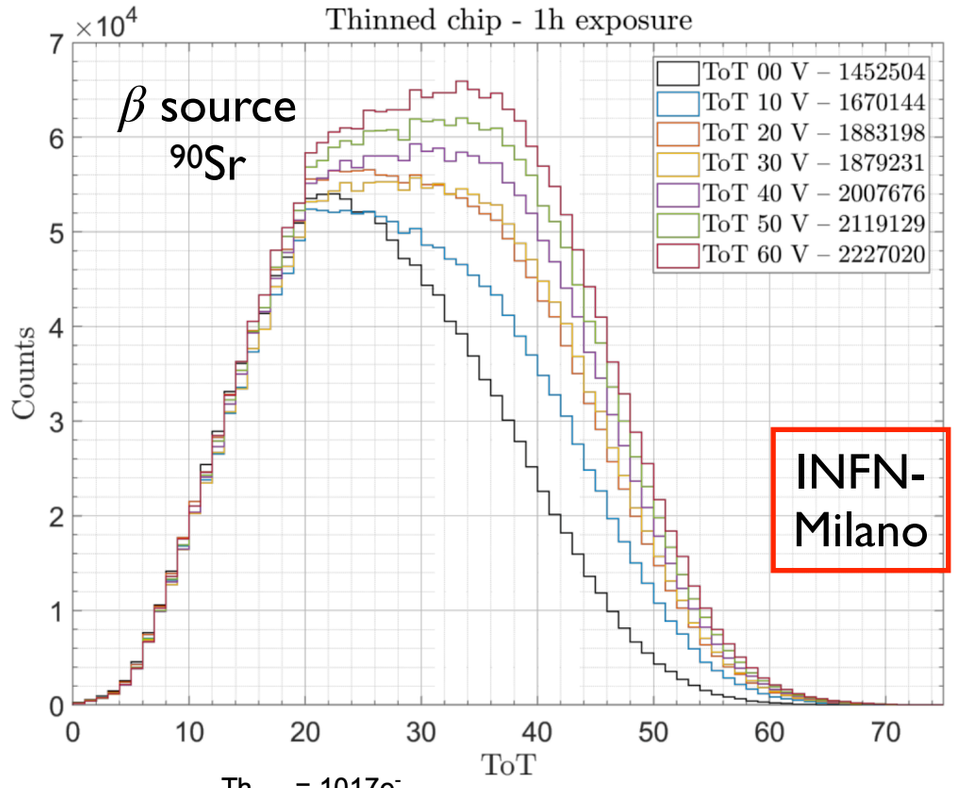


- 2 ATLASPix3.0 wafers diced (some thinned to 150um) and distributed to >10 institutes
  - 3 ATLASPix3.1 wafers currently in OPTIM for dicing and thinning
- O(65) GECCO boards and single chip carriers produced in China and distributed globally
- Many institutes have commissioned lab test stand and started electrical measurements
  - Threshold tuning (global and pixel matrix)
  - Source measurements, e.g. γ-source from ^{241}Am, β-source from ^{90}Sr, and cosmic muons

Highlights of lab measurements on SSC

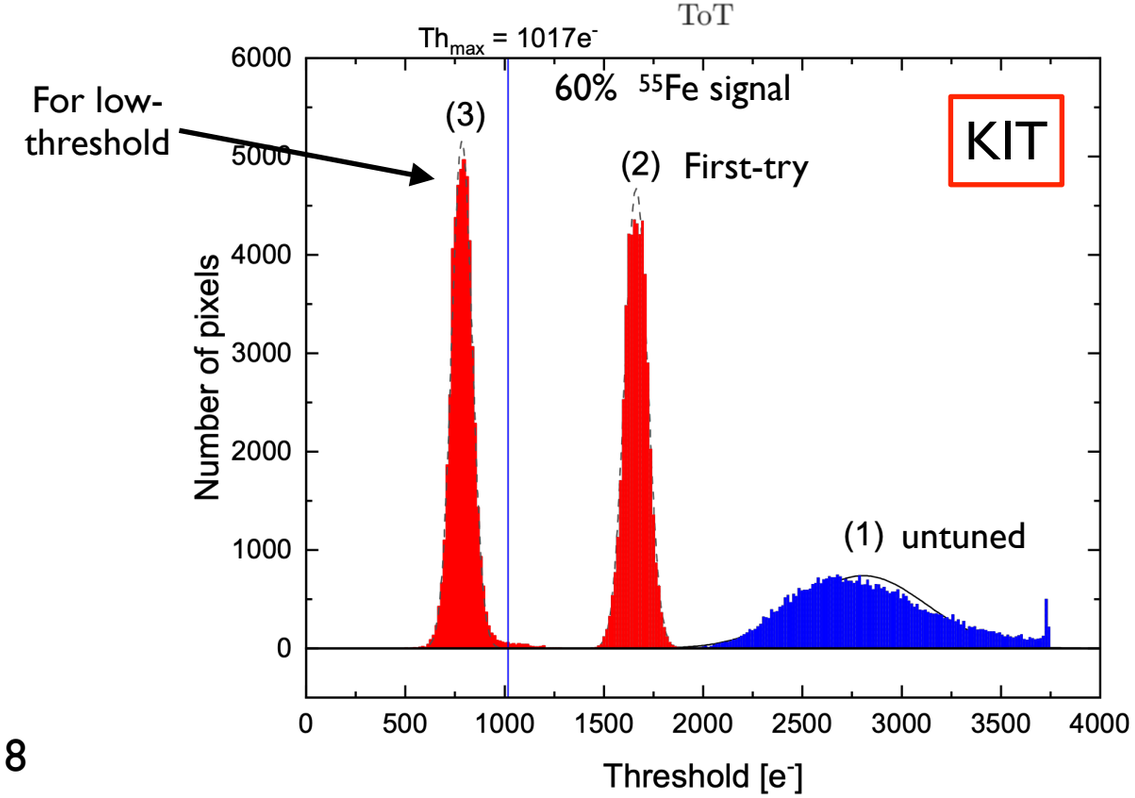
- With tremendous help from KIT (especially Rudolf Schimassek), many institutes commissioned ATLAPix3 DAQ setup
  - IHEP, Bristol, Edinburgh, INFN-Milano, Lancaster..





First round of ATLASPix3.1

Threshold can be tuned to 800e, noise around 70e

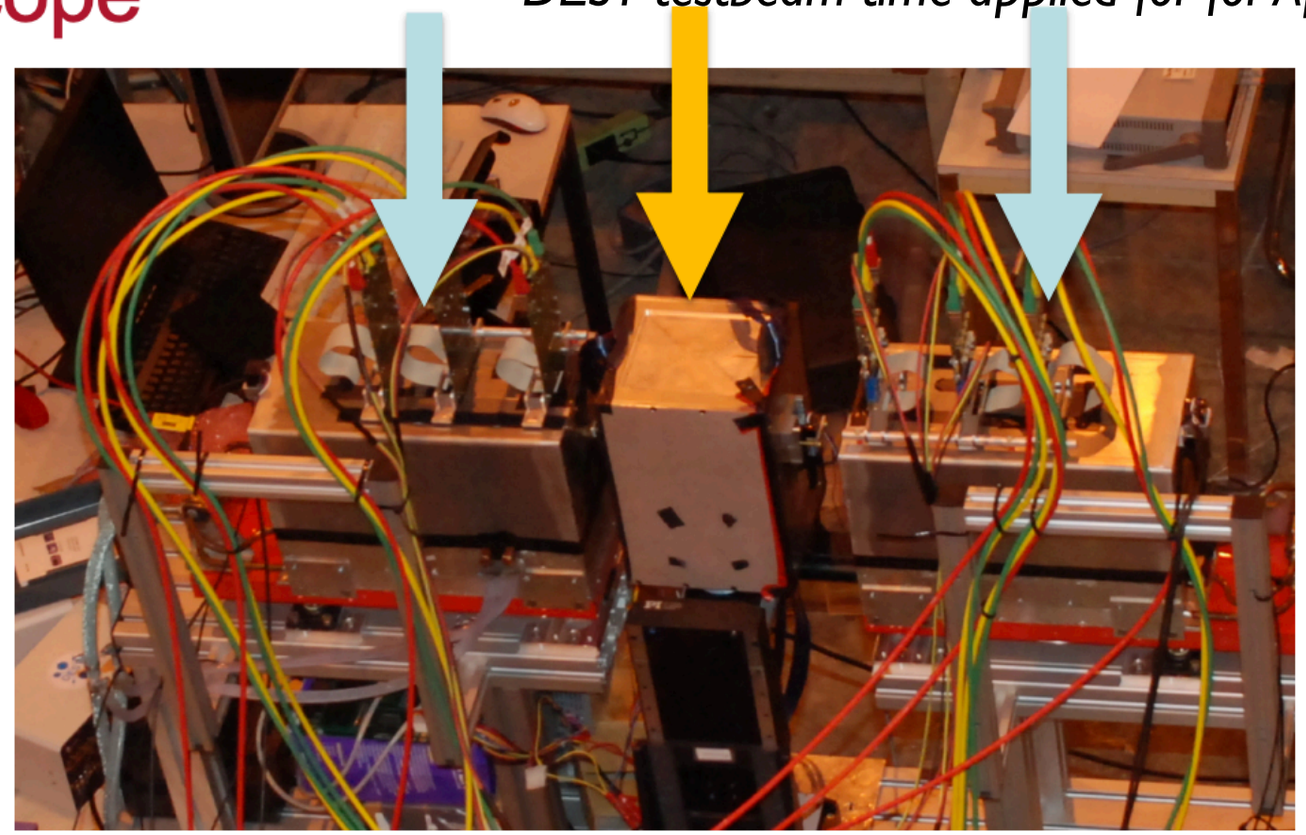


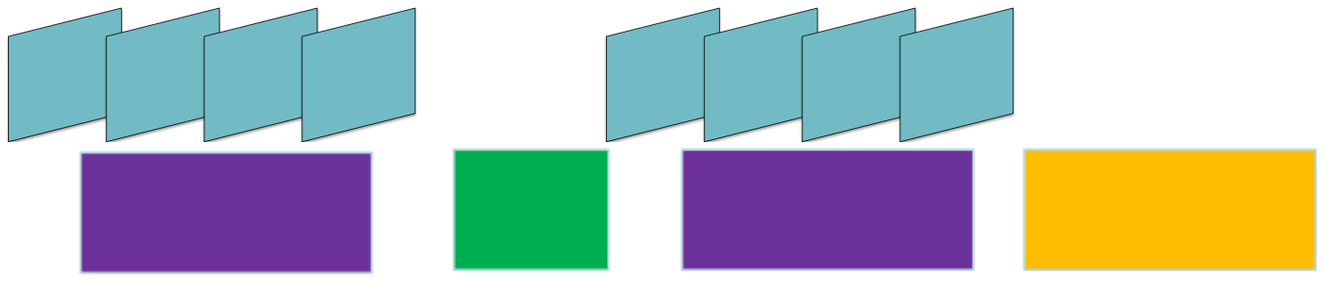
Testbeam plans

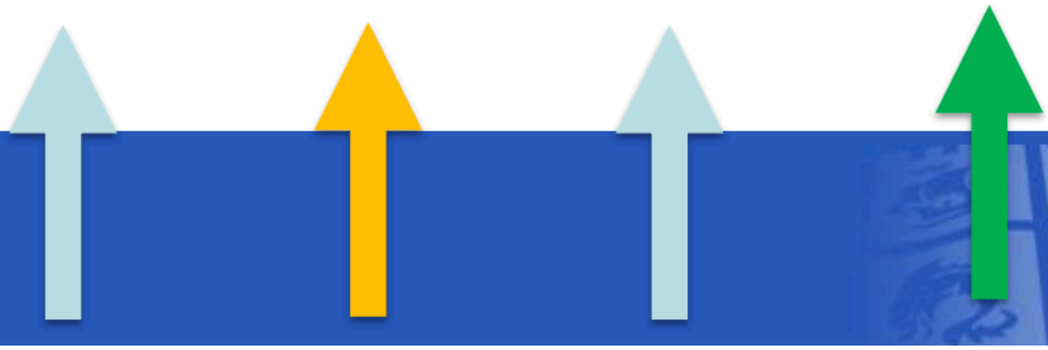
Proposed telescope

DESY testbeam time applied for for April 2022

- Our DAQ system supports 4 ATLASPix3.
- We will make
  - 2 “tracking stations”
  - DUT station
  - Space for additional DUTs
- No need for trigger system: each sensor provides hits and time stamps.
  - Can synchronize the reset signal.



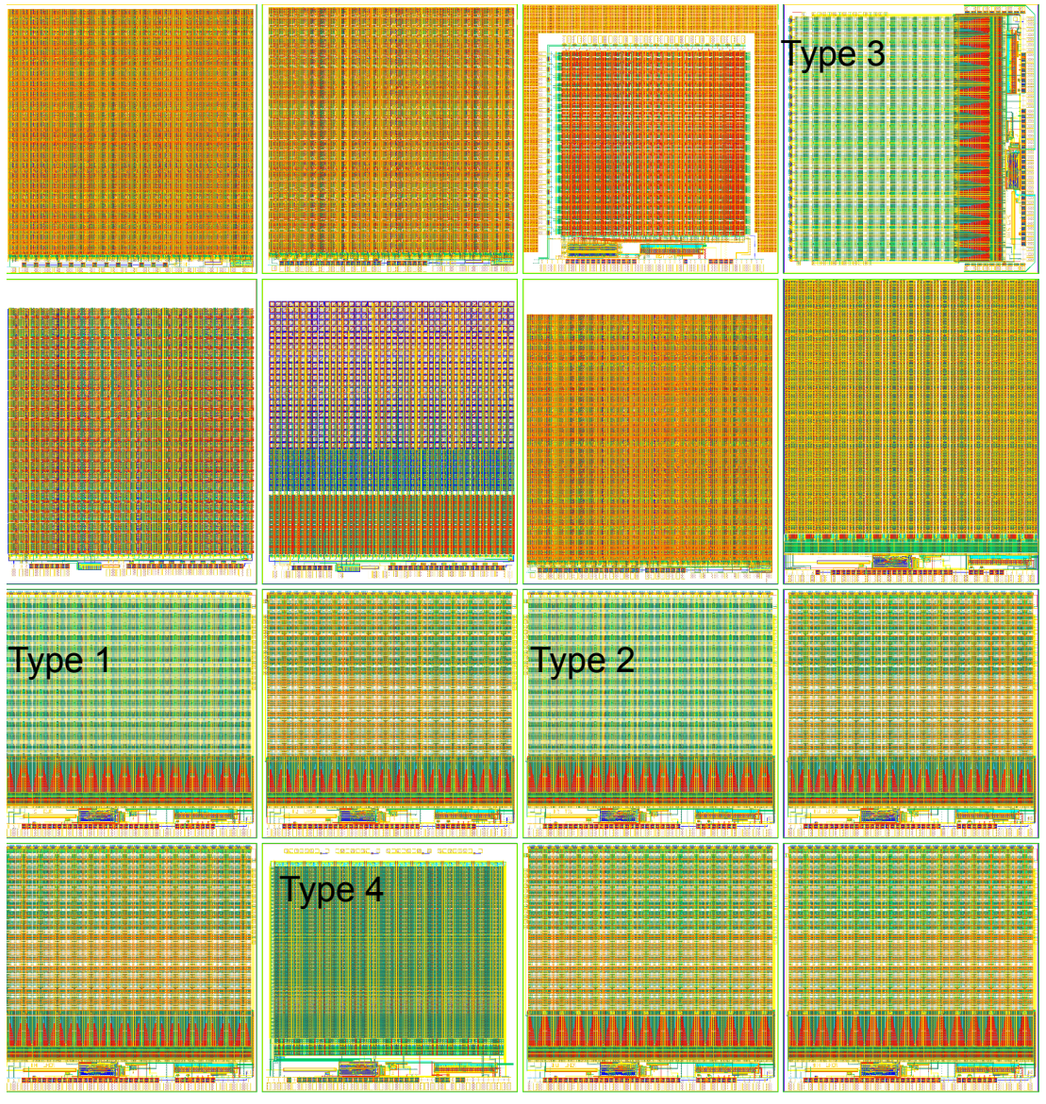




New sensor designs for electron colliders

- New improved sensor designs suitable for tracking detectors for electron colliders
  - Joint engineering run with LHCb 2020
  - Several designs for CLIC, CEPC, DESY telescope upgrade (TELEPIX)
  - Pixels 25µm X 165µm, 25µm X 35µm
- Key improvements
  - Reduced pixel size
  - Different amplifier and comparator types
  - Reduced power consumption

Matrix	Pixel size µm	Pixel type	Amplifier	Comparator
1	25x165	HVCMOS	N/C MOS	NMOS
2	25x165	HVCMOS	N/P MOS	CMOS
3	25x165	HVCMOS	NMOS	distributed
4	25x35	DMAPS	NMOS	CMOS

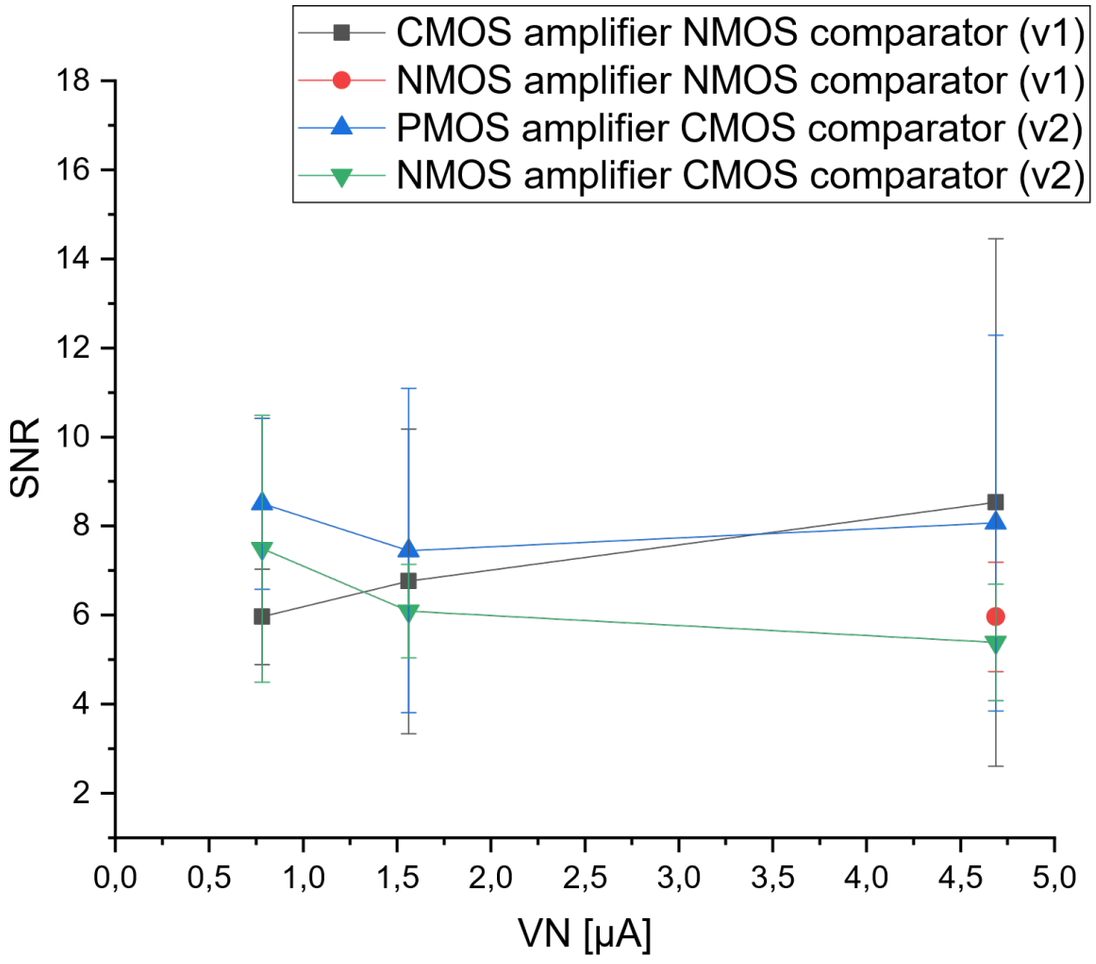


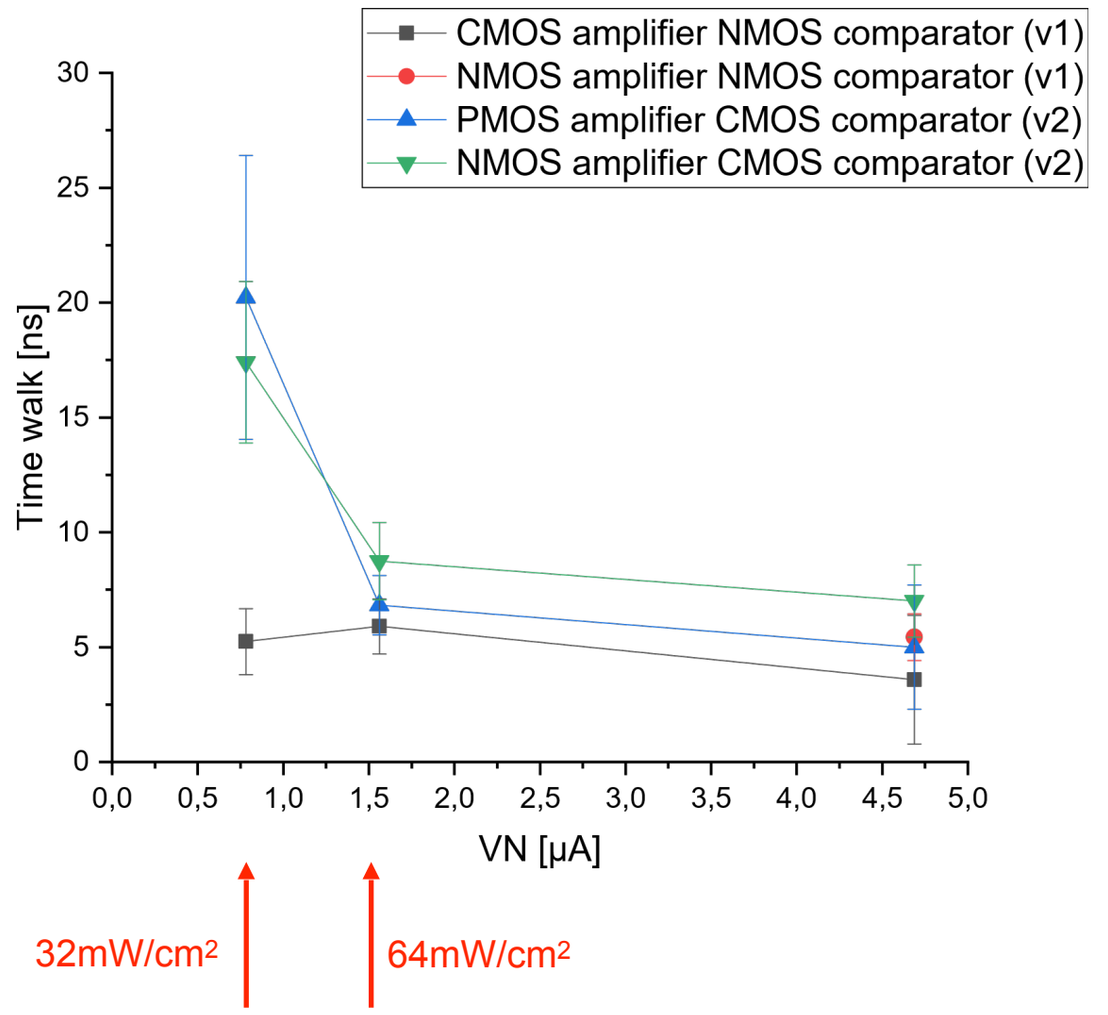
Reticle map

Ivan Peric: UK-CEPC tracker workshop

Preliminary measurements and implications

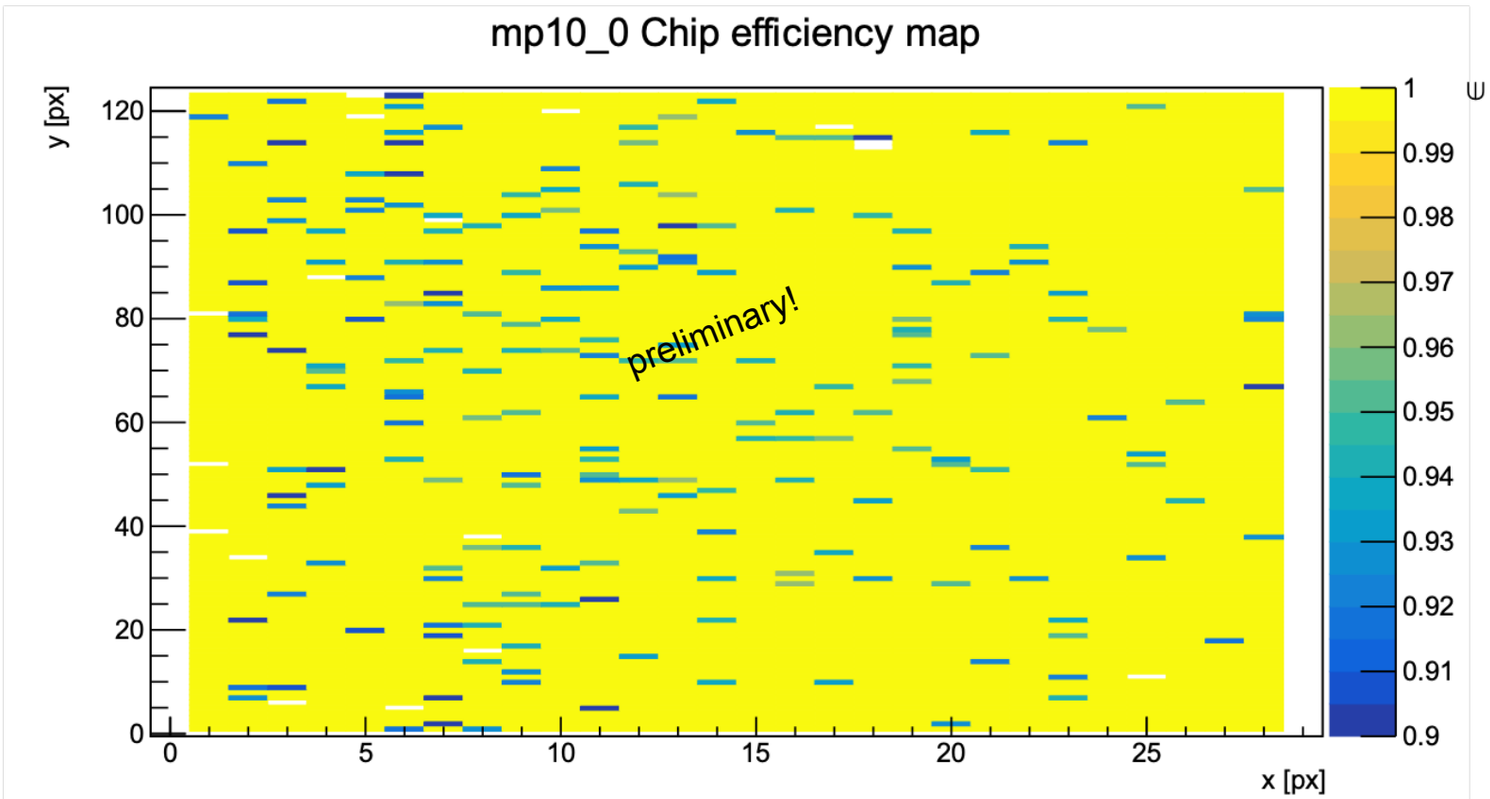
- Pixel matrices with three amplifier types have been operated with smallest possible threshold
- Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured
- CMOS amplifier has smallest time walk
- Low power consumption is possible (up to factor of 4 reduction compared with ATLASPix3)

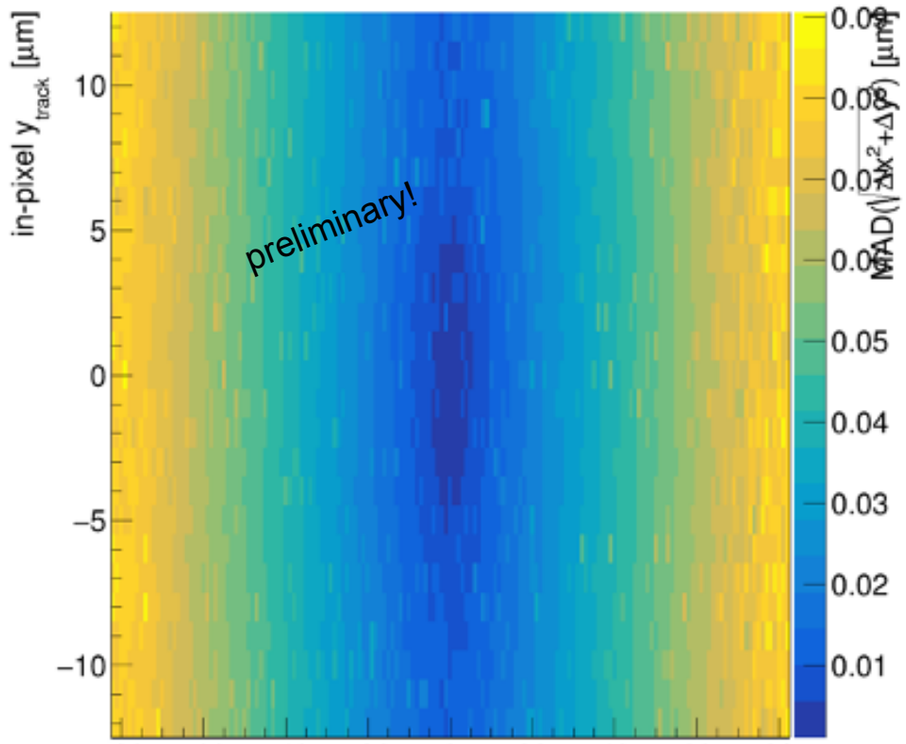


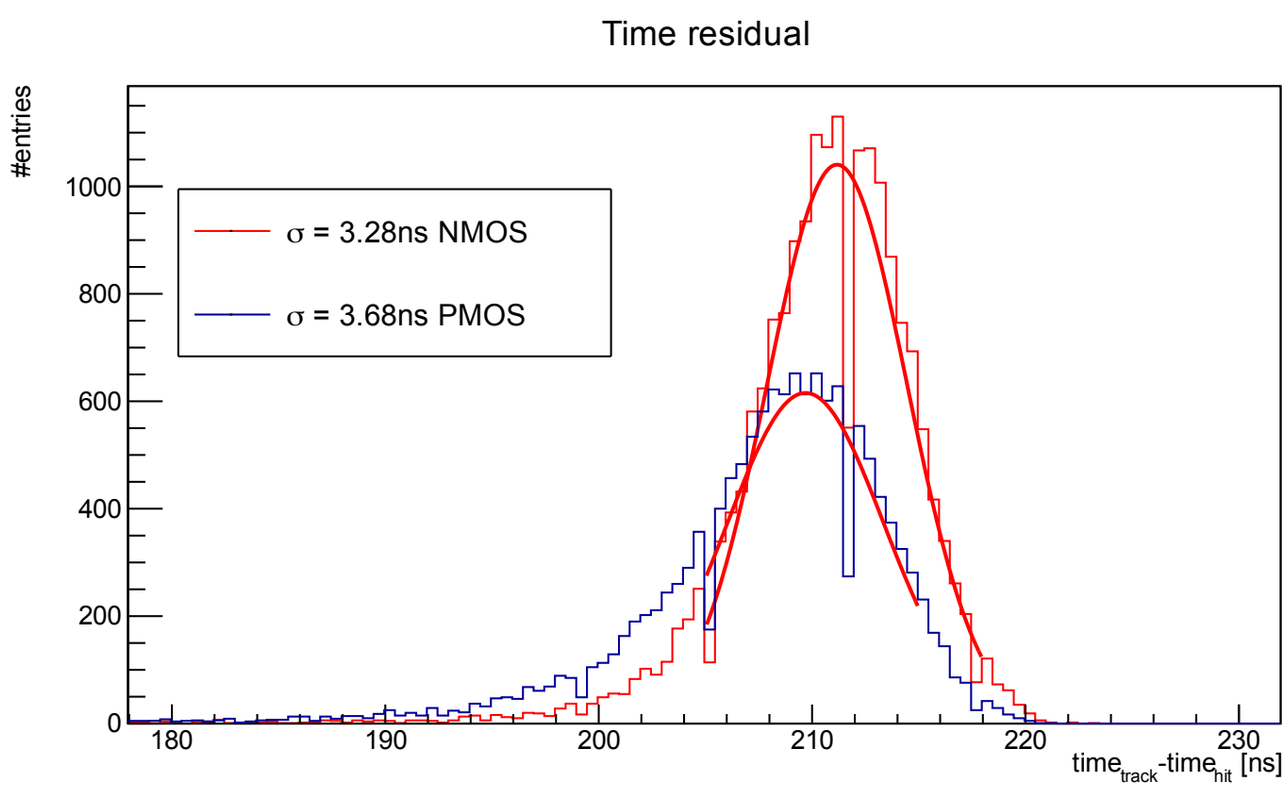


ATLASPIX3: 140mW/cm²

Test beam results - curtsey of Dohun Kim (LHCb)







Resolution:
- X: 165µm pitch: 47.0µm resolution
- Y: 25µm pitch: 8.2µm resolution

Resolution along Y is slightly worse than expected (<7.2µm). Likely due to telescope pointing resolution – needs to be verified

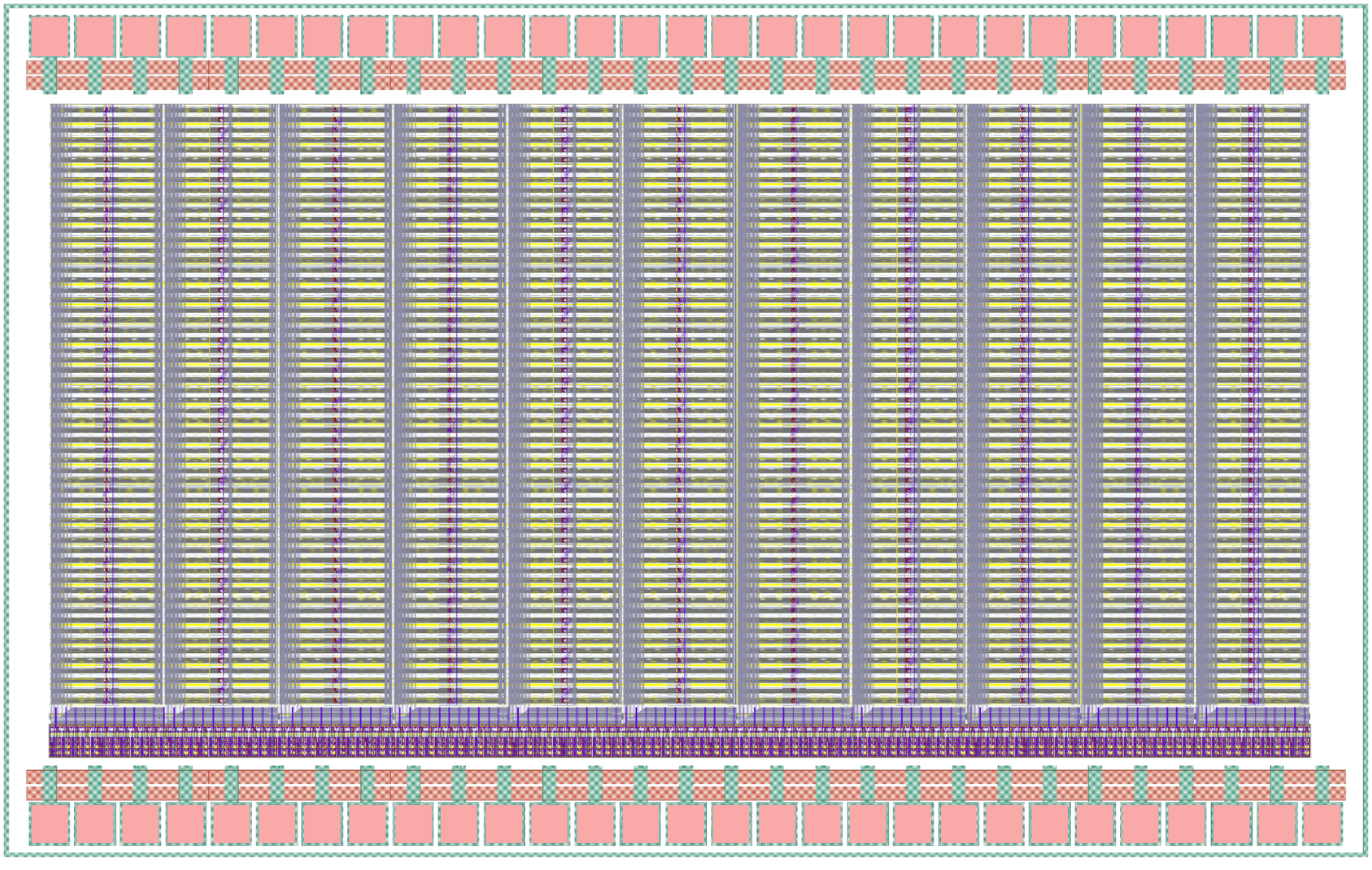
Time resolution: 3.3ns without corrections

HV-CMOS sensor in 55nm technology (I)

- We have started with design of the dedicated CEPC design in the HLMC 55nm HVCMOS technology
  - HLMC technology offers similar layers as TSI
- The test sensor should be submitted within an MPW run
- The run was originally planned for August 2021, it is postponed to March 2022
- An area of 3 x 2 mm is reserved for our design

HLMC 上海华力微电子有限公司 Shanghai Huali Microelectronics Corporation

Chip layout



KIT
IHEP

HLMC foundry

上海华力微电子有限公司
Shanghai Huali Microelectronics Corporation

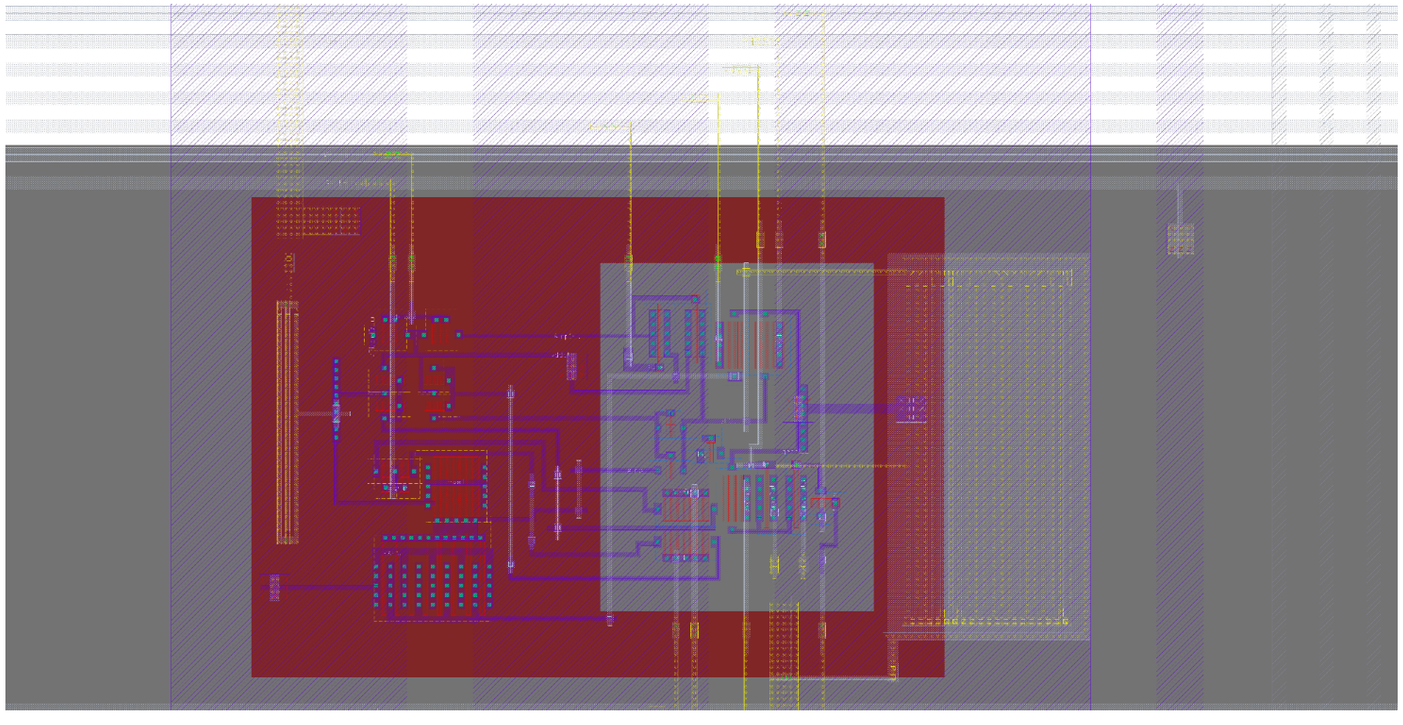
Shanghai Huali Microelectronics Corporation (**HLMC**) is a Chinese foundry. As of 2018, HLMC had 55 nm, 40 nm, and 28 nm process technologies and are capable of producing up to 35,000 wafers per month.

- HLMC technology offers similar layers as TSI
- Especially important is the floating logic structure with deep n-well
- The maximum voltage for HV transistors is 32V
- Deep n-well to p-substrate should have higher breakdown
- Metal layers 1 – 6 can be used for fine pitch routing
- The realistic pitch is down to 0.2um – relaxed and according to recommendation is 0.3 (in 180nm was 0.6)
- There are tree more thick metal layers, suitable for power
- Low voltage power supply is 1.2V
- There are only hspice models available, we used Mentor Calibre for DRC LVS

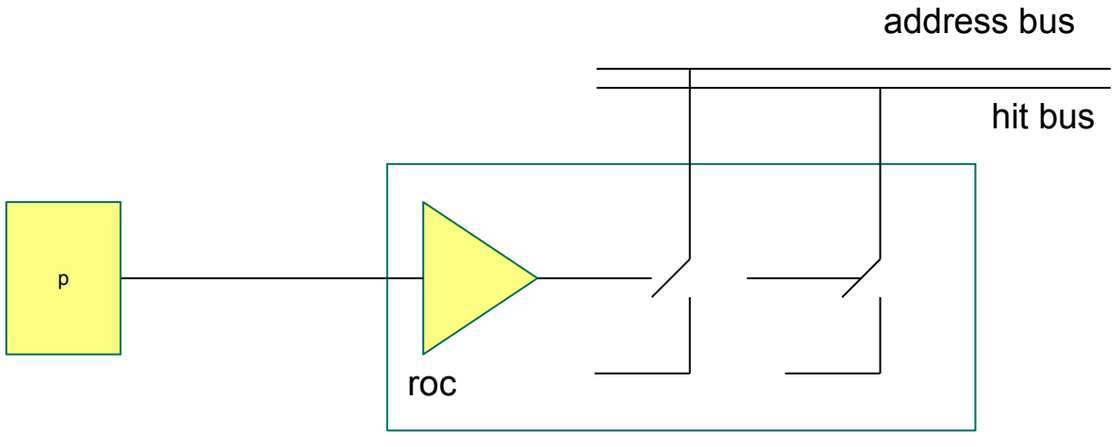
Ivan Peric: UK-CEPC tracker workshop

HV-CMOS sensor in 55nm technology (II)

- The pixel size is **x = 252 µm, y = 22 µm** (smaller x dimension is possible)
- The pixel contains CSA, CR filter and differential output driver
- Every pixel has a readout cell placed at the periphery
- One readout cell contains differential receiver – the driver (in pixel) and the receiver form a distributed comparator
- The structure of readout cell is simple, the comparator output is connected to hit bus driver and to address ROM. The ROM cells pass the data to the 10 bit address bus
- The readout cell also contains two bit-register to store comparator enable and injection enable bits
- The size of the readout cell is 4.2µm x 60µm (relaxed layout)



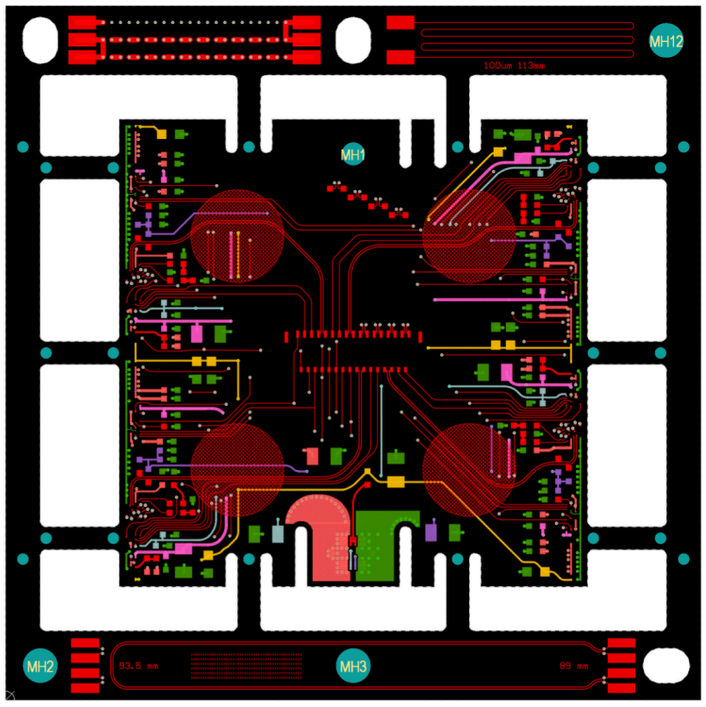
Pixel layout

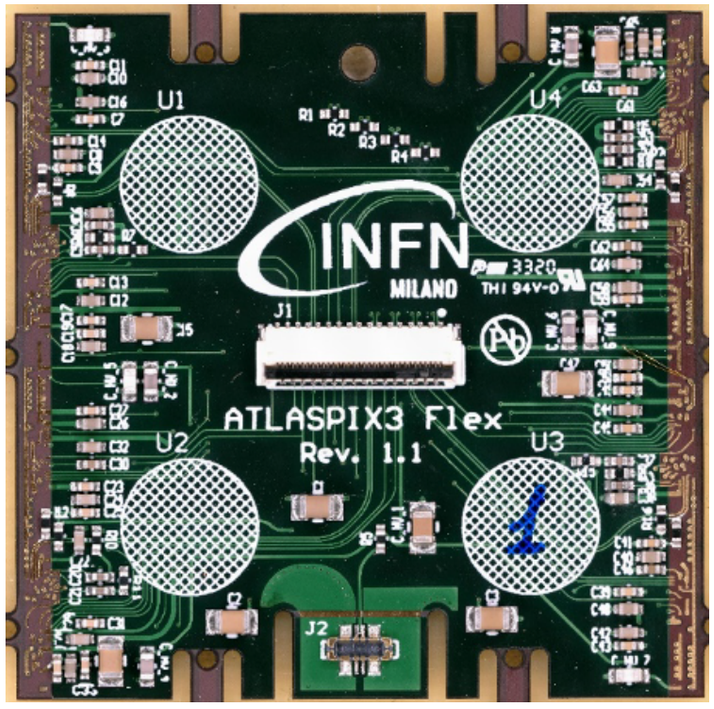


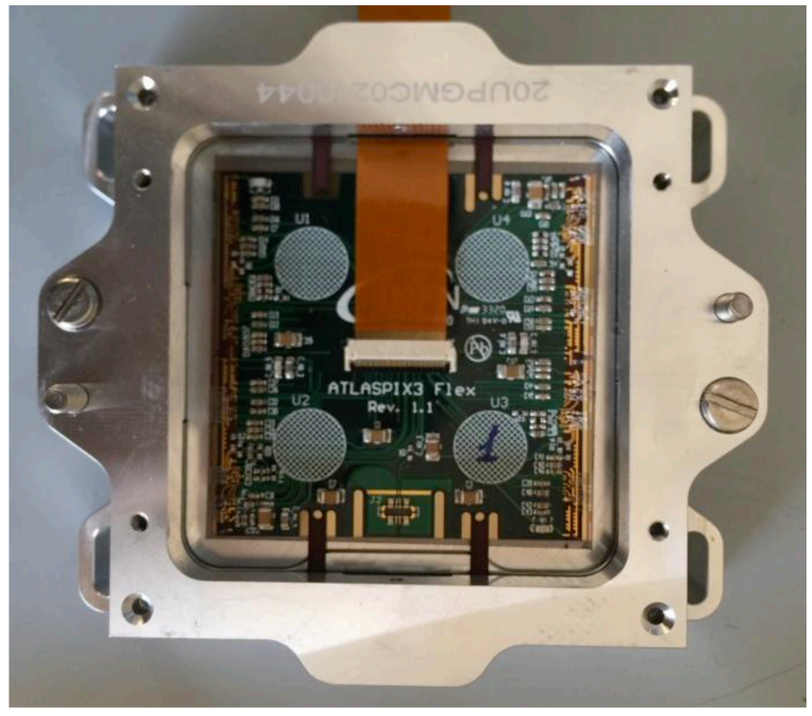
pixel p and readout cell

Quad-module

- Inspired by the ATLAS ITk quad-module concept for large area applications
  - Four chips sharing services by common power connections and configuration lines
  - Default configuration: command decoder
- 4-layer flex hybrid: 2 power layers, 2 signal layers with impedance-matching lines





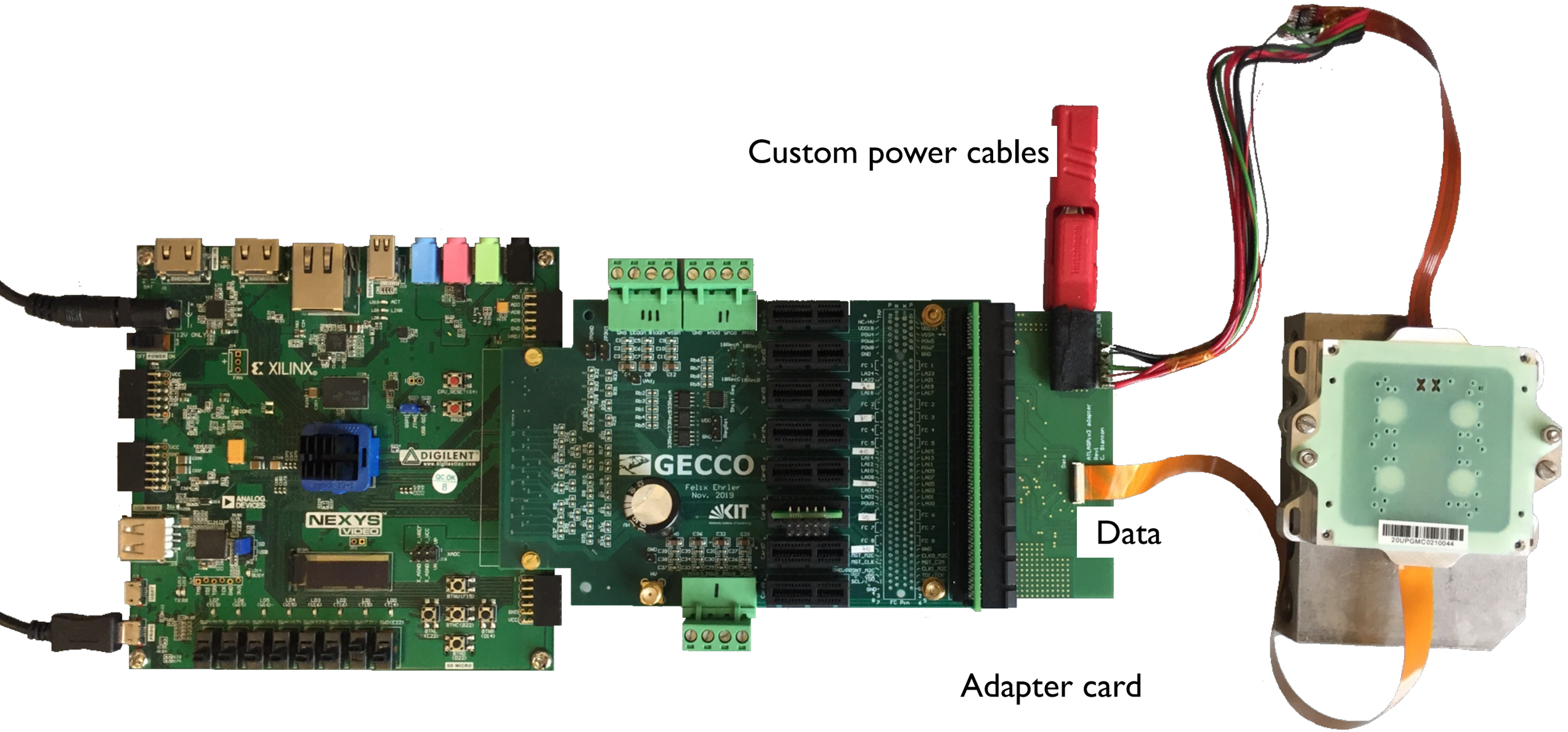


From Bianca Raciti, PSD2021 poster

INFN-Milano and KIT

Quad-module readout - lab setup

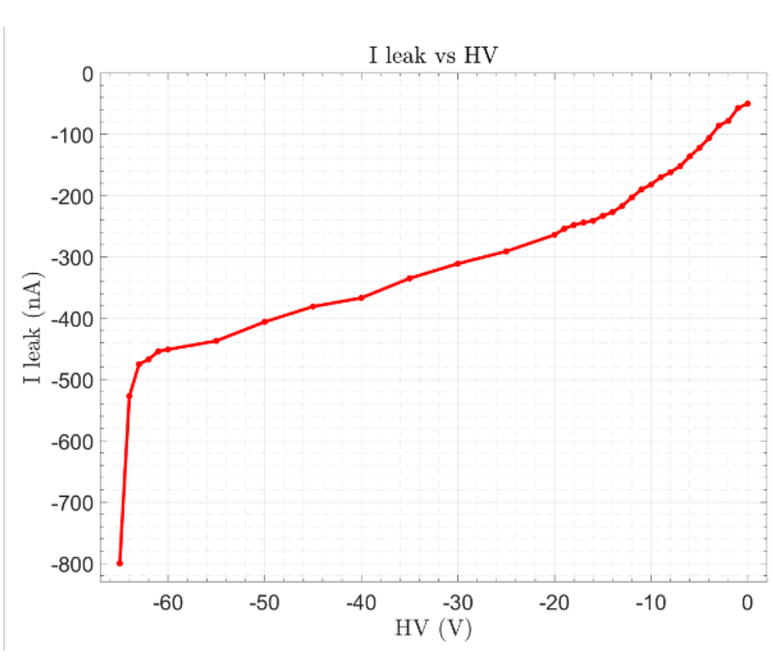
- Adapter card for connecting to the GECCO readout board
  - Quad-module constructed and tested for the first time

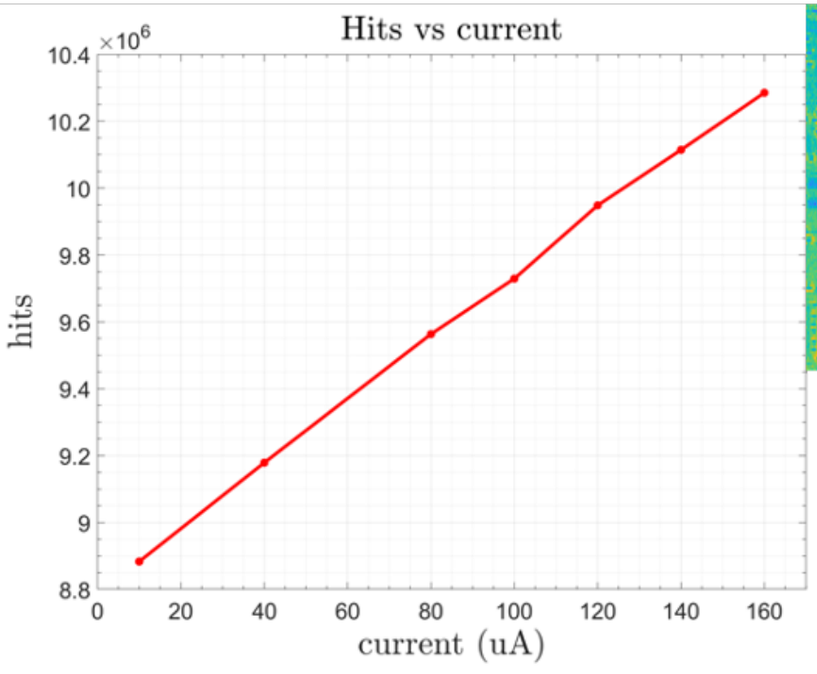


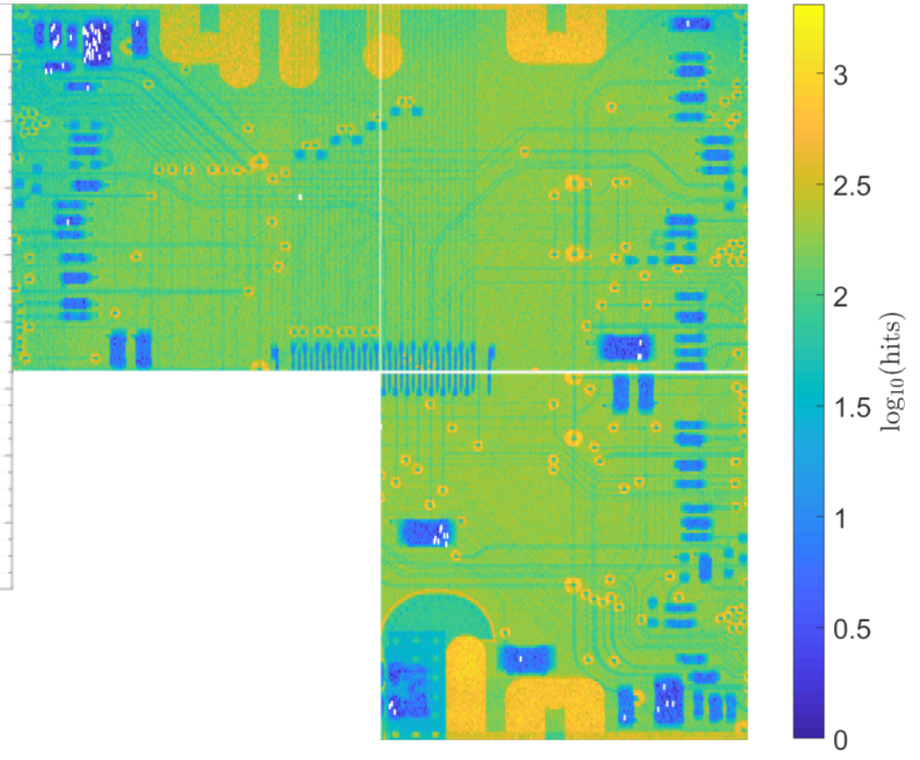
INFN-Milano, KIT, Edinburgh

Quad-module - highlight of lab measurements

- All 4-chips can be configured, 3/4 read out successfully
  - $|I_{\text{leakage}}| < 400$ nA when |HV| < 60 V, Breakdown voltage = -65 V, consistent with SSC result
  - Current consumption is 1.33 A for VDD = 1.9 V
- Lab measurements with X-ray tubes (Amptex Mini-X2)
  - 5-minutes source runs without HV → linear readout rate seen at 25kV without low-energy filters





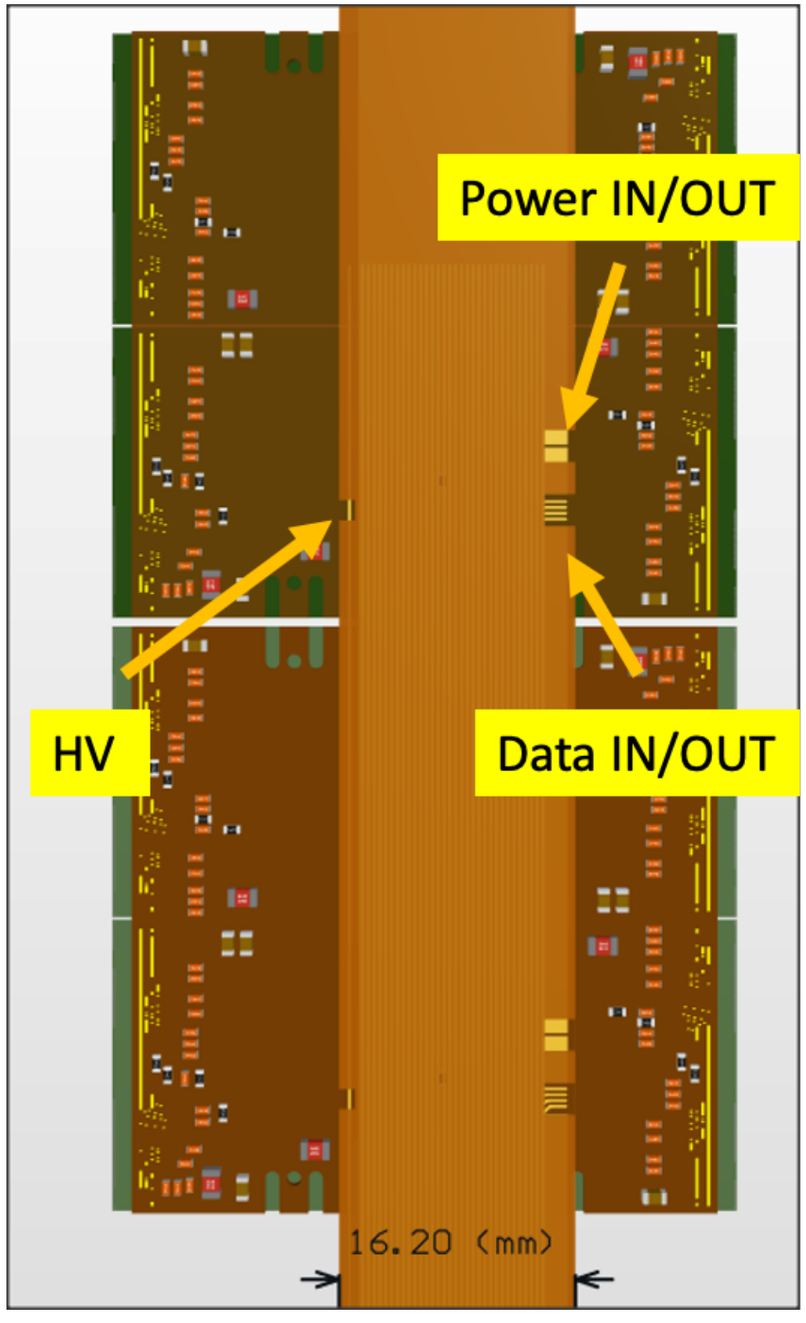


From INFN-Milano group: B. Raciti, F. Sabatini, A. Andreazza, presented at the AIDAInnova WP5

Serial powering chain and electrical bus

- From quad to serial powering chain (stave)
  - Distribute power and data signals along the stave
- Assume minimal I/O connection on chip:
  - All biases generated internally by shunt-LDO regulators
  - chip-to-chip data transmissions: local data aggregation on module
  - clock data recovery
- Preliminary design requirements:
  - LVDS command input
  - LVDS data output at 640 Mbps on ~700 mm (half)-stave length
  - Serial powering assuming 0.5 A/chip, 2 A/module
  - HV distributed in parallel to all modules
- Integrated signal and power bus:
  - Power distribution and return layers
  - Signal lines on top and bottom layers
  - Interconnection by soldering or wire bonding
- Alternative under study: power/data separated

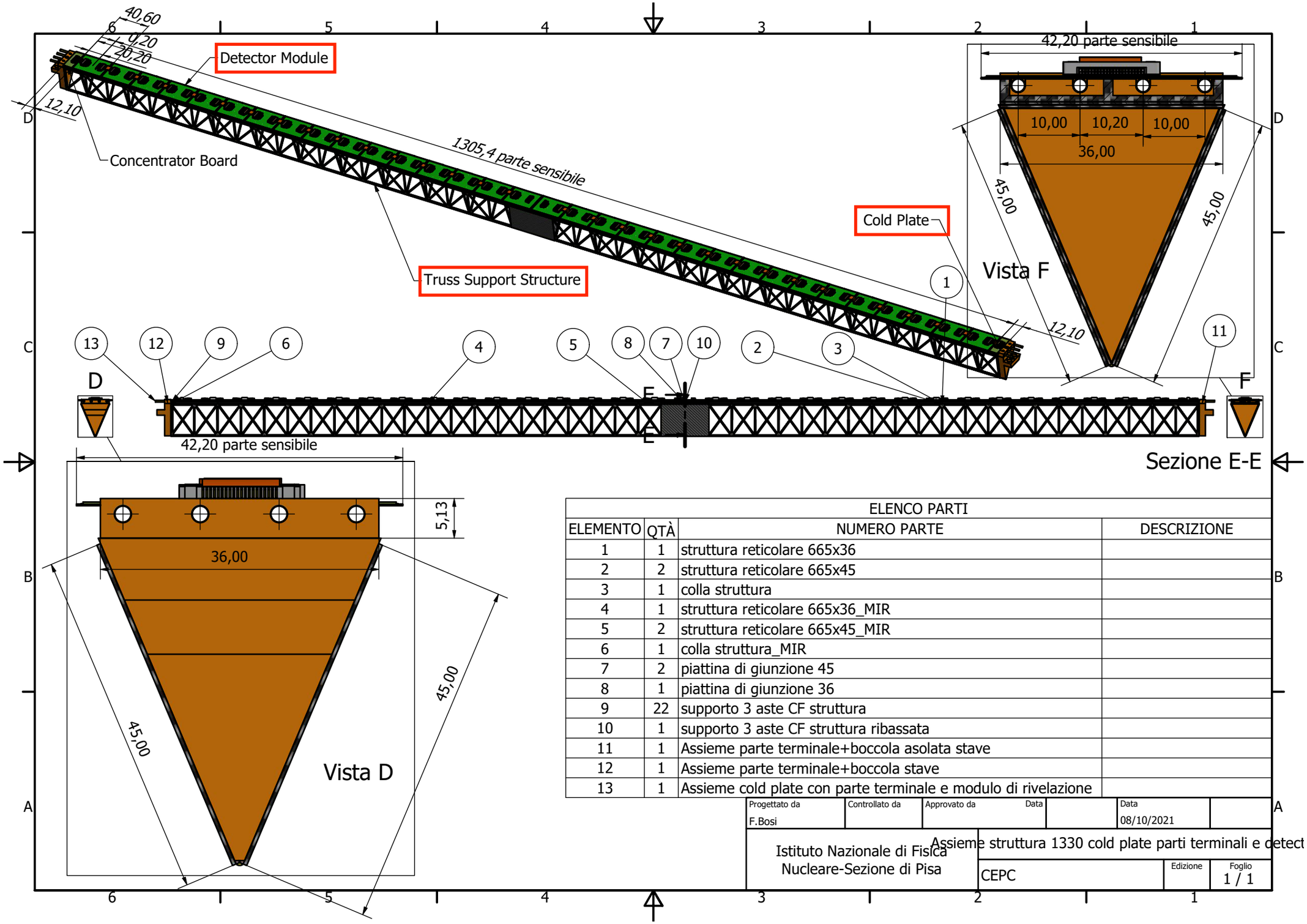
Serial powering chain 16 quad (4cm*64cm)



F. Palla, F. Bosi, A. Andreazza, F. Sabatini
CEPC Sitracker meeting 4-Nov-2021

INFN-Milano/Pisa

System design concept - 1.3m long stave (SIT2)



ELENCO PARTI			
ELEMENTO	QTÀ	NUMERO PARTE	DESCRIZIONE
1	1	struttura reticolare 665x36	
2	2	struttura reticolare 665x45	
3	1	colla struttura	
4	1	struttura reticolare 665x36_MIR	
5	2	struttura reticolare 665x45_MIR	
6	1	colla struttura_MIR	
7	2	piattina di giunzione 45	
8	1	piattina di giunzione 36	
9	22	supporto 3 aste CF struttura	
10	1	supporto 3 aste CF struttura ribassata	
11	1	Assieme parte terminale+boccola asolata stave	
12	1	Assieme parte terminale+boccola stave	
13	1	Assieme cold plate con parte terminale e modulo di rivelazione	

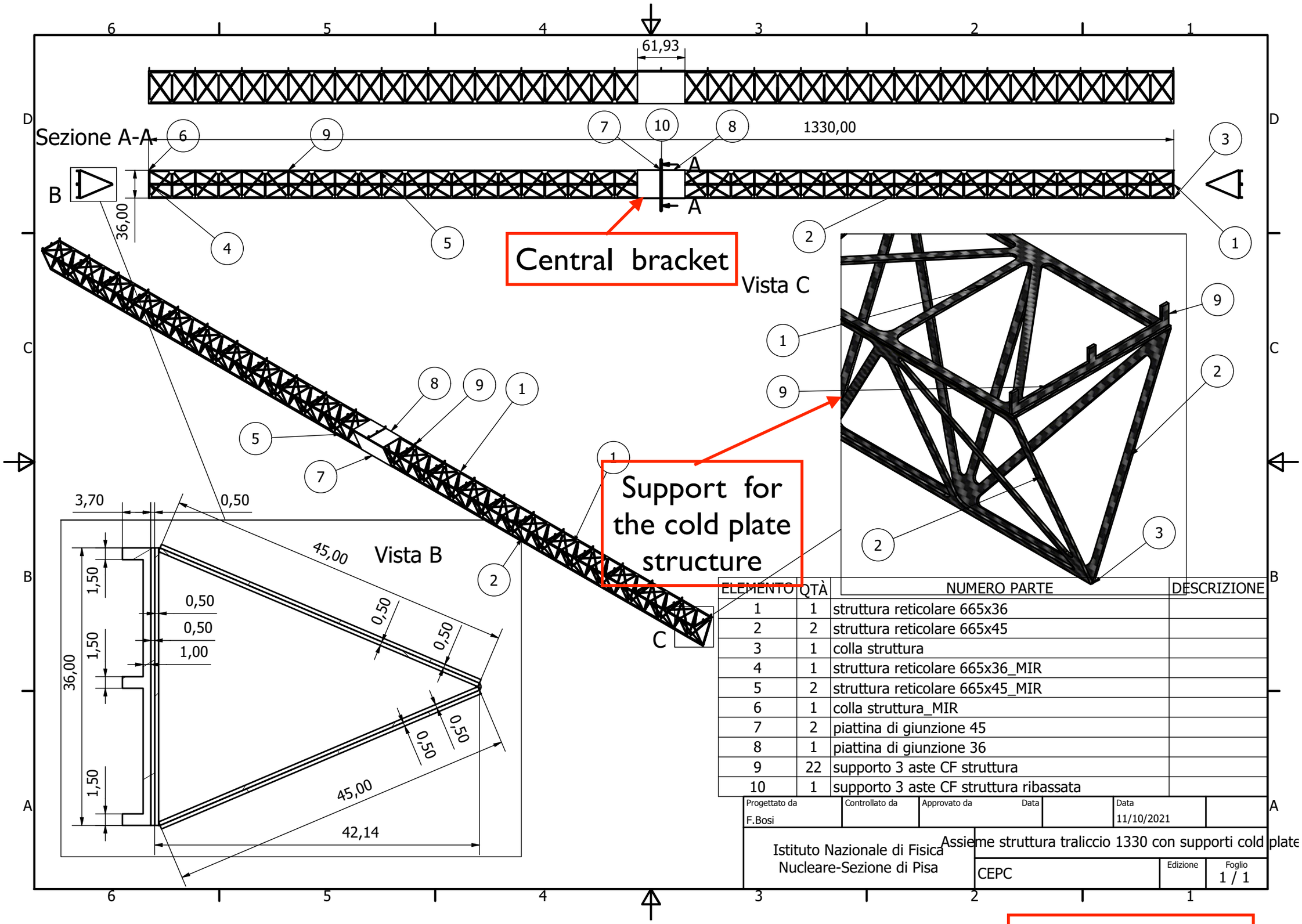
Progettato da	Controllato da	Approvato da	Data		Data	
F.Bosi					08/10/2021	

Istituto Nazionale di Fisica Nucleare-Sezione di Pisa

Assieme struttura 1330 cold plate parti terminali e detect

CEPC | Edizione | Foglio 1 / 1

Closer look at the truss structure



ELEMENTO	QTÀ	NUMERO PARTE	DESCRIZIONE
1	1	struttura reticolare 665x36	
2	2	struttura reticolare 665x45	
3	1	colla struttura	
4	1	struttura reticolare 665x36_MIR	
5	2	struttura reticolare 665x45_MIR	
6	1	colla struttura_MIR	
7	2	piattina di giunzione 45	
8	1	piattina di giunzione 36	
9	22	supporto 3 aste CF struttura	
10	1	supporto 3 aste CF struttura ribassata	

Progettato da	Controllato da	Approvato da	Data		Data	
F.Bosi					11/10/2021	

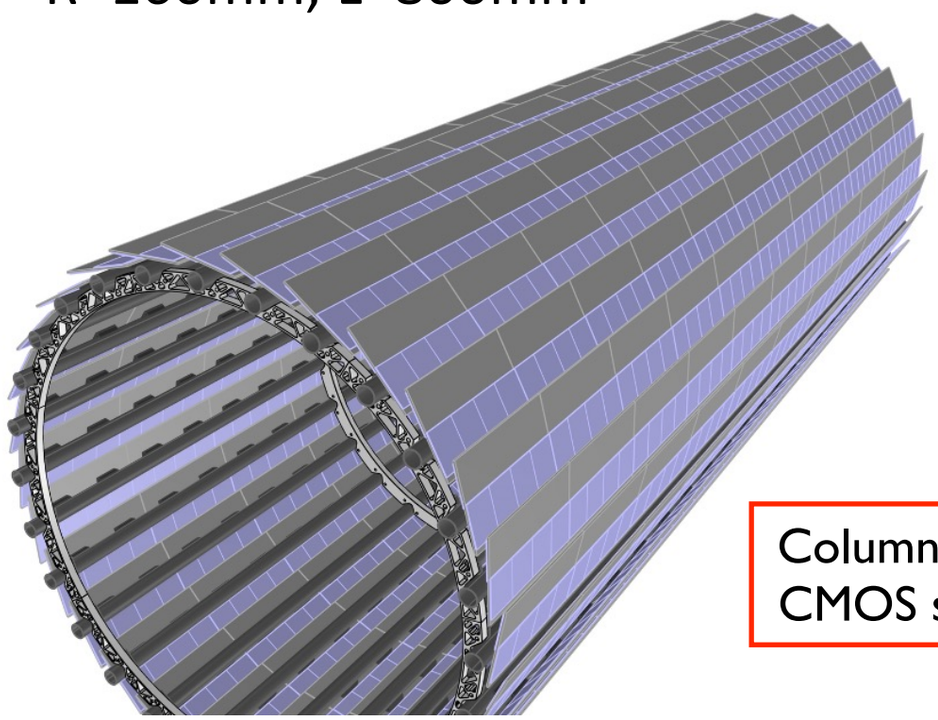
Istituto Nazionale di Fisica Nucleare-Sezione di Pisa

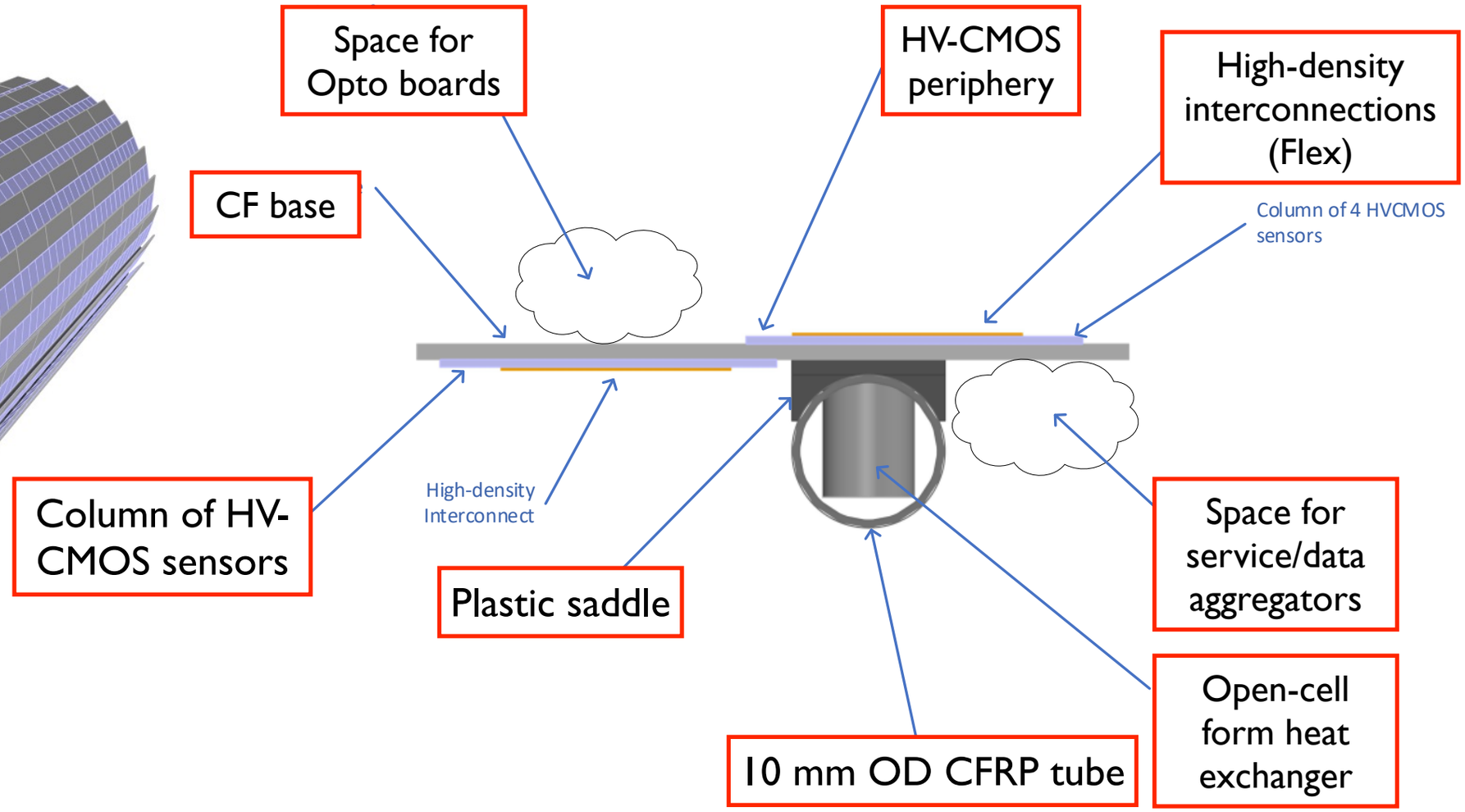
Assieme struttura traliccio 1330 con supporti cold plate

CEPC | Edizione | Foglio 1 / 1

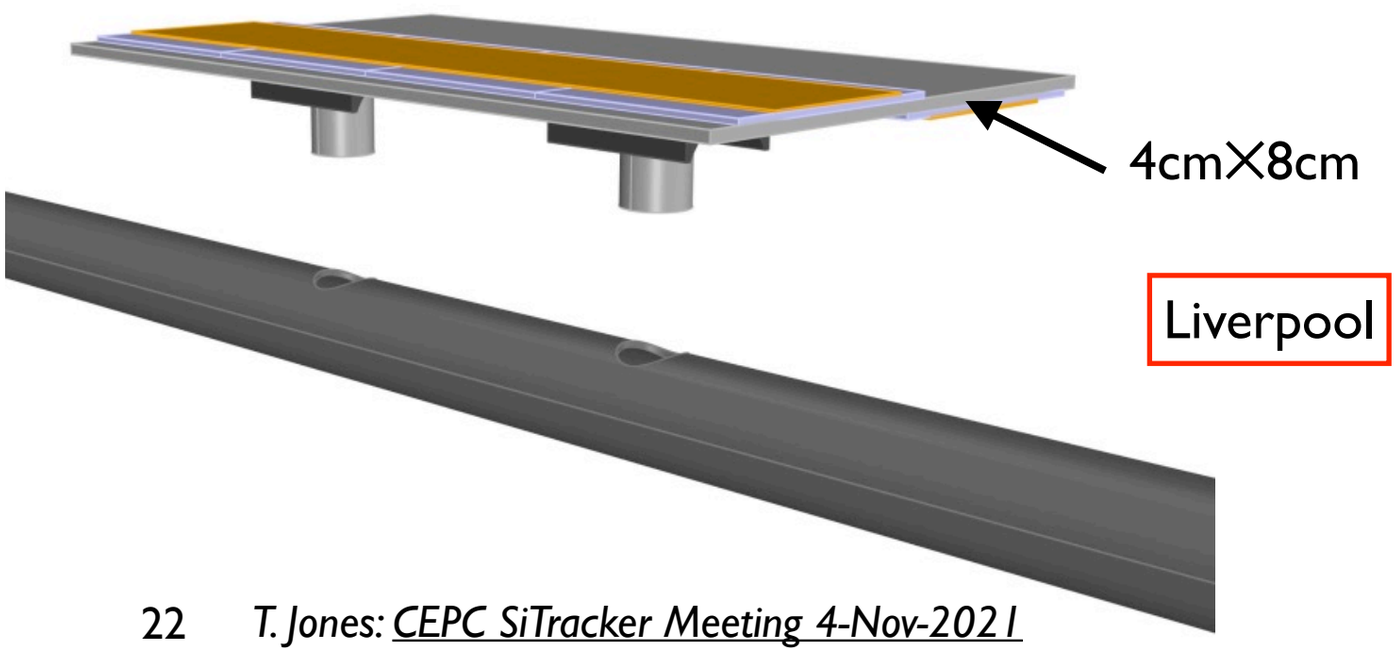
Mechanical design concept for SIT-1

R=160mm, L=800mm



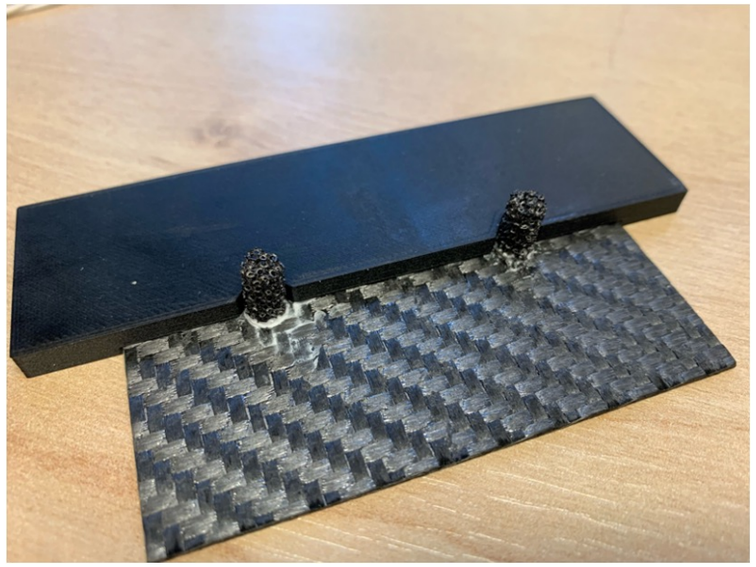


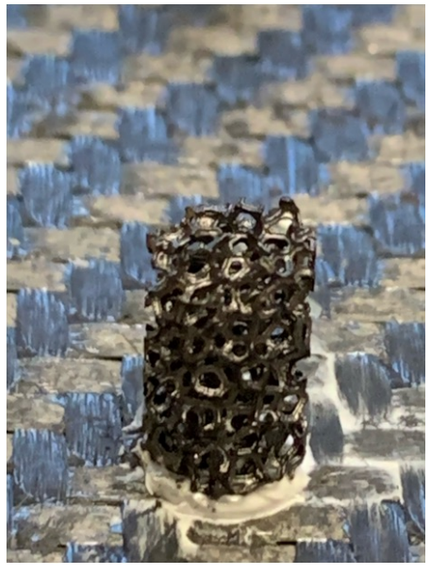
- HV-CMOS sensors glued to CF base
  - Asymmetric arrangement with peripheral areas as close as possible to the middle where power consumption is max
- Base attaches to support tube via two saddles
- Saddles have apertures through which the foam heat exchangers pass and glue to the base

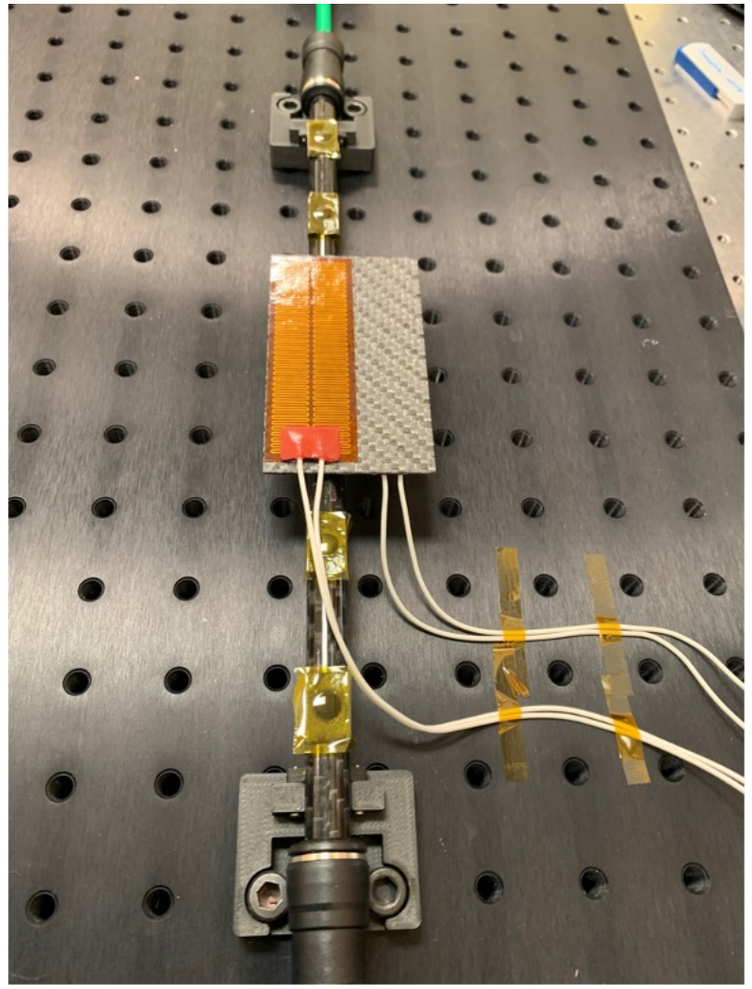


Pre-prototype thermal evaluations

Pre-prototype: Base attached to tube & heaters on







- Investigate performance of high-thermal conductivity (eg Allcomp) foams as a heat exchanger
  - Combination of large area and increased stream velocity through foam can lead to high efficiency
- Characterise performance (i.e. temperature rise vs power) for different flow velocities
- Develop FEA models simulating the fluid flow through foams

*First look: at 3.1W power (expected from 8cm*4cm area), temperature rise ~10 degrees w.r.t. CDA*

Liverpool

T. Jones: CEPC SiTracker Meeting 4-Nov-2021

Summary and next steps

- Made many progresses in the tracker R&D programme over the last year
  - Many institutes have gained valuable operation experiences with ATLASPix3.0 chips
  - Several new chip designs on-going targeting CEPC tracker applications
    - Significant step in HVCMOS 55nm technology with Chinese foundry HLMC
  - First quad module constructed and evaluated - significant step towards large area application
  - Exploring several mechanical design concepts and ready for (pre-)prototyping
- For next year or two
  - Continue with CMOS design efforts, in particular on the 55nm technology
  - Wrapping up ATLASPix3.0 based studies
    - assembly O(10) quad modules, new test beam with telescope (beam time submitted for Apr. 2022)
  - ATLASPix3.1 based programme
    - Evaluate shunt-LDO operation, new hybrid designs, electrical bus designs for stavelet
    - Assembly as many modules as possible, populate stavelet, and study serial powering chain
  - Mechanical and thermal studies for support structures targeting SIT layers

Backup slides

ATLAS Pix3.1

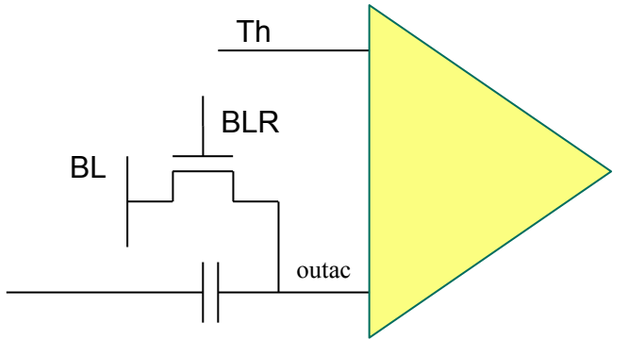
ATLASpix3.1

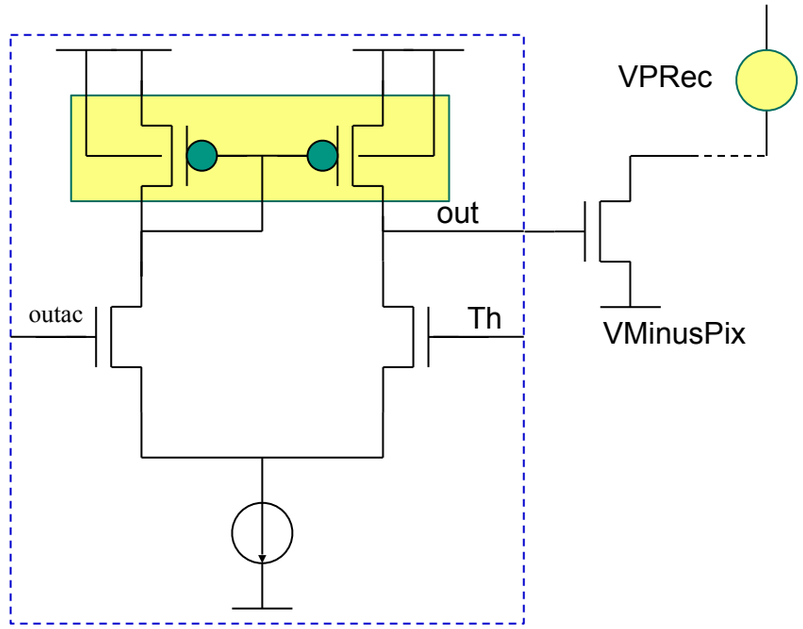
- ATLASpix3.1 submitted in December and delivered in February
- Redone masks for 8 Layers
- 12 wafers produced
- Reduced detector capacitance by replacing M2 shield with M3 shield (from about 250fF to 130fF)
- Modified design of the guard ring
  - Larger distance between DN and PW ring (see slides)
  - M1 ring disconnected from PW
  - Idea set substrate to -120V and M1 ring to -60V
- Added stability capacitor to the power regulator

Ivan Peric

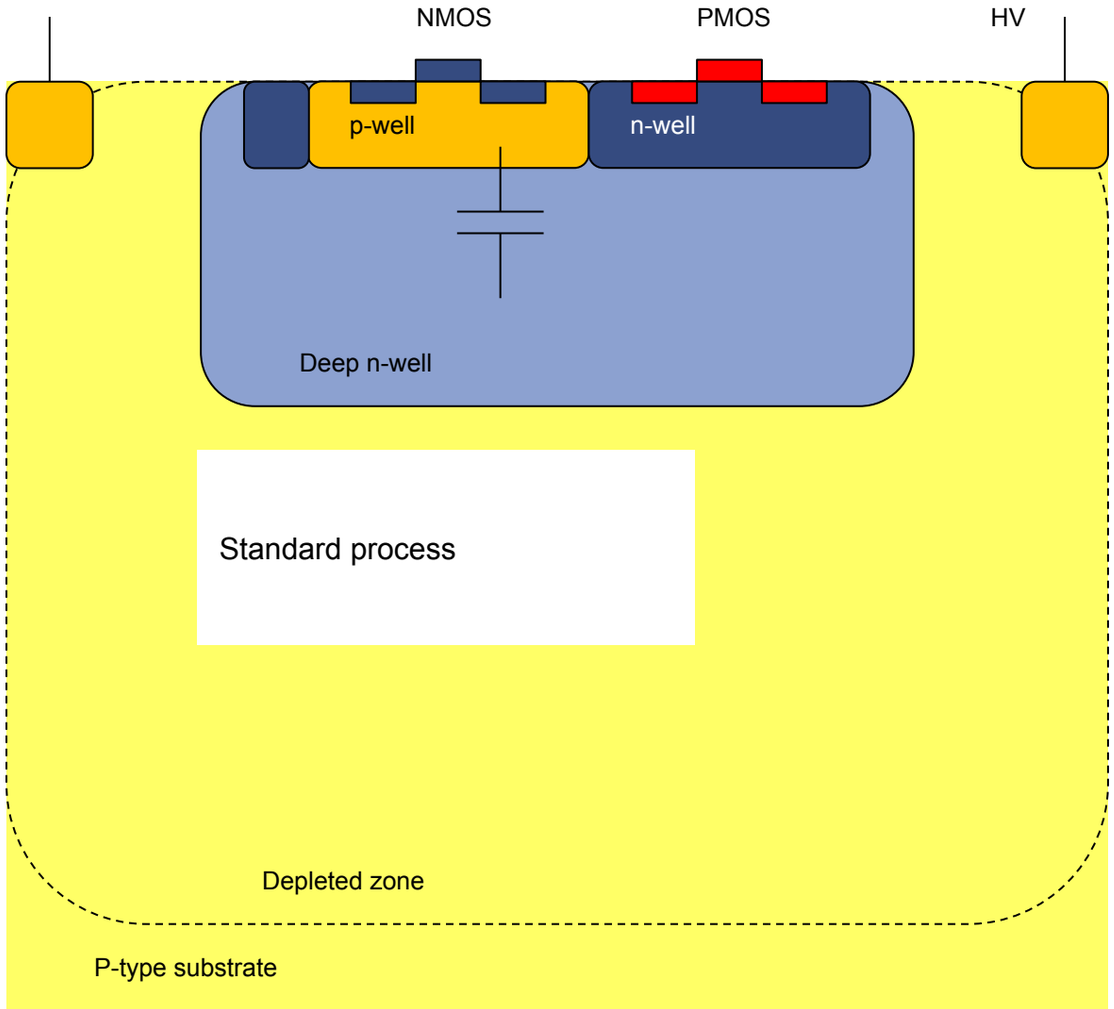
CMOS comparator

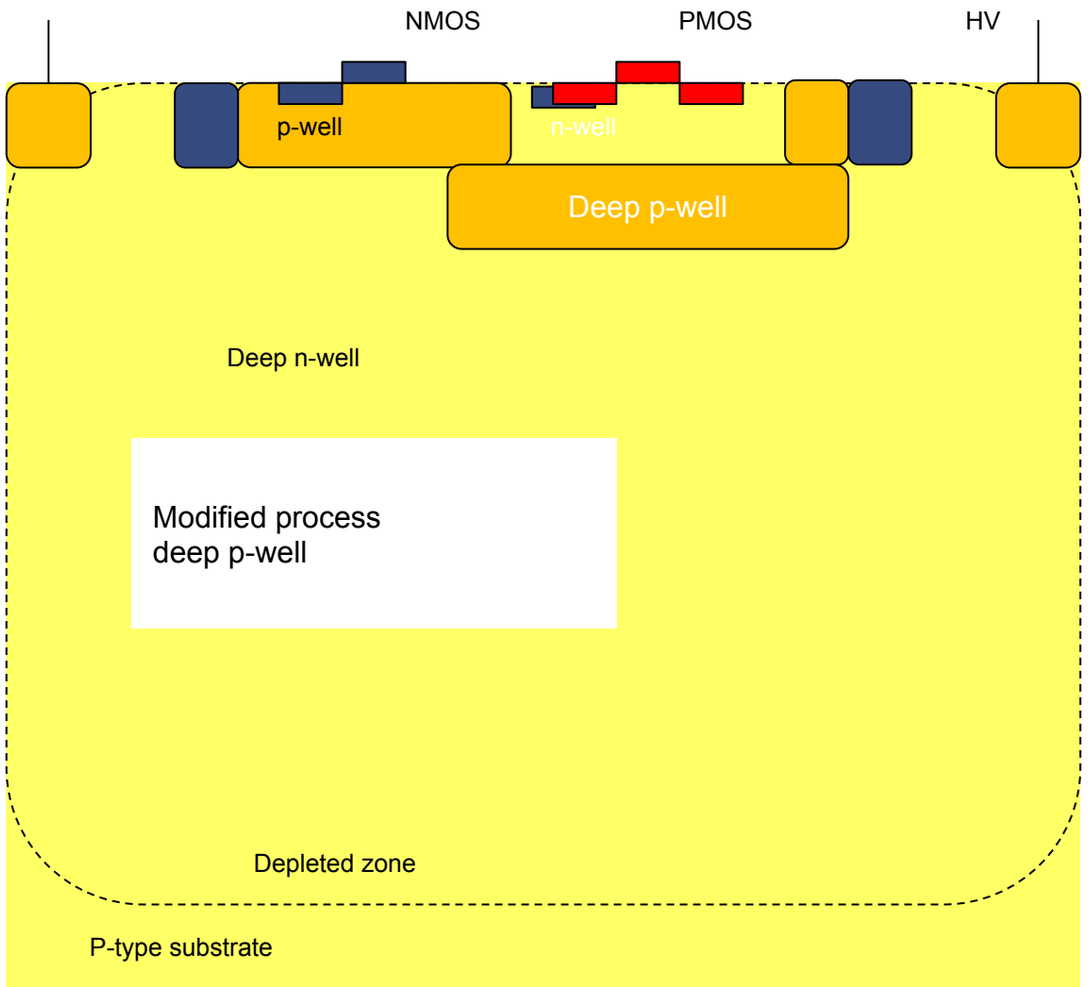
- Needs deep p-well
- Works with smaller bias current





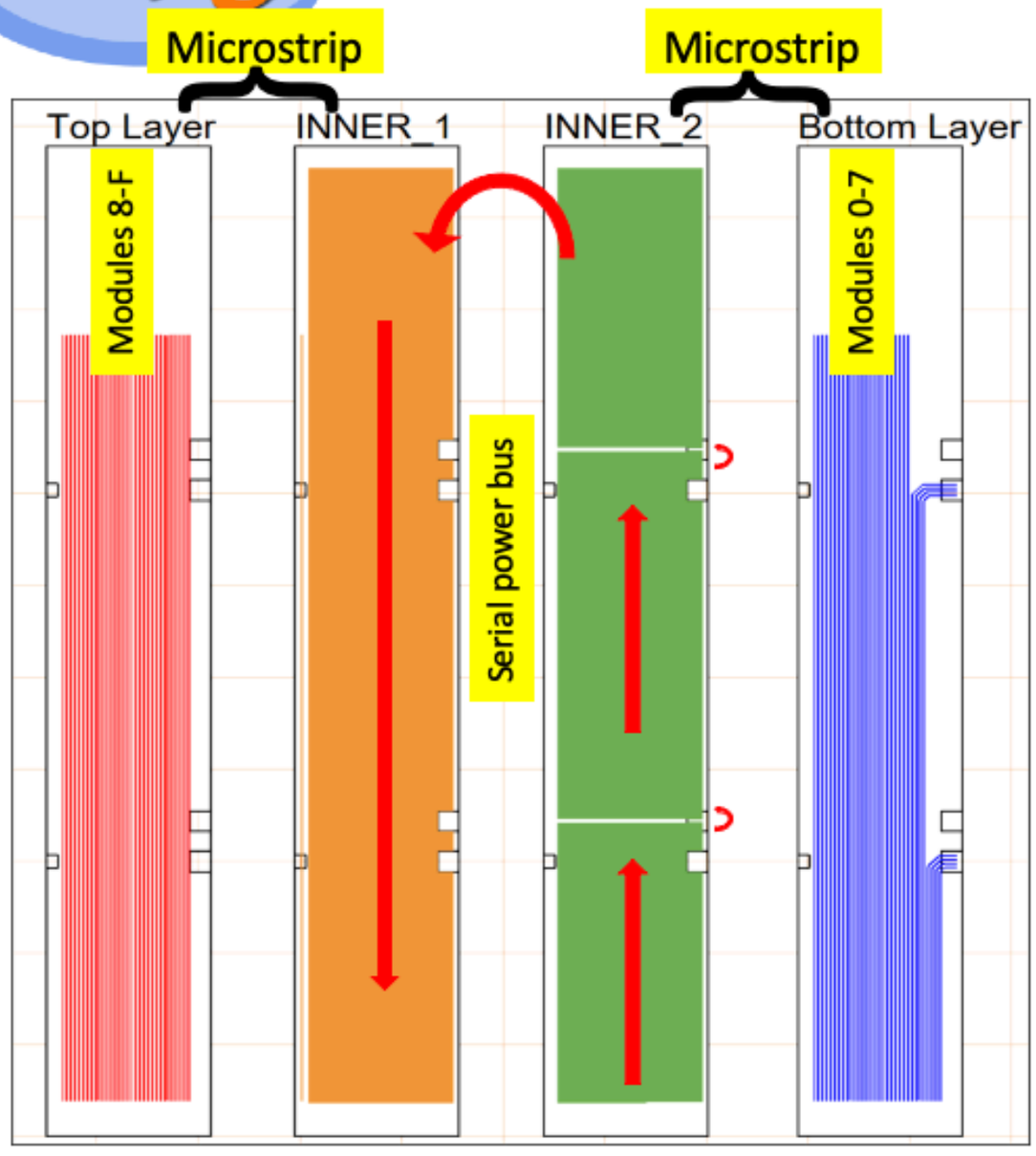
Ivan Peric: *UK-CEPC tracker workshop*

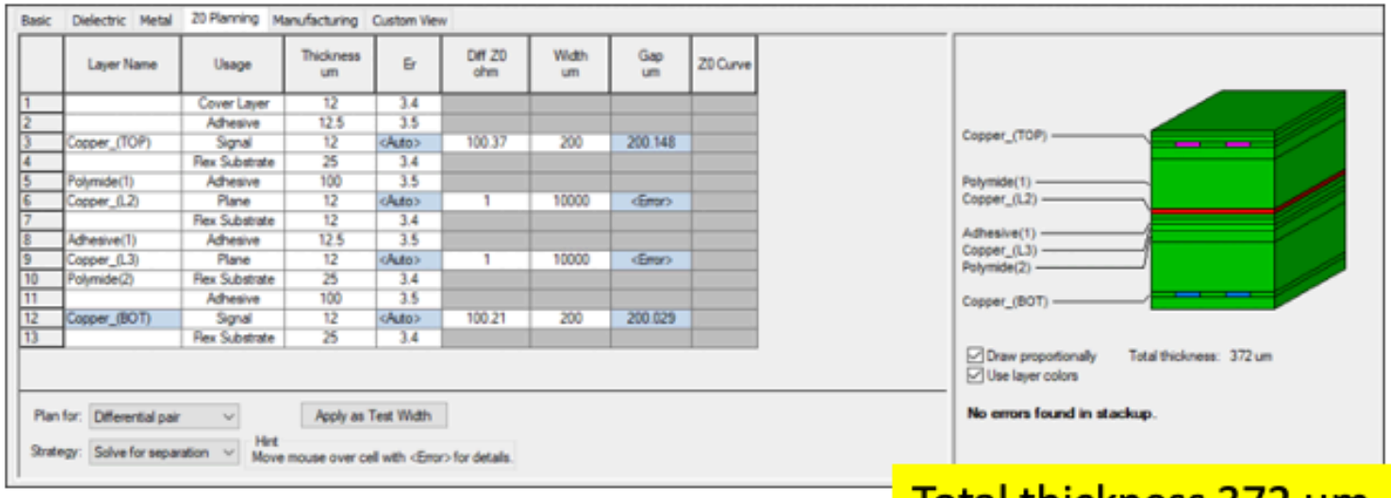




Stave electrical bus properties

Stave electrical bus properties





Total thickness 372 µm
Total copper 36 µm

Signals:

- LVDS trace width = 200 µm
- resistance for a length of 70 cm ~ 5 Ω
- Stack-up minimizes cable thickness,
  but bottom signal lines face module hybrid circuit

Power:

- Plane width = 14 mm
- resistance for 70 cm~ 0.08 Ω
- current I~2 A (@ 20 + 3 °C)

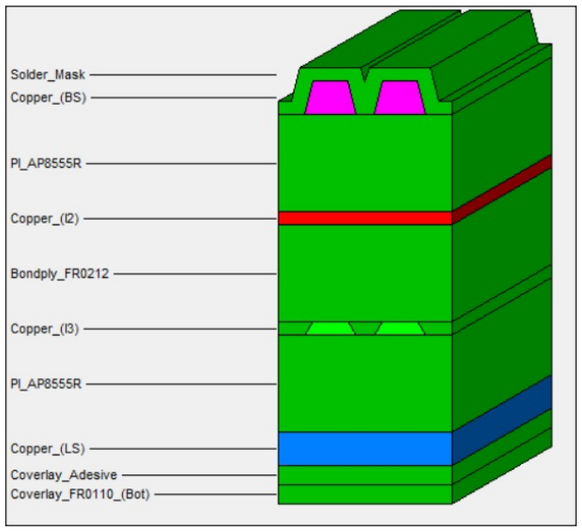
INFN PISA
Istituto Nazionale di Fisica Nucleare
Sezione di Pisa

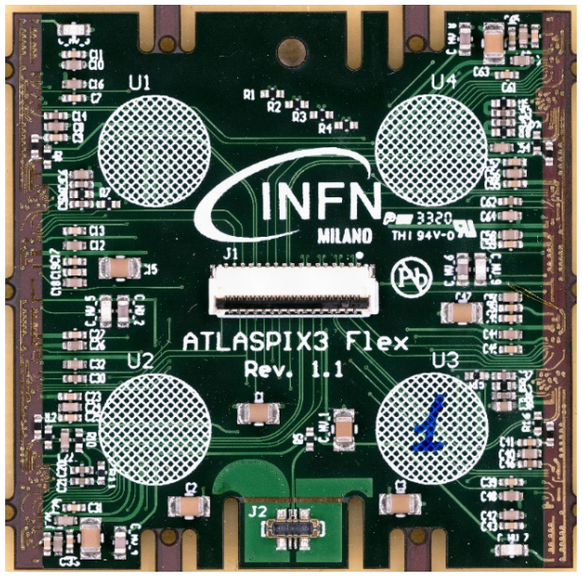
INFN-Milano/Pisa

Module PCB flex

Description of the flex: stackup

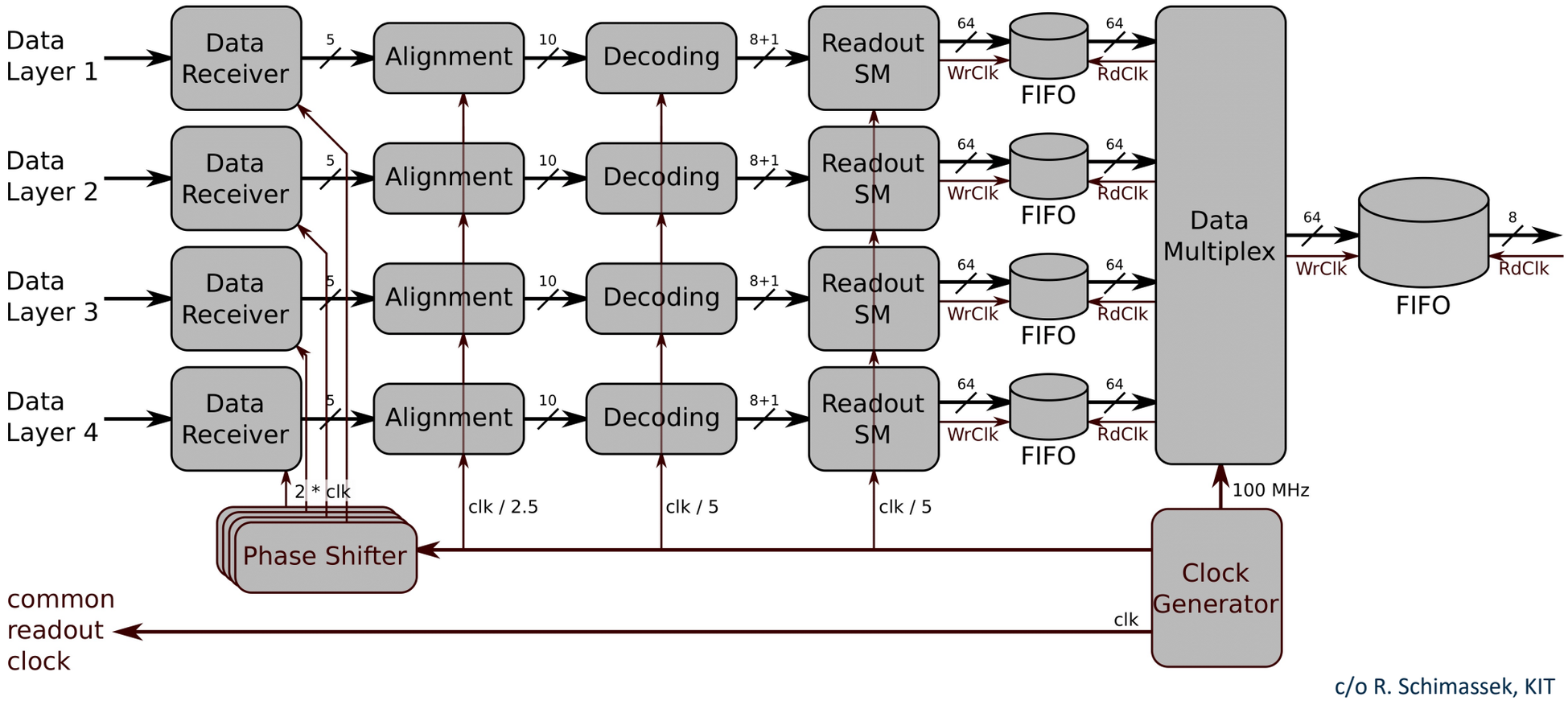
- In this initial version emphasis is on signal integrity, rather than minimizing material:
  - 4 layers
  - External layers copper: 43 um
  - Inner layers copper: 18 um
  - Total thickness: 565 um
  - Via diameter: 300 um
  - Via hole size: 150 um
- 100 ohm **impedance match** on differential lines both on the Top and the Inner layer





Firm-/Software changes for quad

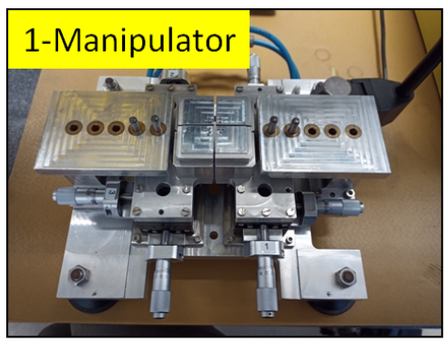
- Firmware:
  - Multiplication of the **elemental structure** for the single chip
- Software:
  - Configuration with SPI and CMD
  - Chips can be configured **simultaneously** or **individually**

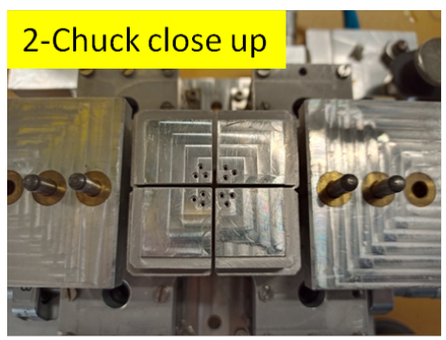


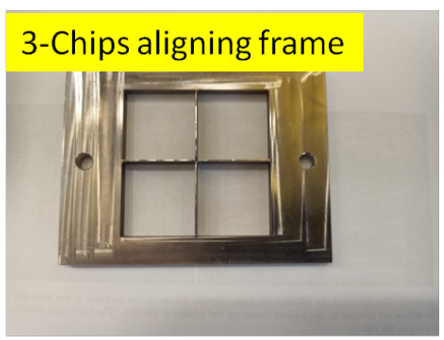
c/o R. Schimassek, KIT

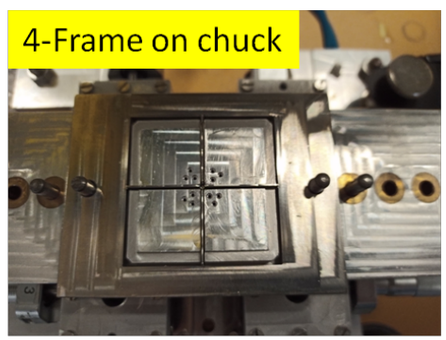
Assembly procedure

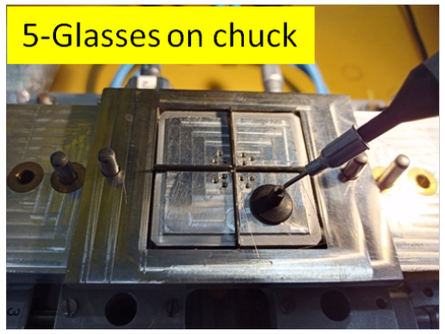
- Shown with **glass squares**: same procedure also used for real module assembly
- Gap between chip of **100 um ± 50 um** has been achieved

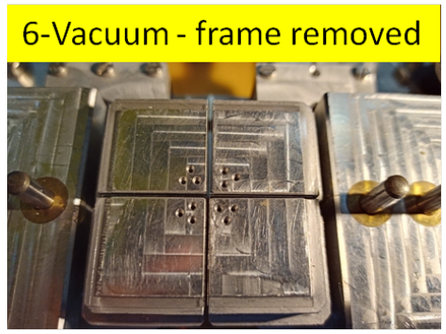


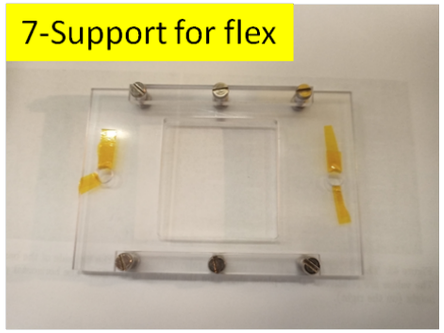


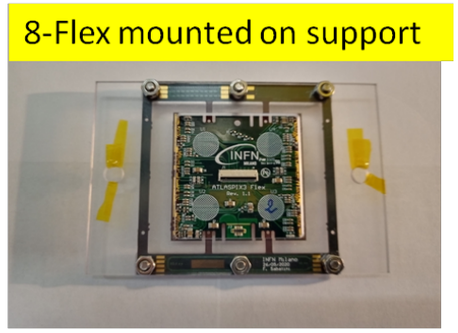


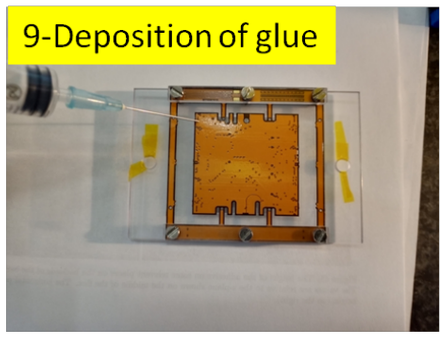


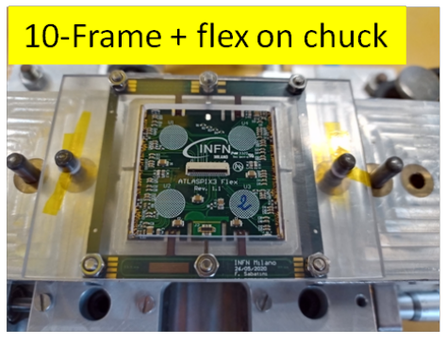


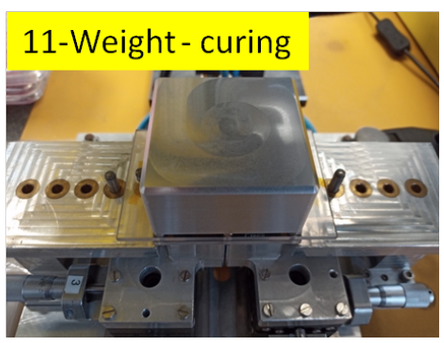


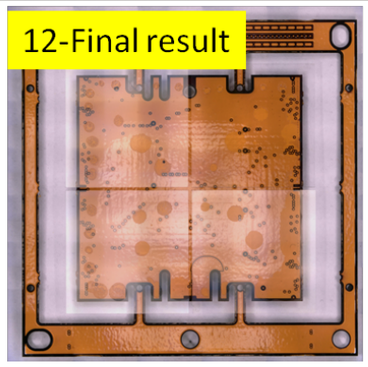












Improvements for sensors beyond ATLASPix3

Ivan Peric

- Options:
  - Different pixel sizes
  - Different amplifier types (NMOS and PMOS)
  - Different comparator types (NMOS, CMOS and distributed)
  - Different TDAC types (placed in pixels or in periphery)
- Fixed improvements versus ATLASPIX3
  - Hit buffer cell with time to digital converter (supports time resolution ~ 100ps), TDAC, differential receiver for distributed comparator
  - Possibility of daisy-chain readout – one chip acts as data collector for another
  - Possibility to bias pixel n-well with voltage higher than 1.8V, and to bias pixel p-well with voltage lower than 0. It reduces capacitance. Reduced capacitance means better time resolution for the same power consumption.
- PMOS amplifier has lower noise than the NMOS amplifier when the bias current is high (~10µA). It has better (smaller) time walk for threshold of nine sigma noise. PMOS amplifier is more suitable for larger pixels i.e. pixels with larger capacitance (larger than 150fF)
- NMOS amplifier has better time walk for nine sigma noise for small bias currents (~1µA). It is a good choice for small pixels with little capacitance. Some risk because NMOS has more flicker noise and because we have little experience with this amplifier type
- NMOS comparator is the standard comparator type we used so far. It has some disadvantages: rather high current consumption (~3µA), larger delay than CMOS comparator, need for additional bias voltage of 2.1V, output signal of reduced amplitude, it occupies large area and causes large detector capacitance
- CMOS comparator does not have the disadvantages of NMOS comparator, it is faster for the same current consumption, potentially more radiation tolerant, smaller. Disadvantage is that CMOS comparator needs additional deep p-well implant (iso-PMOS option). This implant will be produced by TSI for the first time – there is some risk that it does not work.
- Distributed comparator has only three transistors in the pixel and adds very little capacitive load. The receiver and TDAC are placed in the hit buffer at the periphery. It is fast, low power and does not require additional iso-PMOS. The disadvantage is that it requires two lines per pixel to connect it with the hit buffer. This is not a problem for pixels larger than 50µm x 150µm.
- TDAC can be placed in pixel but it adds detector capacitance. TDAC can also be placed at the periphery, in this case it makes periphery slightly larger