CEPC Low Level RF R&D

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Institute of High Energy Physics

On behalf of LLRF CEPC R&D team

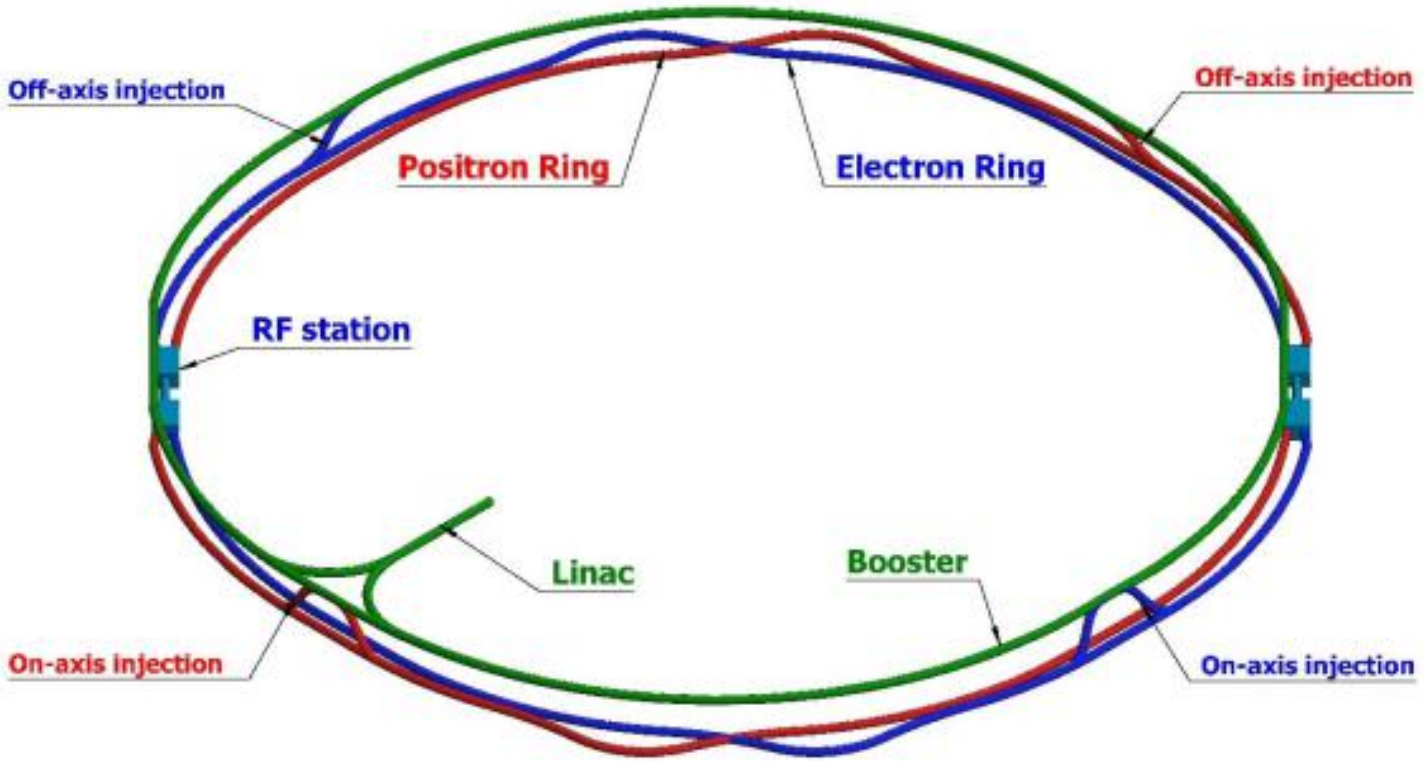
2021-11-09

Outline

- ☐CEPC LLRF overview and requirements
- ☐CEPC LLRF research and development
- ☐Future plan

CEPC Layout

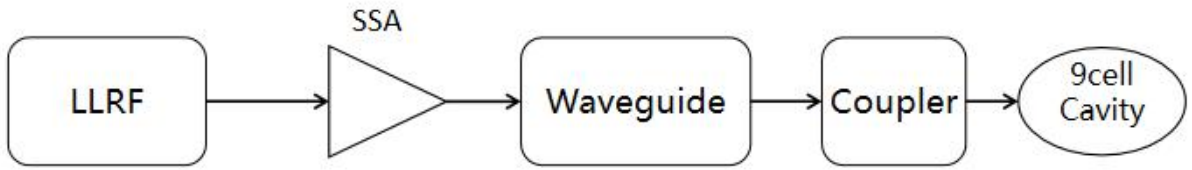
LLRF for:
Collider SC Cavities;
Booster SC Cavities;
Linac NC Acc-tubes;



from CEPC CDR

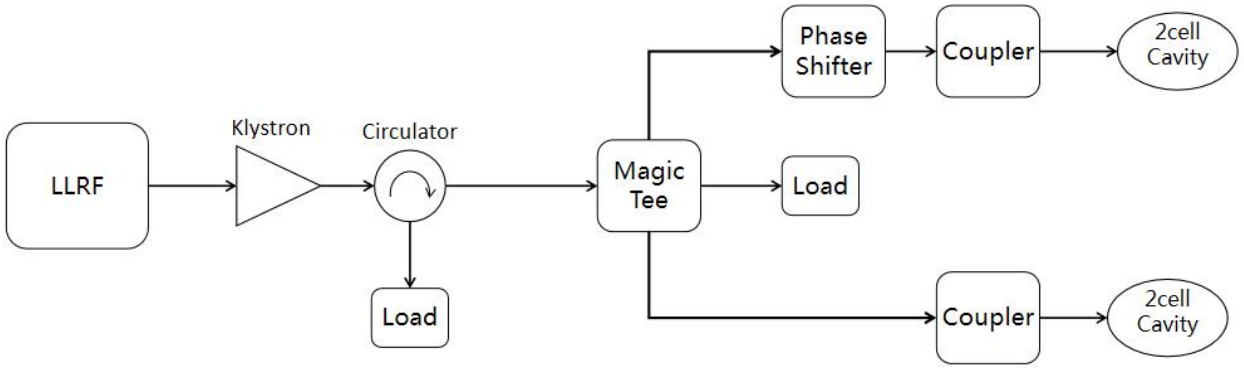
Superconducting Cavities of CEPC Accelerator

Booster	H	W	Z
RF frequency [MHz]	**1300**	1300	1300
Cavity number	96	64	32
Injection and extraction cycle [s]	13.5	16.5	26.5
QL	1E7	1E7	1E7
Lorentz force detuning [Hz]	-337.3	-111.0	-117.5
Microphonics detuning [Hz]	20	20	20
Cavity bandwidth [Hz]	**130**	130	130
Cavity time constant [μs]	2449	2449	2449
Injection cavity voltage [MV]	0.9	1.4	2.8
Extraction cavity voltage [MV]	19.1	10.9	11.3
SSA power [kW]	**25**	25	25
SSA number	**96**	64	32



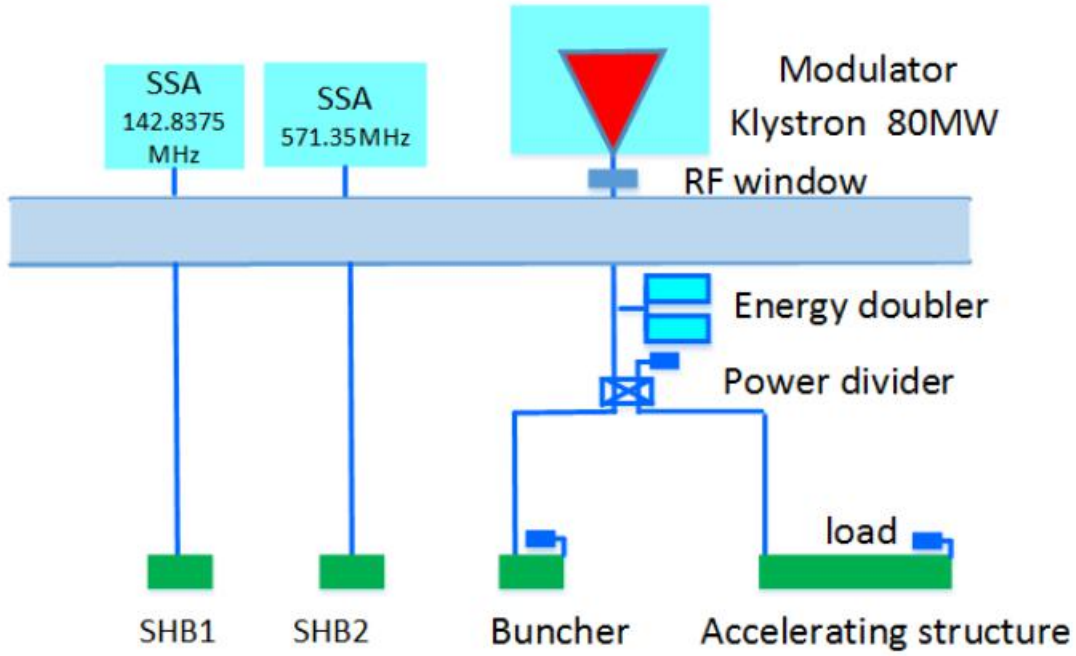
Superconducting Cavities of CEPC Accelerator

Collider	H	W	Z
RF frequency [MHz]	**650**	650	650
Cavity number	240	216	120
Beam Energy [GeV]	120	80	45.5
Optimal QL	1.5E6	3.2E5	4.7E4
Optimal detuning [kHz]	-0.2	-1	-17.8
RF voltage [GV]	2.17	0.47	0.1
Cavity bandwidth [kHz]	**0.4**	2.0	13.7
Beam current / beam [mA]	17.4	87.7	460
Cavity operate gradient [MV/m]	19.7	9.5	3.6
Synchrotron phase [deg]	37.1	43.7	68.9
Input power / cavity[kW]	**250**	278	275
Klystron number	**120**	108	60



Linac MW system parameters

SHB1 Freq [MHz]	**142.8375**
Power [kW]	10
SHB2 Freq [MHz]	**571.35**
Power [kW]	7
MW Freq [MHz]	**2860**
Power [MW]	80
Pulse width [us]	4
Repetation Rate	100
MW Freq [MHz]	**5720**
Power [MW]	50



Courtesy by ZHANG Jingru, this conf, CEPC linac injector status and R&D

LLRF Requirements

Booster/Collider requirements	Value
Phase stabilization	0.1deg (rms)
Amplitude stabilization	0.1% (rms)
Run mode	CW

Linac	Value
Phase stabilization	0.2deg (rms)
Amplitude stabilization	0.2% (rms)
Run mode	Pulsed

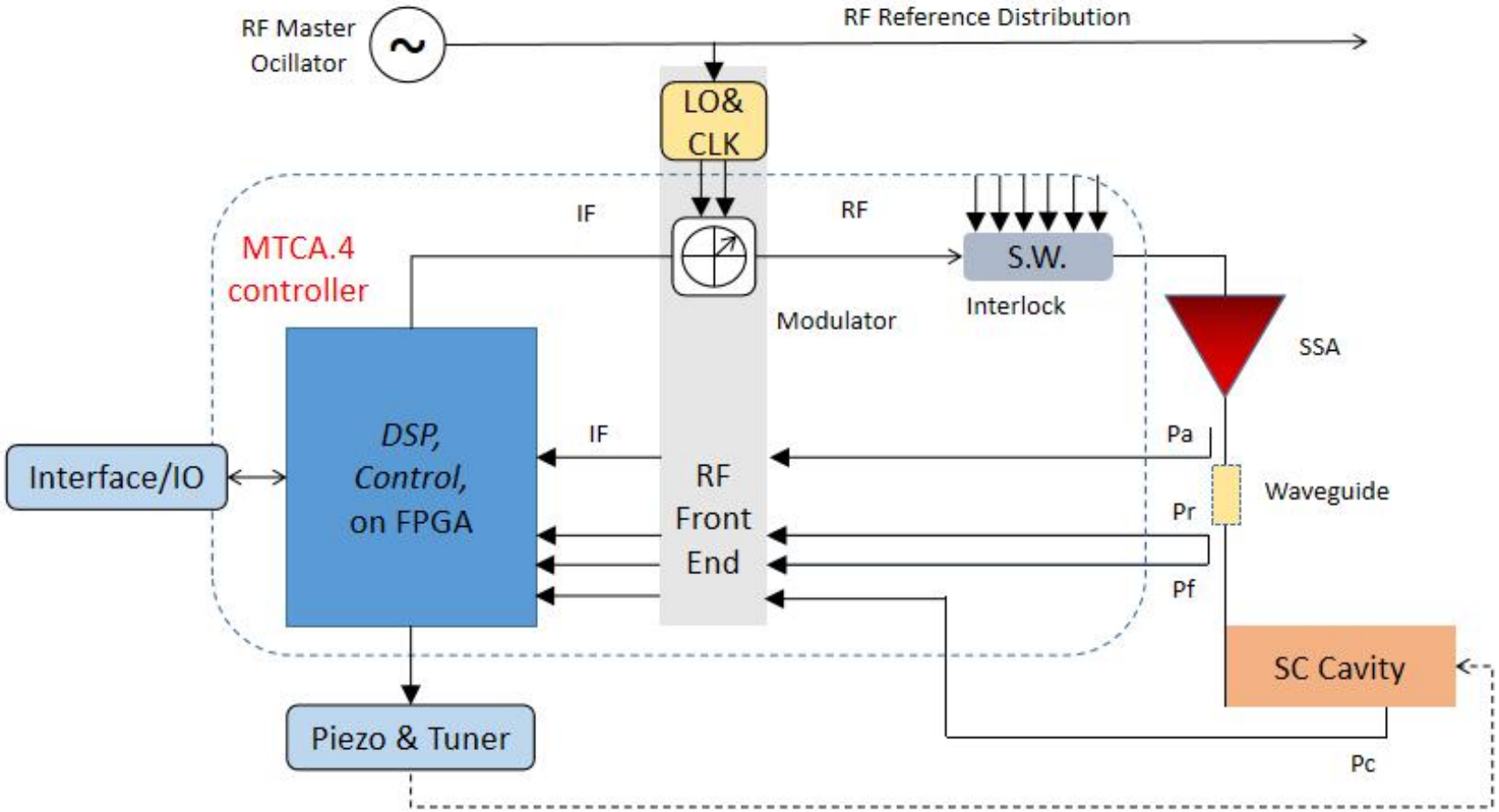
Aim of LLRF:

- control of phase/amplitude/frequency
- feedback/feedforward
- beam loading compensation
- quench detection
- monitoring of forward/reflected/pickup power
- calculate vecter-sum of double-cavities driven by one klystron
- life protection of klystron
- to/from interlock/BI/timing system
- remote diagnose and control
- sufficient smart and automation
- high reliability, stability
- easy maintanence

CEPC LLRF research and development

LLRF Structure for Booster cavities

Similar of Collider cavities/Linac except for high power sources and cavities

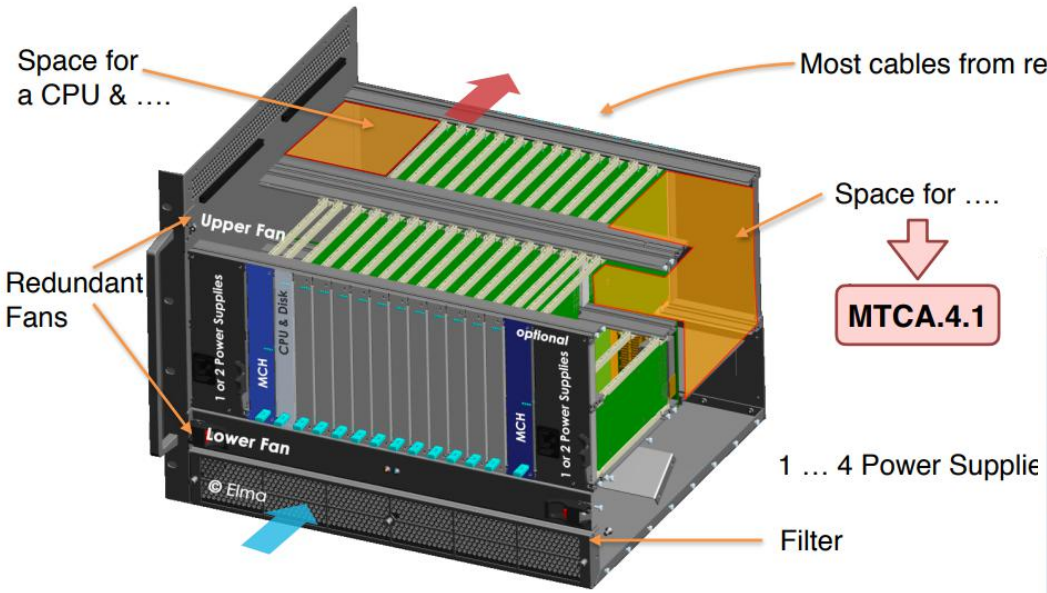


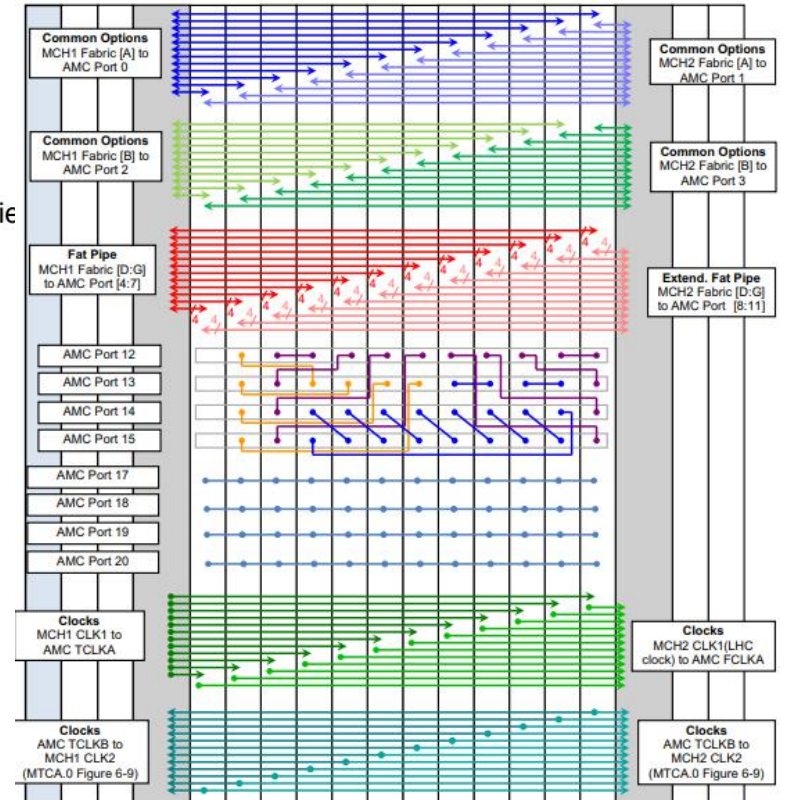
Why we choose MicroTCA.4 standard

- Big project like CEPC, maintanence and reliability are ulta important, as many controller stations exists all over the machine km away. And the trip rate should be considered (not zero), on-site maintance every time will not acceptable.
- So LLRF system MUST remote accessable through Ethernet, diagnose remotely and control directly into the electronics board level and crate/rack level - management of the crates. Automatic operation of the hardware system, stability 99.999%(with 2x redundancy).
- LLRF system MUST monitor all the signals of the RF/cavity system, 125MHzx16chx2Bytes=4GBytes, VME/CPCI/PXI... will not fulfill the task.

	Data rate	management	remote	stability	Cost	vendor	Clock
MicroTCA.4	10GB/s-40GB/s	IPMI	Yes	99.999%	$$$	medium, full standarized	trigger, WR..
OpenVPX	10GB/s	IPMI, not req	Yes	99.9%-	$$$$$	customized	Yes
CPCI-Serial	10GB/s	IPMI, not req	Yes	99.999%?	$$$	few	No
PXIe	10GB/s	No	No	?	$$	many	No

MicroTCA.4: A Modular Crate System

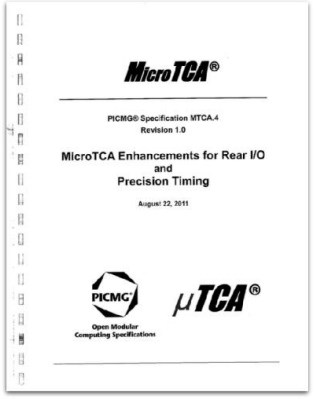




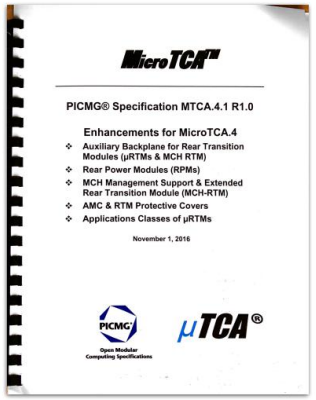
Courtesy by Kay Rehlich, DESY

MTCA Specifications

MicroTCA.0



MicroTCA.4



MicroTCA.4.1

Community members

欧洲	Euro-XFEL/FLASH	德国DESY
	ESS	瑞典Lund U.
	FAIR	德国GSI
	SOLEIL	法国ESRF
	Diamond	英国DLS
	SPS	瑞士CERN
	ITER	法国ITER
	MYRRHA	法国IPNO
	CMS	瑞士CERN
美洲	APS-U	美国ANL
	FRIB	美国MSU
	LCLS-II	美国SLAC
	SNS	美国ONL
	Sirius	巴西LNLS
日本	KEKB/cERL/STF	KEK
	SPring-8	RIKEN
	JPARC	JPARC
中国	SXFEL/DCLS	SARI
	C-ADS/BEPCII/HEPS	IHEP
	NSRL	NSRL

LLRF Control System @ PAPS for 650MHz CEPC SC Cavities

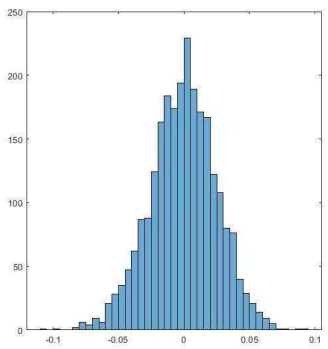
LLRF system includes:

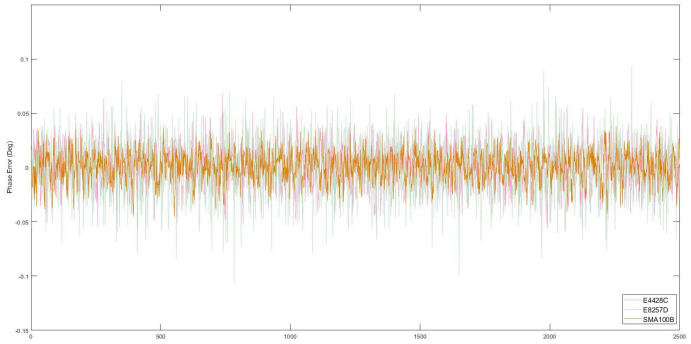
- MicroTCA.4 based hardware, very high stability and reliability, maintainance, remote managable, 10Gb data bandwidth;
- sampling all signals(>18) of powers source and couplers and cavities and HOMs;
- control of piezo/motor for frequency stablility;

LLRF Rack

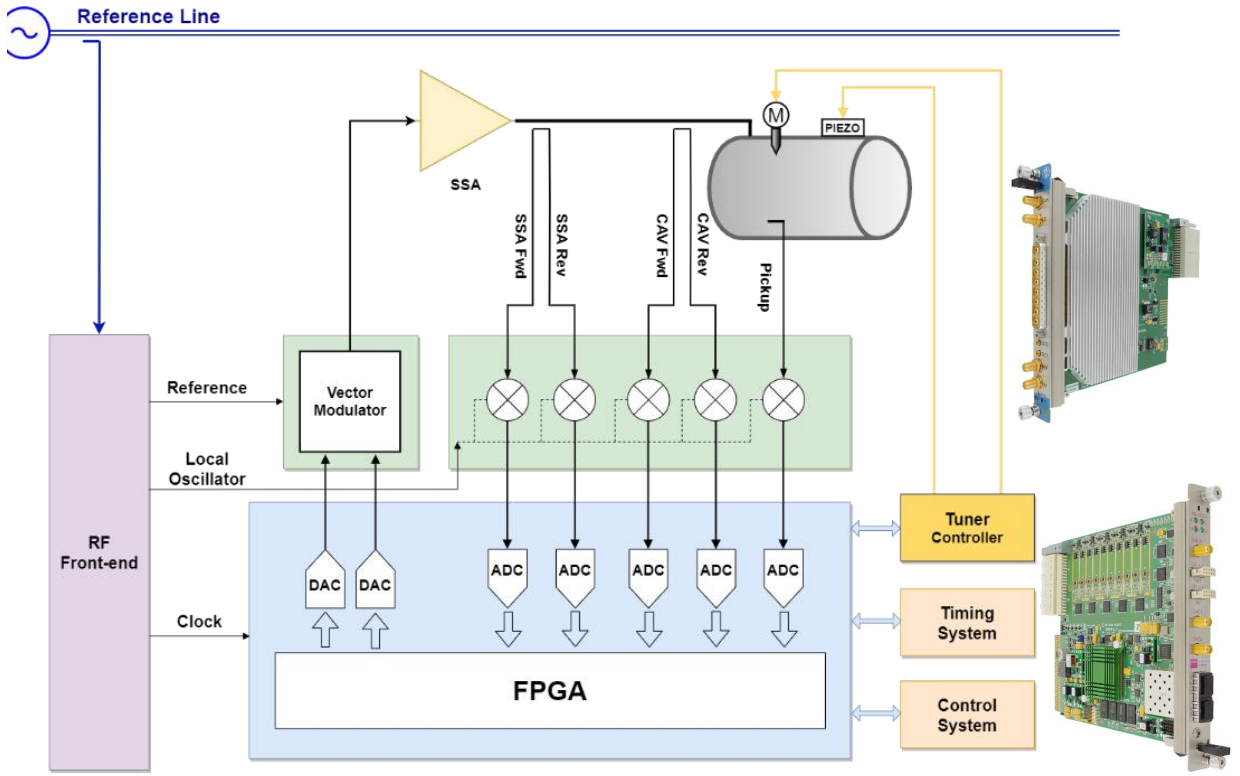
LLRF hardware and test for SC cavities

LLRF test: phase stability :<0.02°rms





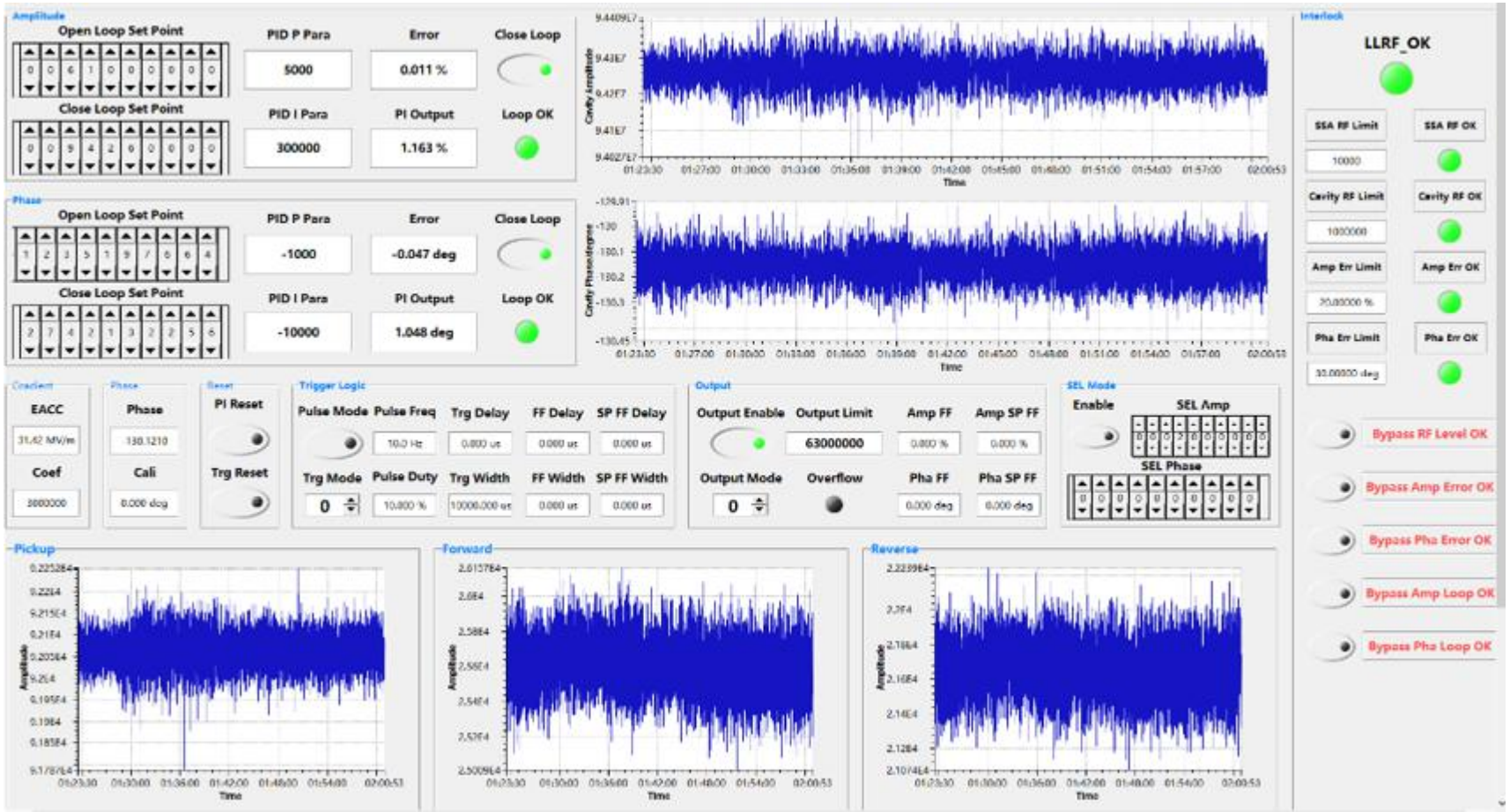
- Ref: 650MHz ;
- Crate: nVent-9U, PS: Wiener-1kW;
- MCH/CPU: NAT MCH-PHY80/RTM;
- SIS8300L2/DWC8VM1 from Struck;
- 8 ADC ; 2 DAC ;
- Timing: trigger through backplane;



LLRF has been working for horizontal test of CECP Cavities

Generate drive signals;
Monitoring all signals;
Vacuum, radiation recorded;
Cryo ；

Typical User Interface of the LLRF system using CSS based on EPICS

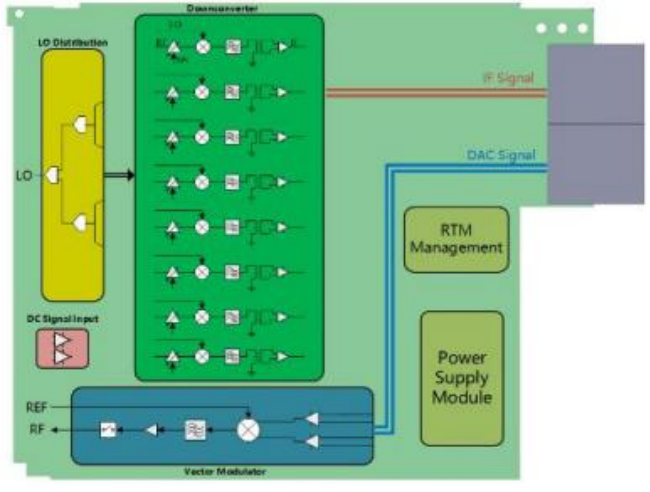


LLRF development for Linac

LLRF development for Linac

- Frequency bandwidth:300MHz-6GHz ;
- 8 ch ADCs ; 2 ch DACs ;
- RF Front-end: generate LO and CLK ;
- 3U MicroTCA.4 crate ;

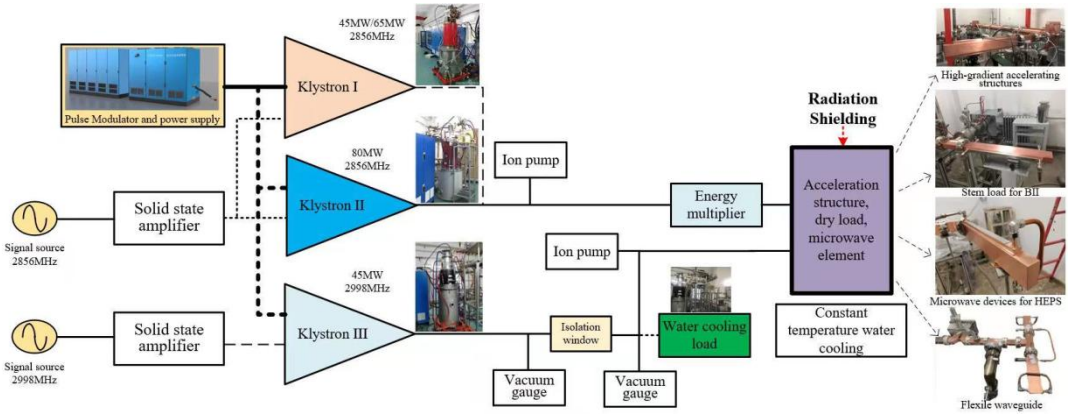
Downconverter
could be used for 2860MHz and 5720MHz, 1.3GHz



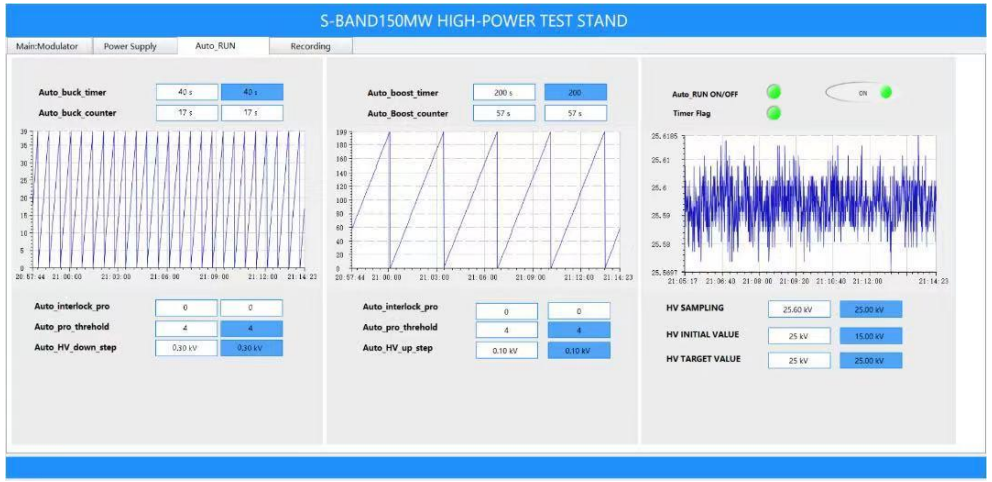
For Klystron and Acc tube conditioning (S-band)

LLRF development for Linac

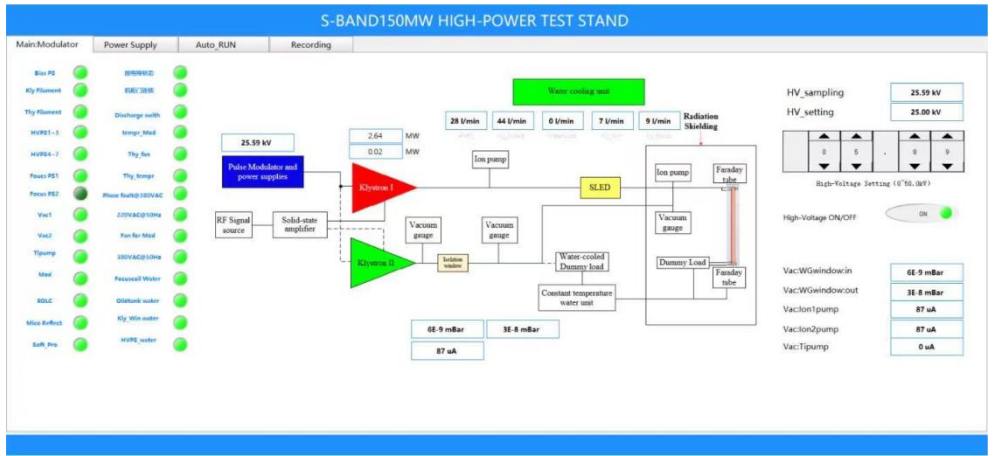
Platform for conditioning and test of Linac



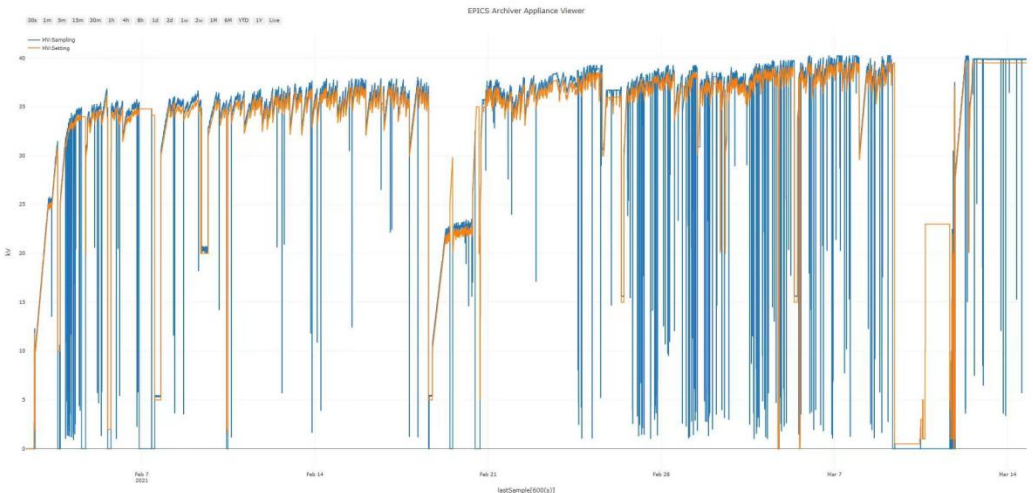
User interface of auto-conditioning



automatic conditioning by PLC

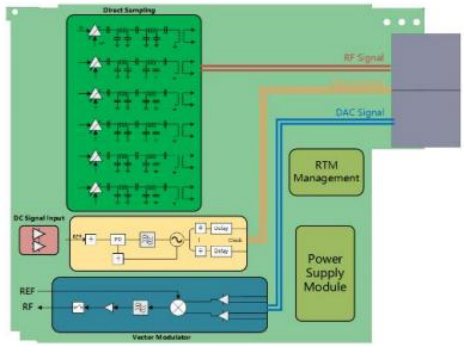


High Voltage during conditioning

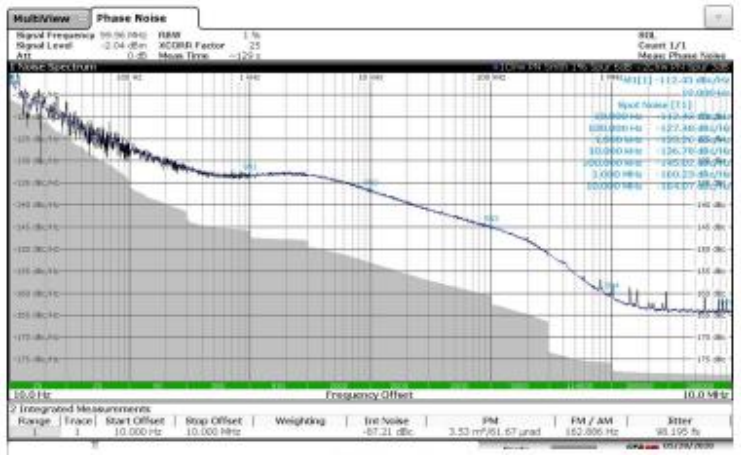


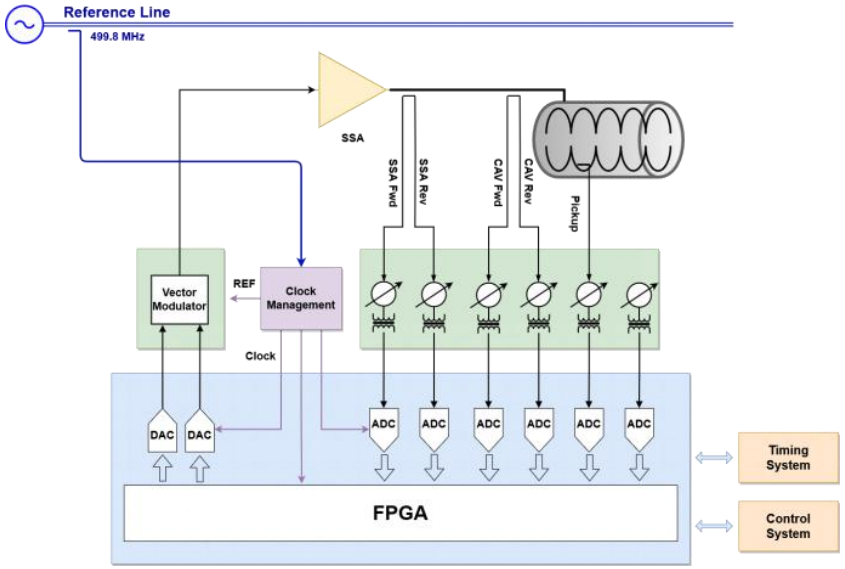
LLRF development for Linac

- Direct sampling RTM board
- Input bandwidth: 0-650MHz : **for both SHB and 650MHz SC Cavities;**
- 99.96MHz clock jitter: 98fs（10Hz-10MHz）；
- 6 ADC，2DAC；
- need no LO, CLK module integrated in one board;



Courtesy by Gan Nan



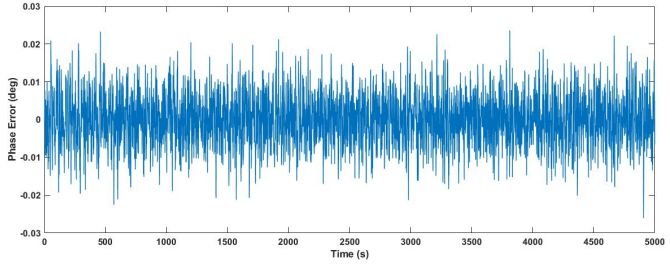


LLRF development for Linac

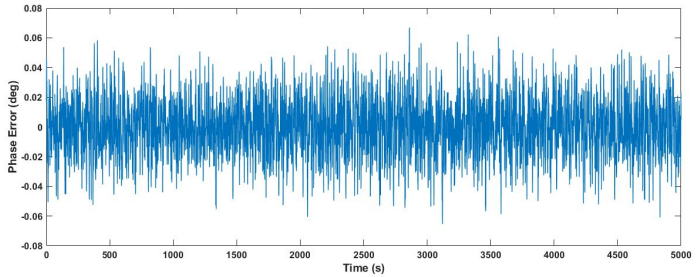
Courtesy by Gan Nan

preliminary tested with Struck SIS8300L2

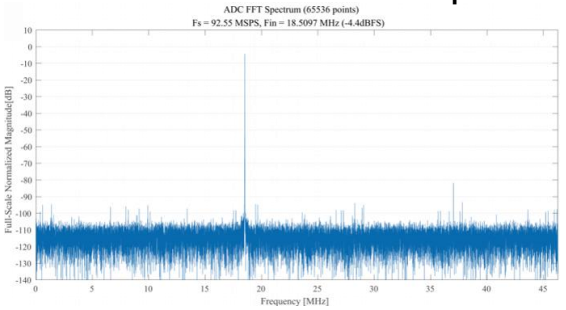
166MHz DS
P-P Err < ±0.02°
RMS Err = 0.007°



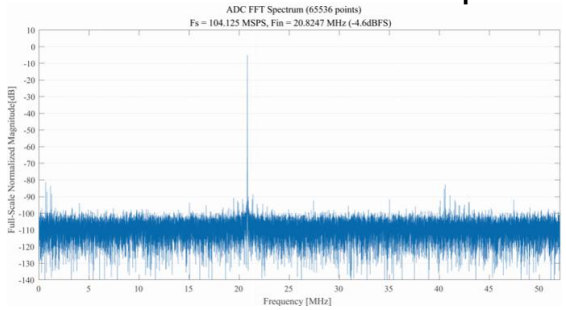
499MHz DS
P-P Err < ±0.07°
RMS Err = 0.019°



166.6MHz direct sampled



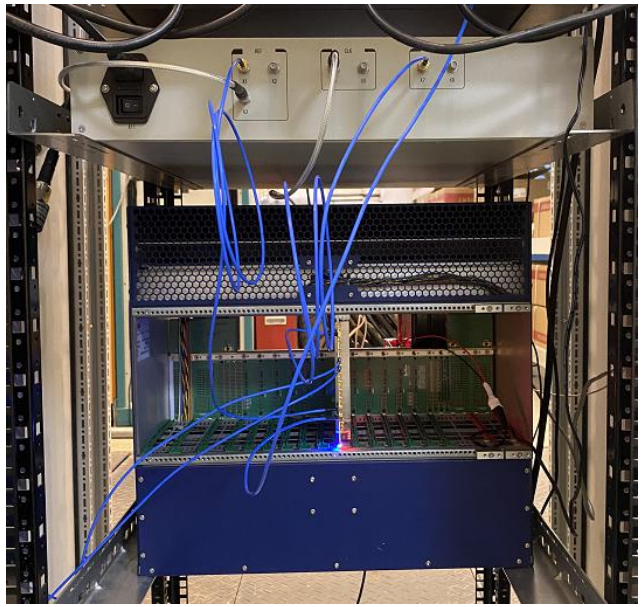
499.8MHz direct sampled



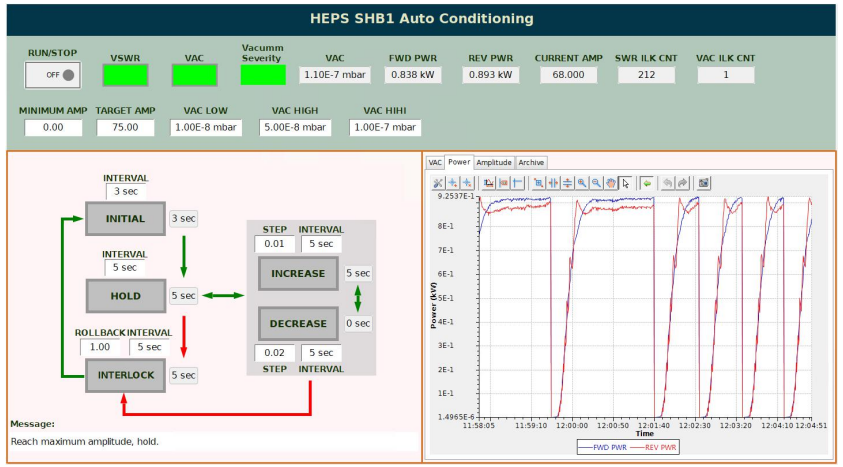
SFDR better than 80dB

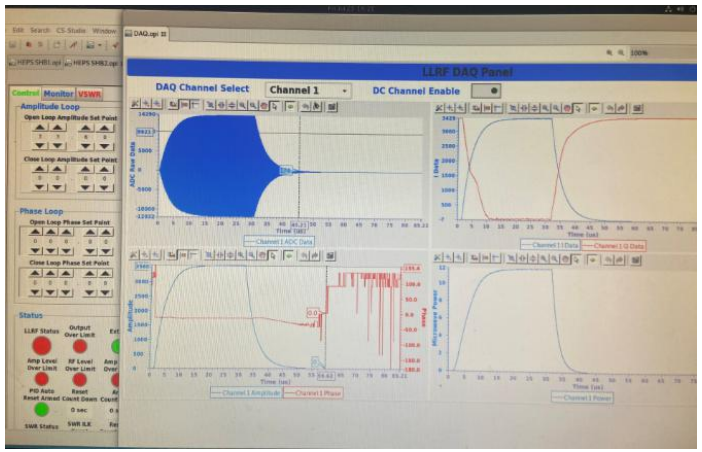
LLRF development for Linac

DWC RTM on HEPS TB
@2998.8MHz



DS RTM on HEPS SHB TB
@166.6/499.8MHz





LLRF development for Linac

2019.10

Signal Fanout

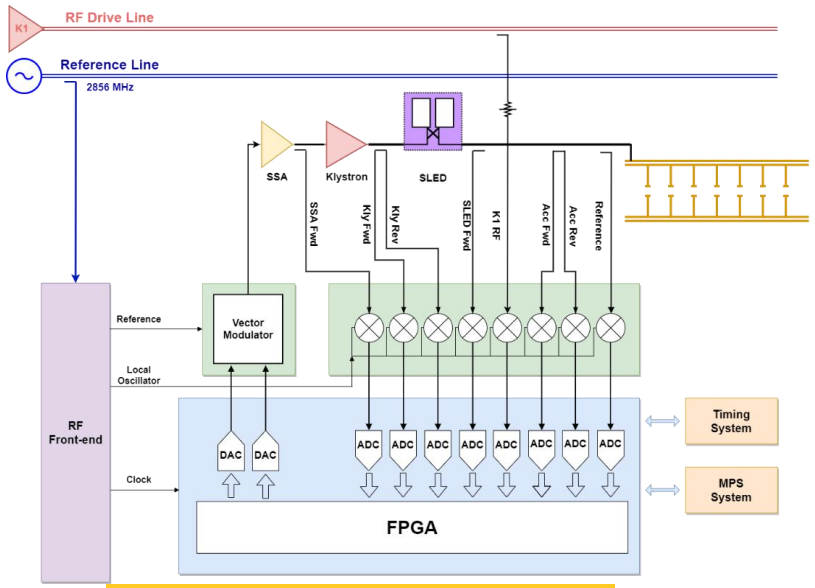
Power Meter

MicroTCA
LLRF Crate

Front-end

SSA

UPS



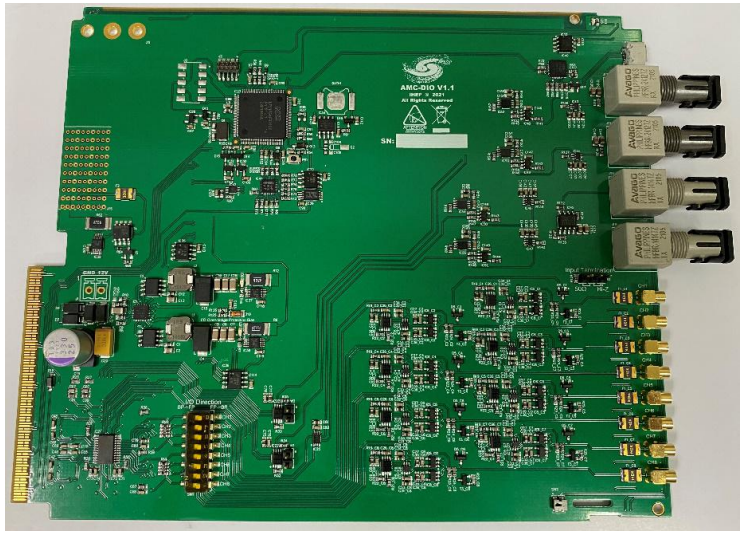
LLRF for S band Linac

- 8ADC ; 2DAC ;
- vector modulator ;
- Ref: 2856MHz ;
- 8 microwave monitor ;
- 2 HV/I monitor ;
- Trigger ;
- digital PSK for SLED ;
- fully digiital ;

- Y20-Y21, 6 new S-band LLRF system installed on BEPCII Linac and in operation stable

LLRF development for Linac

- **Timing/interlock fanout board**
- **used for local timing of modulator/SSA/LLRF/power meter...**
- using openmmc;
- work well with MicroTCA.4 crates;
- 8 electro-IOs & 4 optical-IOs to backplane MLVDS



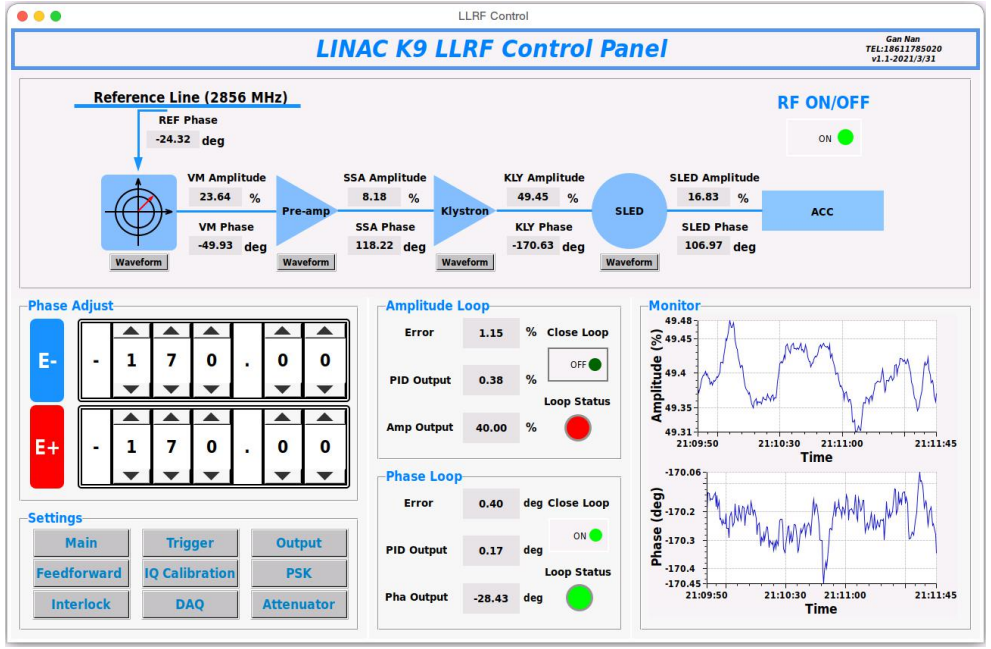
Remote monitor and control
FRU, HOTSWAP, PAYLOAD, SDR(TEMP, VOLTAGE, CURRENT), GPIO

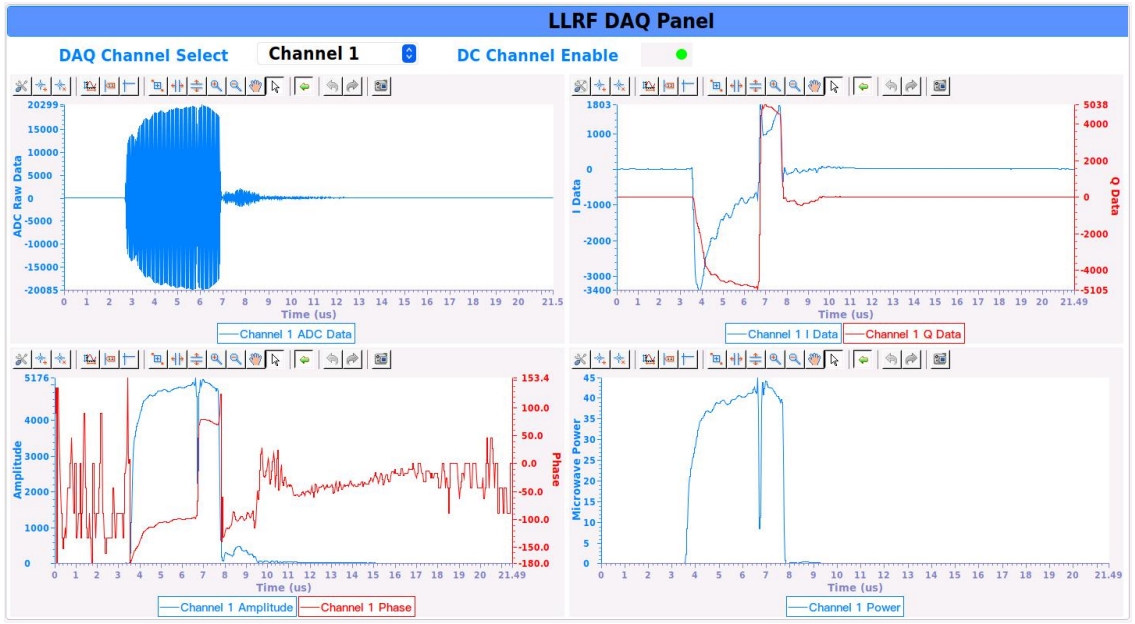
```
nat> show_sensorinfo 8
Sensor Information for FRU 8 / AMC4
=====================================================================
  #   SDRType  Sensor Entity Inst  Value   State    Name
---------------------------------------------------------------------
  -   MDevLoc          0xc1  0x64                   DIO 1.0
  1   Compact  0xf2    0xc1  0x64  0x01             HOTSWAP AMC
  2   Full     Voltage 0xc1  0x64  3.280 V    ok     AMC +3.3V
  3   Full     Voltage 0xc1  0x64  4.984 V    ok     AMC +5.0V
  4   Full     Voltage 0xc1  0x64  0.000 V    <=lnr  RTM +12V
  5   Full     Current 0xc1  0x64  1.824 A    ok     AMC +3.3V Curr
  6   Full     Current 0xc1  0x64  0.800 A    ok     AMC +5.0V Curr
  7   Full     Current 0xc1  0x64  0.000 A    ok     RTM +12V Curr
  8   Full     Temp    0xc1  0x64  27.5 C     ok     TEMP 1
  9   Full     Temp    0xc1  0x64  30.5 C     ok     TEMP 2
 10   Full     Temp    0xc1  0x64  27.5 C     ok     TEMP 3
 11   Full     Temp    0xc1  0x64  28.5 C     ok     TEMP 4
 12   Compact  0xf0    0xc1  0x64  0x10             HS 008 AMC4
---------------------------------------------------------------------
```

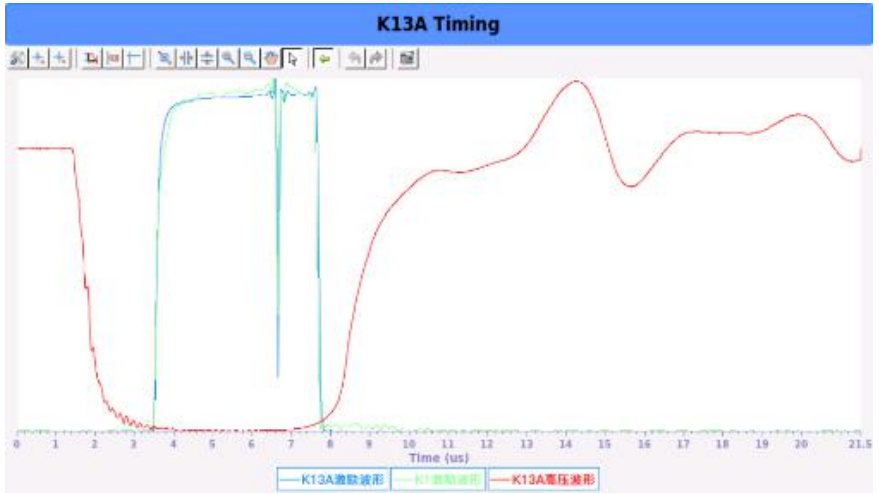
```
nat>show_fruinfo 8
----------------------------------------
FRU Info for device 8:
----------------------------------------
Common Header    : 0x01 0x00 0x00 0x01 0x07 0x10 0x00 0xe7
----------------------------------------
Internal Use Area : -
----------------------------------------
Chassis Info Area : -
----------------------------------------
Board Info Area          : at offs=8, len=48
Manufacturer(05)         : IHEP
Board Name(08)           : AMC-DIO
Serial Number(10)        : SN:000000
Part Number(04)          : DIO
FRU file ID(08)          : DIO-FRU
----------------------------------------
Product Info Area        : at offs=56, len=72
Manufacturer(05)         : IHEP
Product Name(08)         : AMC DIO
Product Number(08)       : DIO-1.0
Part Version(04)         : 1.0
Product Serial Number(10): SN:000000
Asset Tag(12)            : Generic FRU
FRU file ID(08)          : DIO-FRU
----------------------------------------
```

LLRF development for Linac

- Modulator HV/Current monitoring ; 1) perveance monitor 2) digital trigger btw HV and MW pulses ;
- timing through backplane , SSA/modulator/PSK ;
- input drive signal customized ;
- reverse protection ;
- feedforward ;
- I/Q modulator calibration ;
- interlock ;



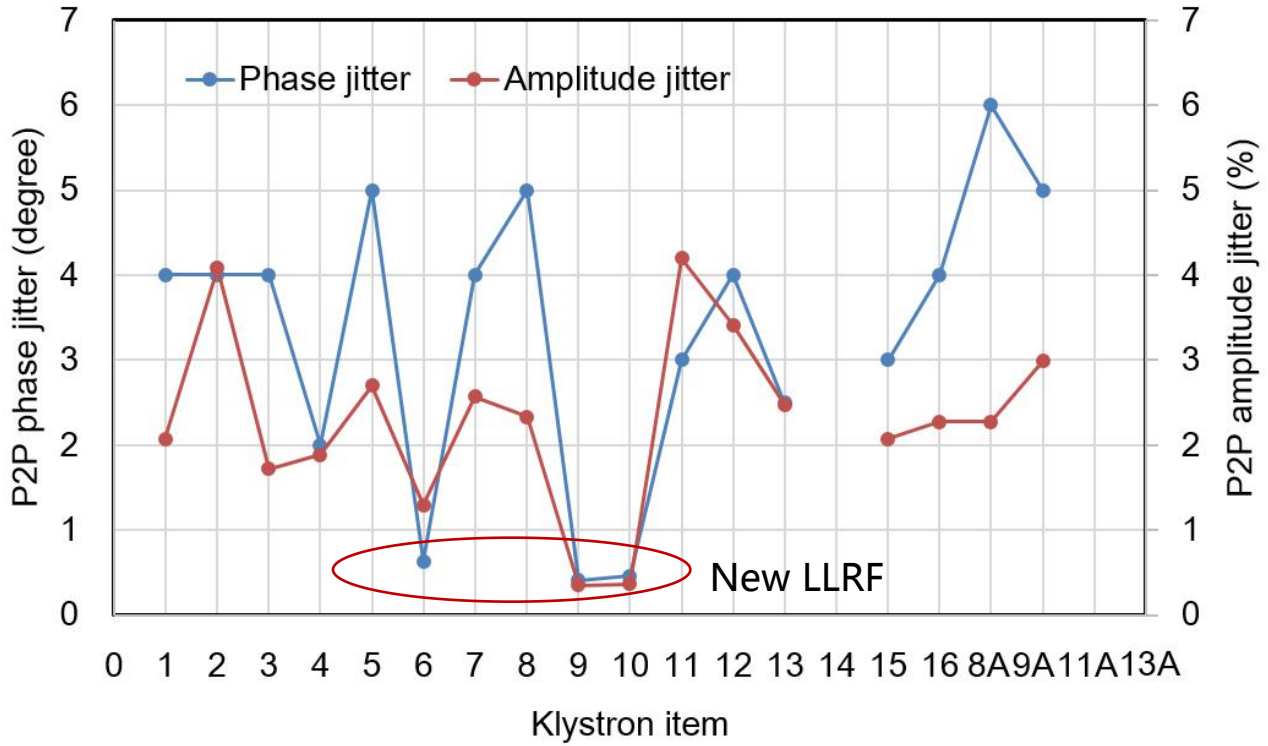




LLRF development for Linac

- Stability

  short term amplitude 1%(p-p)，phase 0.5°(p-p)，x4 better



Future plans

- A universal LLRF solution has been developed for 100MHz-6GHz applications, Optimize hardware and software will be continued to next version.
- 650MHz Cavities test and beam experiment @PAPS will continue in the next months;
- Cavity-Beam interaction and control, cavity control using modern control algrithom are being studied, will be tested on the real cavities and beam next.
- we will continue to strength the local MicroTCA.4 vendors, and an industry-research alliance is considered in China for big-science project control system.