65nm FEE ASIC R&D for TPC

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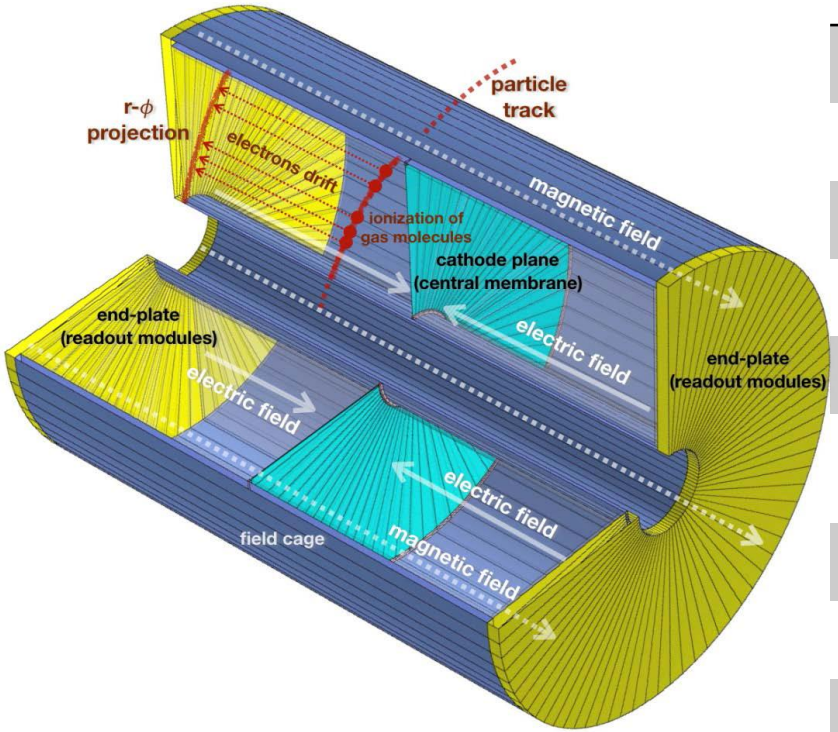
Outline

- Introduction
- Chip architecture and specifications
- The test progress on WASA_V0
- The design progress on WASA_V1
- Summary

Introduction



Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm × (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6mm) are needed, resulting ~1 million channel of readout electronics
- Need low power consumption readout electronics working at continuous mode

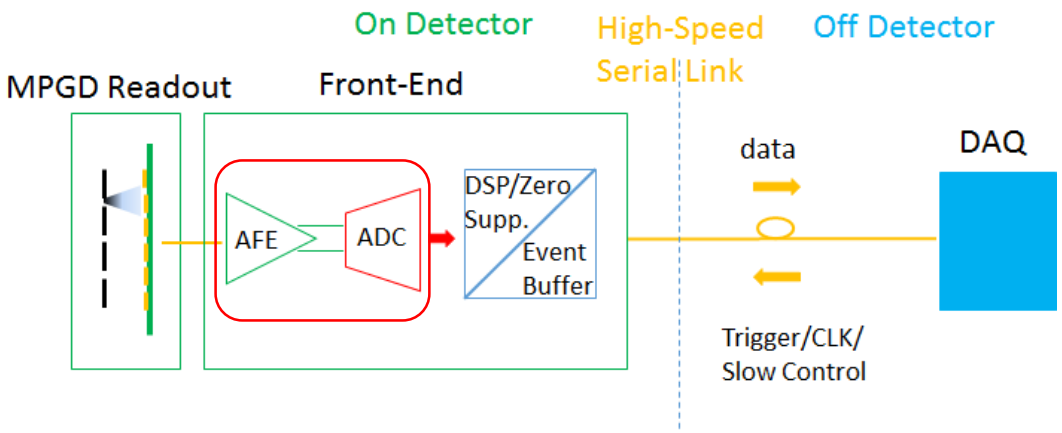
Current TPC Readout ASICs

- Waveform sampling (8-10 bit, ~10MS/s) is required for TPC signal processing
- Direct ADC sampling is more preferable than SCA for high rate applications
- Lower power consumption → less cooling → less material

	PASA/ALTRO	AGET	Super-ALTRO	SAMPA
TPC	ALICE	T2K	ILC	ALICE upgrade
Pad size	4x7.5 mm^2	6.9x9.7 mm^2	1x6 mm^2	4x7.5 mm^2
Pad channels	5.7 x 10^5	1.25 x 10^5	1-2 x 10^6	5.7 x 10^5
Readout Chamber	MWPC	MicroMegas	GEM/MicroMegas	GEM
Gain	12 mV/fC	0.2-17 mV/fC	12-27 mV/fC	20/30 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^2$	CR-$(RC)^4$	CR-$(RC)^4$
Peaking time	200 ns	50 ns-1us	30-120 ns	80/160 ns
ENC	385 e	850 e @ 200ns	520 e	482 e @ 180ns
Waveform Sampler	ADC	SCA	ADC	ADC
Sampling frequency	10 MSPS	1-100 MSPS	40 MSPS	20 MSPS
Dynamic range	10 bit	12 bit(external)	10 bit	10 bit
Power consumption	32 mW/ch	<10 mW/ch	47.3 mW/ch	8 mW/ch
CMOS Process	250 nm	350 nm	130 nm	130 nm

Chip Architecture

- In order to reduce the power consumption:
  - Using more advanced 65 nm CMOS process favoring digital logics
  - Reducing analog circuits:
    - CR-$(RC)^n$ →CR-RC, moving high order shaping to digital domain
    - ADC structure : pipeline → SAR (Successive Approximation Register)



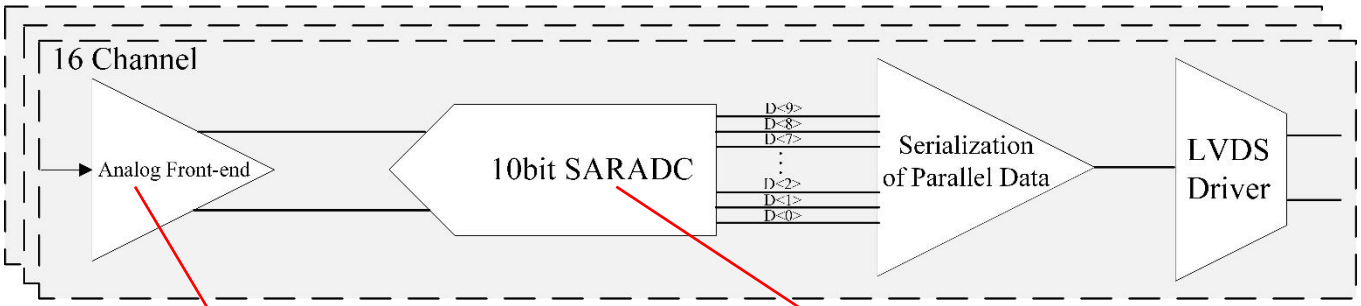
Specifications

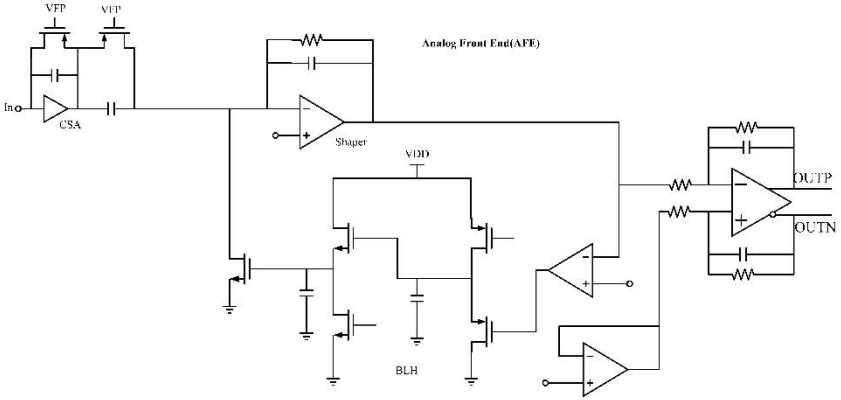
- Process: TSMC 65nm LP
- Power supply: 1.2V

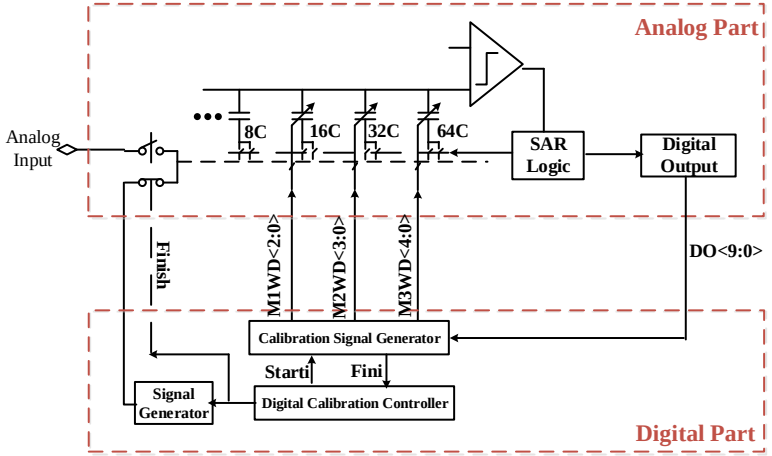
AFE(Analog Front-End)	
Signal Polarity	Negative
Detector Capacitance	5-20 pF
Shaper	CR-RC
Shaping Time	160 ns
ENC (Equivalent Noise Charge)	<500 e @ 10pF
Dynamic Range	120 fC max.
Gain	10-40 mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<1%
Power Consumption (AFE)	<2.5 mW/ch

SAR-ADC	
Input Range	-0.6 V ~ 0.6 V diff.
Resolution	10 bit
Sampling Rate	40 MS/s
DNL	<0.6 LSB
INL	<0.6 LSB
SFDR @ 2MHz, 40MSPS	68 dBc
SINAD	57 dB
ENOB	>9.2 bit @ 2MHz
Power Consumption (ADC)	<2.5 mW/ch

The WASA_V0





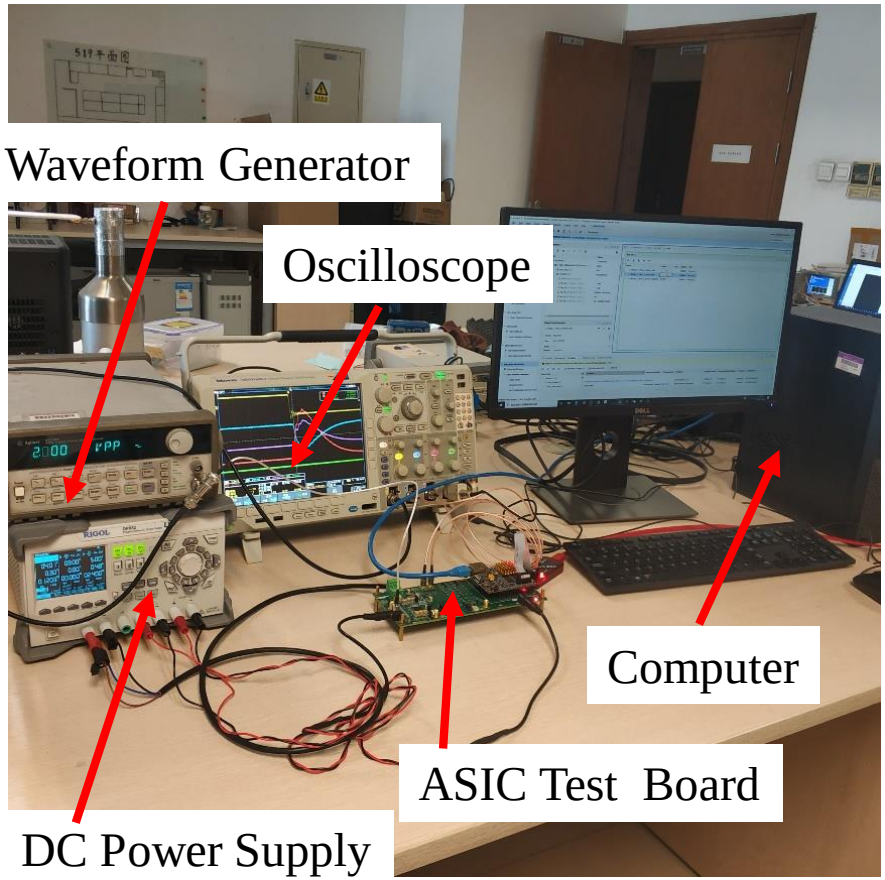


The WASA_V0:

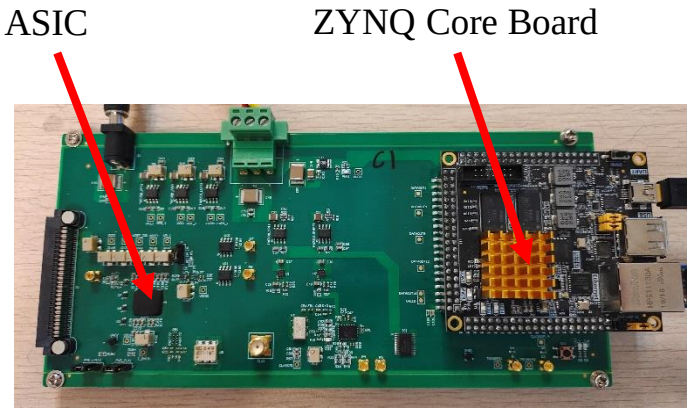
- 16 channel AFE+ADC+LVDS data output
- The Power consumption of the AFE optimized from 2.02 mW/ch to 1.4 mW/ch
- ENC optimized from 589 e to 303 e @10 pF

Test Setup for WASA_V0

- Test Setup

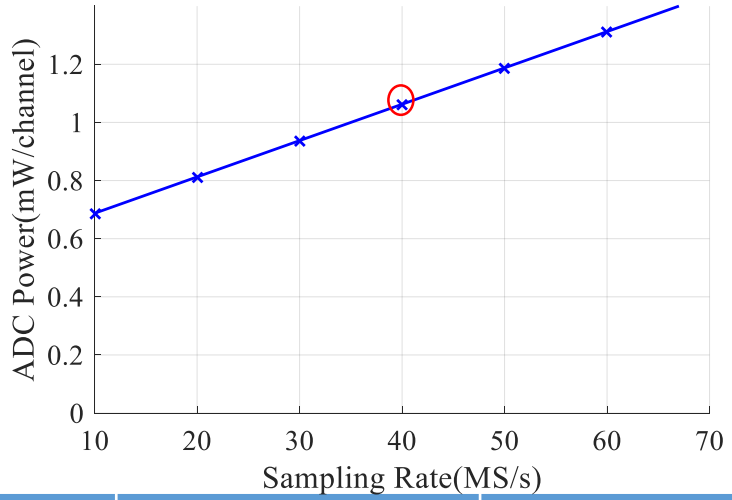


- ASIC Test Board



Power Consumption

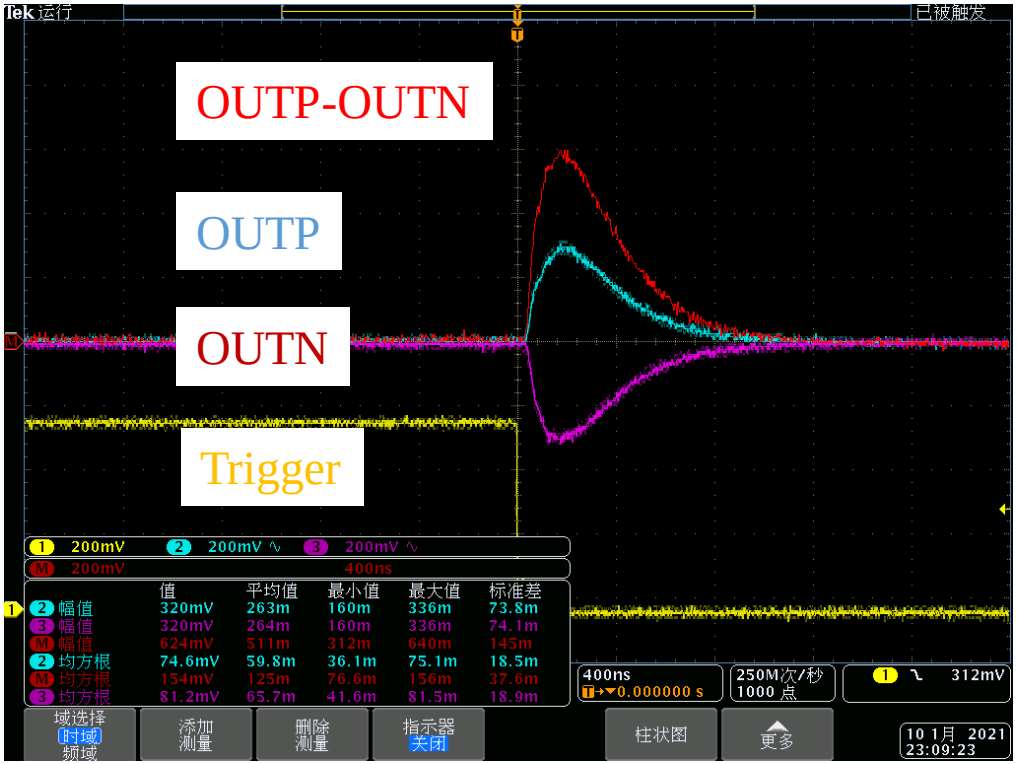
- The power consumption of the AFE: **1.43 mW/ch** (1.40 mW/ch sim.)
- The power consumption of the ADC increases as the sampling rate



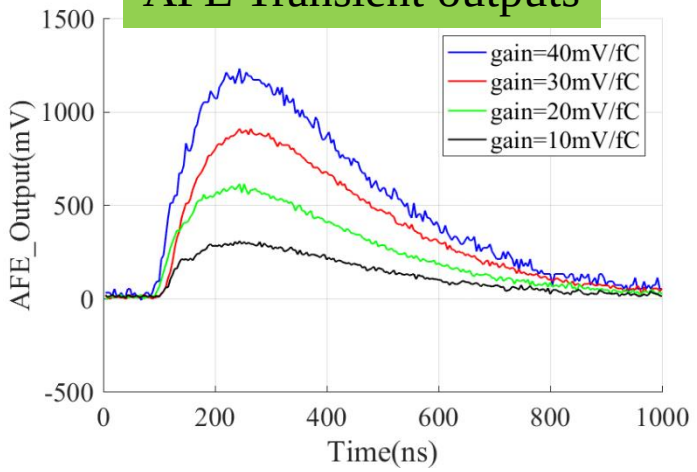
	AFE (mW/ch)	ADC (mW/ch)	Total (mW/ch)
Frist run (simulation)	1.93	1.0	2.93
First run (measured)	2.02	1.0	3.02
Second run (simulation)	1.40	1.0	2.40
Second run (measured)	1.43	1.06 @40MS/s	2.49

Transient Waveforms

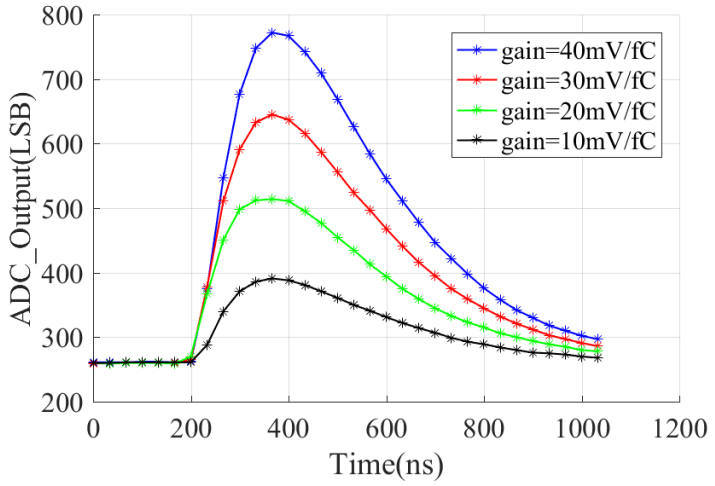
- Transient outputs
  - Differential baseline can be externally adjusted



AFE Transient outputs

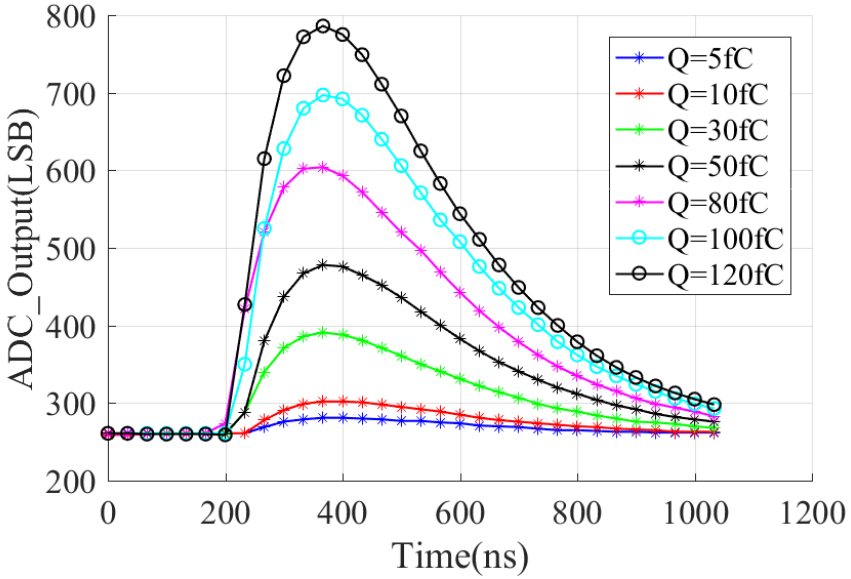


ADC Transient outputs @ 30MSPS

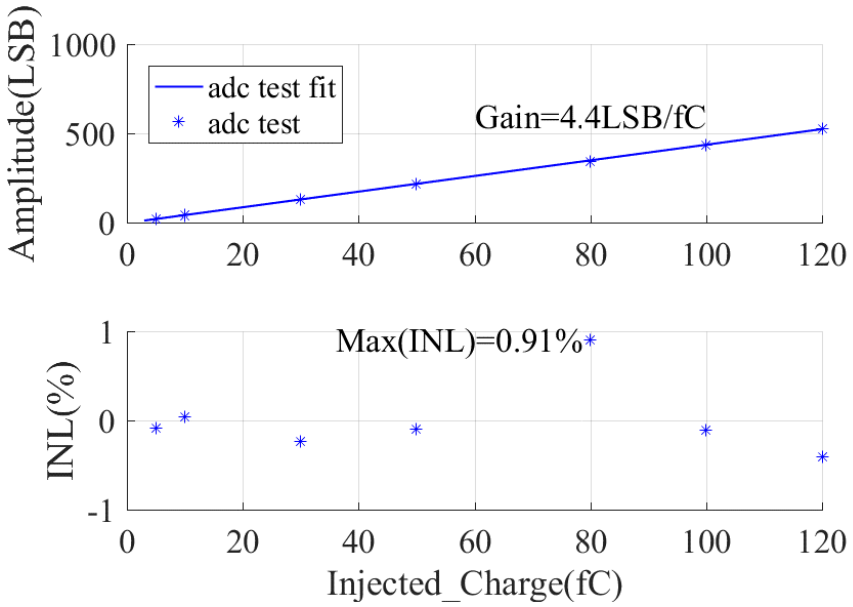


Non-Linearity

- Transient outputs



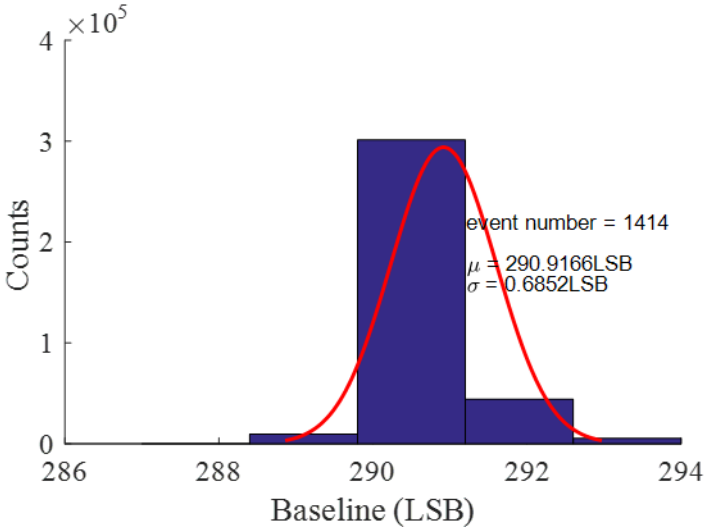
- The linearity @ gain = 10 mV/fC

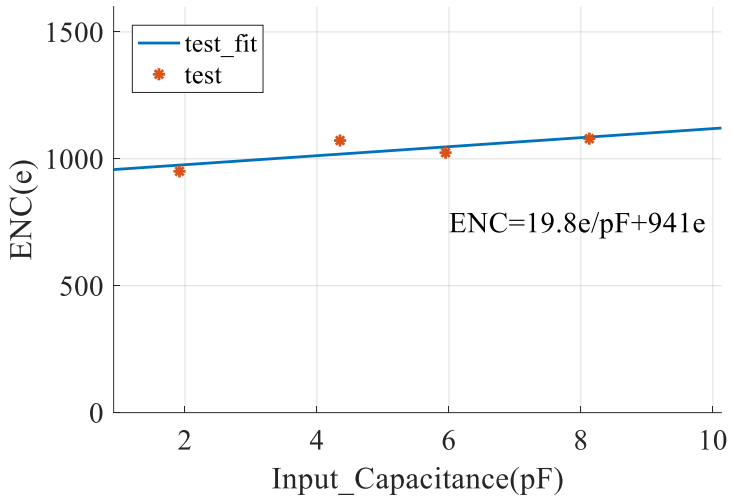


Gain = 4.4 LSB/fC = 4.4 x 2.34 mV/fC = 10.3 mV/fC

Noise Performance

- The baseline fluctuation @ gain = 10 mV/fC
  - Significant contribution from ADC quantization noise

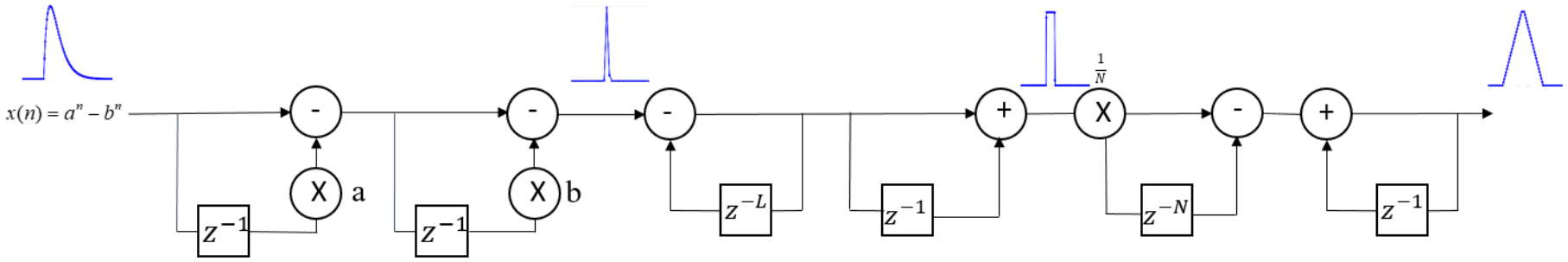




ENC = 19.8 e/pF+941e @ gain = 4.4 LSB/fC

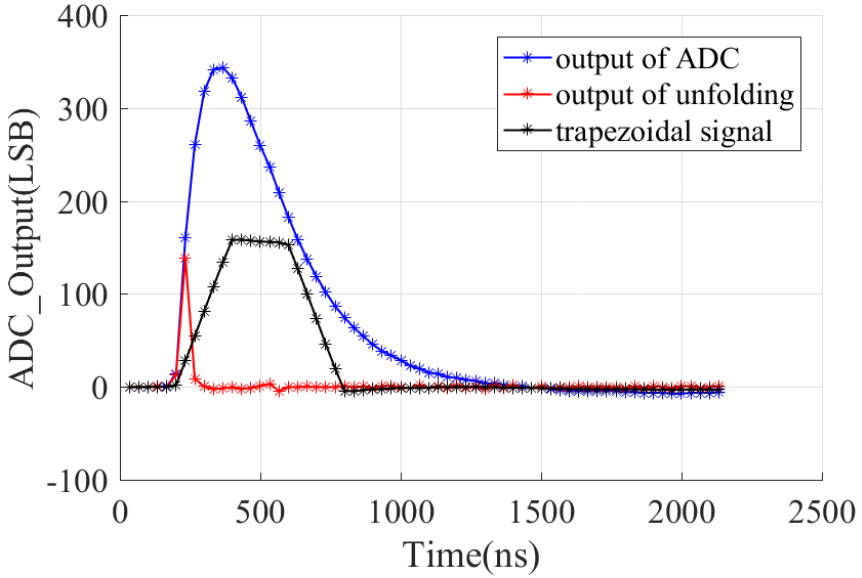
Digital Trapezoidal Filter

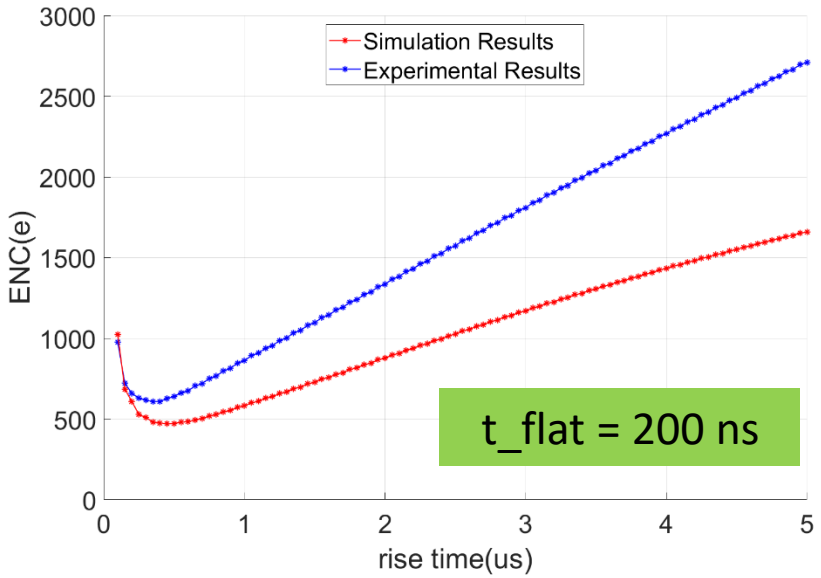
- The waveform is symmetric , can achieve high SNR(signal to noise ratio)
- The ballistic deficit can be avoided
- Hardware resource is low cost, can be well implemented on chip
  - 2 multiplications ,6 additions and subtractions , some shift operations



Noise Performance with Trapezoidal Filter

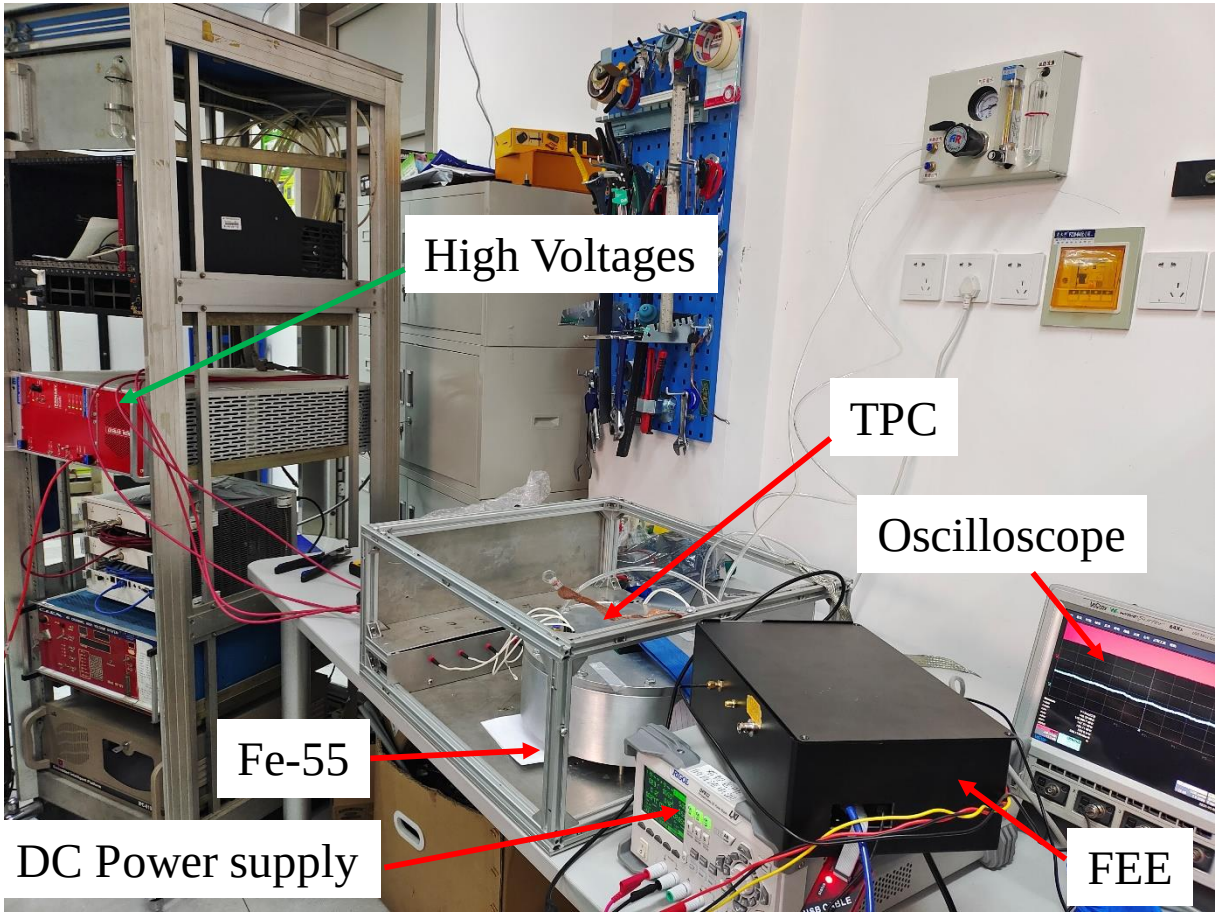
- Noise performance @ C_{in} = 2 pF @ 10 mV/fC
- Trapezoidal filter implemented in MATLAB
- The input simulation signal: output baseline of analog front end add the ADC quantization noise





- Experimental results: minimum ENC = 608 e @10 mV/fC
- Simulation results: minimum ENC = 470 e @10 mV/fC

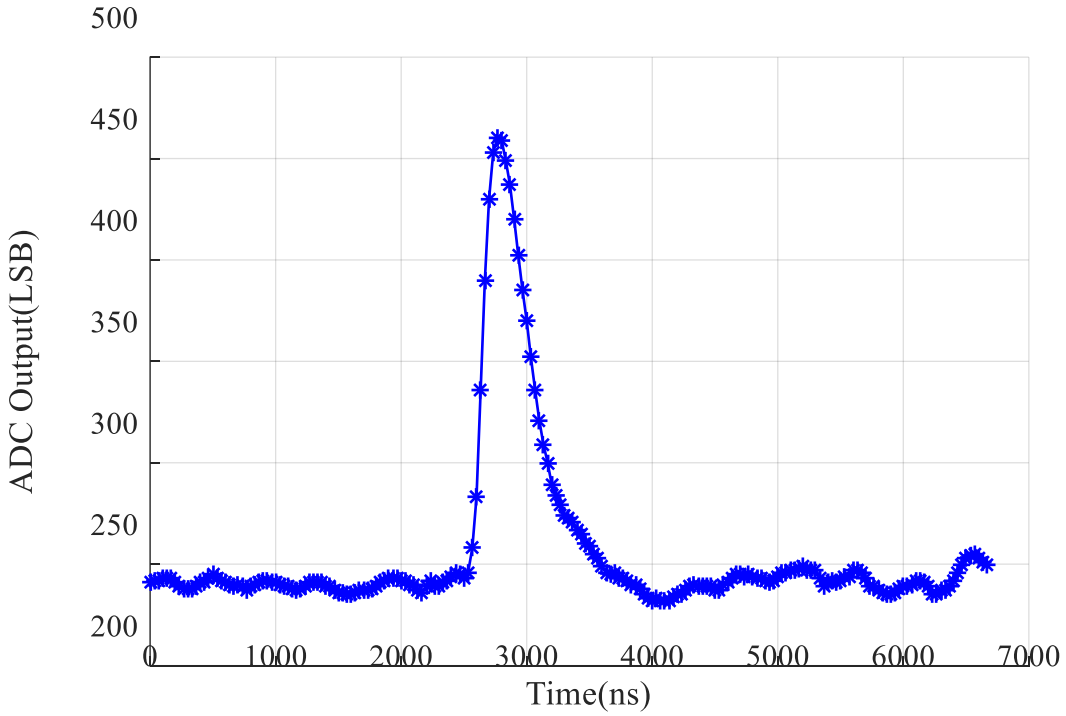
Test Setup for WASA_V0 With TPC



TPC working conditions：

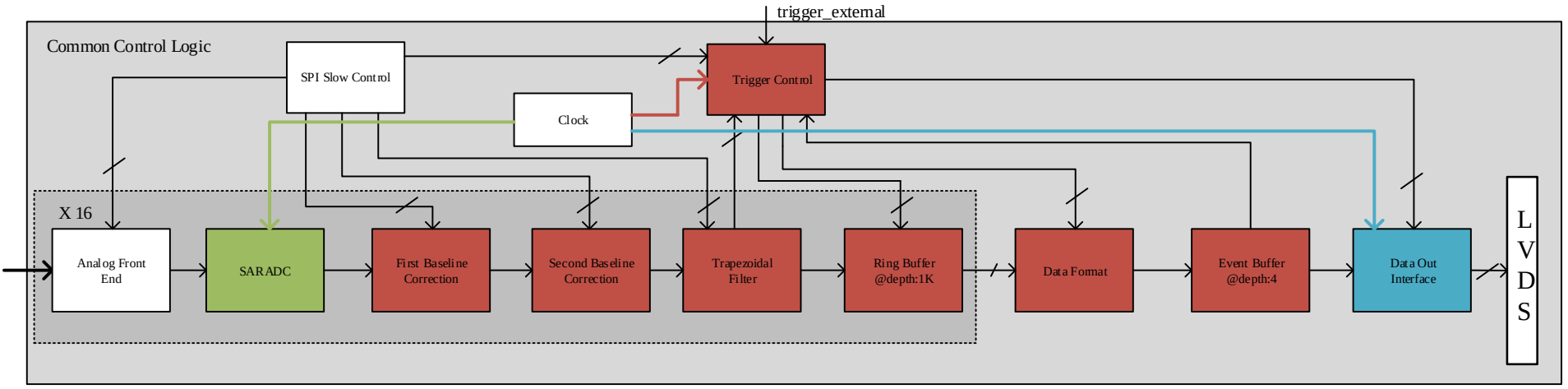
- GEM:310 V
- Working gas： T2K

Transient waveform



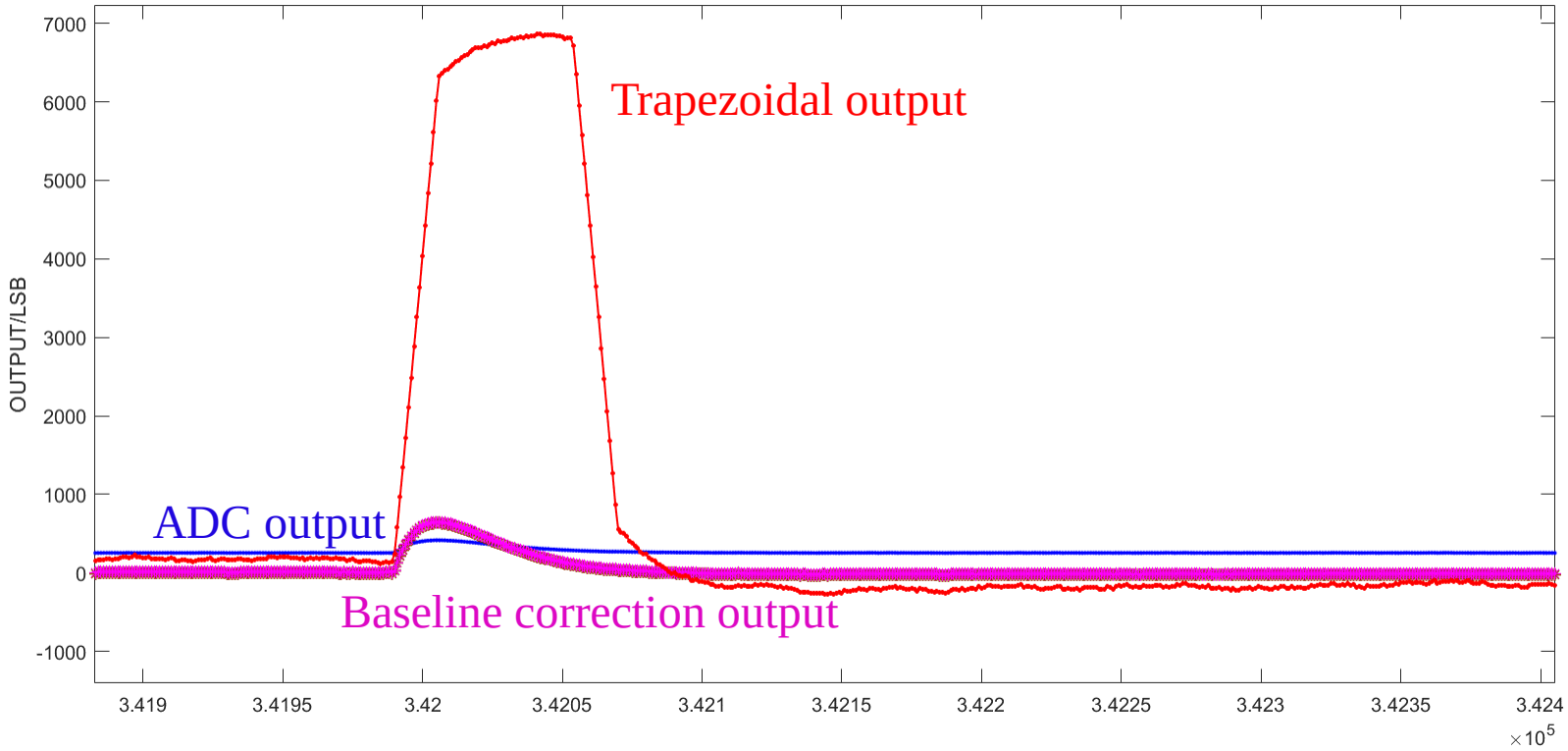
WASA_V1

- Digital signal processing:
  - Two stage baseline corrections, learnt from SAMPA
  - Digital trapezoidal filter, to make pulse shape symmetric and shorter
- Trigger logic with two stage data buffer (ring buffer and event buffer)



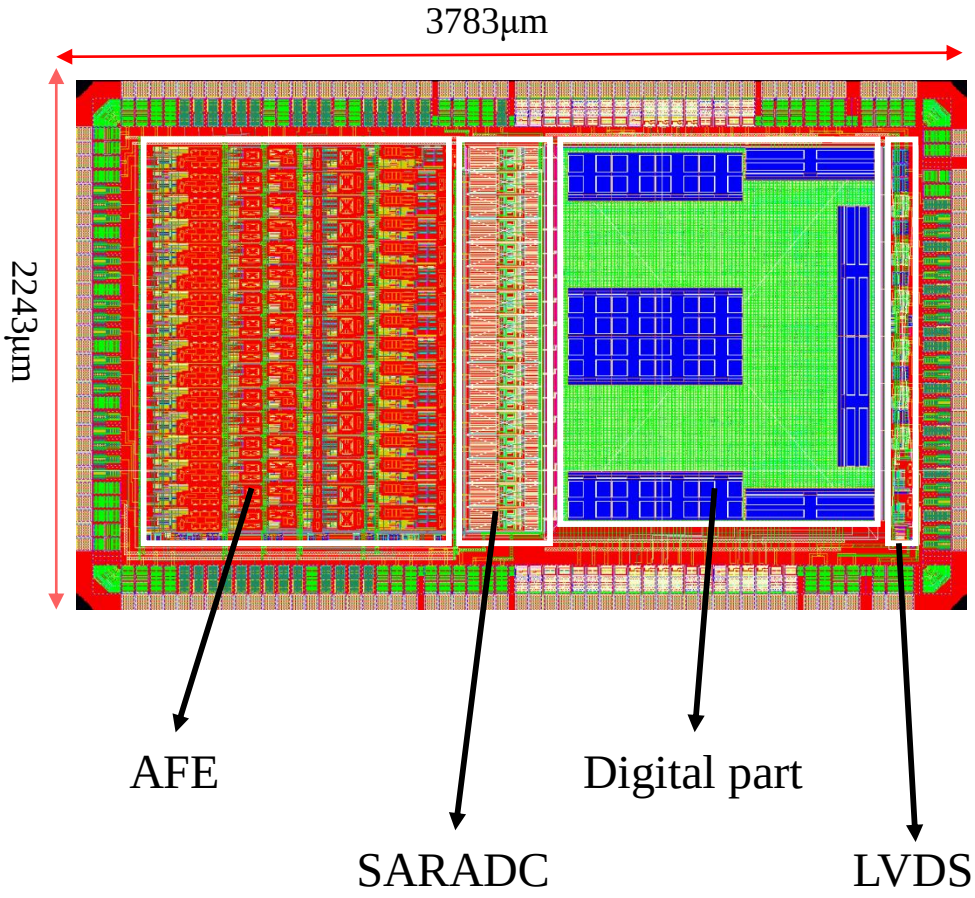
The Simulation Results of WASA_V1

- Transient waveforms of key nodes



- Power consumption(simulation) :1.4+1.0+4.1=6.5mW/ch@100 MS/s

The Layout of WASA_V1



- The floor plan in layout ：
  - The die size： 3783 μm x 2243 μm
  - Analog Front-End , SAR ADC,Digital part, LVDS driver are supplied by separate power
  - Analog Front-End , SAR ADC, Digital part,LVDS driver are separated by guarding ring

Summary

- The WASA_V0 for TPC readout have been developed
  - The power consumption is 2.49 mW/channel:
    - P_{AFE}=1.43 mW/channel
    - P_{ADC} = 1.06 mW/channel @ 40MS/s
  - ENC = 852 e @ Cin=2 pF, gain=10 mV/fC and can be reduced to 608 e using digital trapezoidal filter
- Based on WASA_V0, the WASA_V1 have also been developed ,including AFE, SARADC, digital part.
- Future Plan
  - More tests with TPC detectors such as Fe-55 energy spectrum, laser

Thank You