The 2021 International Workshop on the High Energy Circular Electron Positron Collider
Nanjing, Nov. 8-12, 2021

Status report about the Chinese projects on MAPS for vertexing at CEPC

Ying Zhang and Yunpeng Lu

On behalf of the CMOS pixel sensor teams

for the MOST1 & MOST2 projects

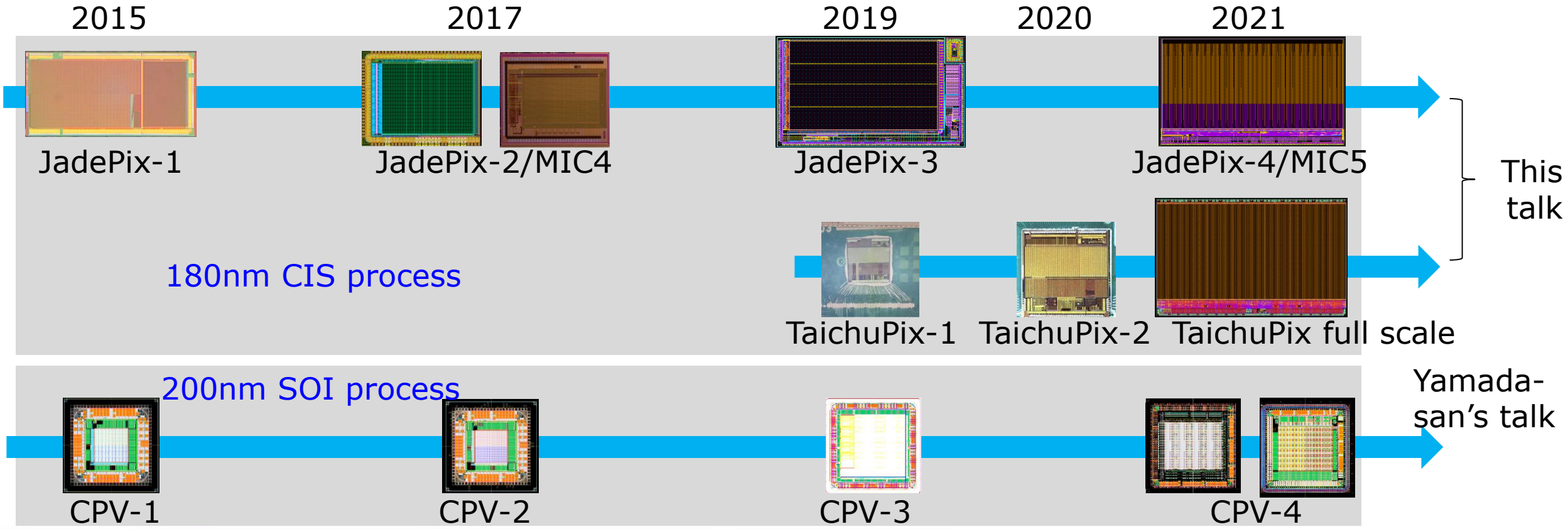
Nov. 8, 2021

Outline

- Overview of pixel sensor development
- Update on the JadePix
  - JadePix-3 test
  - JadePix-4 design
- Update on the TaichuPix
  - TaichuPix-2 test
  - TaichuPix full scale design
- Summary

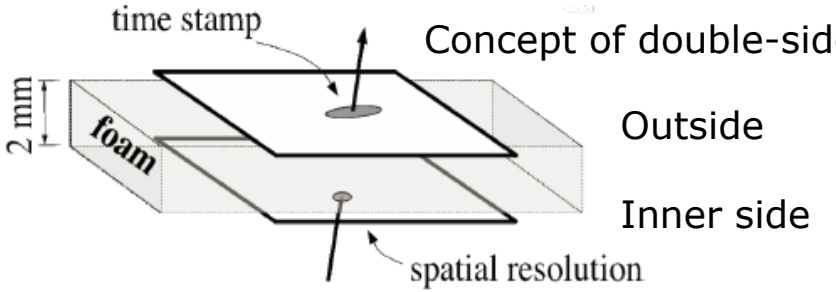
Projects in China

- Development of pixel sensor for CEPC are supported by
  - Ministry of Science and Technology (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation



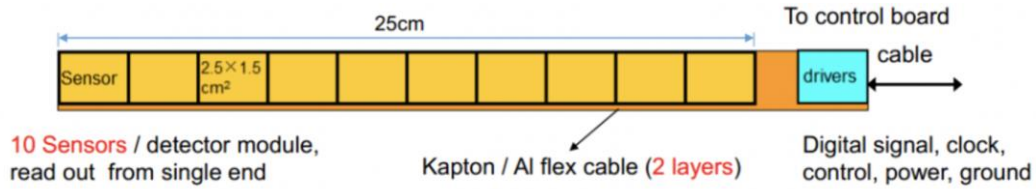
Strategies to address the challenges

- JadePix sticks to a double-sided concept
  - Pitch, power, readout speed
  - A pair of complementary design envisioned



Concept of double-sided layer

- TaichuPix stresses on the system level
  - Full scale prototype for ladder assembly
  - Fine time stamp & Radiation hardness to cope with Z-pole mode



Schematic of full scale sensors on the ladder

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\,\mu m$$

Vertex detector specs

$\sigma_{s.p.}$ ~ 2.8um ----------> **Small pixel** ~ 16um

Material budget ~ 0.15% X_0/layer ----------> **Thinning to** ~ 50um

----------> **low power** ~ 50mW/cm^2

r of Inner most layer ~ 16mm ----------> **fast readout** ~ 1us

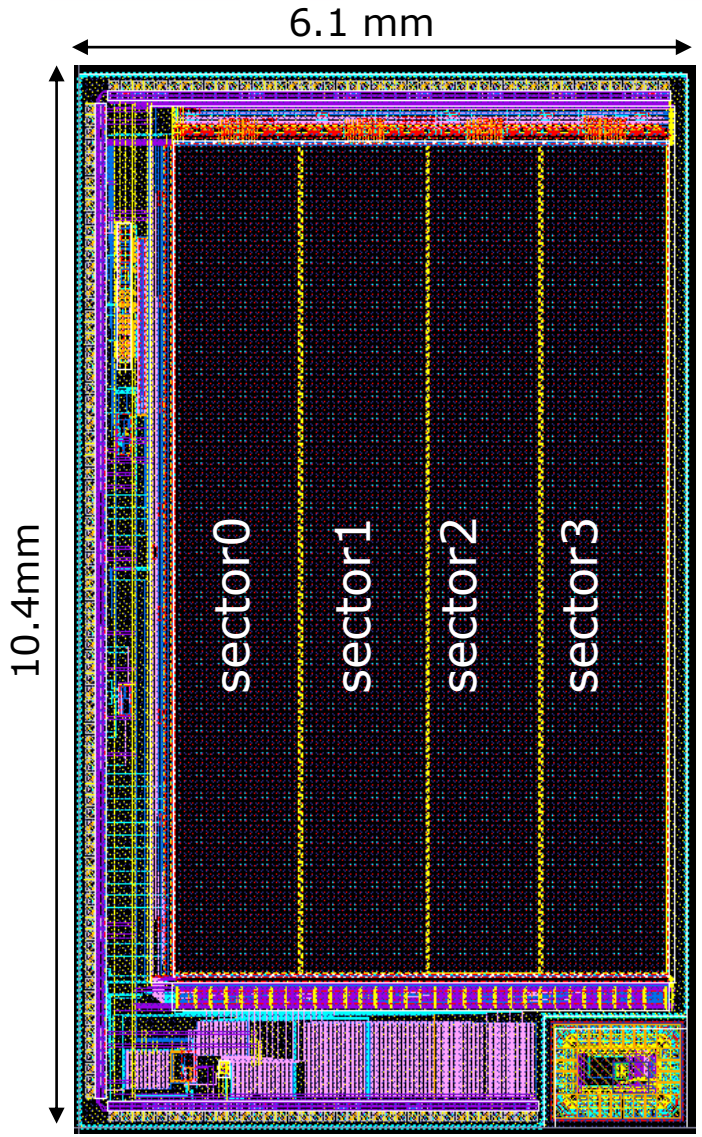
----------> **radiation tolerance** ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\,year)$

Pixel sensor specs

JadePix-3 optimized for small pitch



- **Rolling shutter** to avoid heavy logic and routing in the column-wise
  - Shrink the pixel size by ~ 7 μm
- **Full-sized** in the φ direction
  - Matrix coverage: 16 μm * 512 rows = 8.2 mm
  - Matrix readout time: 192ns/row * 512 rows = **98.3 μs/frame**
- **Extensible** in the z direction
  - 48 columns * 4 sectors

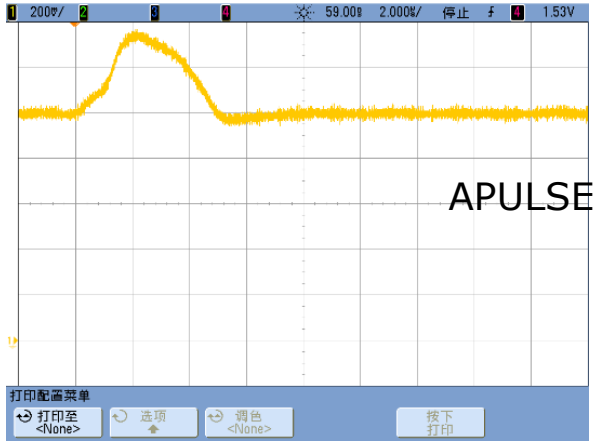
Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm^2
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm^2
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm^2**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm^2

Functional verification

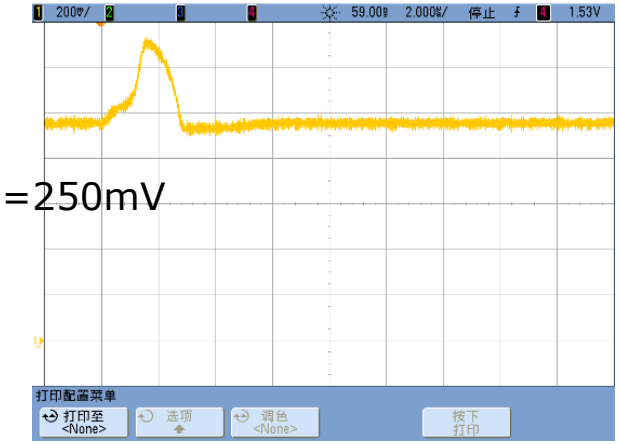
Sheng DONG, Yang ZHOU, Ying ZHANG, Zhan SHI, Yunpeng LU

- **All module** functions verified
  - Configuration of matrix registers
  - Configuration of Global DAC
  - Pulse test
  - Analog output waveform
  - Data readout
  - PLL clock
  - Serializer output pattern
- Response to the radiation as expected
  - Radiative source ^{55}Fe
  - Cosmic ray
  - **Pulsed laser beam**

Low power frontend

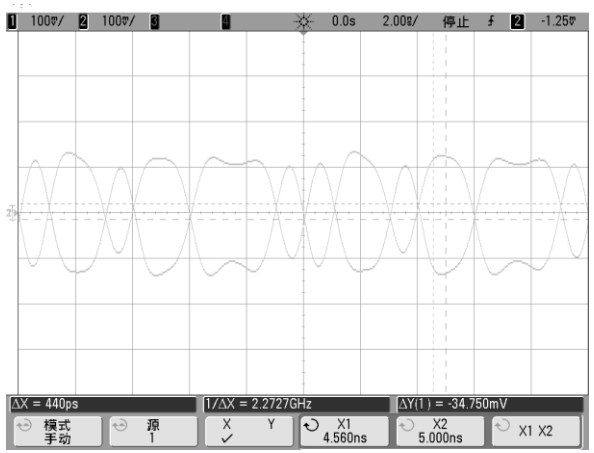


Radiation-enhanced frontend



APULSE=250mV

Output pattern of serializer @ 1Gbps

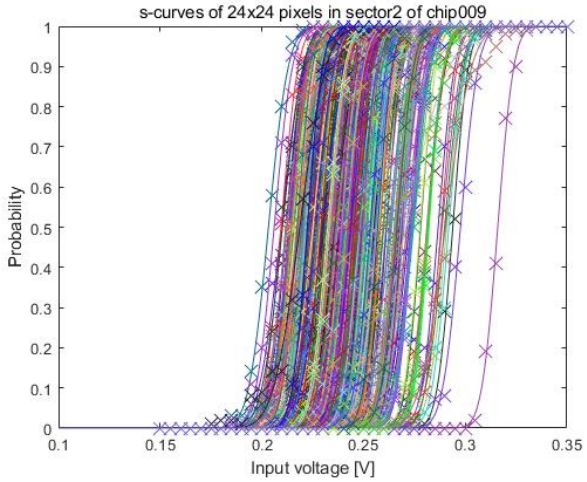


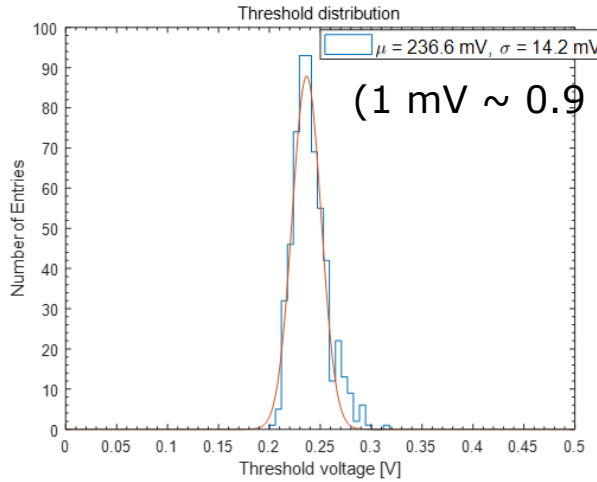
Threshold and Noise (Electrical pulse test)

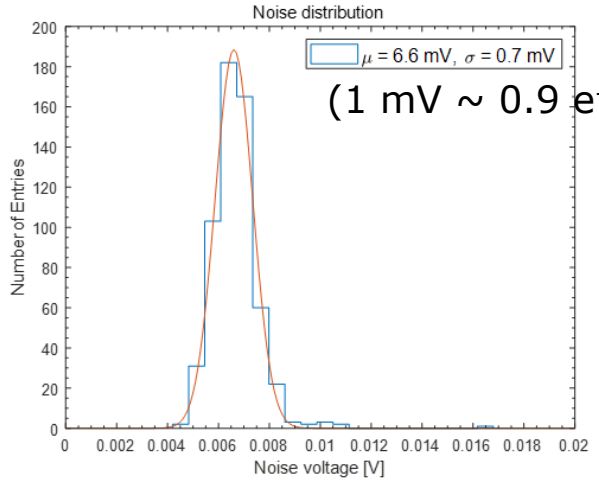
Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

- Pulse amplitude scan and **S-curve*** fit @ nominal threshold

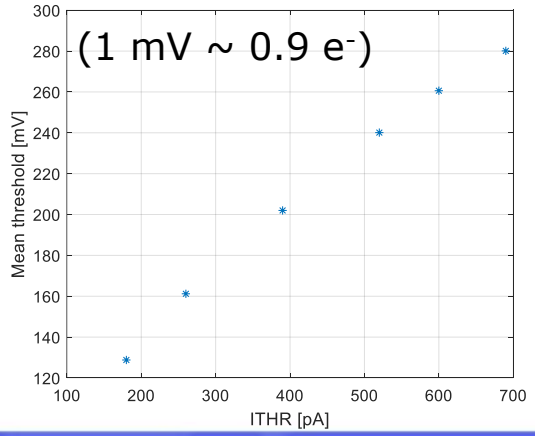
*S-curve: cumulative Gaussian distribution

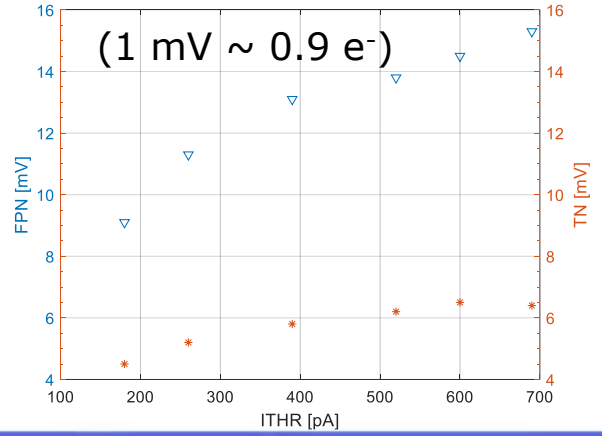


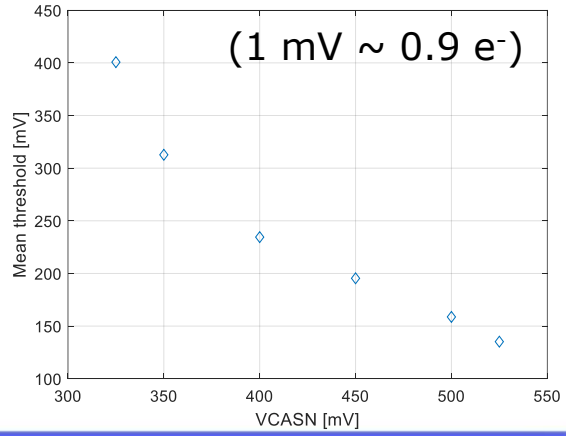


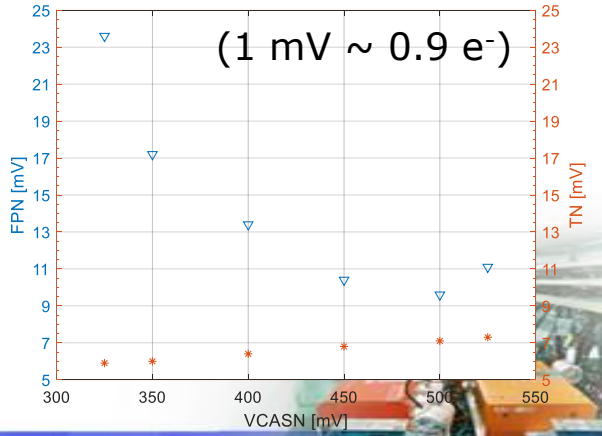


- **Input-referred threshold** as a function of the parameters Ithr and Vcasn
  - Nominal threshold = 220e⁻ @ Ithr = 0.5 nA, Vthr= 400 mV





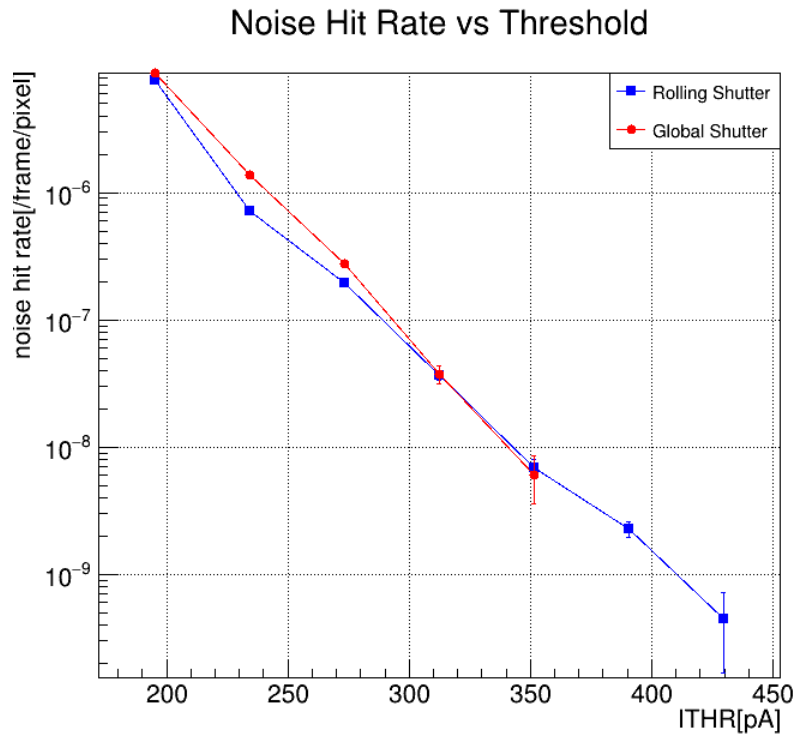


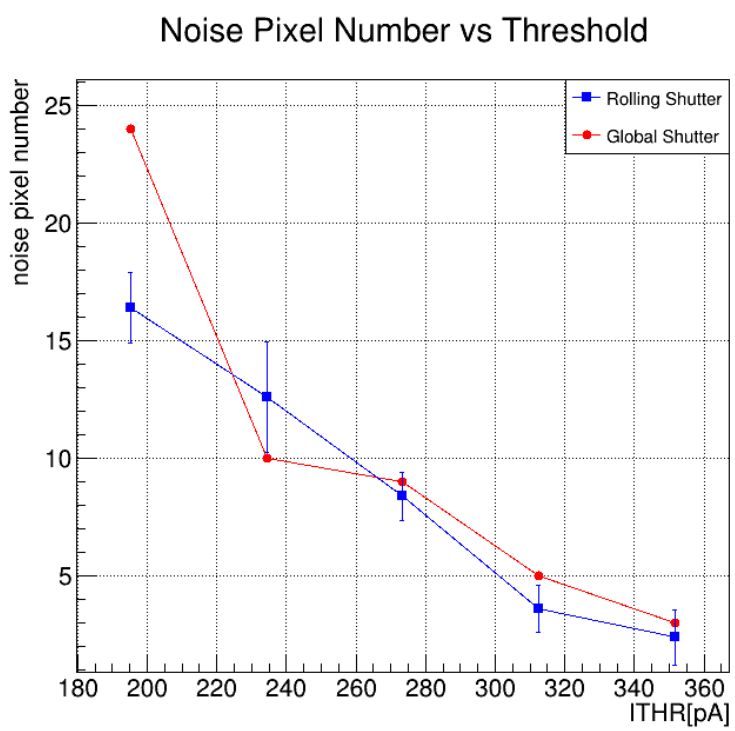


Noise hit rate

Chunhao Tian, Yunpeng LU

- Well below 10^{-6} hits / pixel per frame (98.3 μs)
  - Rolling shutter (**Continuous** readout mode) shows noise hit rate as low as the global shutter (**Single frame** readout mode)
  - No pixel masked

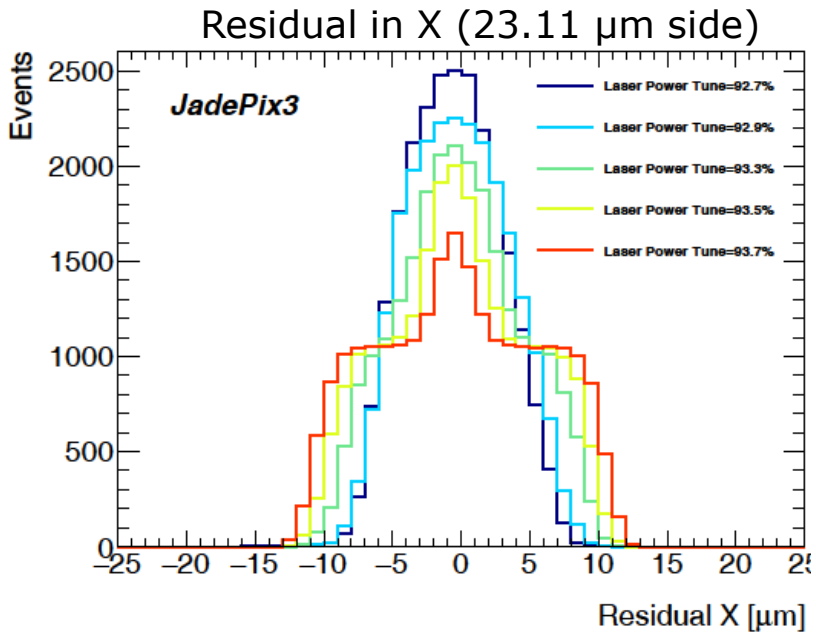


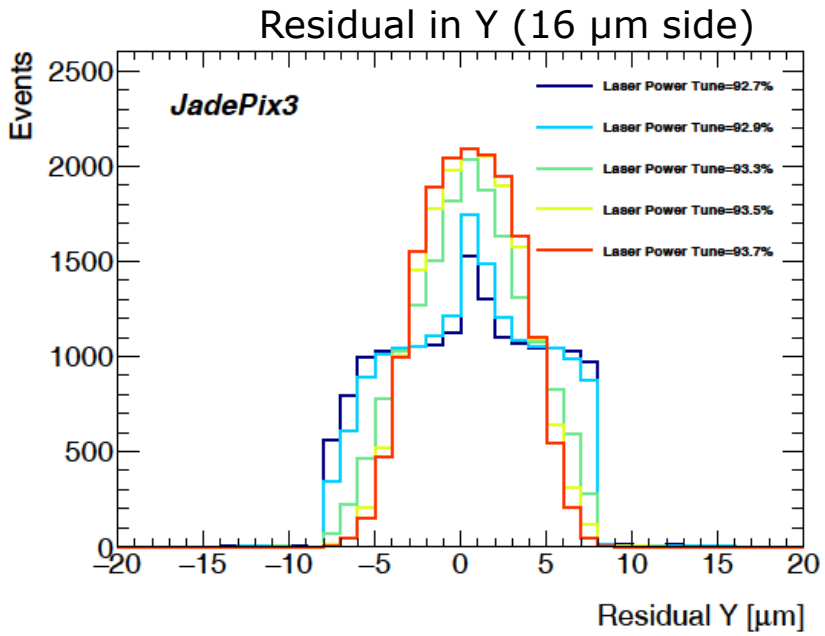


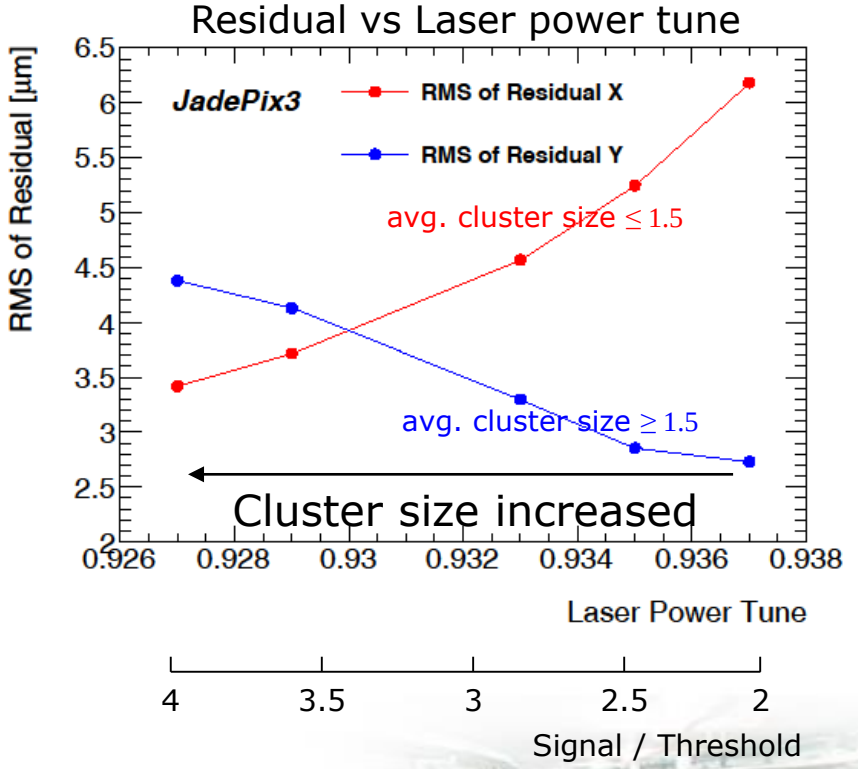
Position resolution

Hulin WANG, Shen DONG, Yunpeng LU

- Threshold set to 220e$^-$, tune the laser power to vary cluster size
  - Laser beam focused to d=3.4 μm
- **Minimum value** as cluster size approaching 1.5
  - 3.34 μm @ signal = 880e$^-$ in X
  - 2.31 μm @ signal = 440e$^-$ in Y







Power consumption

Ying ZHANG, Zhan SHI, Yunpeng LU

- Average power consumption with present chip size, **46.9 mW/cm²**
  - **1.04 * 0.61 cm²**
  - PLL and Serializer not included (parallel bus for data output)
- Extrapolated to a full size chip, **91.44 mW/cm²**
  - **1 cm * 2.56 cm**
  - PLL and Serializer included
- Could be cut off further
  - Analog buffer (1.8mA)
  - Alternative LVDS receiver (1.74mA)
  - PLL test output (11.5mA)

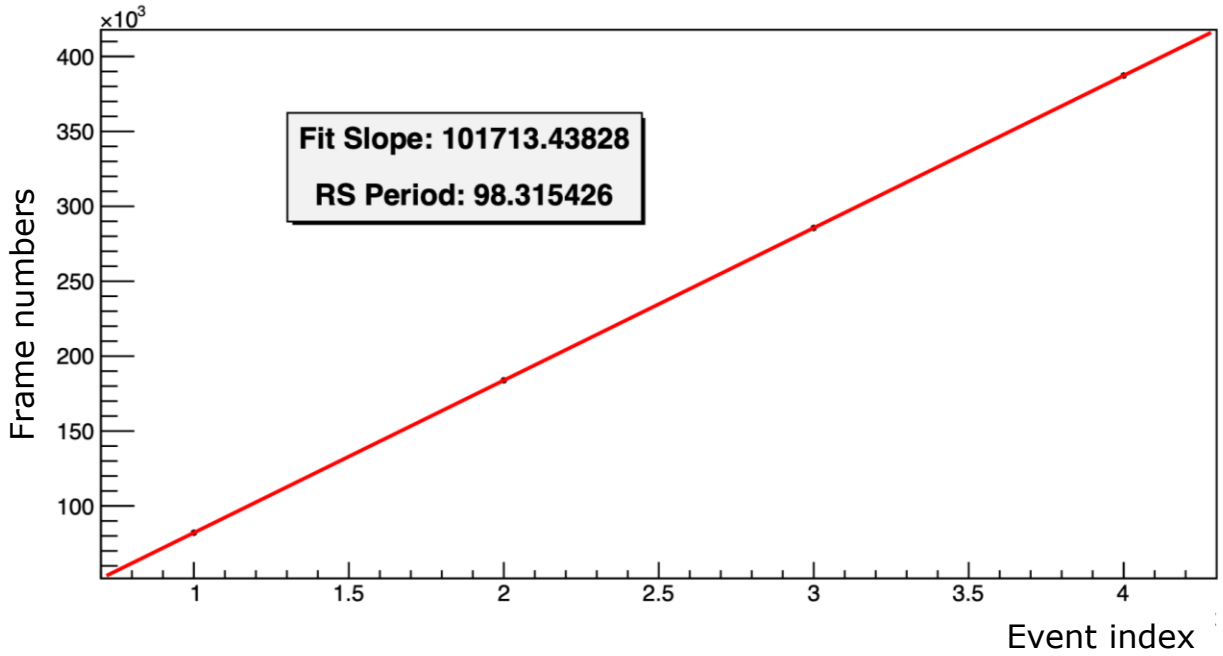
Extrapolation of average power consumption

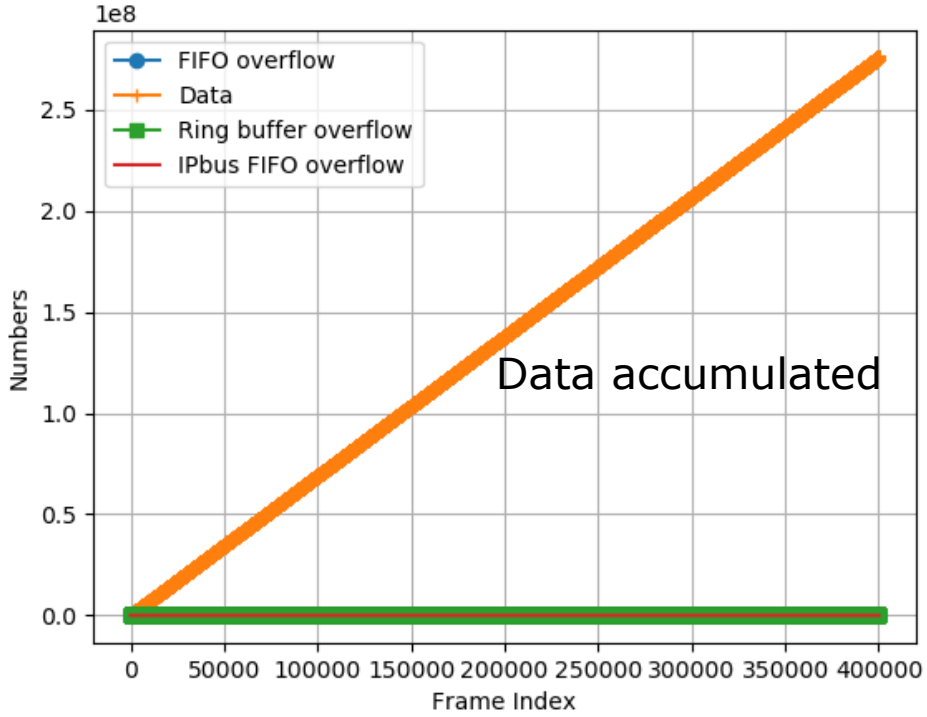
	512*192 (JadePix3)	512*1024 (Full-sized chip)
Matrix	3.15 mA	16.79 mA
Zero suppression and data buffering	12.47 mA	66.47 mA
Shared modules	46.82 mA	46.82 mA
Sum	62.44 mA	130.08 mA

Rolling Shutter Readout

Sheng DONG, Hulin WANG, Yunpeng LU

- Frame period (**Integration time**)
  - Event interval: 10 s
  - Count the frame numbers between 2 events
  - Frame period: **98.315 μs**
- Stability test
  - Hit number per event: 2048
  - Event interval: 110 μs
  - Data throughout: **595.8 Mbps * 39.3 s**



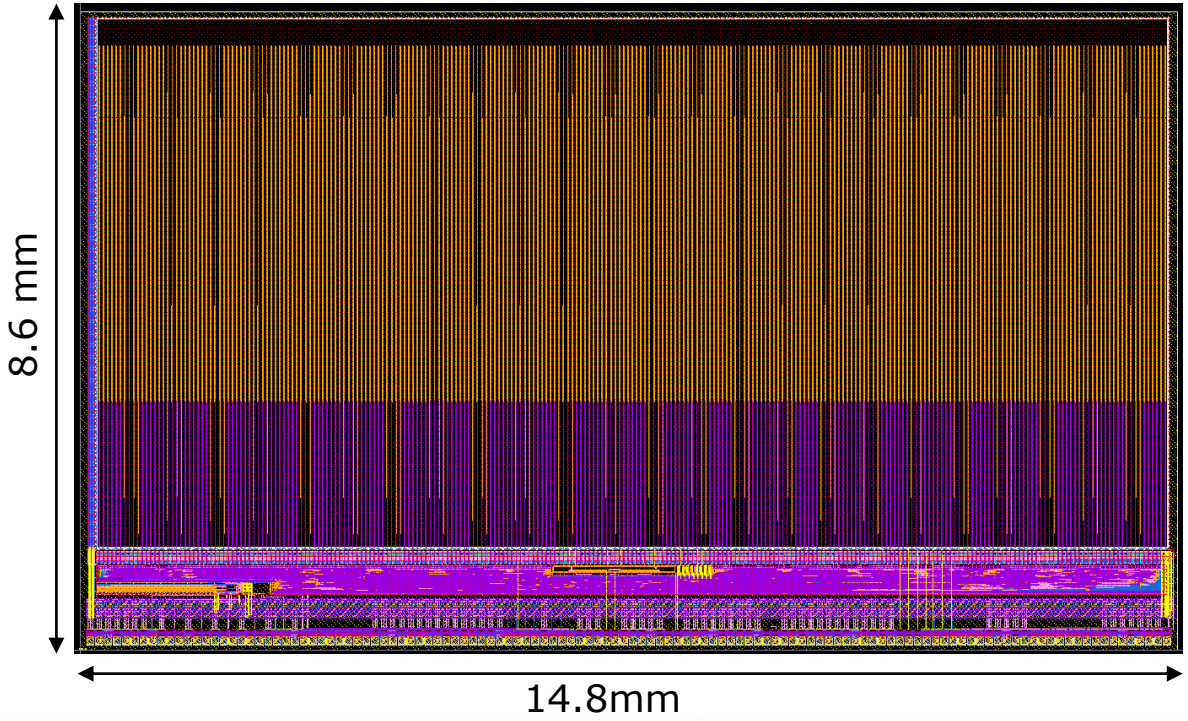


Design specs of JadePix-4/MIC5

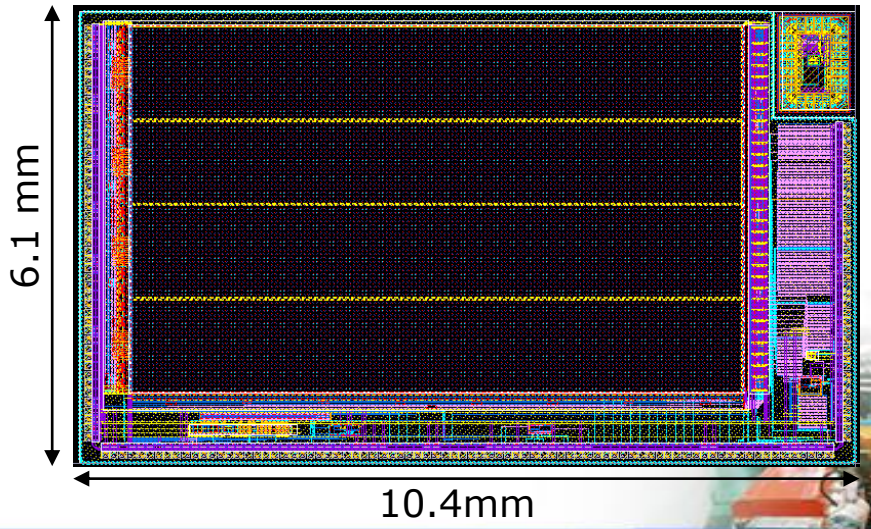
- JadePix-4/MIC5 optimized for fast readout and low power
  - With pixel size ~ 20 μm × 30 μm,
  - Mask area: 14.8 mm × 8.6 mm

	S.P. resolution	Integration time	Average power
JadePix-4	<5 μm	~1 μs	< 100 mW/cm^2
JadePix-3	<3 μm	<100 μs	< 100 mW/cm^2

JadePix-4 Layout

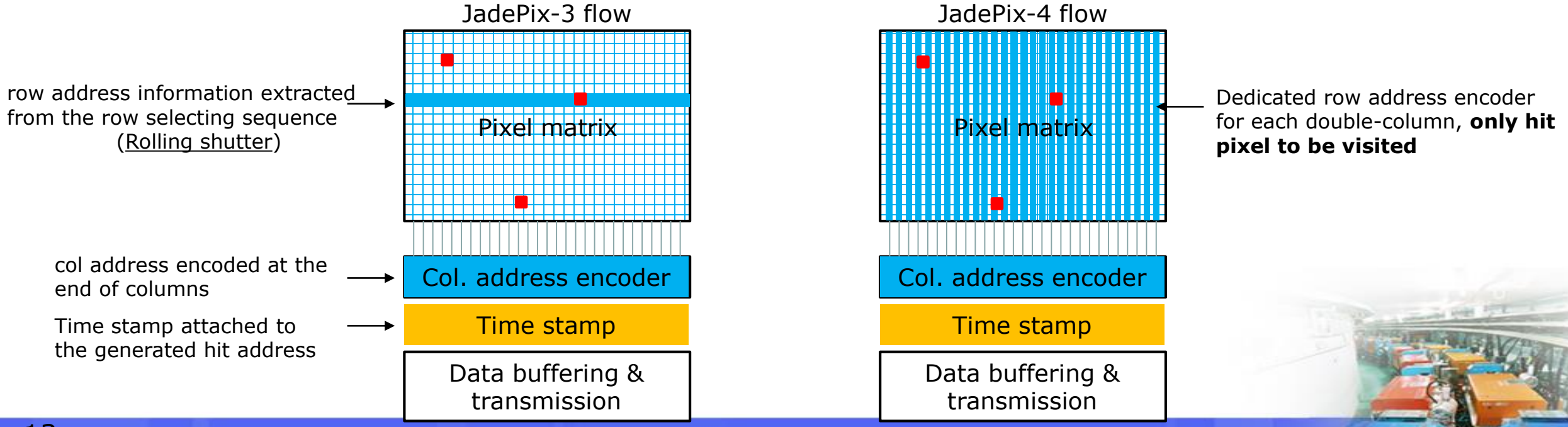


JadePix-3 Layout



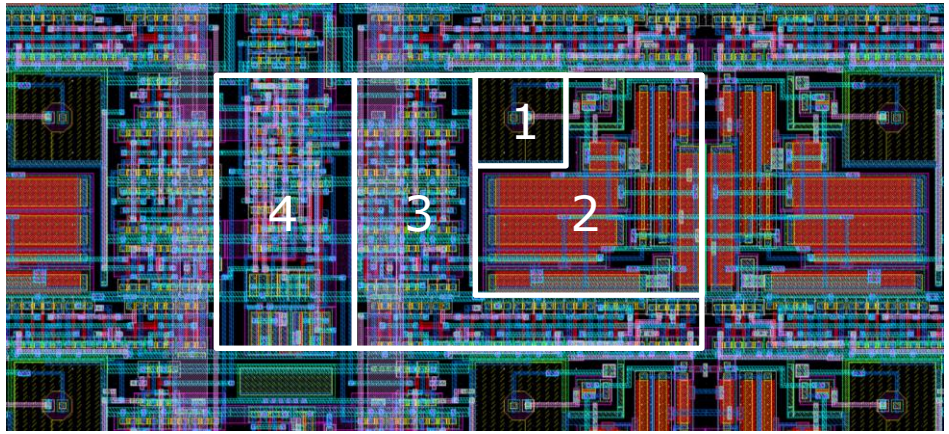
Hit processing flow

- Hit registered in the each pixel needs fast processing
  - Hit position (col. and row address) to be encoded
  - Time stamp to be attached
  - Register to be reset for the next hit
- A major modification on the hit processing flow
  - Row address encoding embedded into the active pixel matrix, which is much faster



Implementation

- Key component verified and reused from JadePix-3
  - Diode
  - Analog frontend
  - Hit register
- Asynchronized Encoder and Reset Decoder (AERD) *
  - Generating col. and row address from hit pixel
  - Tracing back to reset hit pixel
- Final layout of pixel matrix
  - pixel array: 356 row × 498 col.
  - Pixel size: 20 μm × 29 μm

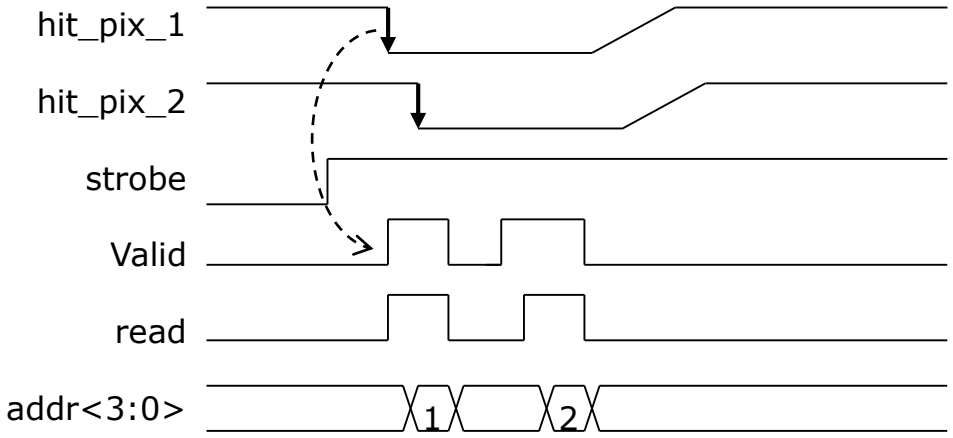


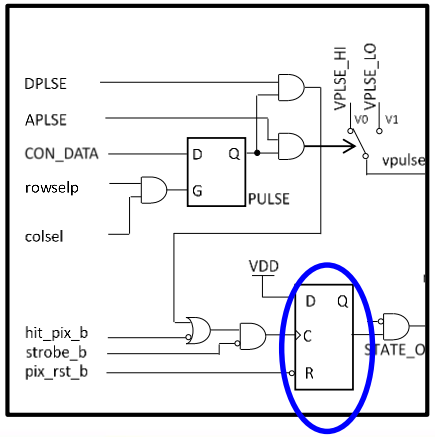
JadePix-4 pixel layout
(MET4 and above not shown)
1. Diode
2. Analog frontend
3. Digital logic
4. AERD shared by 2 col.

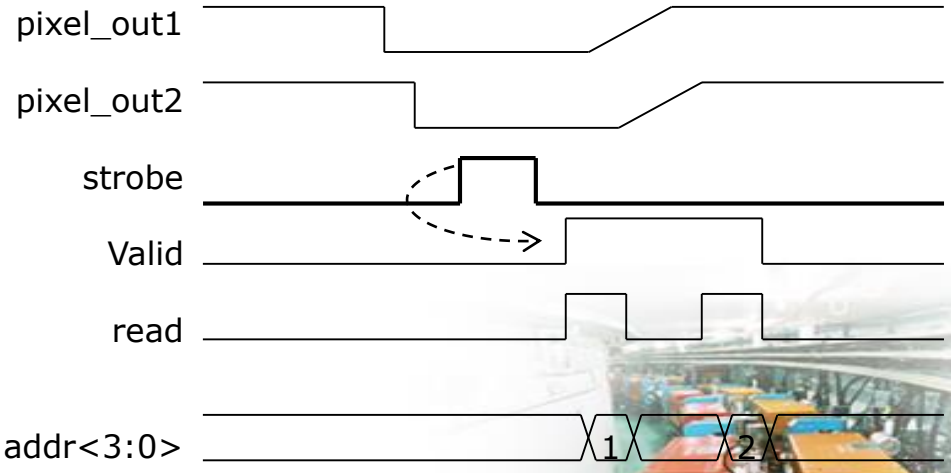
*P. Yang, etc., NIMA 785 (2015) 61-69

Readout modes

- Triggerless mode
  - Global gate signal, **strobe==1**
  - All hits registered at their leading edge
  - 0.2 hits/μs per double col. with the estimated hit density of inner most layer
  - Occupancy 0.02% @ integration time = 1 μs
- Trigger mode
  - Global gate **controlled by trigger signal**
  - Hits registered only when overlapped with a trigger (analog buffer)
  - Capable to handle very high hit density with a dead time for readout, 50 ns/hit







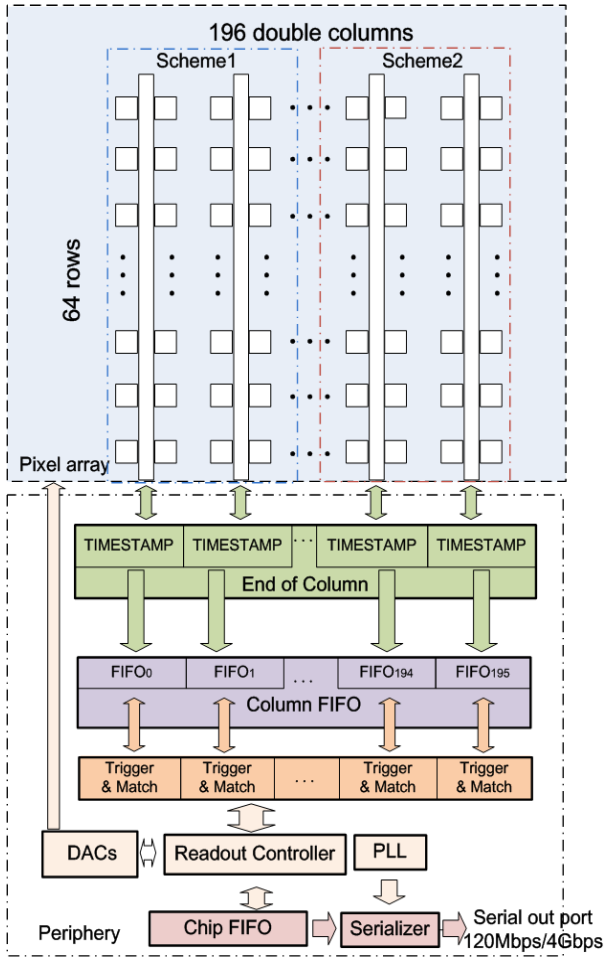
JadePix-4/MIC5 compared with JadePix-3

- JadePix-4/MIC5 is a complementary design to the JadePix-3
  - To complete the R&D for the double-sided concept

	JadePix-3	JadePix-4/MIC5
Pixel size	16 μm × 23.1 μm	20 μm × 29 μm
Integration time	98.3 μs	~ 1 μs
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	356 row × 498 col.
Mask area	10.4 mm × 6.1 mm	14.8 mm × 8.6 mm

- Submitted to a shared engineering run recently.

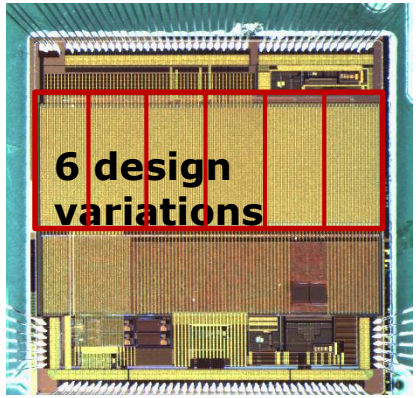
TaichuPix architecture



- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - Priority based data driven readout, zero-suppression intrinsically
  - Modification: **time stamp is added at EOC** whenever a new fast-or busy signal is received
  - **Dead time**: 2 clk for each pixel (**50 ns** @40 MHz clk)
- **Two parallel pixel digital schemes**
  - ALPIDE-like: Readout speed was enhanced for 40 MHz BX
  - FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area
- **2-level FIFO architecture**
  - L1 FIFO: In column level, to de-randomize the injecting charge
  - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
  - Make the data rate in a reasonable range
  - Data coincidence by time stamp, only matched event will be readout

TaichuPix small prototypes overview

TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

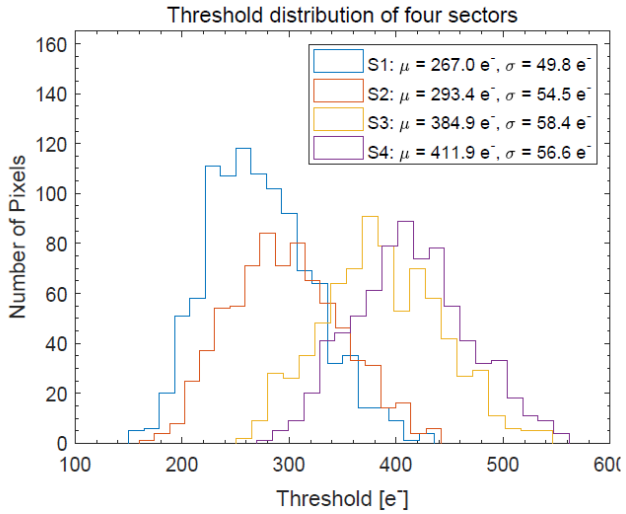


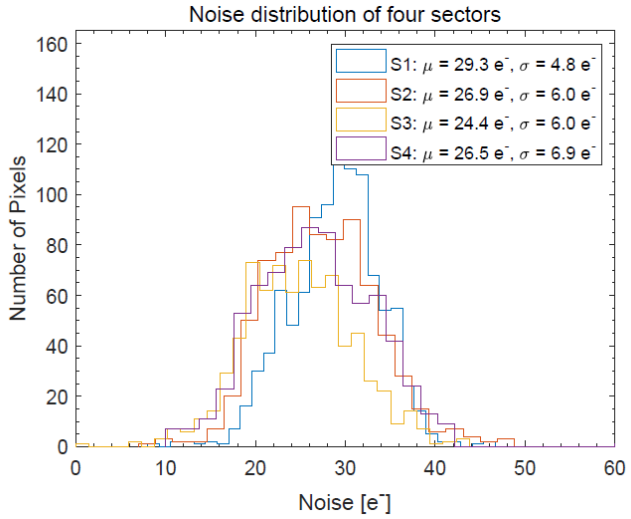
TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the **data-driven readout**
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - **High speed data interface** up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

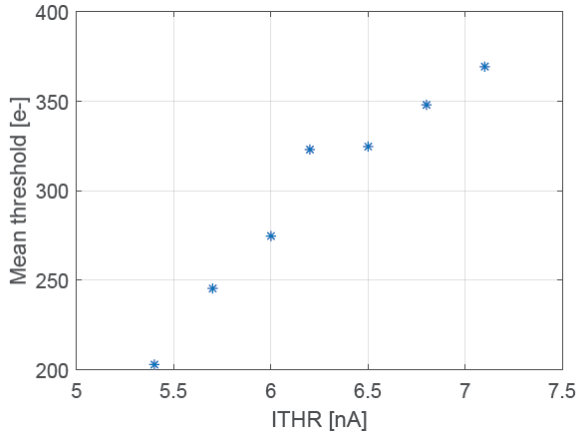
Performance of threshold and noise of TaichuPix2

- **Pixel array includes 4 sectors with different transistor parameters/layout for analog front-end, S1 chosen for the full-scale design.**
- **Threshold can be tuned by changing 'ITHR' (a global current bias)**





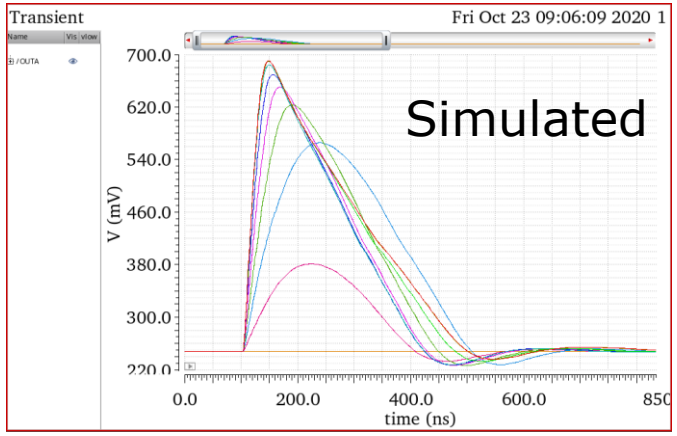
Mean threshold vs. Threshold current ITHR



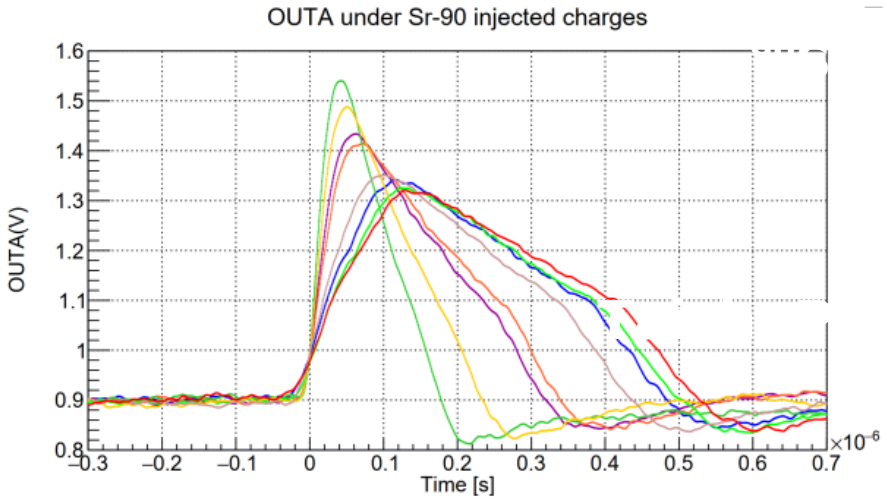
Chip4	Threshold Mean (e⁻)	Threshold rms (e⁻)	Temporal noise (e⁻)	Total equivalent noise (e⁻)
S1	267.0	49.8	29.3	57.8
S2	293.4	54.5	26.9	60.8
S3	384.9	58.4	24.4	63.3
S4	411.9	56.6	26.5	62.5

TaichuPix response to radioactive source

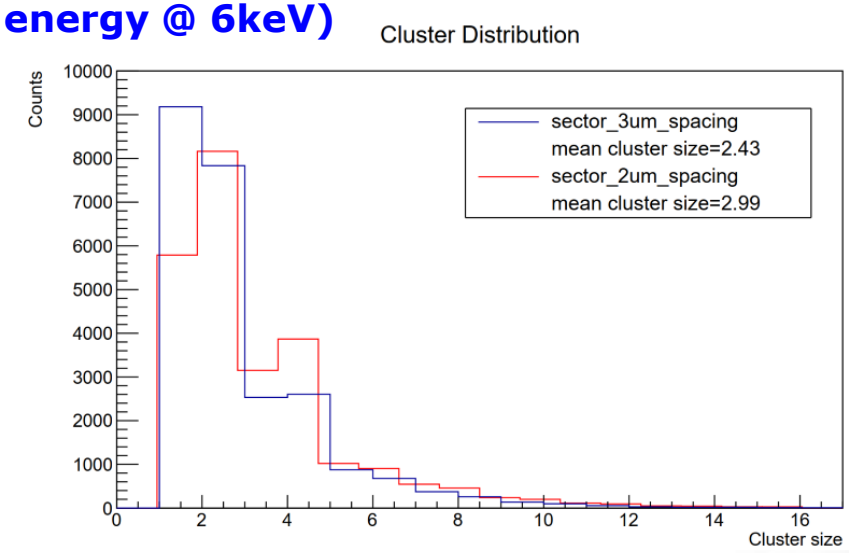
- **Functionality of TaichuPix1&2 proved**



TaichuPix2 response to X-ray tube (cutting energy @ 6keV)

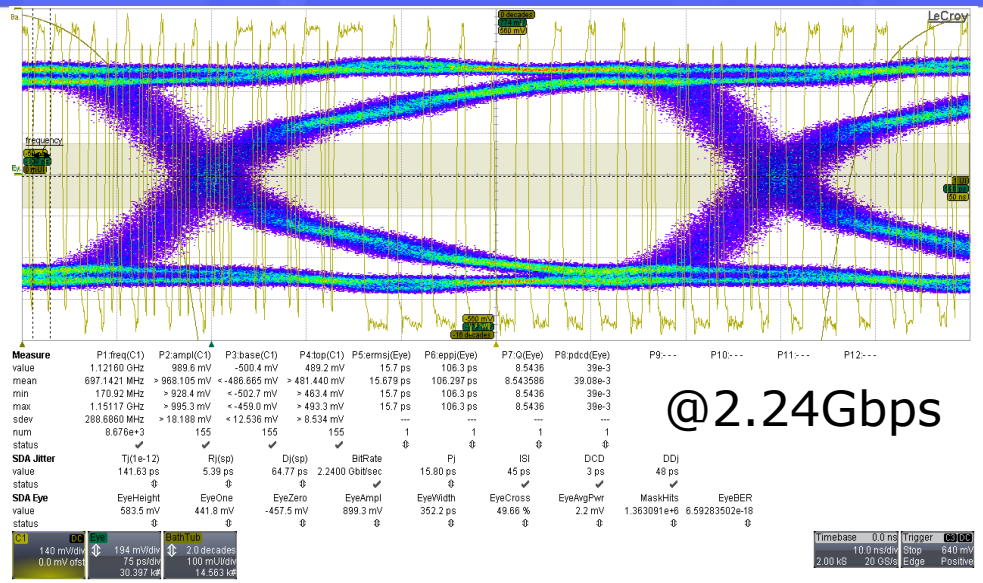


TaichuPix1 response to ^{90}Sr exposure

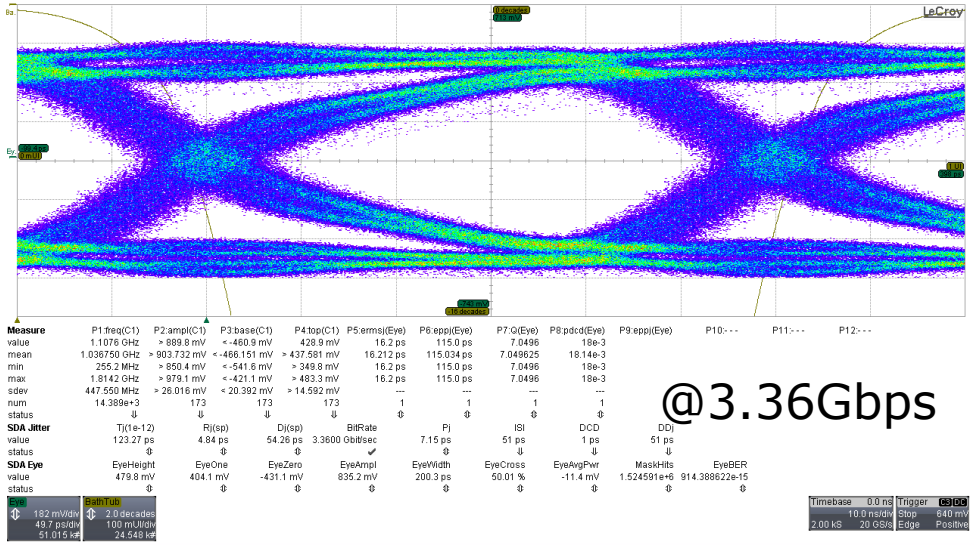


TaichuPix1 cluster size to ^{90}Sr exposure

Test of the data interface



@2.24Gbps



@3.36Gbps

Bit rate	2.24Gbps	3.36Gbps	4.48Gbps
Clk freq	1.12GHz	1.68GHz	2.24GHz
BER	6.59e-18	9.14e-13	3.23e-5
Tj@e-12	141.63ps	123.27ps	147.14ps
Rj	5.39ps	4.84ps	5.35ps
Dj	64.77ps	54.26ps	70.90ps

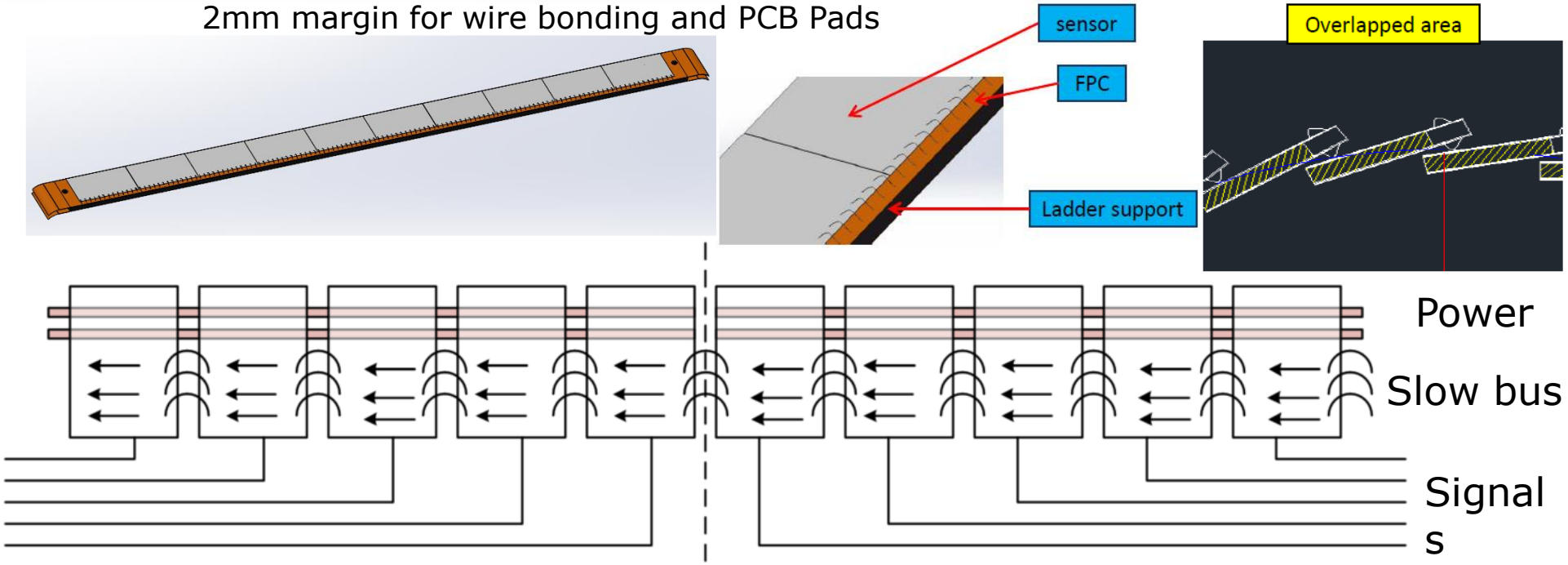
- **Data readout in DDR mode**
- **Data interface was tested by the on-chip PRBS source, a high speed oscilloscope (@16Gsps), and code stream verified in FPGA**
- **BER qualified till 3.36 Gbps, failed at 4.48 Gbps**
- **Concerning the highest data rate for triggerless at 4 Gbps, at least 2 SER interface ports needed**
- **Thus bit rate @2.24 Gbps is safe and power optimized**

Overview of the full scale prototype

1. Pixel array 1024*512
2. Periphery
3. DAC & Bias generation
4. Data interface
5. LDO (test blocks)
6. Chip inter-connection features
7. Scribe-able top power connection features

- Process: 180 nm CMOS Imaging Sensor process (7 metal layers)
- Pixel cell copied exactly from MPW + scaled logic with new layout Periphery + debugged/improved blocks + enhanced power network

Flex cable design consideration

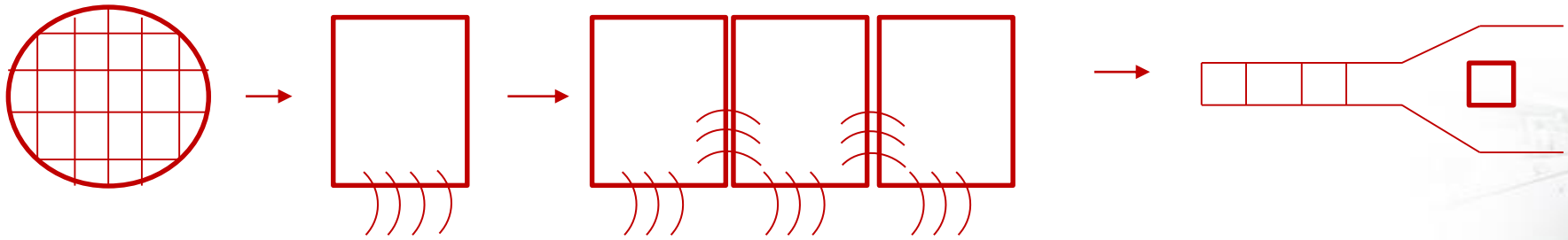


- **Design goals & considerations for the Flex PCB**
  - Minimum material budget
    - Minimum dead zone extension, limited height of PCB
      - Minimum set of signals on Flex
      - Inter-chip connection for slow controls through wire bonding → save some space & metal on PCB
    - Robust power supply
  - Manufacturability

Testability design & test plan consideration

- **All test features reserved, while the connection IOs will be reduced at different stages depending on chip test & study results**
  - Analog probe signals at the top part, accessible from the top pads
  - When mounted on ladder, only minimum self test possibilities can be reserved

1. **Probe Card design for the wafer test**
   - For all the pads at both sides
2. **Single chip test board design**
   - Designed with all the test features for the chip functional study
3. **Multiple chip test board for the ladder debugging**
   - Designed following the same manner as the ladder but on PCB
   - Signals and power supplies will be limited just with the ladder's dimension
   - Extra test signals can be connected to the extended area, to help debugging
4. **The real flex cable design for the ladder**
   - Core design and lessons will be exported from 3



Summary and outlook

- Progress made on the JadePix and TaichuPix development
  - JadePix-4 arose as a complementary design to the JadePix-3
  - TaichuPix full scale completed based on the TaichuPix-2 results
- Is it possible to converge into one design at some point?
  - Both are expecting to migrate to a deeper sub-micro process
  - Established capability to synthesize various design choices for one optimized scheme
- Next generation of CMOS pixel sensor technology
  - 65 nm CMOS technology is being evaluated in Europe
  - Survey on domestic foundry is needed in light of international export control

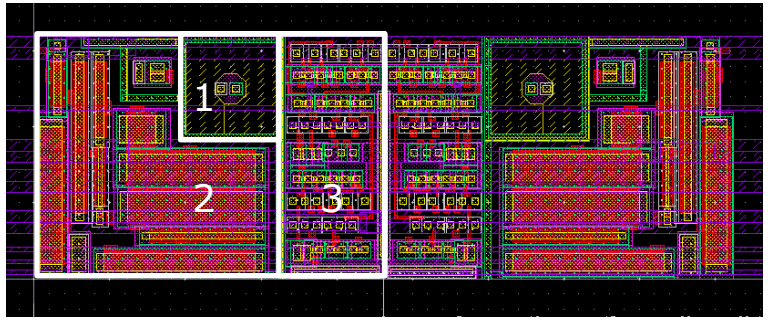
Pixel sensor teams

- JadePix-3/4
  - IHEP: Ying Zhang, Yang Zhou, Zhigang Wu (graduated), Jing, Dong, Wenhao Dong/ USTC, Chunhao Tian/ USTC,Yunpeng Lu, Qun Ouyang
  - CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng (graduated), Anyang Xu (graduated), Sheng Dong, Hulin Wang, Xiangming Sun
  - SDU: Liang Zhang
  - Dalian Minzu Unv: Zhan Shi
- TaichuPix
  - IHEP: Wei Wei, Ying Zhang Xiaoting Li, Jun Hu, Zhijun Liang, Joao Guimaraes da Costa
  - CCNU/ IFAE: Tianya Wu, Raimon Casanova, Sebastian Grinstein
  - NWPU: Xiaomin Wei, Jia Wang
  - SDU: Liang Zhang, Jianing Dong, Long Li

Thank you for your time!

Backup Slides

Small pixel implemented in the JadePix3

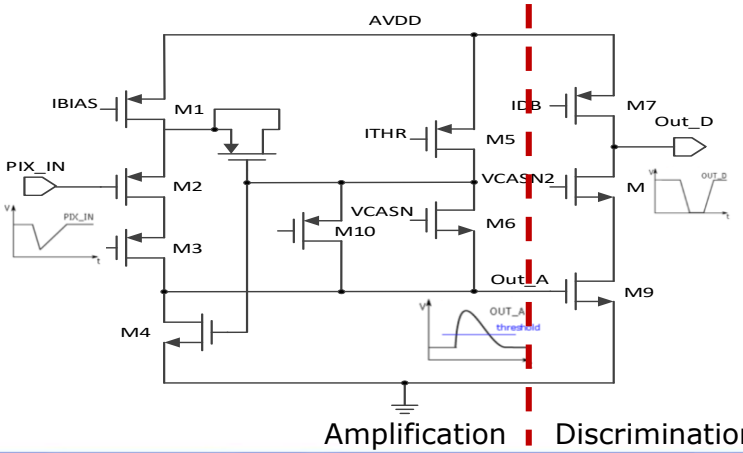


Minimal pixel footprint: **16 µm* 23.11 µm**
1: Sensing diode
2: Analog frontend
3: digital frontend

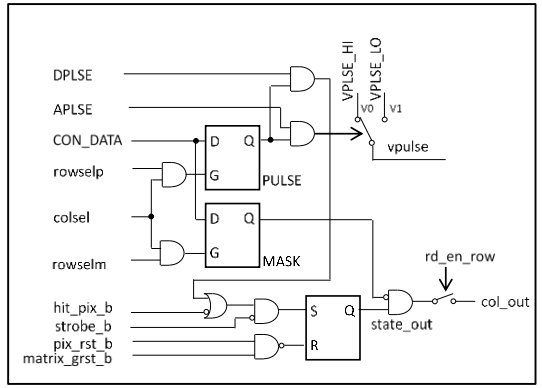
- Small footprint
  - Sensing diode of minimized geometry verified on JadePix1
  - Frontend with **tradeoff** between layout area and FPN*
- Fix φ direction to **16 µm** and allow the z* to vary
  - 3 variants of digital frontend
  - D-FlipFlop vs RS-latch
- Mirrored layout to share bias lines between two columns

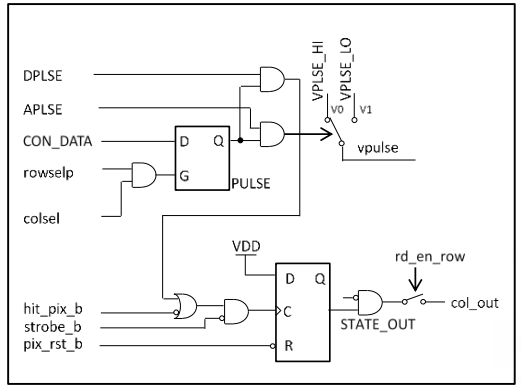
* D. Kim, etc. 2016 JINST 11 C02042

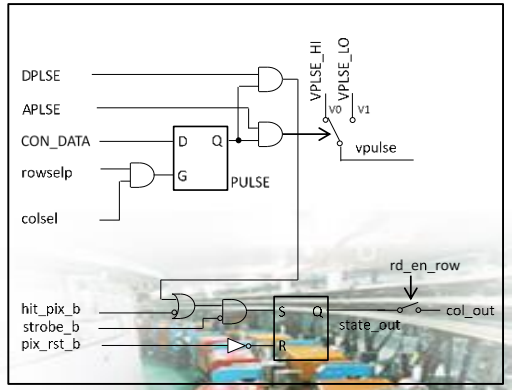
analog frontend



3 variants of digital frontend

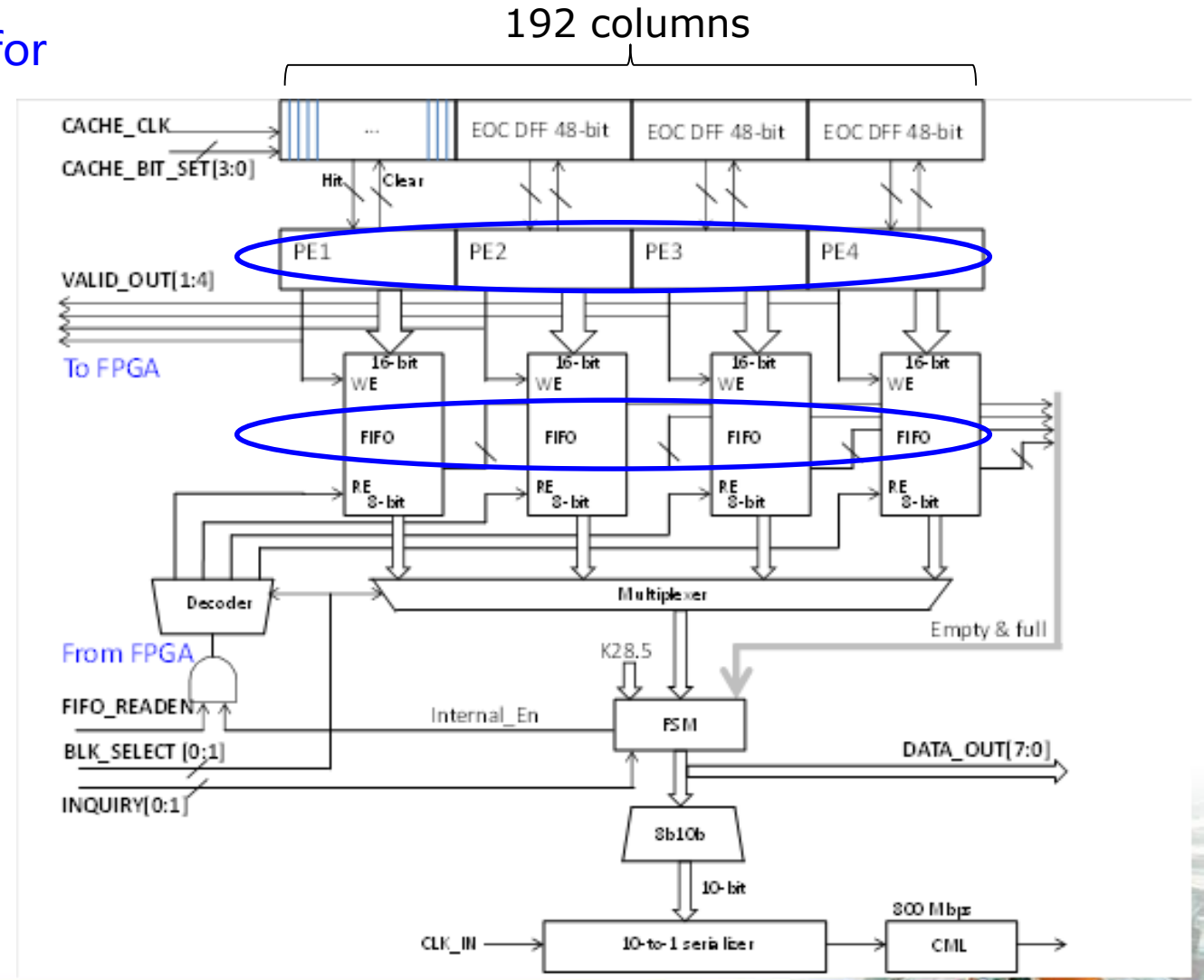






Lower power design in the JadePix3

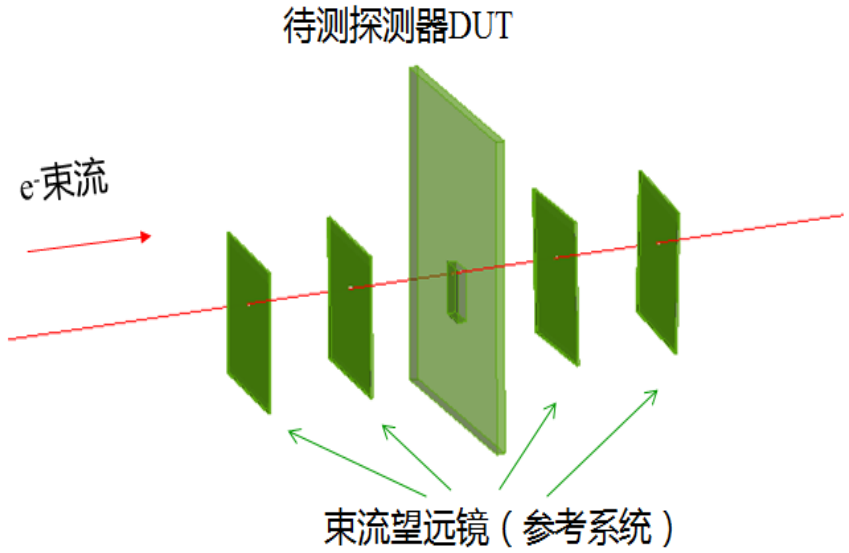
- A low power frontend of **20 nA static current**, equivalent to 9 mW/cm^2
  - Except for the sector 3, where 60 nA used for the comparison of radiation tolerance
- Zero suppression at the end of column
  - **Priority Encoded (PE)** address of HIT pixel
- Data buffering
  - 4 parallel FIFOs * 48 depth
  - Multiplexer controlled by FPGA
  - Allow the **test of readout strategy**
- Extensible along with the matrix sectors



Measurement method of position resolution

Charged particle beam

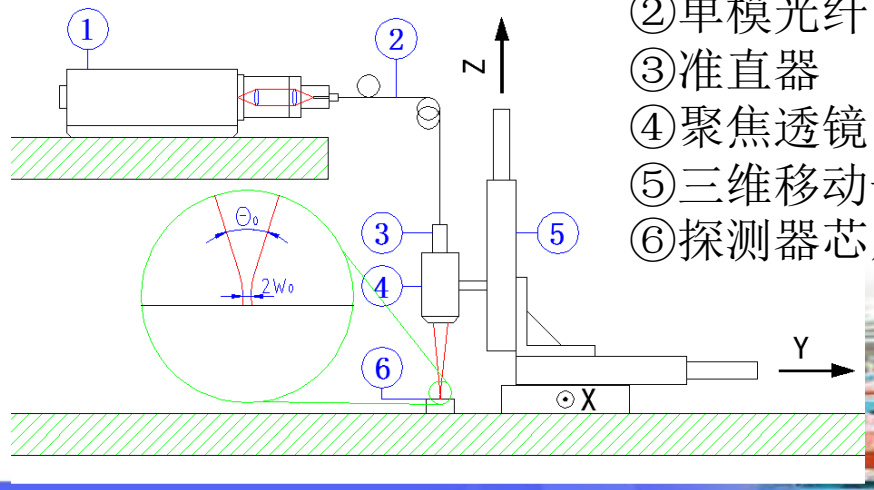
- Random hit position on the full matrix
  - One hit per particle
  - Reconstructed reference position by beam telescope
  - σ of residual = measured - reference
  - Cluster size can be adjusted by threshold tuning

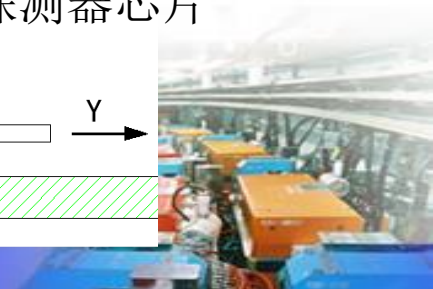


Pulsed laser beam

- Well controlled **scan of laser position** on a **single pixel**
  - One hit per laser pulse
  - Reference position given by the 3-D motion stage
  - σ of residual = measured - reference
  - Cluster size can be adjusted by threshold tuning and **laser power tuning**

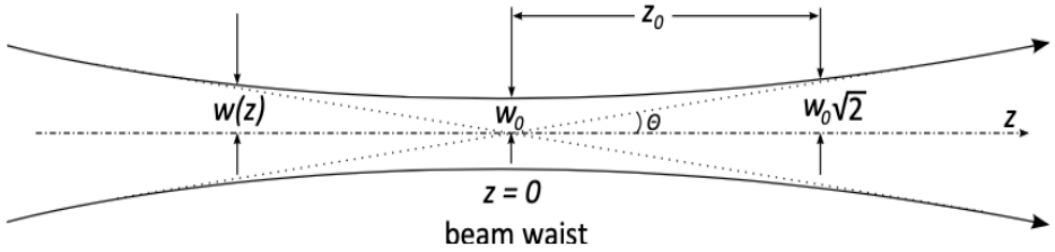
①红外脉冲激光器
②单模光纤
③准直器
④聚焦透镜
⑤三维移动平台
⑥探测器芯片





Laser beam characteristics

Hulin WANG, Shen DONG, Yunpeng LU



- Laser beam characterization
  - Wavelength: 1064 nm
  - Beam waist **ω_0 ~ 1.7 μm**
  - Rayleigh range z_0 ~ 8.5 μm
  - Divergence Angle **θ = ~ 11°**
  - Laser pulse duration ~100 ps
- Laser power tune and coarse calibration
  - 0% : maximum power; 100% : minimum power
  - For final results, use 92.7%, 92.9%, 93.3%, 93.5%, 93.7%
  - 92.7% ~ **4 × threshold** (threshold set to ~220 e-)
  - 93.7% ~ **2 × threshold**