Status Report on SOI

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and SOI PIXEL R&D group

The 2021 International Workshop on the High Energy Circular Electron Positron Collider, 8th November, 2021

SOI Pixel Sensor

SOI: Silicon-on-Insulator technology

Utilize 0.2 μm FD-SOI CMOS process by
Lapis Semiconductor Co. Ltd.

SOI Pixel Detector: Monolithic type detector

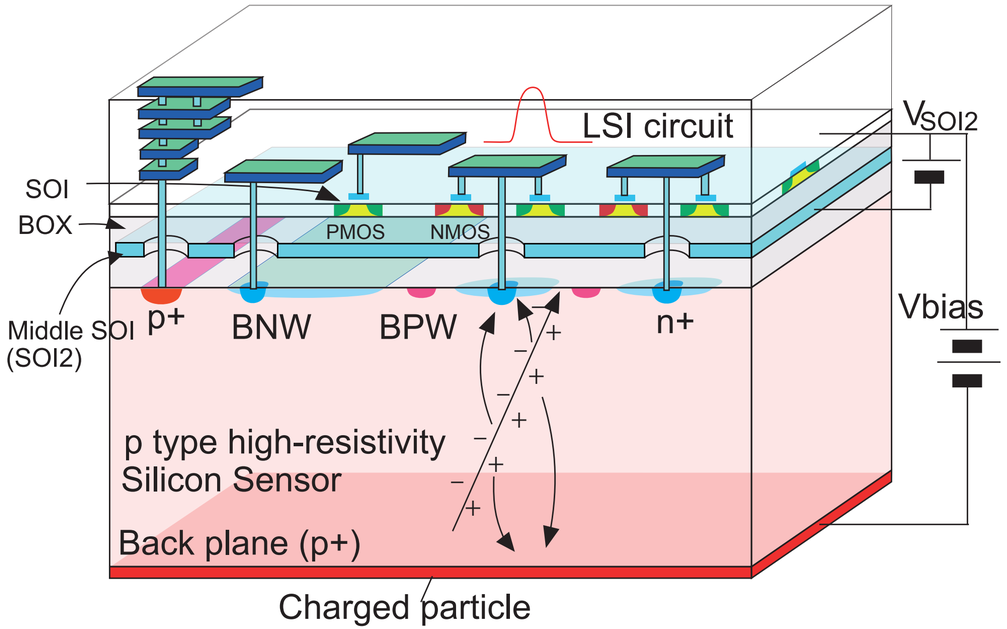
- LSI is processed on Buried Oxide layer (BOX)
- Smaller pixel size, complex circuit in pixel
- Low material budget
- High speed, low power
- Less single event effects (SEE) probability
- Low cost

Double SOI Pixel Detector

Middle Si layer suppresses

- Back gate effect
- Sensor-Circuit cross talk
  - Middle Si layer shields coupling between sensor and circuit.
  - It is useful for analog and digital mixed circuit in pixel.
- Radiation damage (TID)
  - It is able to compensate electric field generated by trapped holes in the BOX.
  - It can be used in high radiation environment (~1MGy).
  - (K. Hara, Vertex2017, Sep. 11-15, 2017, Las Caldas)

Double SOI Pixel Detector



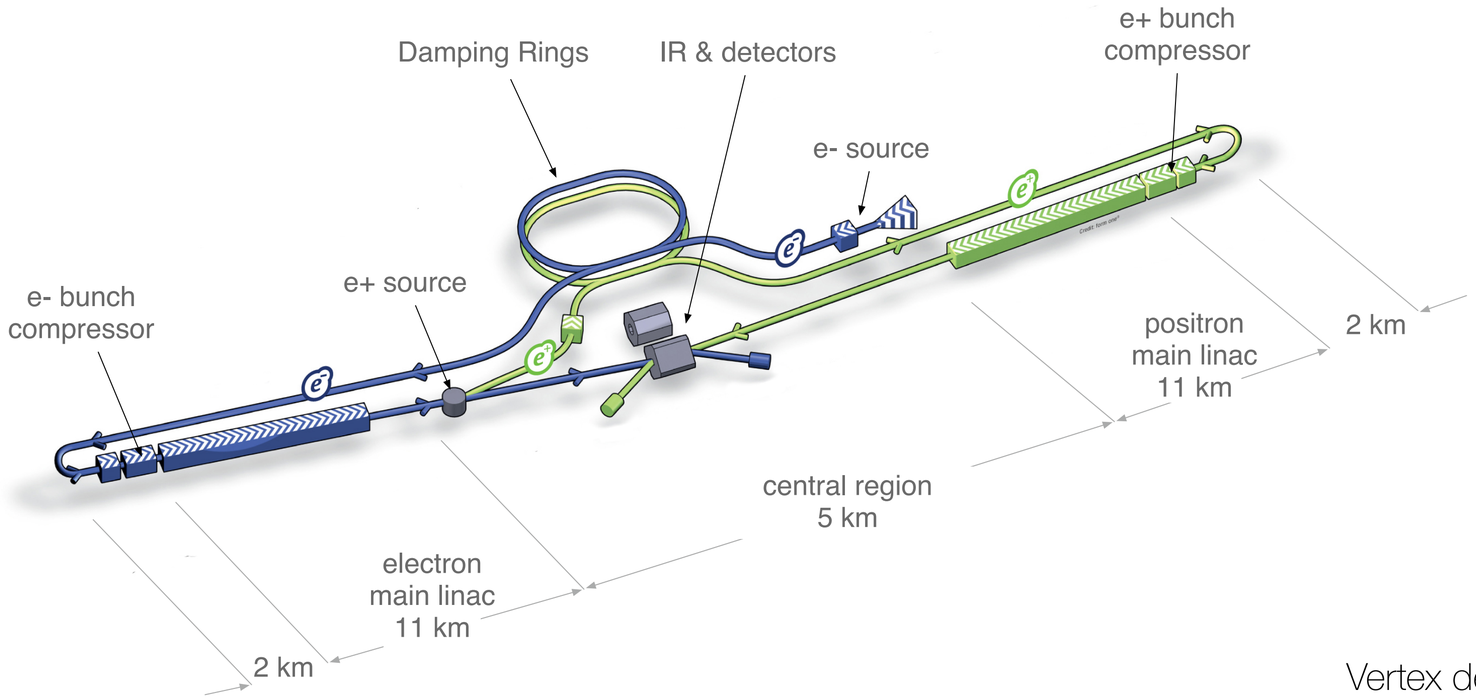
Illustrated by T. Tsuboyama (KEK)

Sensor thickness: 50 - 500 μm
Sensor Resistivity: > 1 kΩ·cm
SOI2 thickness: 150 μm (*n*-type)
SOI2 Resistivity: < 10 Ω·cm

ILC Experiment and Vertex Detector

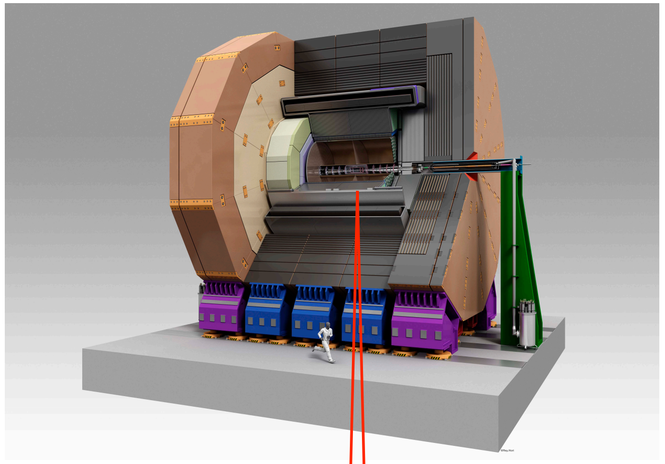
ILC Experiment

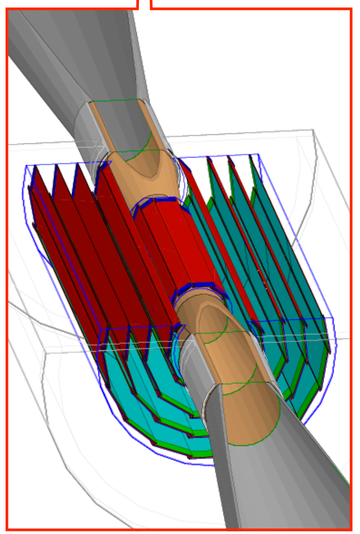
- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for physics beyond the Standard Model



ILC TDR vol.4: Detectors
ILD Concept Group, T. Abe et al., arXiv:1006.3396 [hep-ex].

ILC detector concept (ILD)



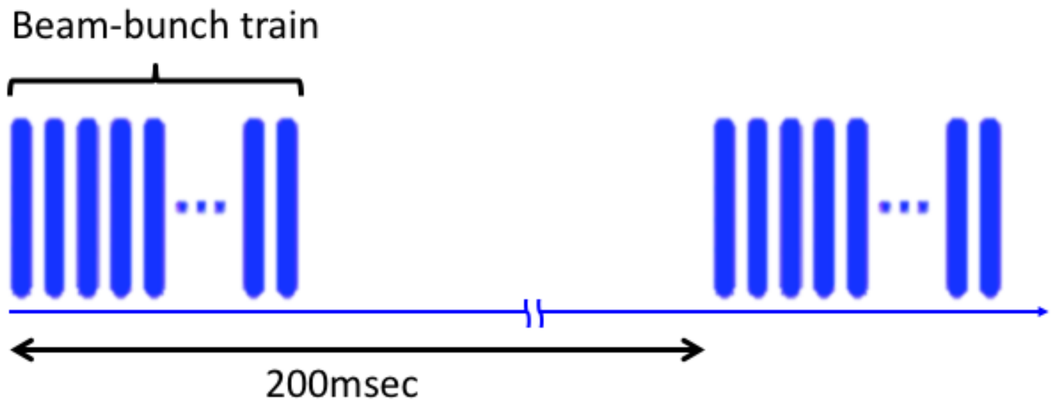


Vertex detector geometry (VTX-SL)

ILC Experiment and Vertex Detector

Requirements:

1) Single point resolution: better than 3 μm
   Pixel size: ~20 × 20 μm^2
2) Time resolution: single-crossing (554 ns interval) time resolution
3) Detector occupancy: < 2 %
4) Low material budget: $X \leq 0.1 - 0.2\ \%\ X_0$ / Layer
   corresponds to ~ 100 - 200 μm Si, (supports, cables and cooling add further material)
   low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year



ILC TDR v4 Detector
LC Vertex / Tracking R&D 2nd Nov. 2015

Architecture of SOFIST

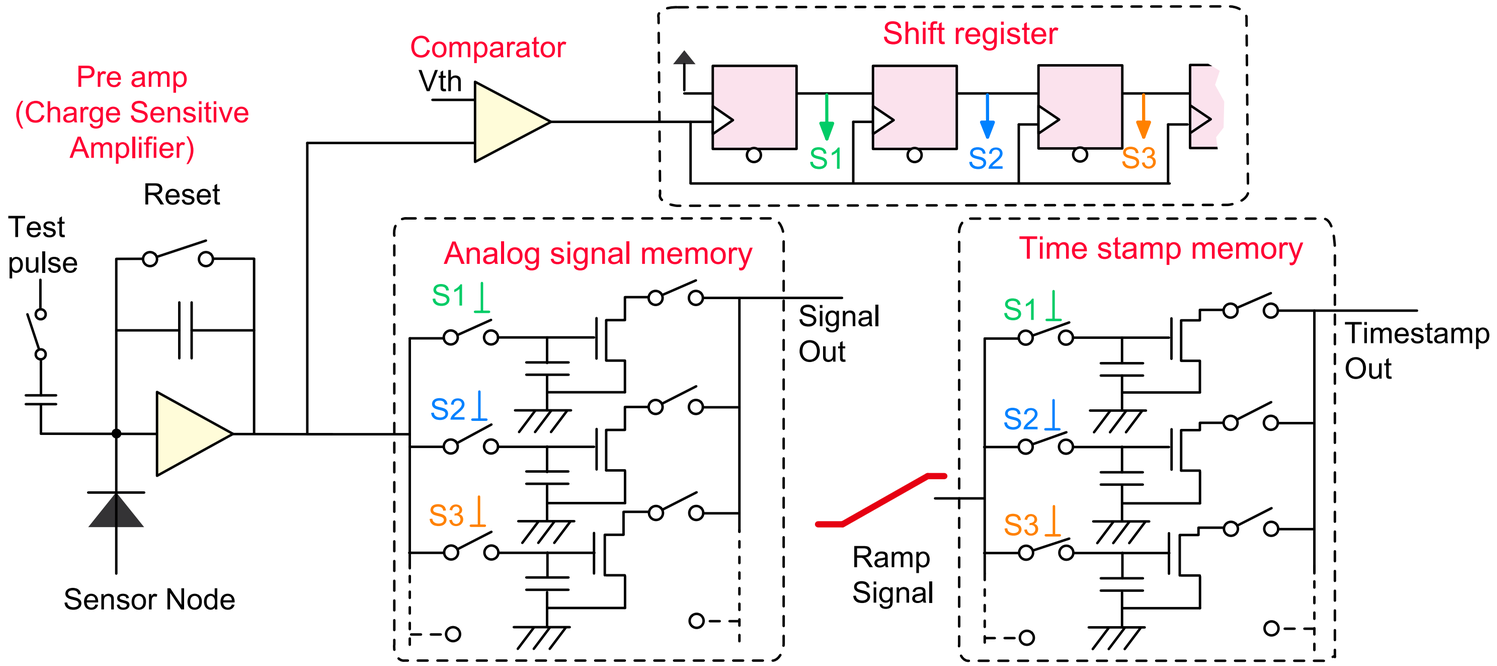
In a Pixel

- **Pre-amplifier**
- **Comparator**
  Keep the analog signal and time stamp if a signal exceeds a threshold V_{th}.
- **Shift register (Hit memory)**
  Latch for multiple memories.
- **Analog signal memory**
  Store signal charges up to two (or more) hits.
- **Time stamp circuit**
  Store time stamps up to two (or more) hits.

On Chip

- **Column ADC**
  Digitize analog signal and time stamp.
- **Zero-Suppression logic**
  Extract hit pixels and reduce the data to transfer to backend.

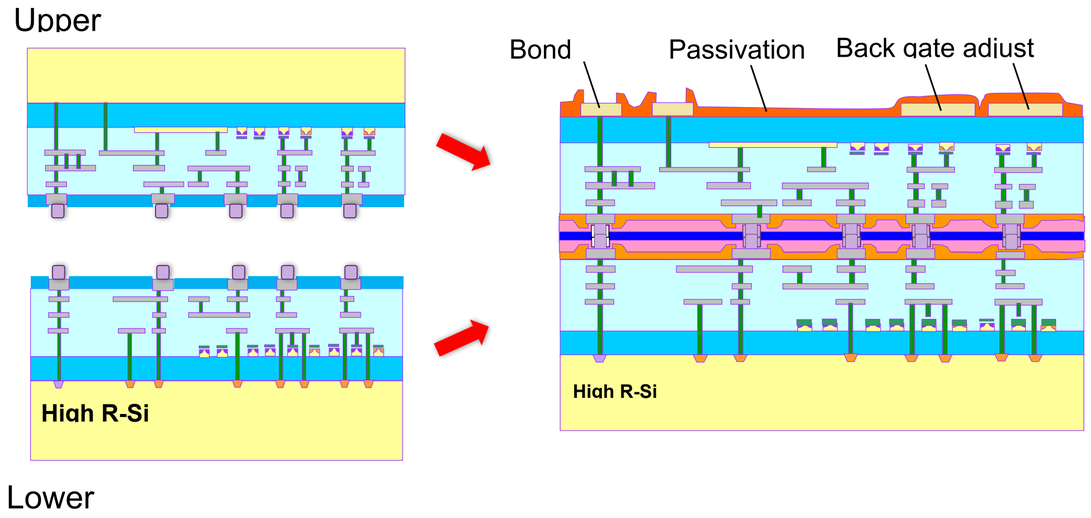
SOFIST Pixel Circuit

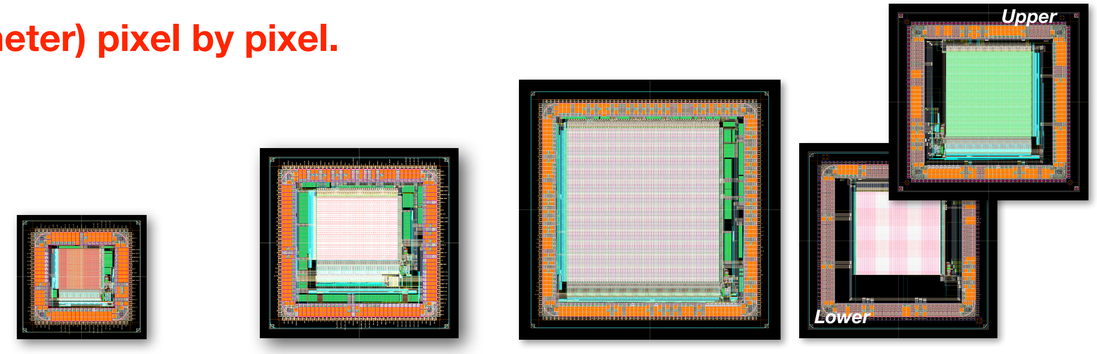


SOFIST4

by Tohoku-Micro Tec (T-Micro), M. Motoyoshi
http://www.t-microtec.com

Two SOFIST4 chips (lower and upper) are connected by **micro bump (3 μm diameter) pixel by pixel.**
→ Keep pixel size small and implement complex circuit three dimensionally.





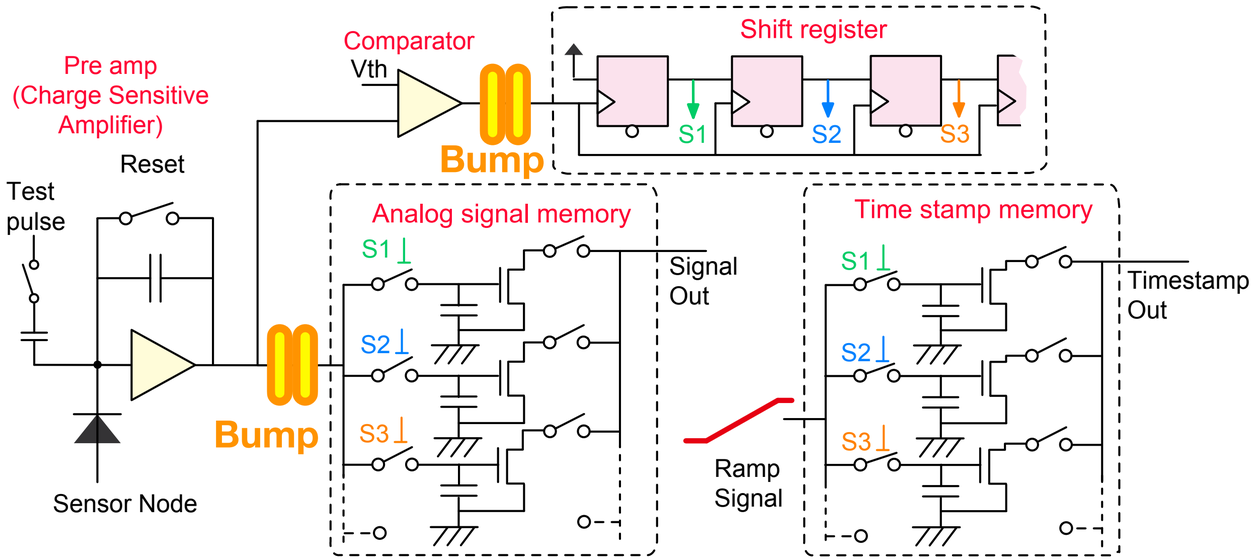
SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

SOFIST3
Full function
(30×30 μm² pixel)

SOFIST4
Full function
(20×20 μm² pixel)

Lower Chip (Pixel):
Used as sensor and implement analog circuit in a pixel.
Upper Chip (Pixel):
Sensor layer is removed by wet etching and then formed Al pad for wire bonding on the BOX.
Digital circuits/memories are implemented in a pixel.



SOFIST4

Two SOFIST4 chips (lower and upper) are connected by micro bump (3 μm diameter) pixel by pixel.
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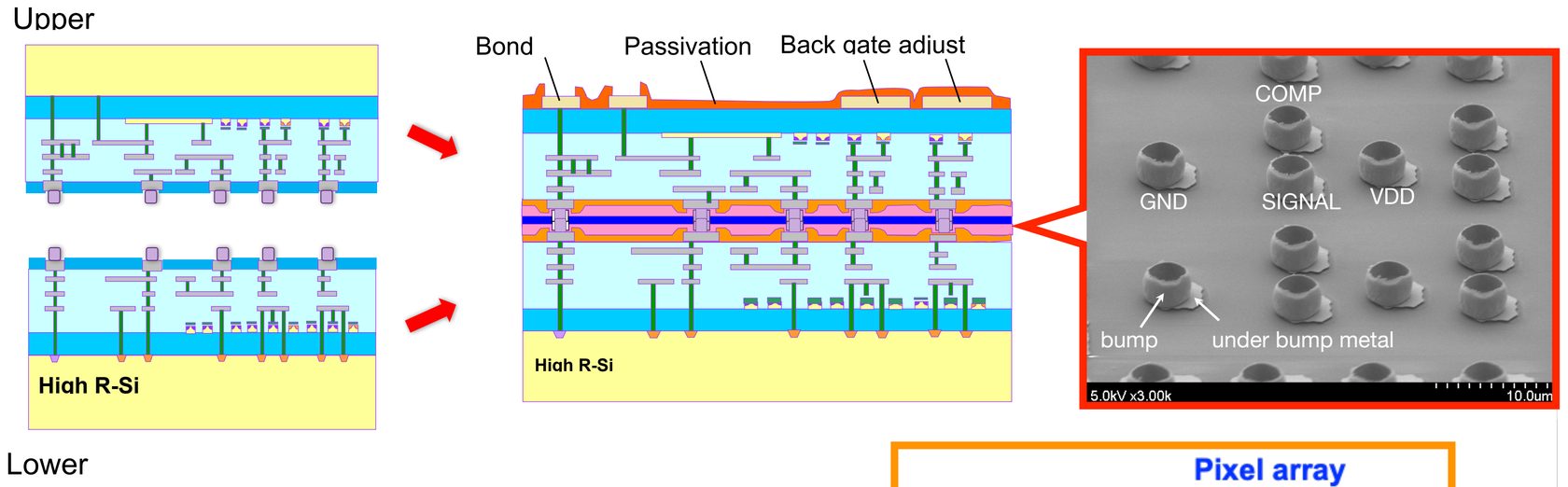
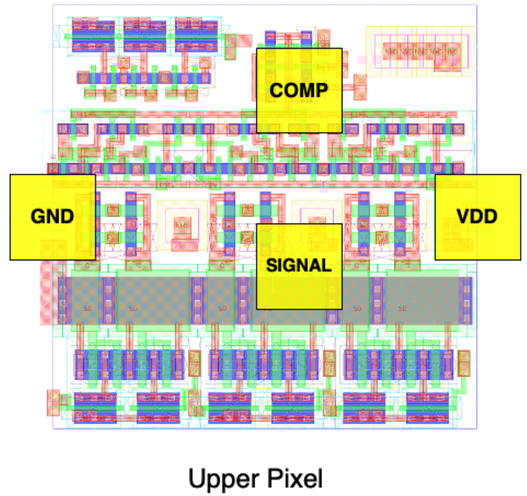
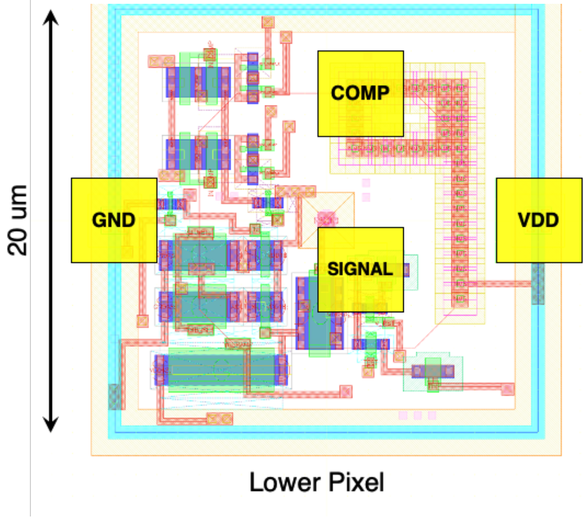
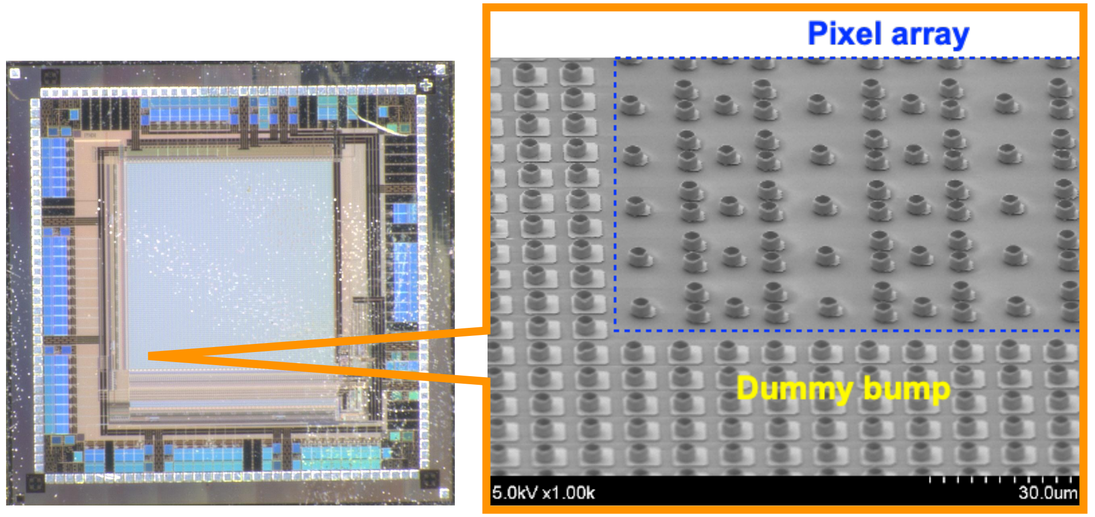


Lower and Upper Pixel Layout







SOFIST4 Chip

- Chip size: 4.45 × 4.45 mm^2
- Pixel size: 20 × 20 μm^2
- Active area: 2.08 × 2.08 mm^2
- Sensor type: FZ p-type
- Sensor thickness: 300 μm
- Sensor resistivity: 3 – 10 kΩ・cm

Beam Test

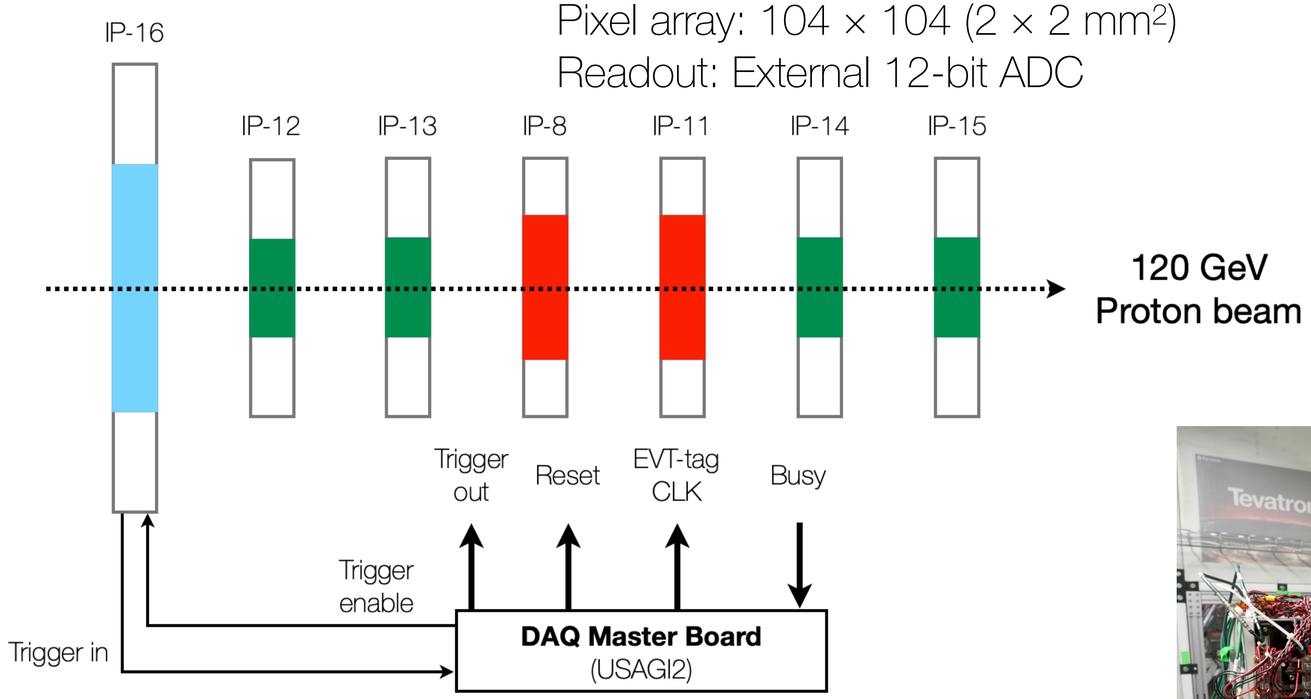
Beam: 120 GeV proton (Fermilab Beam Test Facility)
DAQ rate: ~120 events/s

SOFIST4

Pixel size: 20 × 20 μm²
Pixel array: 104 × 104 (2 × 2 mm²)
Readout: External 12-bit ADC

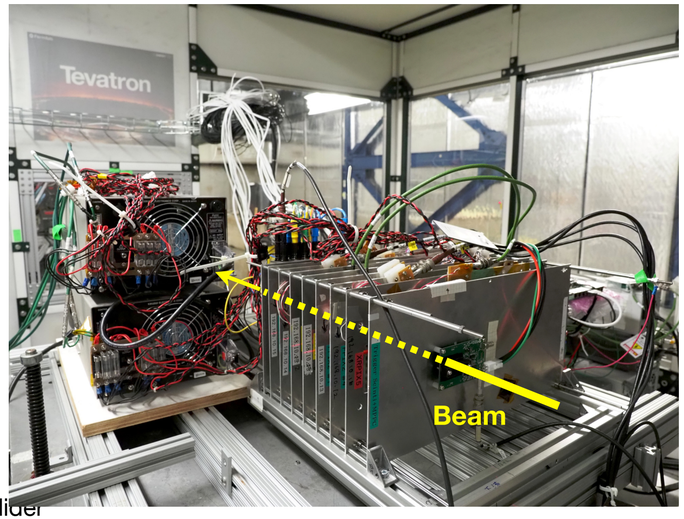
FPIX2 (SOIPIX)

Telescope for SOFIST
σ ~0.7 μm
Pixel size: 8 × 8 μm²
Pixel array: 128 × 128 (1 × 1 mm²)
Readout: External 12-bit ADC



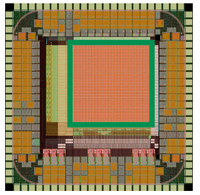
XRPIX5 (SOIPIX)

Trigger counter
Pixel size: 36 × 36 μm²
Pixel array: 608 × 384 (24.6 × 13.8 mm²)
Region of Interest function
Readout: External 12-bit ADC

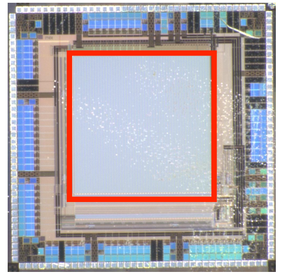


* **Active area:** FPIX2: 1 × 1 mm², SOFIST4: 2 × 2 mm²

FPIX2



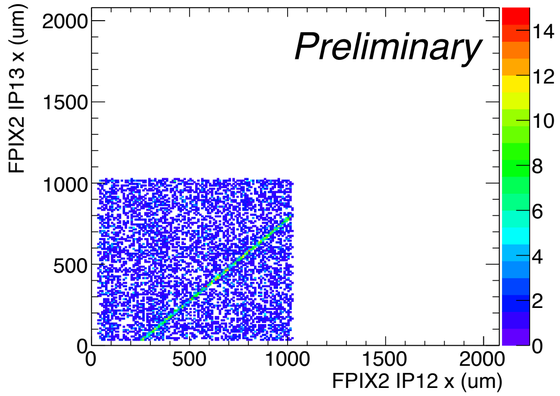
SOFIST4

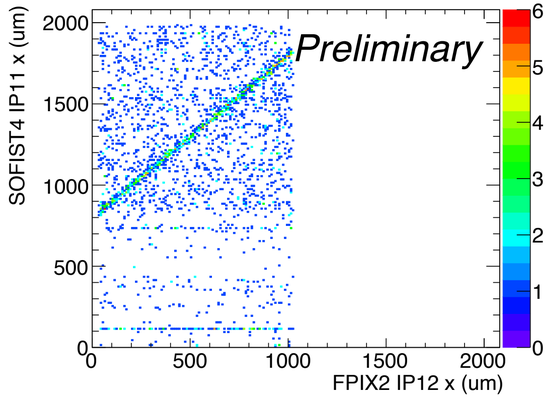


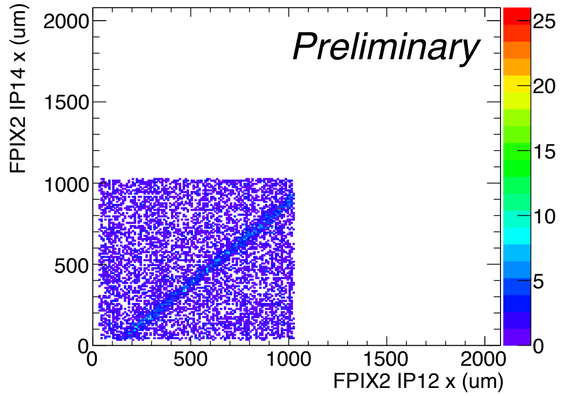
Hit Correlation

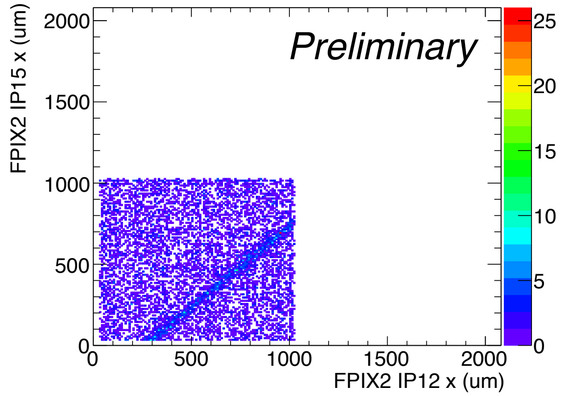
Hit position correction between **telescope (FPIX2) and SOFIST4 IP-11** in *x* and *y*-direction.

x-direction

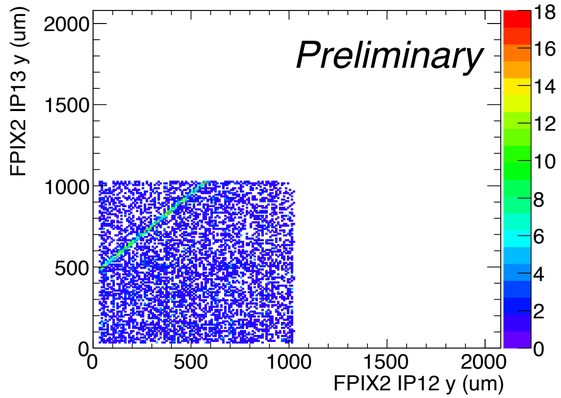


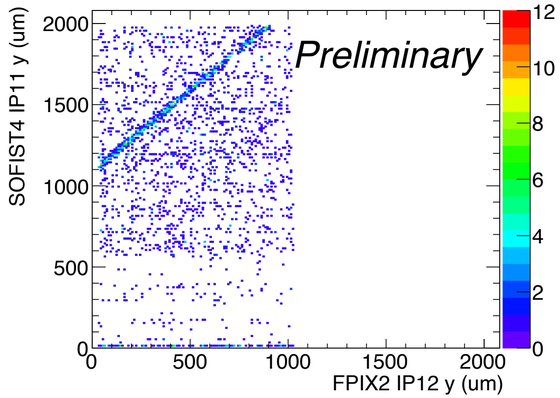


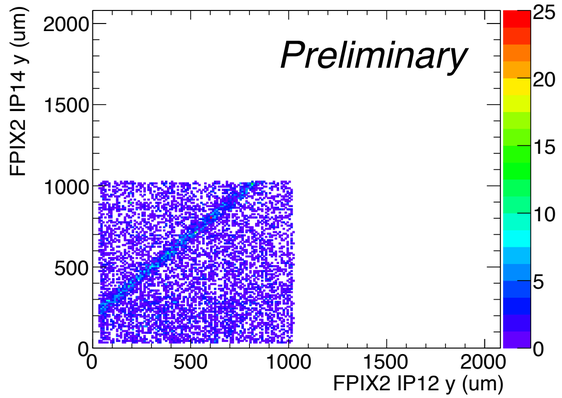


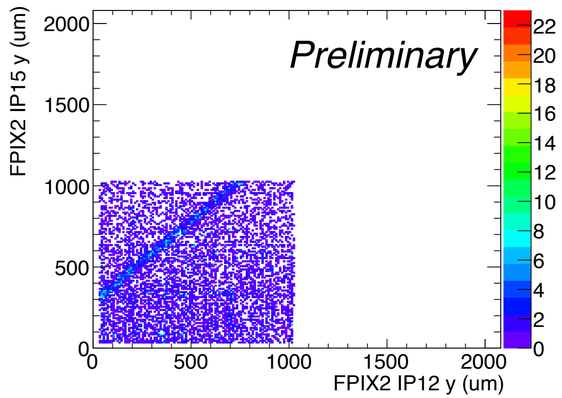


y-direction









Development for the CEPC vertex

- SOI technology offers unique opportunity to meet the challenge
  - Identified as a sensor option in the CDR (Concept Design Report)
  - Active R&D by the IHEP group
- Precision of flavor tagging driven by the physics program
  - Tagging efficiency and purity
  - Higgs @ 250GeV, W @ 160 GeV, Z @ 90 GeV
- Continuous colliding mode
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z
  - Strong constraint on the operation mode and power consumption of pixel sensor
  - Power pulsing proposed for the linear collider, not beneficial here

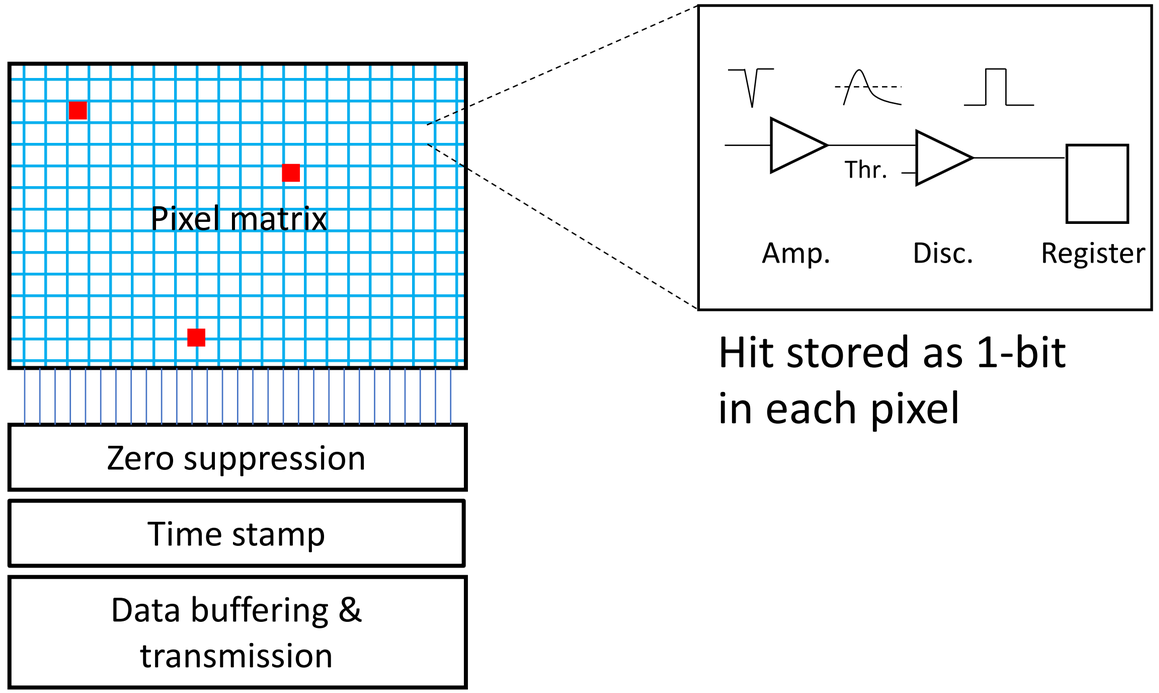
Colliding mode and bunch spacing

	Higgs	W	Z (3T)	Z (2T)
Center-of-mass energy (GeV)	240	160	91	
Luminosity/IP (10^{34} cm^{-2} s^{-1})	3	10	16	32
Total Integrated Luminosity (ab^{-1}) -2 IP	5.6	2.6	8	16
Bunch numbers (**Bunch spacing**)	242 (**680 ns**)	1524 (**210 ns**)	12000 (**25ns + 10% gap**)	

Design guideline in general

- 1-bit binary readout scheme adopted in the pixel sensor design
  - Small pixel size to enable spatial resolution < 3 μm
  - In-pixel discriminator to eliminate the excessive driven current
  - Zero-suppression to minimize the data load on-chip
  - Hit processing within O(1 μs) to keep the occupancy low

} for low power

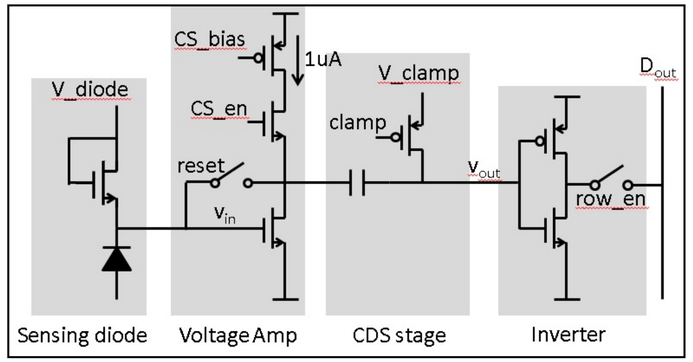


Hit stored as 1-bit
in each pixel

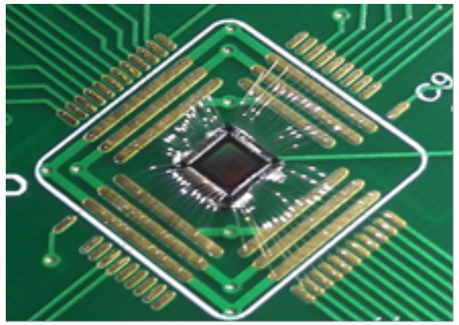
Sketch to illustrate the readout scheme

Investigation on the spatial resolution

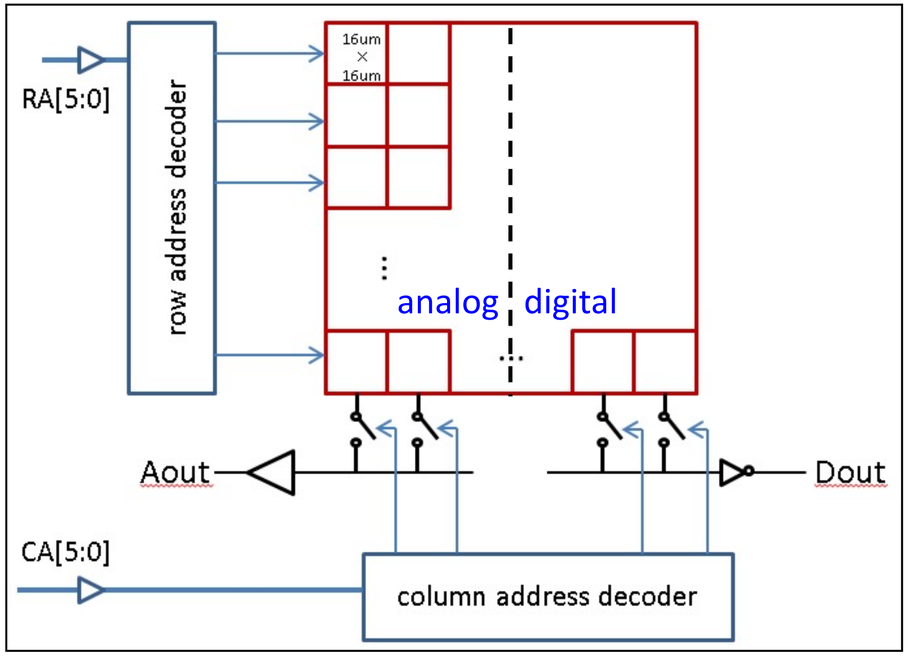
- Pitch and cluster size (# of pixel per hit) are the most relevant
  - Shrinking of pitch is limited by the layout area of pixel circuit
  - Cluster size relies on the signal charge sharing and discriminator threshold applicable
- CPV-1/2/3 dedicated to study spatial resolution
  - Voltage amplifier, DC Gain ~ 10
  - CDS to eliminate the KT/C reset noise
  - Inverter as discriminator
  - Sequential readout via a single port
  - **Minimum matrix pitch = 16 µm**



Schematic of the pixel in CPV-1/2



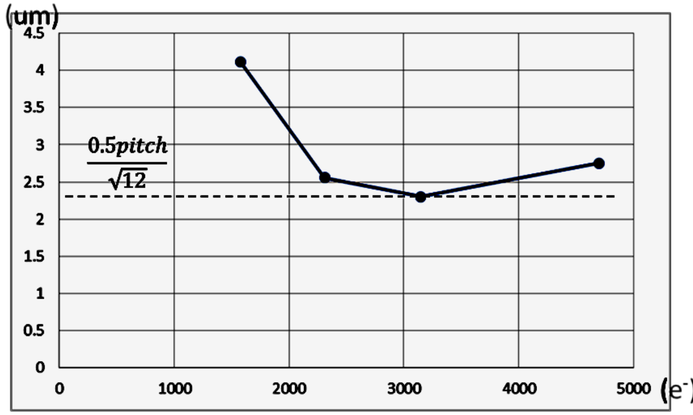
CPV-2 (2.9 ×2.9 mm^2) mounted on the PCB



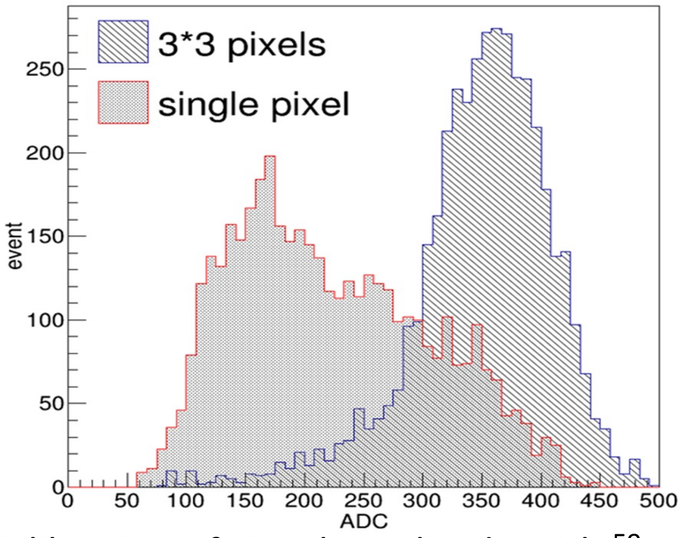
Matrix and steering logic in CPV-1/2

Highlight of test results from CPV-2

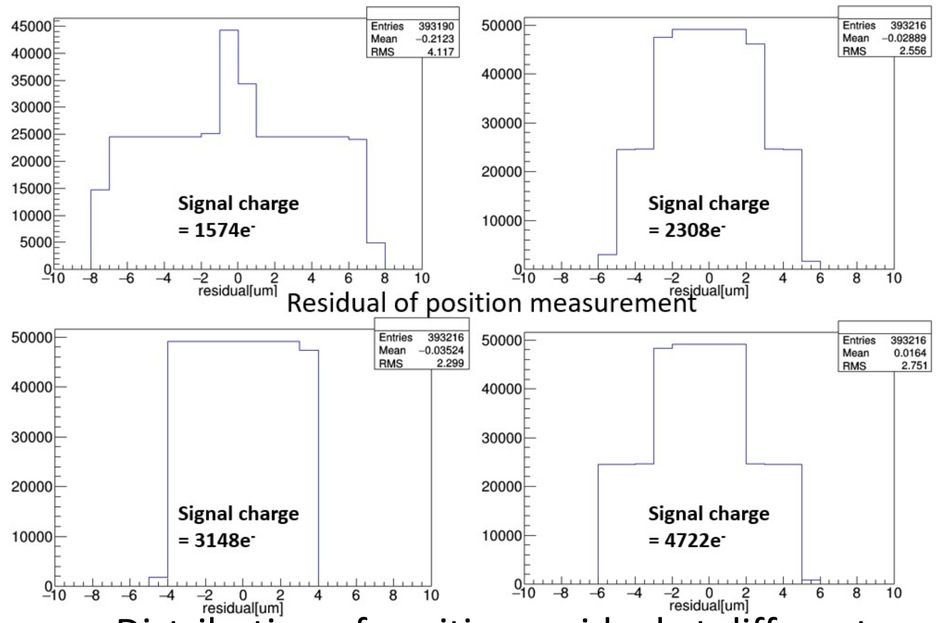
- Position residual measured on the CPV-2
  - Fully depleted sensor thickness 75 µm
  - **1064nm laser beam, focused to 3.4 µm**
  - Calibrated with ^{59}Fe X-ray source
  - Threshold set to 200 e^-
- σ = 0.5 pitch / √12 = 2.3 µm achieved
  - **Small pitch (~16 µm) is essential**



σ of position residual at different laser beam intensity



Calibration of signal amplitude with ^{59}Fe X-ray



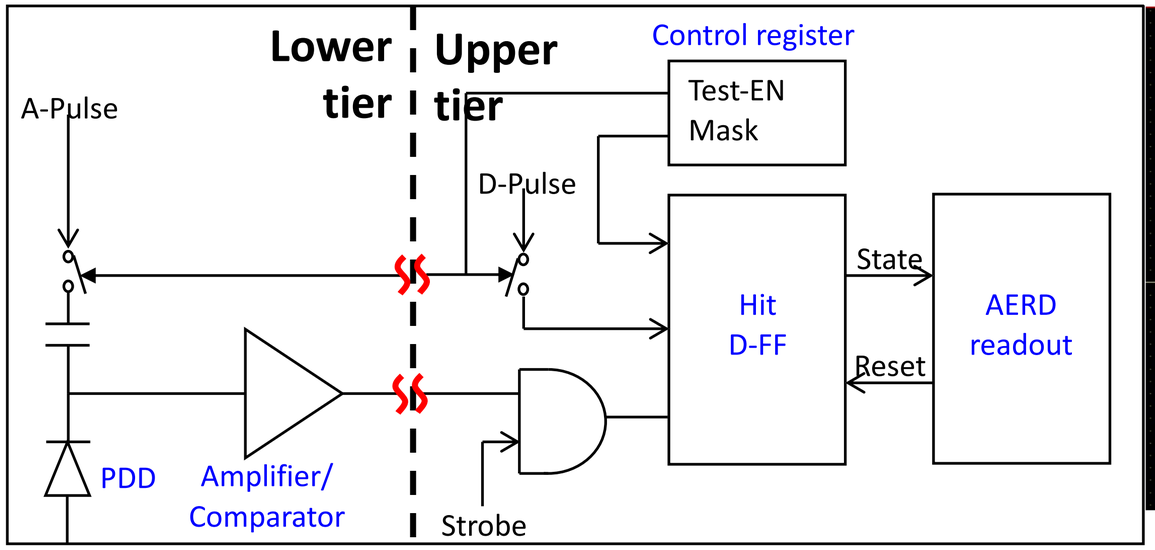
Residual of position measurement

Distribution of position residual at different laser beam intensity

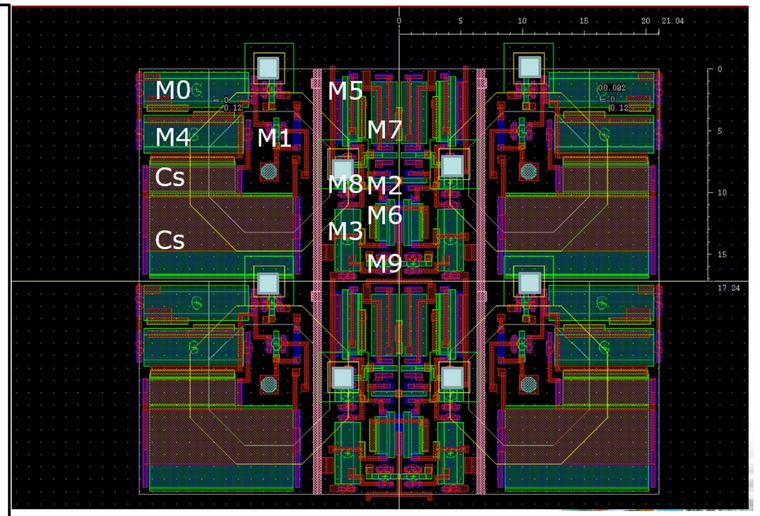
Exploring the 3D technology on CPV4 design

- 2 tiers to accommodate the full-functioned pixel: **17 × 21 µm² on each**
  - Lower tier: PDD sensing diode + amplifier/comparator
  - Upper tier: Hit D-Flipflop + Control register + AERD readout*
- 2 vertical connections in each pixel: comparator output and test switch
  - Power / ground connection implemented in the I/O pad ring
- Critical to make the PDD and analog front-end compatible
  - $V_{thr.}$ shift by -70 mV/PMOS, 50 mV/NMOS as the PDD depleted (-4V)

*AERD proposed in NIMA 785 (2015) 61-69



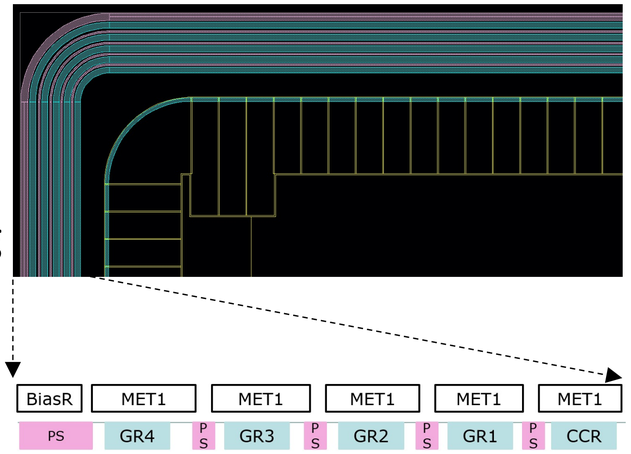
3D bumps marked with ▢

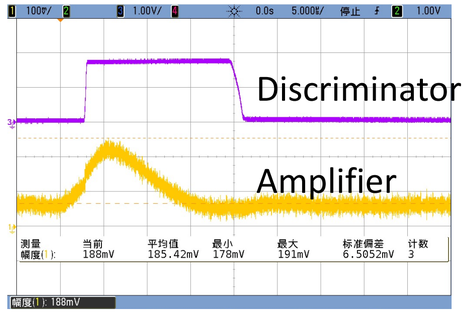


4 pixels arranged in 2 columns

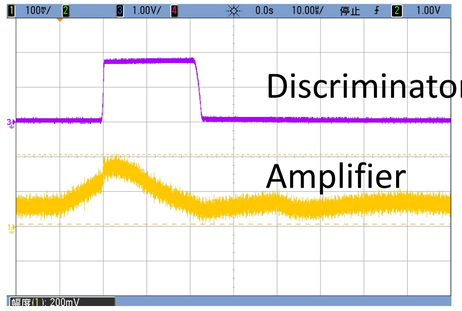
Functional verification of CPV-4 before 3D integration

- Quick test on the Lower and upper tier **separately**
  - Checkpoint before the 3D integration
- Leakage current reduced successfully by
  - Optimization of PDD implant dose
  - 1 Bias Ring + 4 Guard Ring + 1 Current Collecting Ring
- Analog frontend operated with the PDD sensor
  - Analog waveform inspected on oscilloscope
- Digital logic functions have been verified also

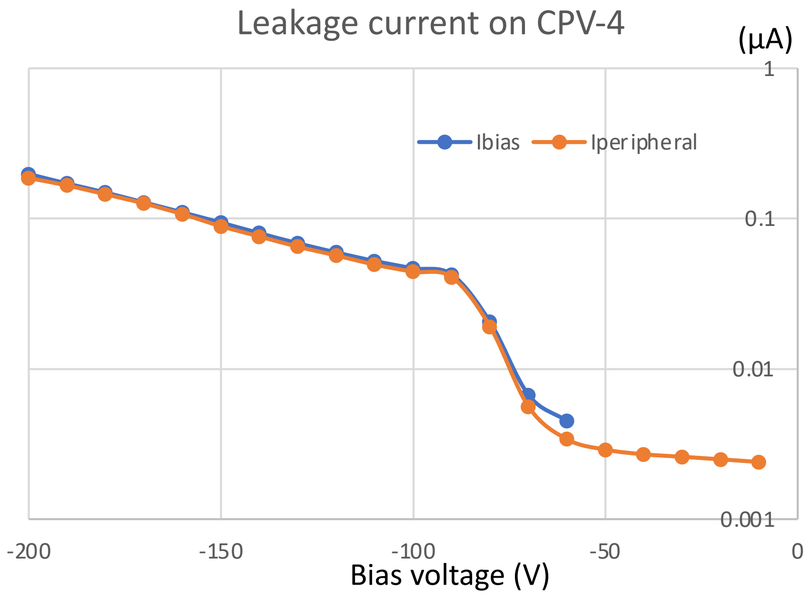




Analog frontend w/o PDD
Test charge injected ~ 100 e-



Analog frontend with PDD
Test charge injected ~ 750 e-



Summary

We are designing and developing a monolithic type pixel detector with SOI technology for vertex detector.

SOFIST4 and CPV4 is SOI based 3D stacking pixel sensor using Au micro bump connection pixel by pixel

SOFIST1 & 2:
Position resolution: ~1.4 μm, Time resolution: ~1.55 μs (Analog signal readout)

SOFIST4:
3D stacking bump connection yield ~99.9 %
Successfully detected hits by 120 GeV proton beam.
Confirmed hit correlation between telescopes.
→ Still working on the beam test data analysis (alignment, tracking and position resolution).

CPV 2:
Position resolution: ~2.3 μm (Binary readout)

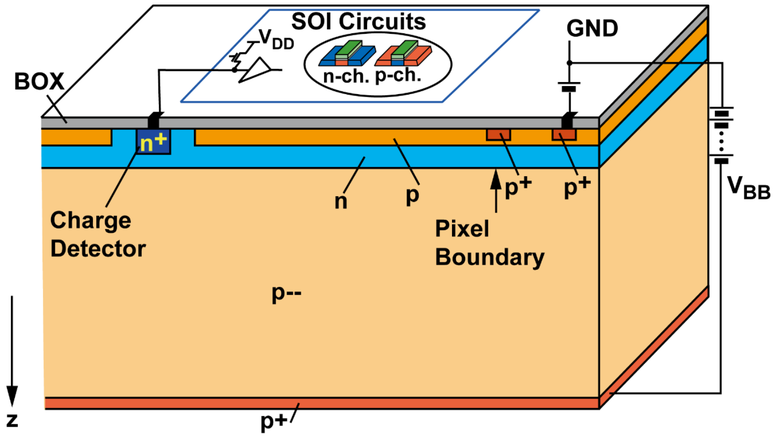
CPV4:
Lower and Upper chips have already delivered to IHEP.
Quick test before 3D stacking for the analog signal amplifier and discriminator (lower tier) are working well.
Digital part (upper tier) test have also verified.

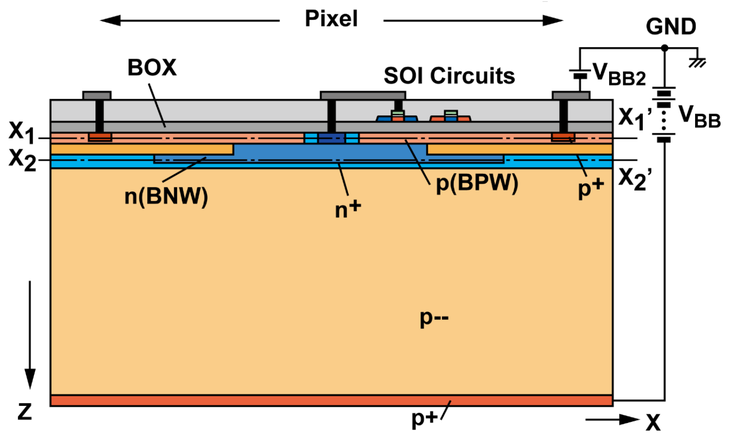
High spatial resolution, highly-integrated, complex circuit, low power and low material budget are common issues for the ILC and CEPC experiment.

Backup

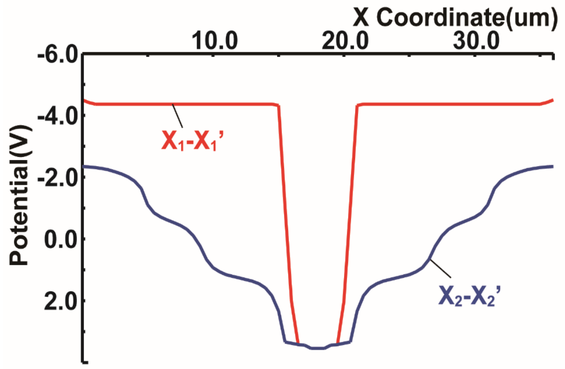
PDD

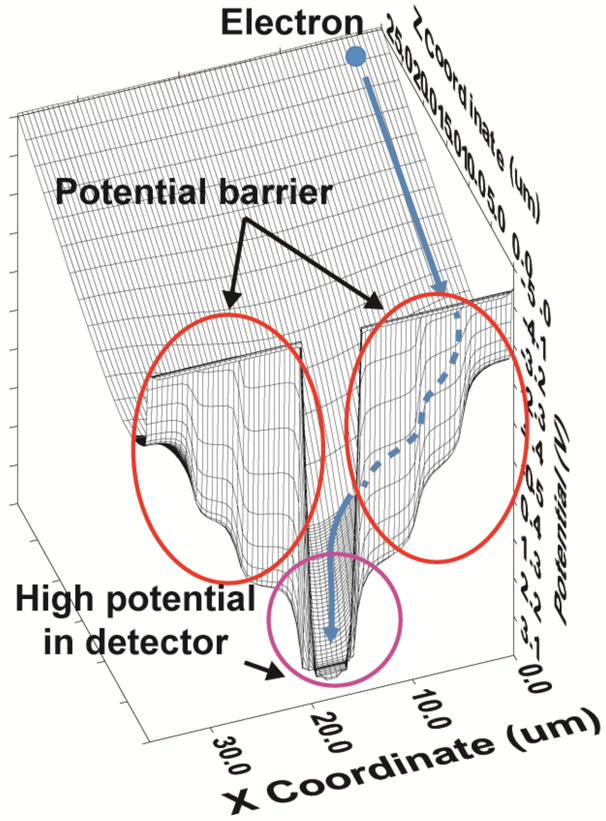
A SOI Pixel Detector Using Pinned Depleted Diode Structure (SOIPIX-PDD)





VBB=-15V
VBB=-4V
25kΩcm, 200μm
36μm x 36μm





- Pinned Surface of Si Substrate with High Density Holes
  → Very Low R-G Dark Current
- Buried Channel → No Carrier Loss Due to Si-SiO_2 Interface Traps
  → Nearly 100% Charge Collection Efficiency
- Lateral Electric Field to Gather Electrons into an n^+ Sensing Node
  → High Sensitivity and Low Noise Due to Small Sensing Capacitance

Shizuoka University, University of Kyoto, University of Miyazaki and KEK of SOIPIX R&D Group

SOIPIX Silicon-On-Insulator Pixel Detector Project

ILC Experiment and Vertex Detector

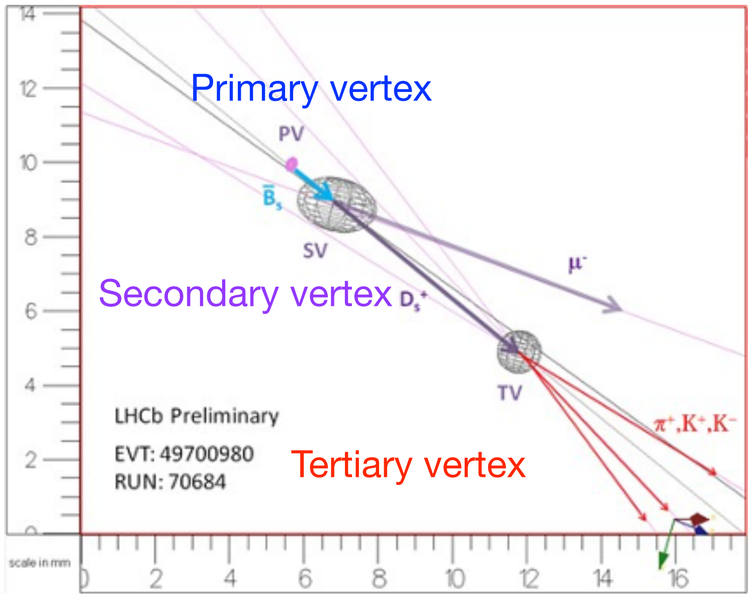
ILC Experiment

- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for physics beyond the Standard Model

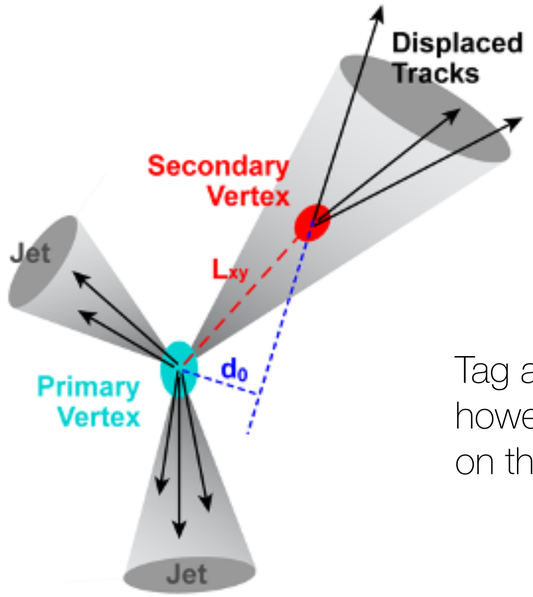
Existence of *b*, *c* quarks and tau lepton in event

Tagging of *b*, *c*, and tau,
reconstruct tracks of daughter charged tracks
interpolate tracks to collision point to reconstruct vertices
→ Displaced vertex and large significance of impact parameter d0 are evidence of existence of *b*, *c*, and tau.

Typically ~10 μm spatial resolution for pixel detector



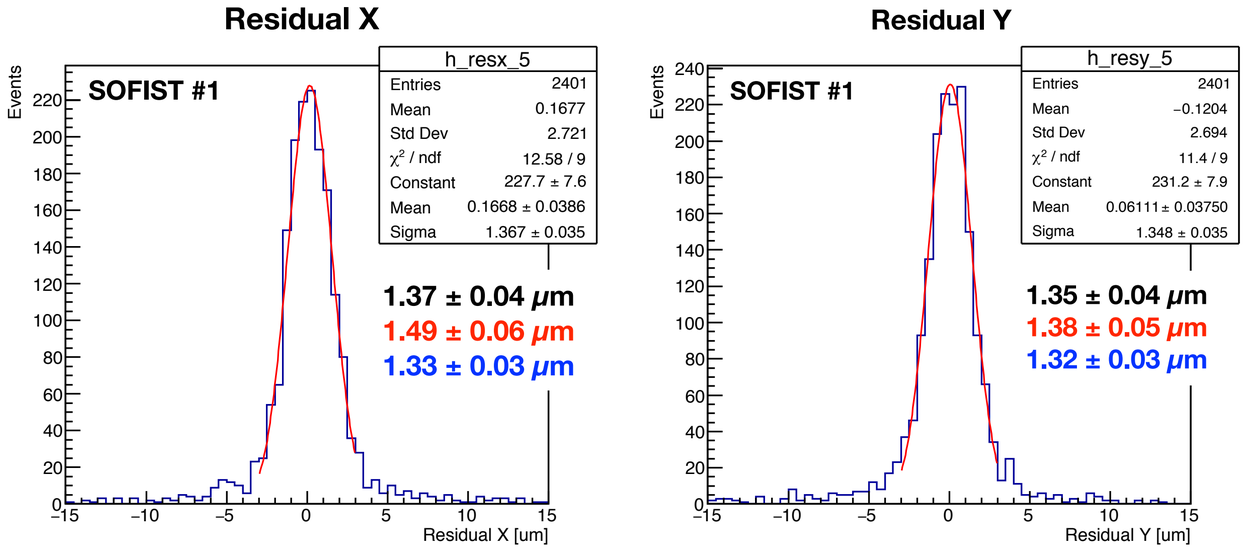
Ref: LHCb Collaboration

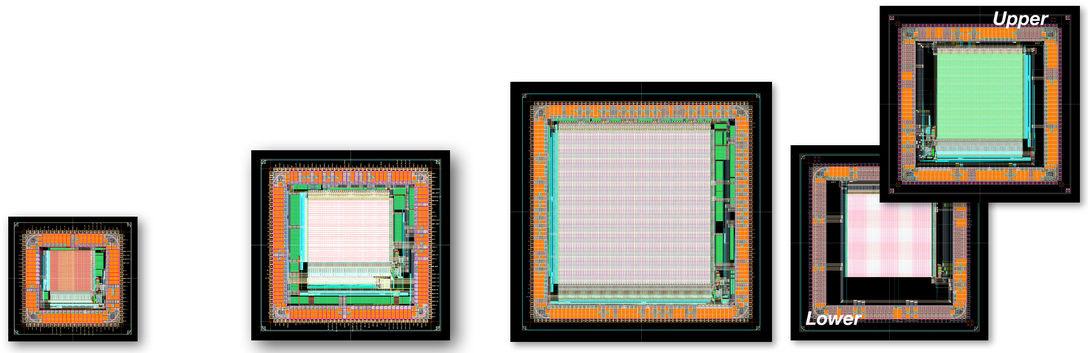


Ref: D0 experiment

Tag algorithms have been developed in each experiment, however, precision of *b*, *c*, and tau identification depends on the performance of the silicon detectors.

SOFIST1





SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

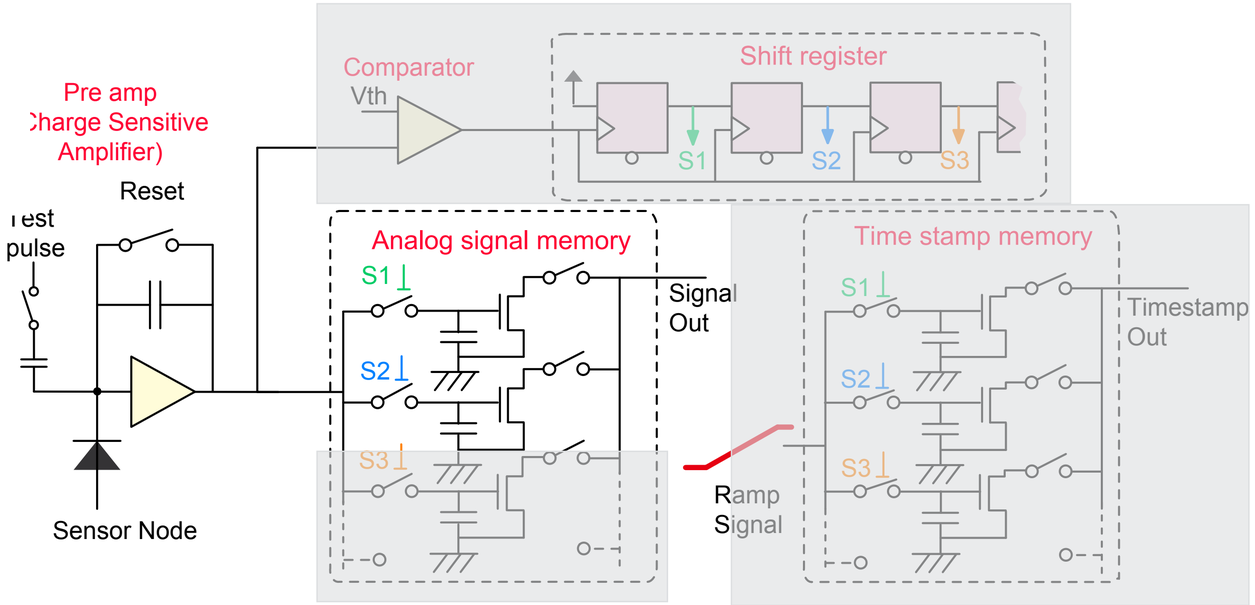
SOFIST3
Full function
(30×30 μm² pixel)

SOFIST4
Full function
(20×20 μm² pixel)

Sensor Thickness: 500 μm

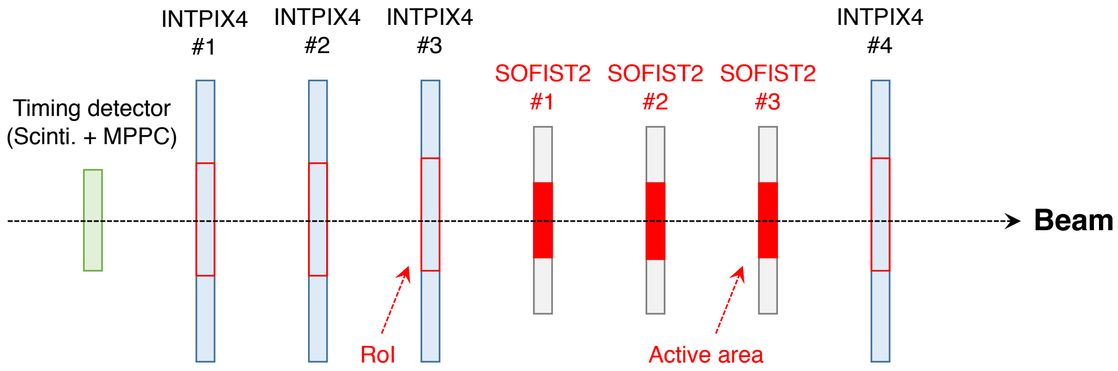
Readout and Sensor depletion layer

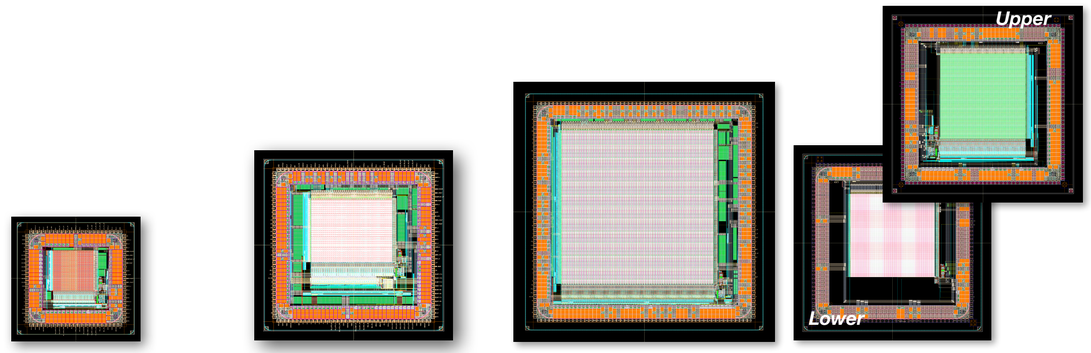
12-bit external ADC, 500 μm (Full depletion)
8-bit on-chip ADC, 500 μm (Full depletion)
12-bit external ADC, 200 μm (Partial depletion)



SOFIST2

Sensor Thickness: 65 μm





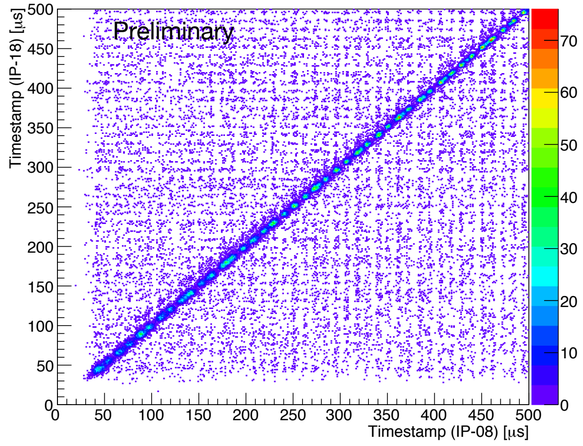
SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

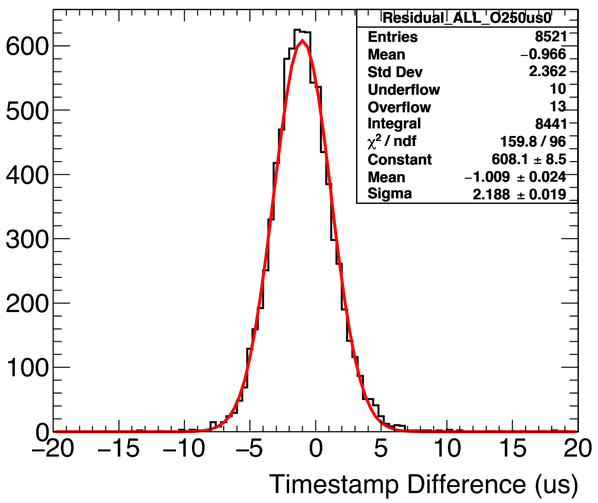
SOFIST3
Full function
(30×30 μm² pixel)

SOFIST4
Full function
(20×20 μm² pixel)

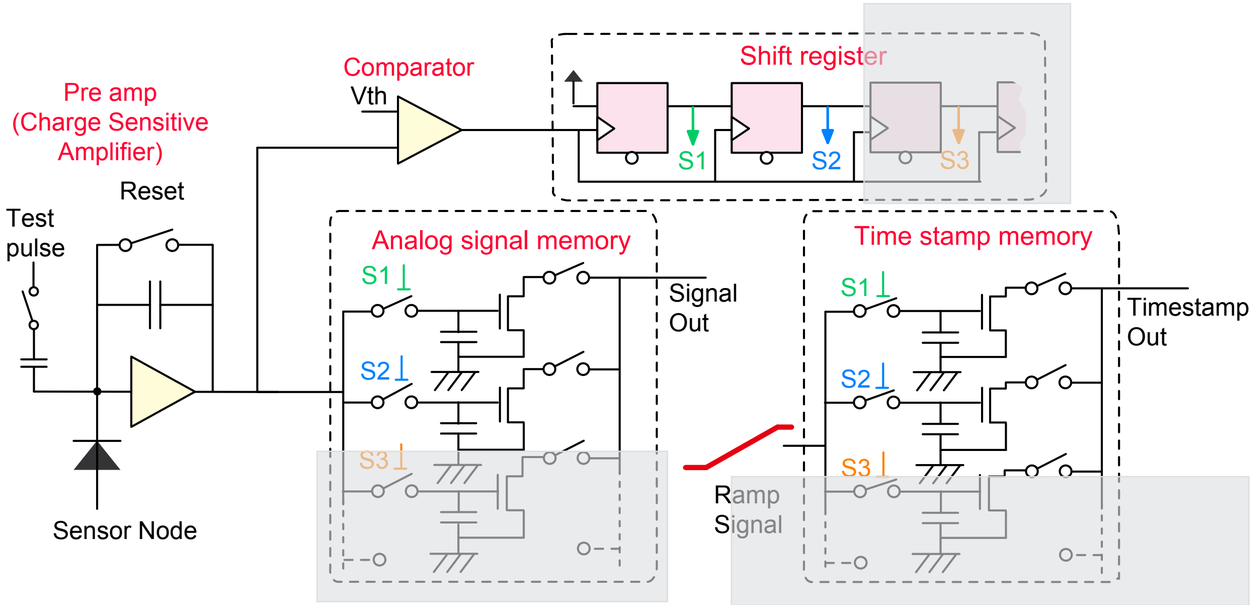
Timestamp correlation between SOFIST ver.2 #1 and #2



Timestamp difference between SOFIST ver.2 #1 and #2



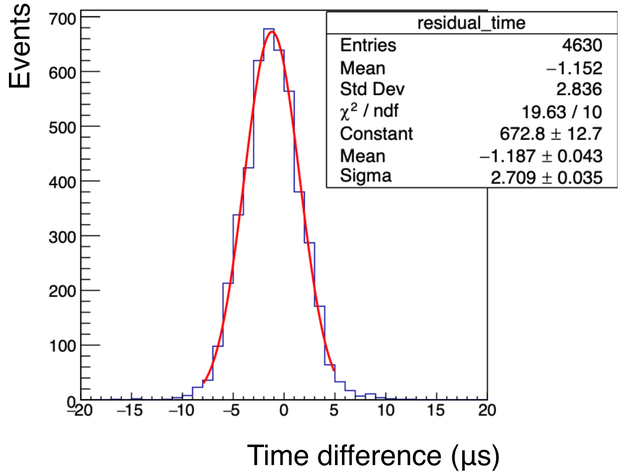
Intrinsic resolution: 2.19/√2 ~ 1.55 *μs*



SOFIST3

Timestamp residual

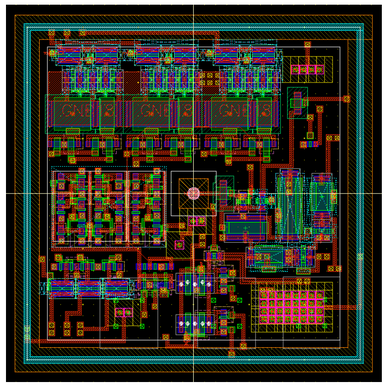
Timestamp difference between #1 and #4.



Intrinsic resolution: 2.71/√2 ~ 1.92 *μs*

Sensor Thickness: 300 μm

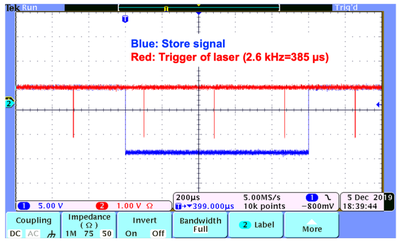
Pixel size: 30 × 30 μm²

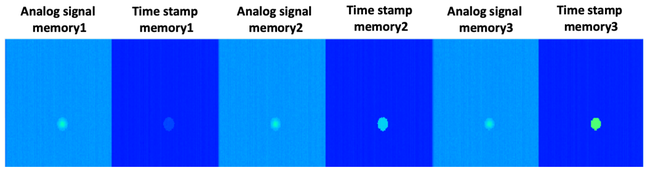


Multi-memory readout test

SOFIST3 has three hit, analog signal and timestamp memories.

Multi-memory readout scheme was tested by injecting a IR laser three times in a 1 ms period.



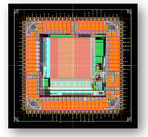


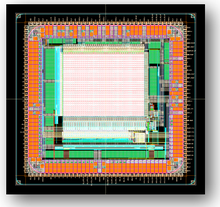
Analog signal

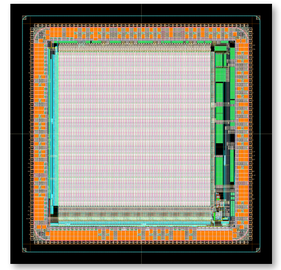
Represent stable laser pulses (~180 ADC).

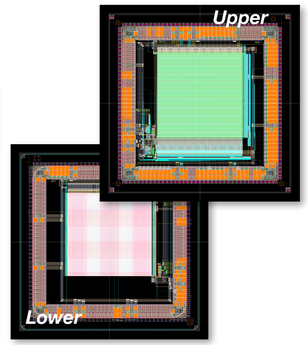
Timestamp

Show different timing of the laser injection (110, 490, 880 ADC).







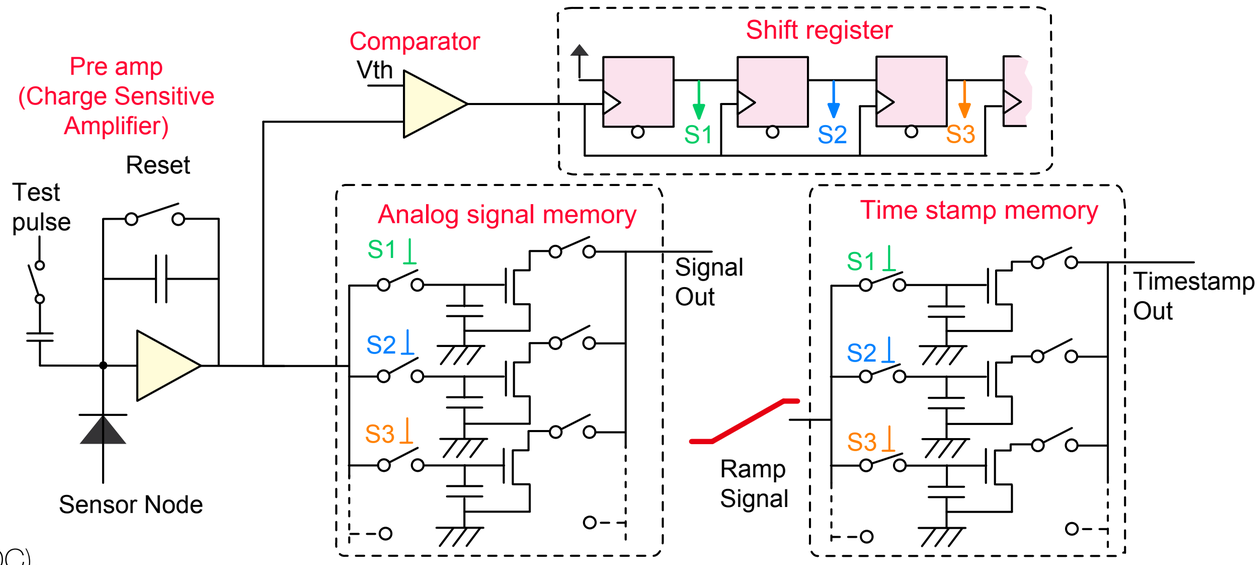


SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

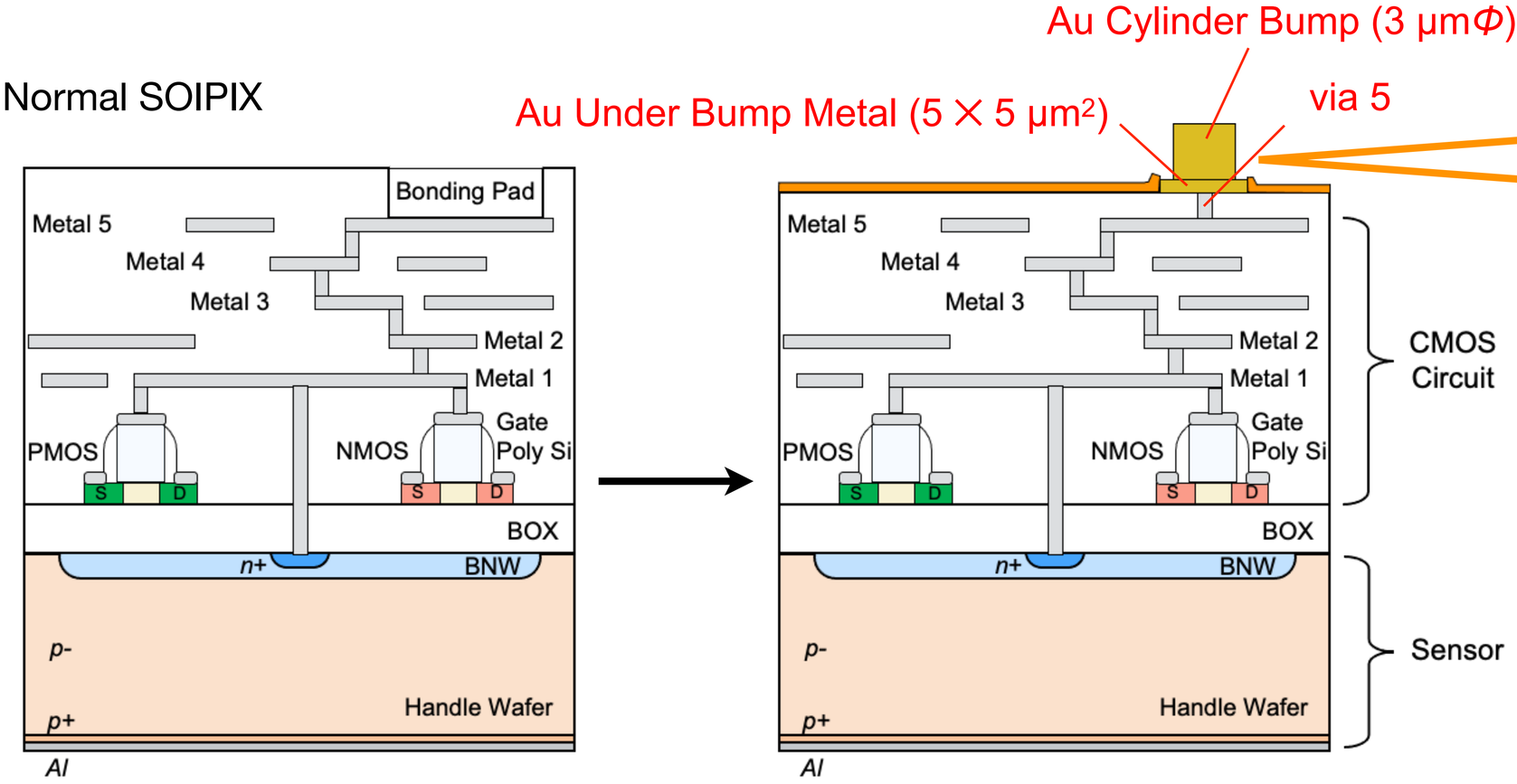
SOFIST3
Full function
(30×30 μm² pixel)

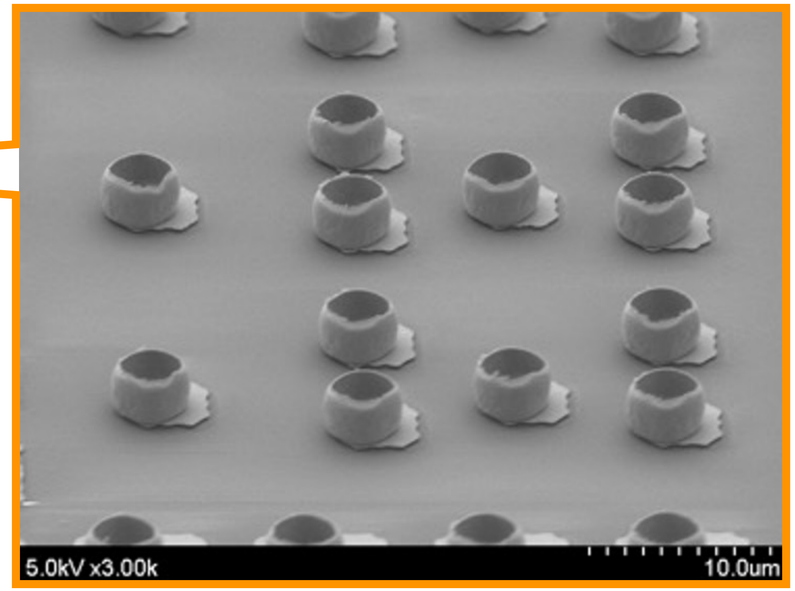
SOFIST4
Full function
(20×20 μm² pixel)



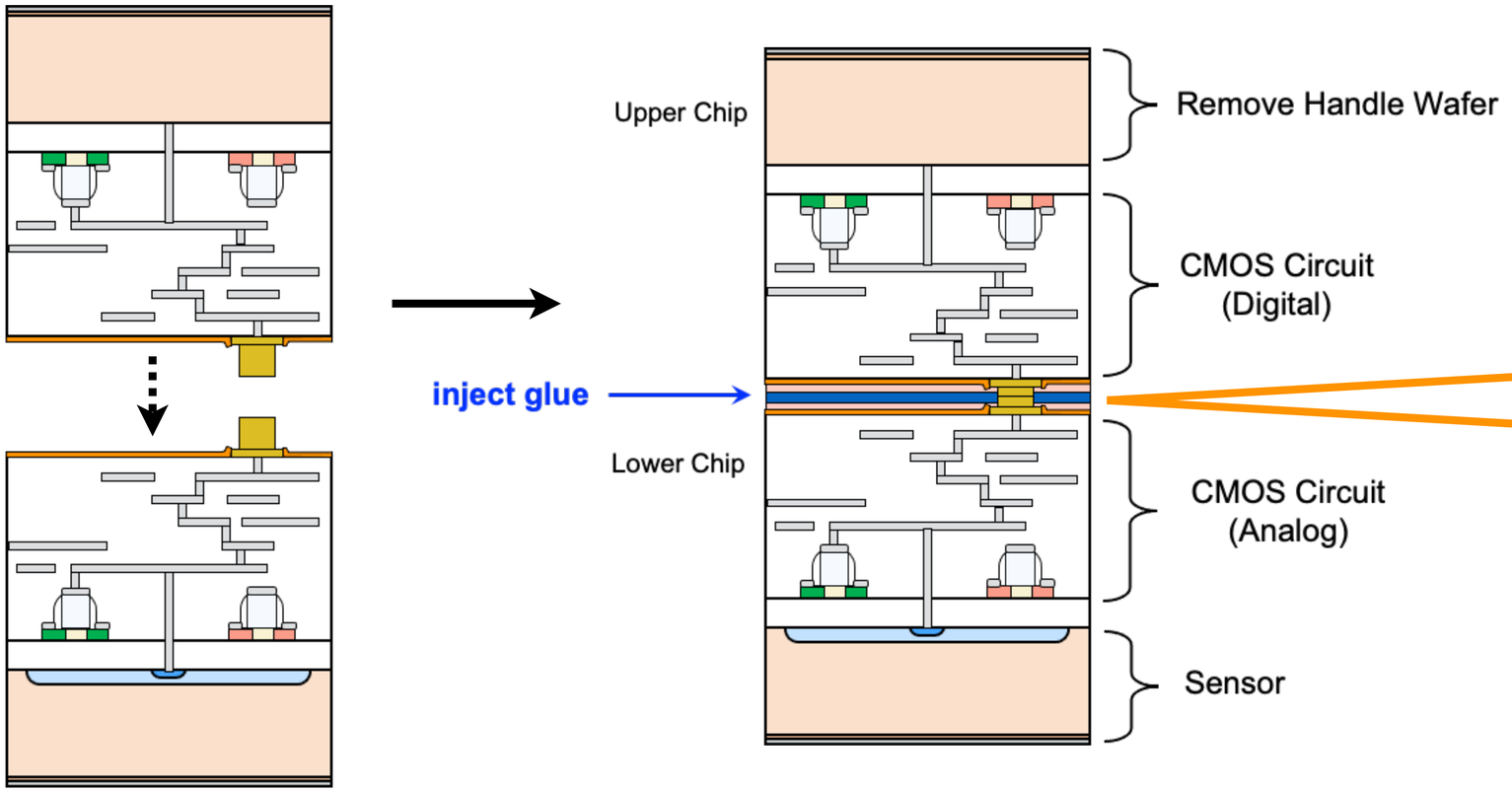
SOIPIX 3D Stacking Technology

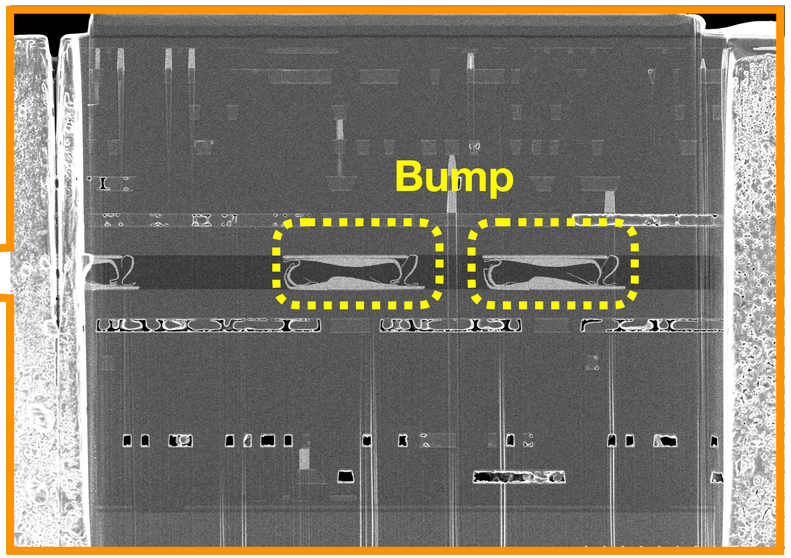
Normal SOIPIX



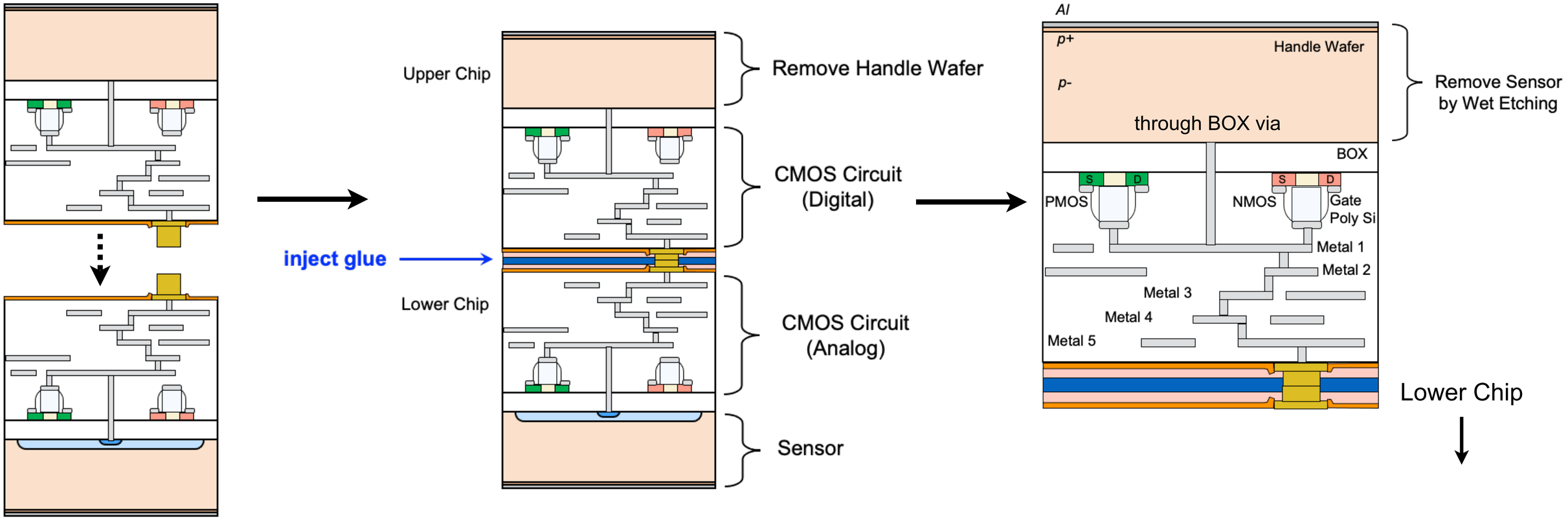


SOIPIX 3D Stacking Technology

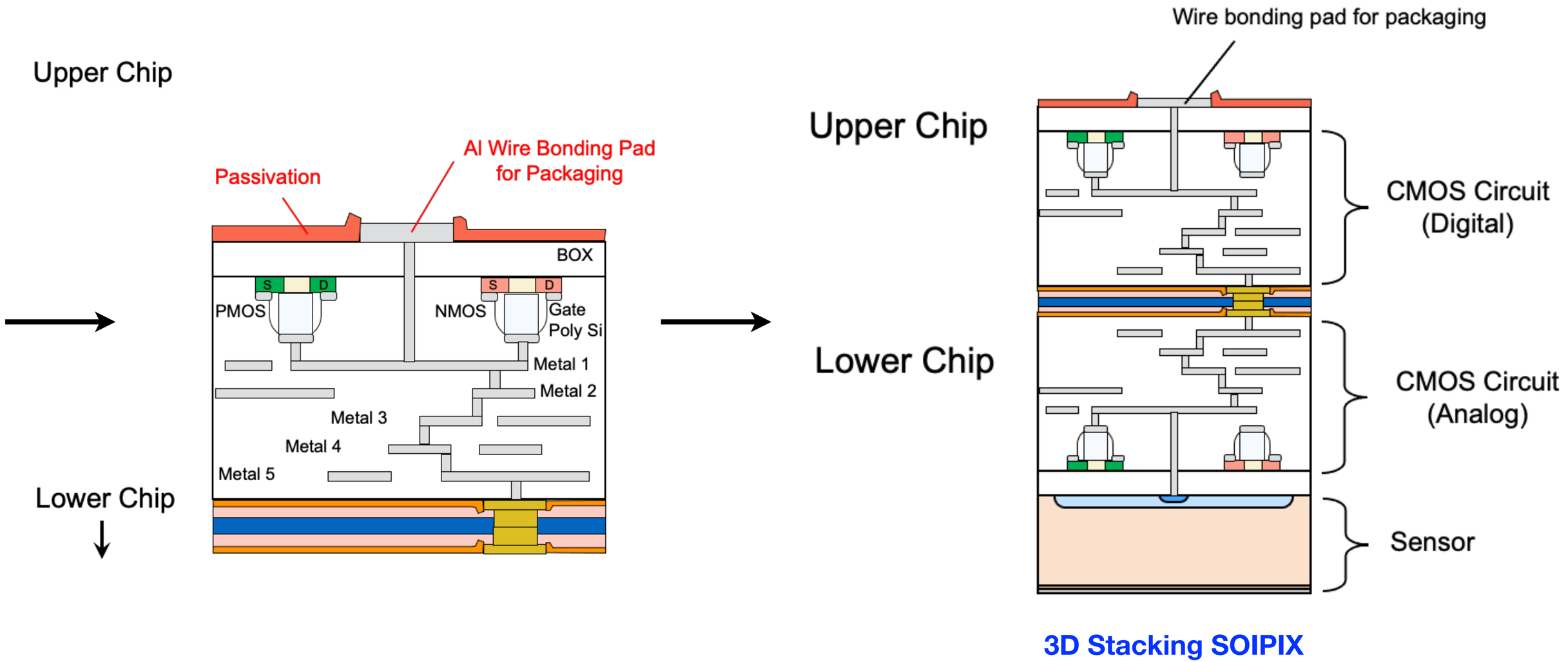




SOIPIX 3D Stacking Technology



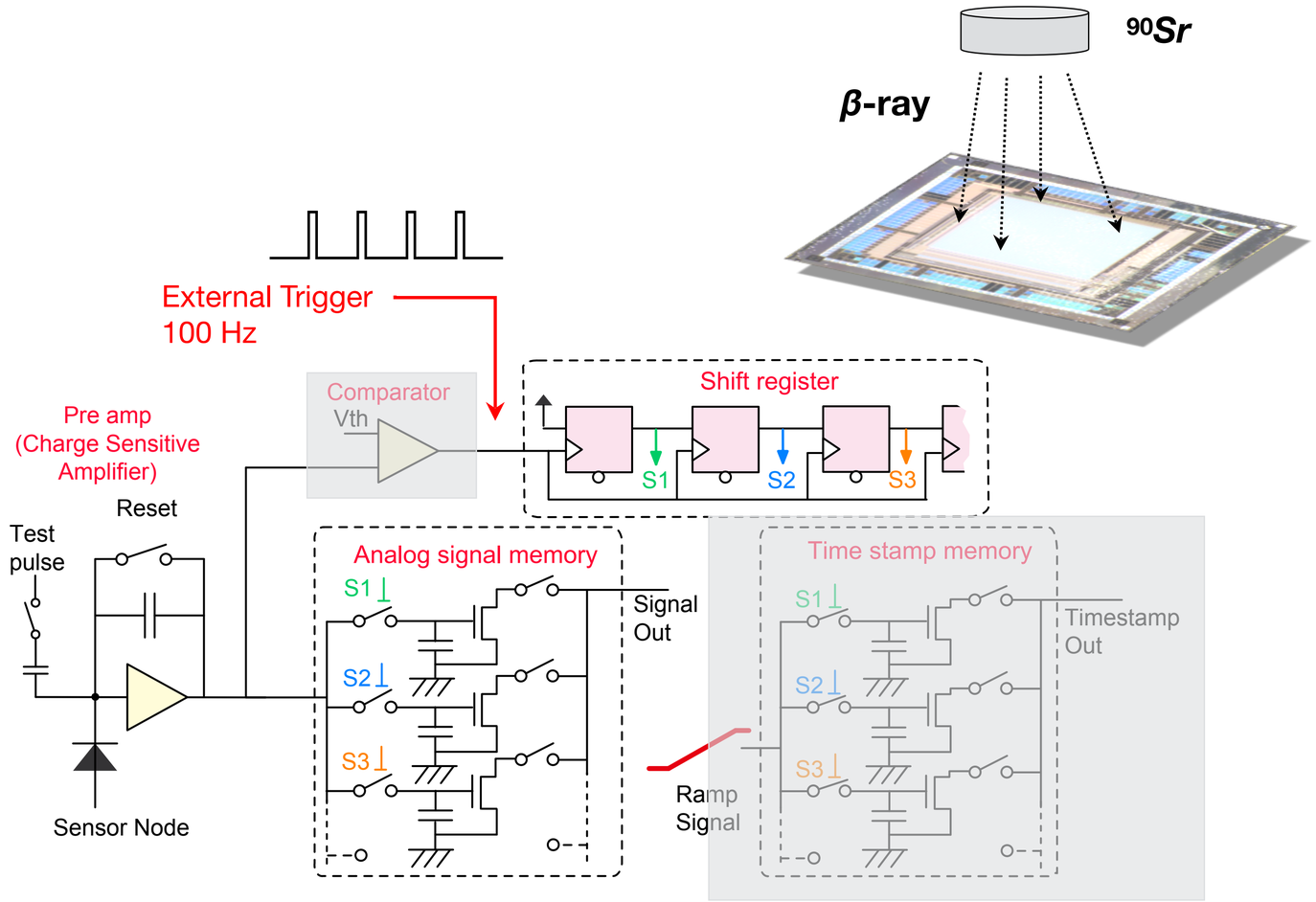
SOIPIX 3D Stacking Technology

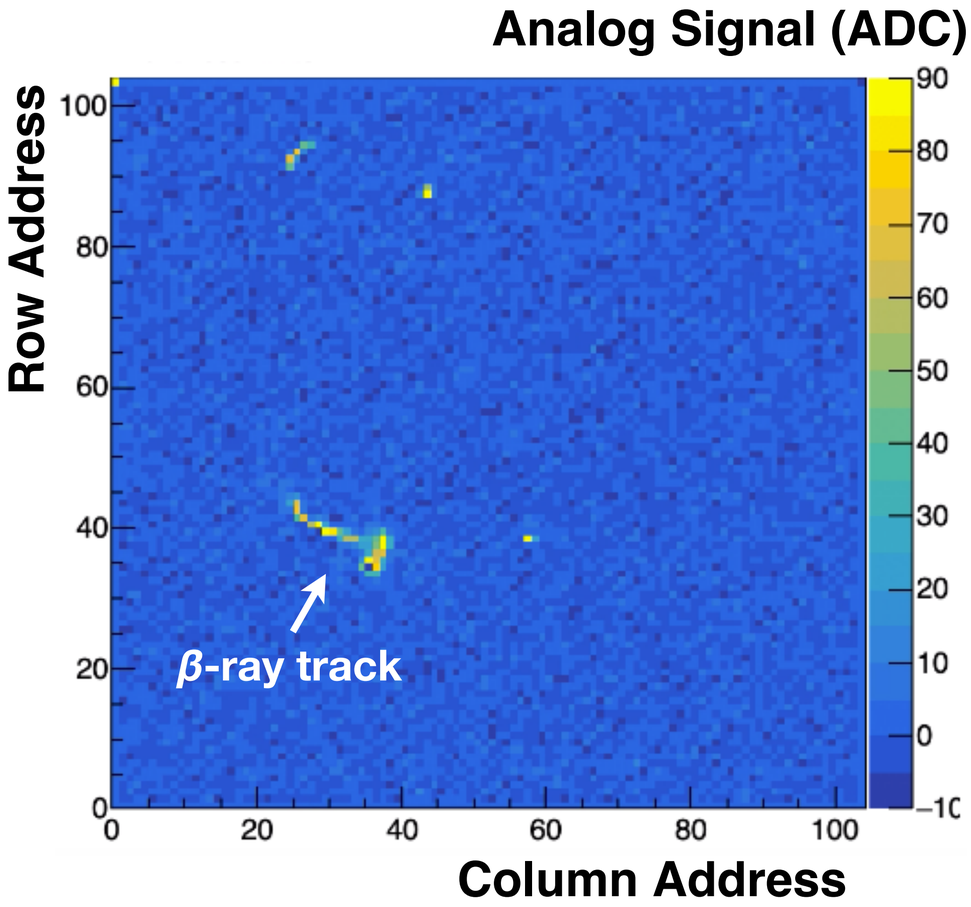


3D Stacking SOIPIX

SOFIST4, β-ray track

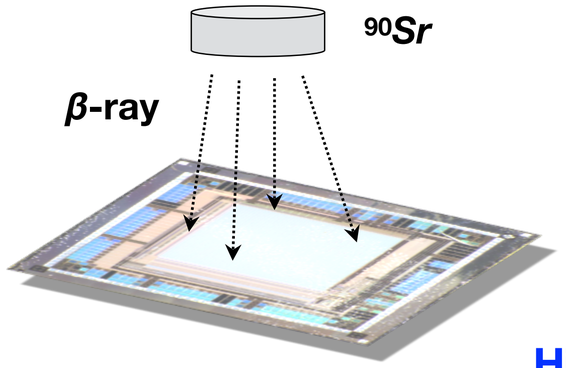
*The sensors we have evaluated were single-SOI FZ-n type sensor due to the process issue of the 3D stacking.
→Comparator, Shift-register and Timestamp functions does not work at this time.

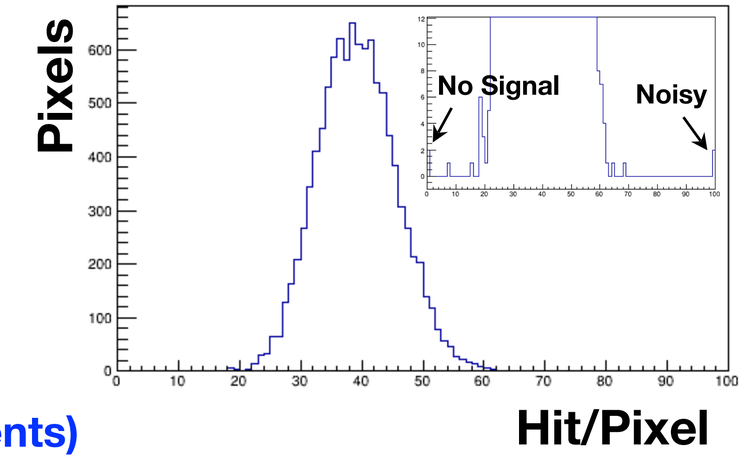


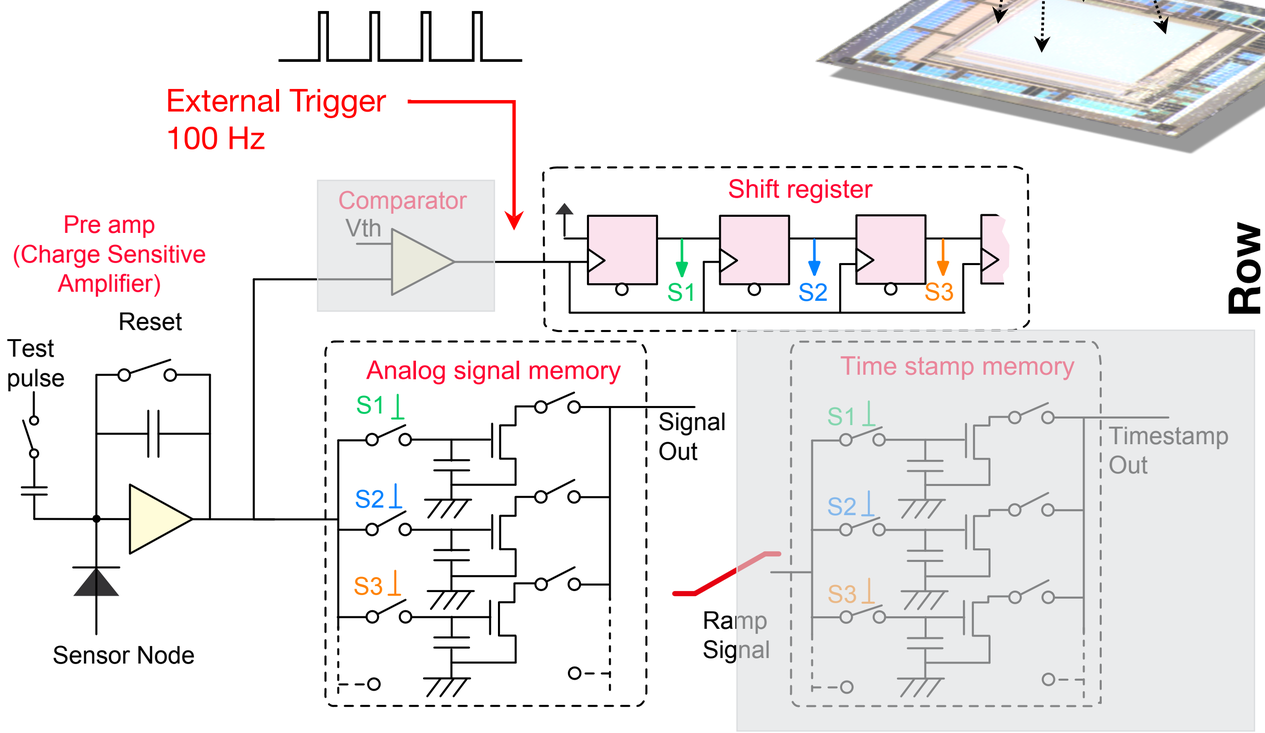


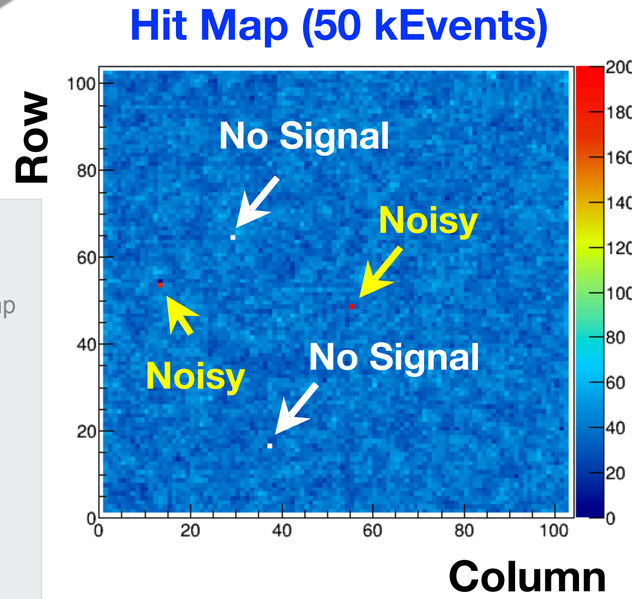
SOFIST4, Bump Connection Yield

*The sensors we have evaluated were single-SOI FZ-n type sensor due to the process issue of the 3D integration.
→Comparator, Shift-register and Timestamp functions does not work at this time.







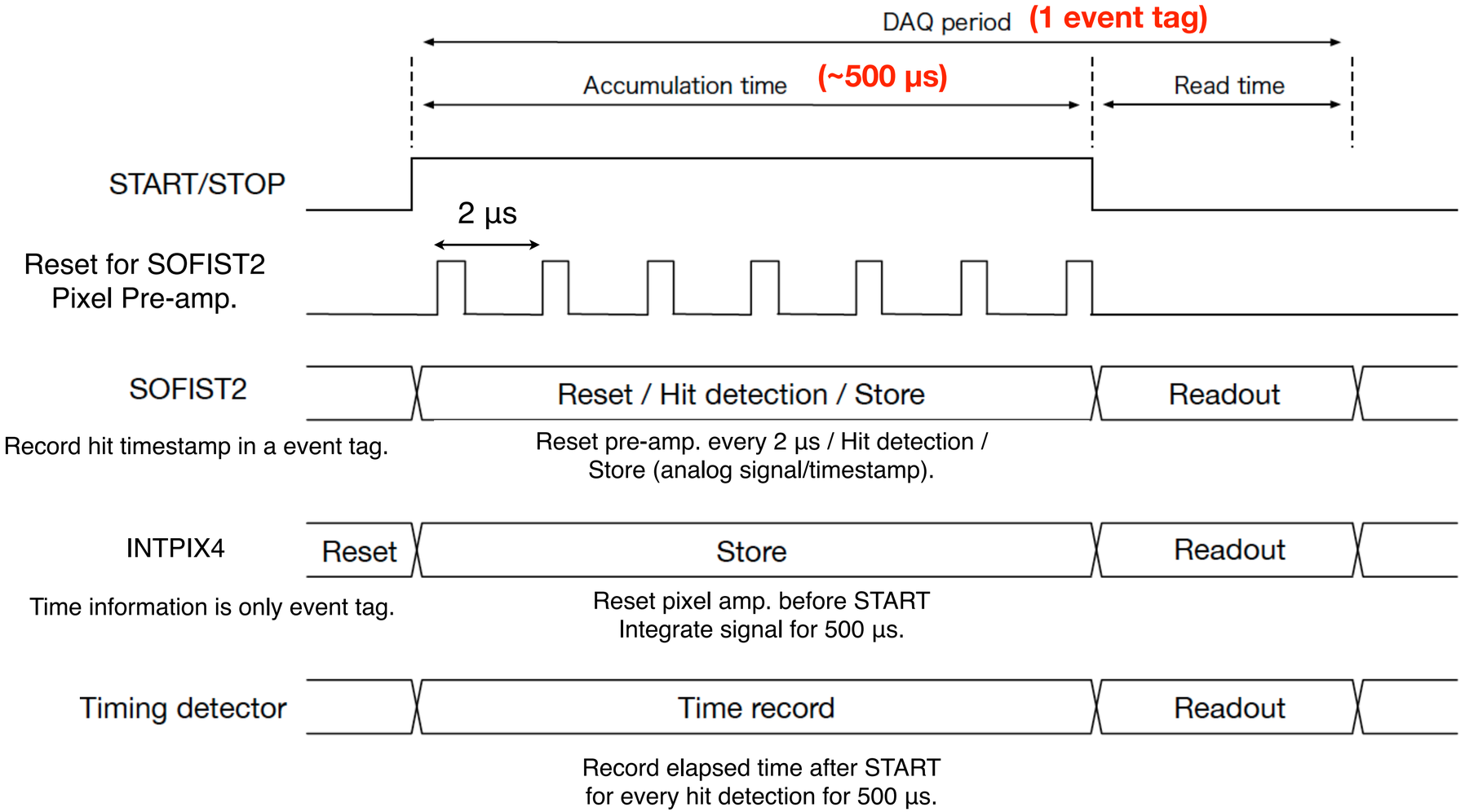


Connection Yield:
(102 × 102 – 2) / 102 × 102
~ 99.98 %

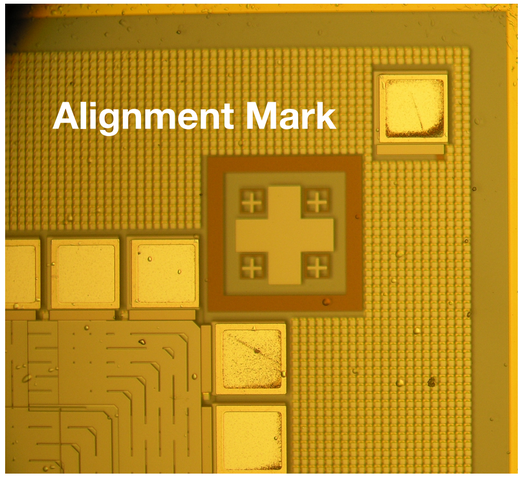
Reject the outermost pixels for the calculation.

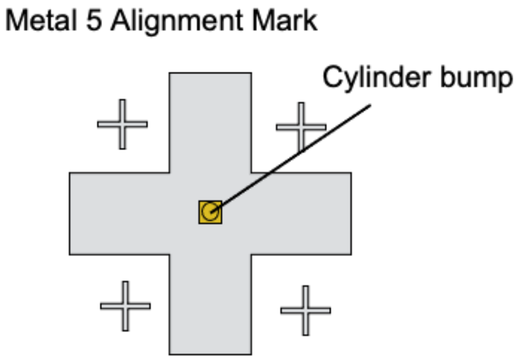
DAQ

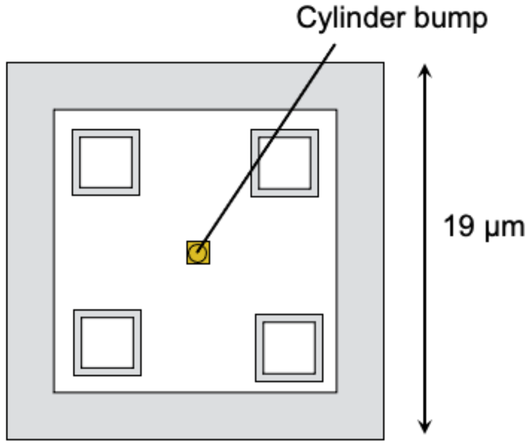
Operation of each detector in 1 event tag (DAQ period)

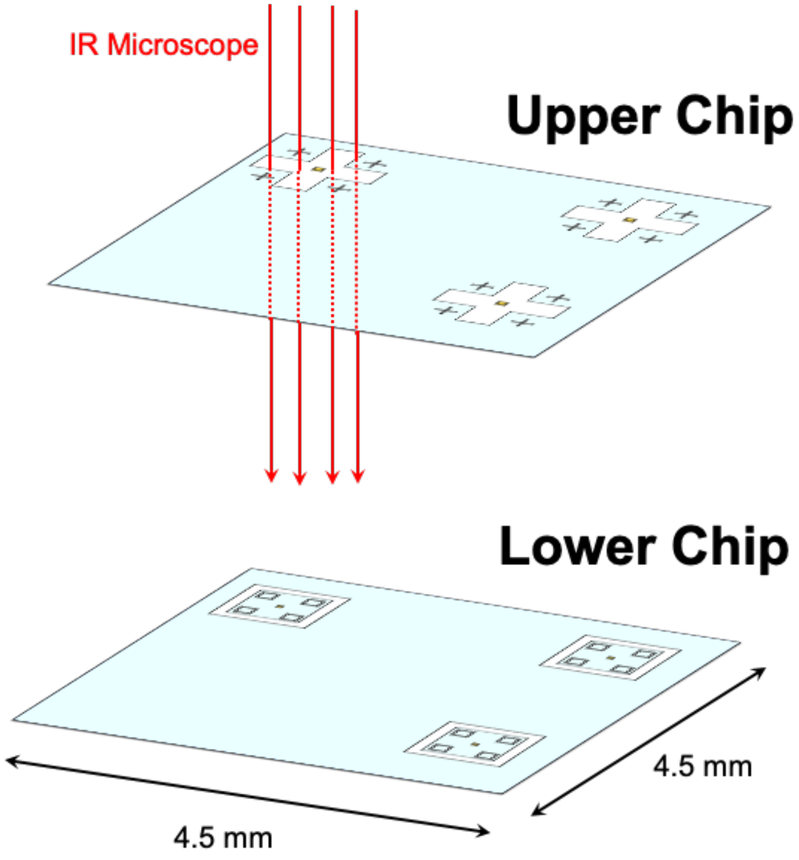


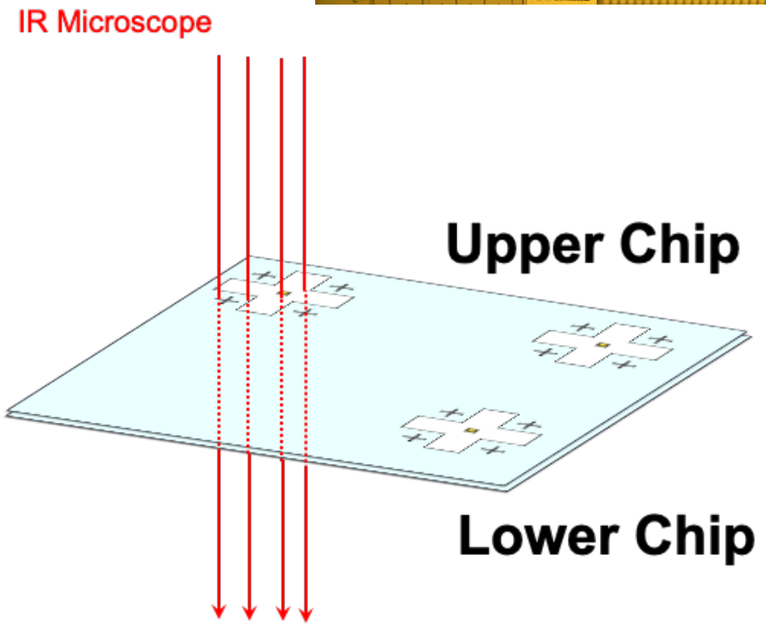
Alignment by Infrared Laser





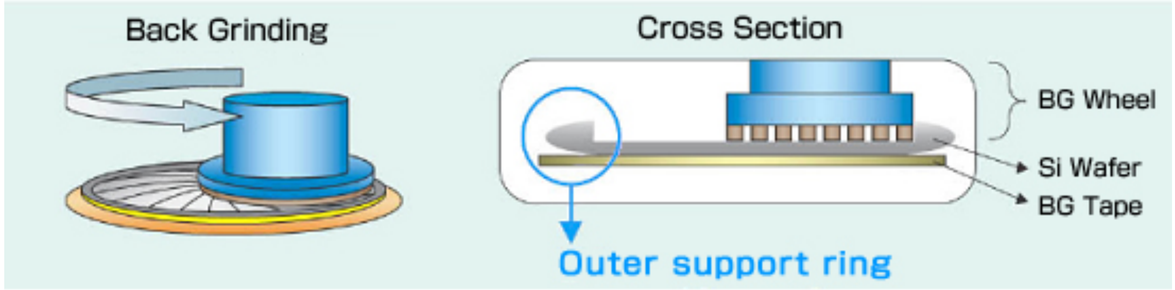






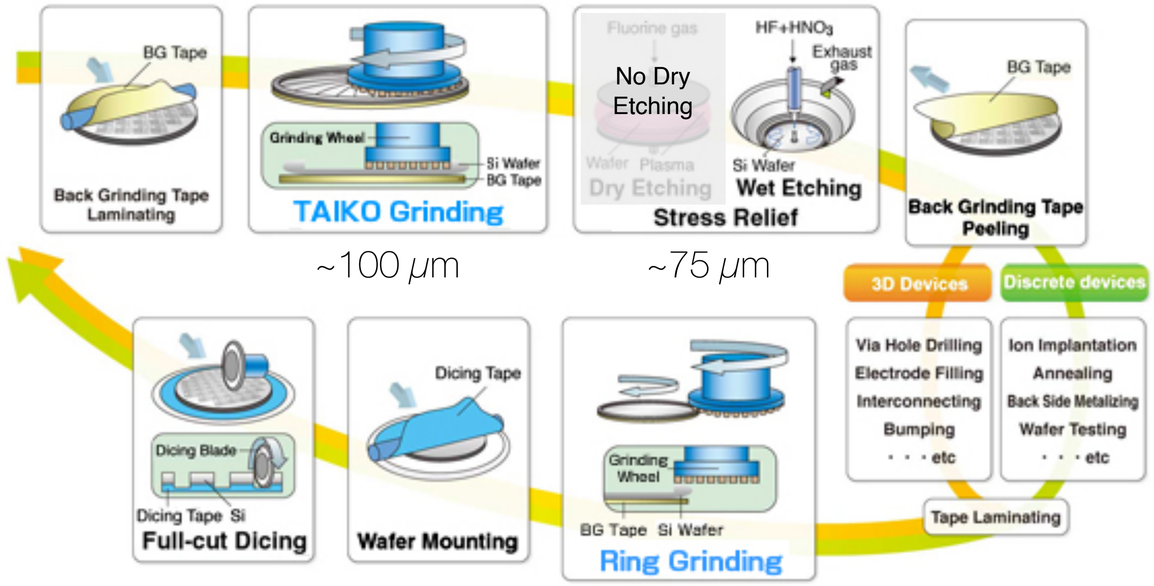
Sensor Thinning by DISCO TAIKO Process

TAIKO Process by DISCO Corporation (Japan) https://www.disco.co.jp/eg/index.html



DISCO
Kiru·Kezuru·Migaku Technologies

Stress relief with wet etching by
Mimasu Semiconductor Industry Co., Ltd. (Japan)

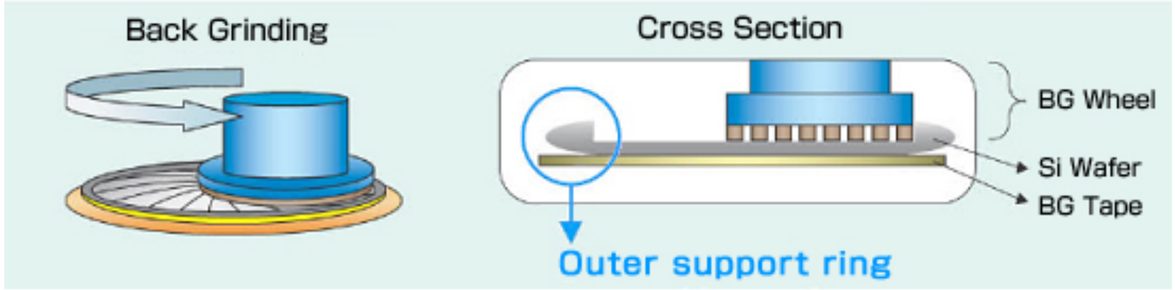


TAIKO Process
with outer support ring
- Lower wafer warpage
- Improve of wafer strength
- Easy wafer handling
- Easy backside processing (ion implantation, annealing, Metalizing etc) after thinning

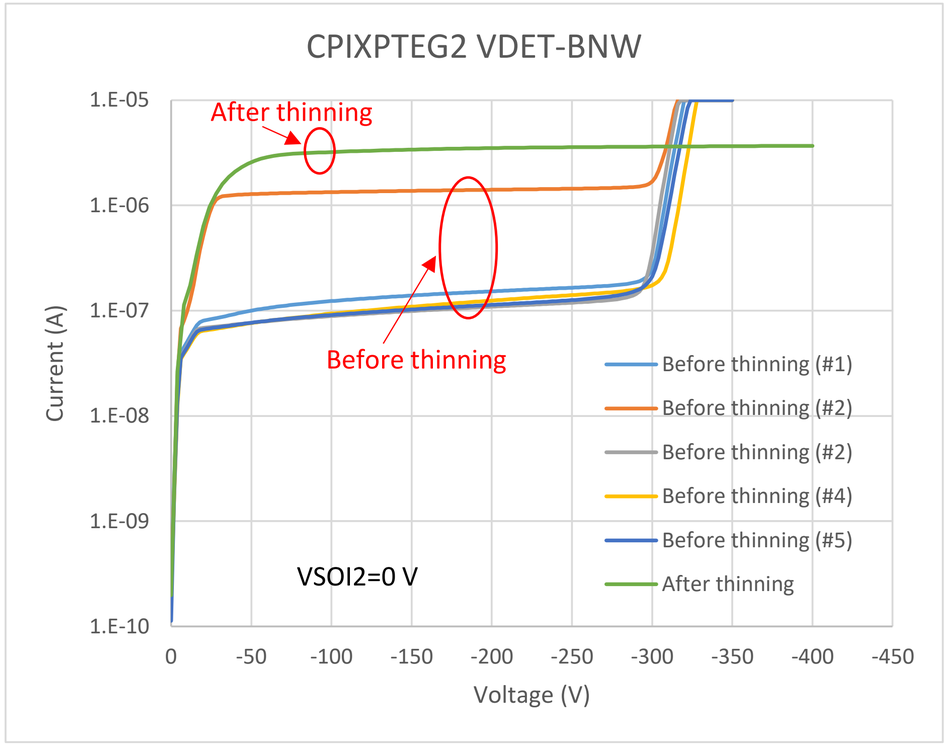
Back side process after thinning
- Boron implantation (ULVAC, Japan)
- Laser Annealing (SHI, Japan)

Sensor Thinning by DISCO TAIKO Process

TAIKO Process by DISCO Corporation (Japan) https://www.disco.co.jp/eg/index.html



DISCO
Kiru·Kezuru·Migaku Technologies

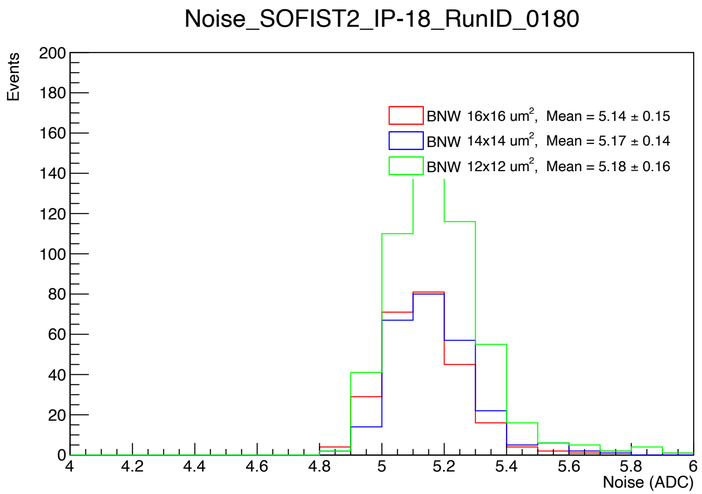


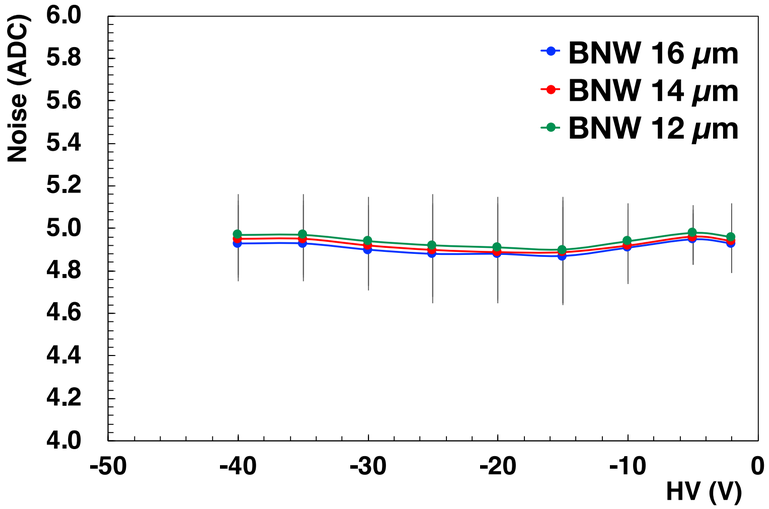
Sensor I-V after thinning (other SOIPIX)

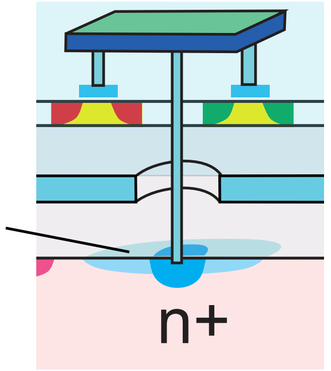
Leak current increased by ~1.5 orders of magnitude.
No break down by 400 V after thinning.

Still investigating these behavior.

S/N







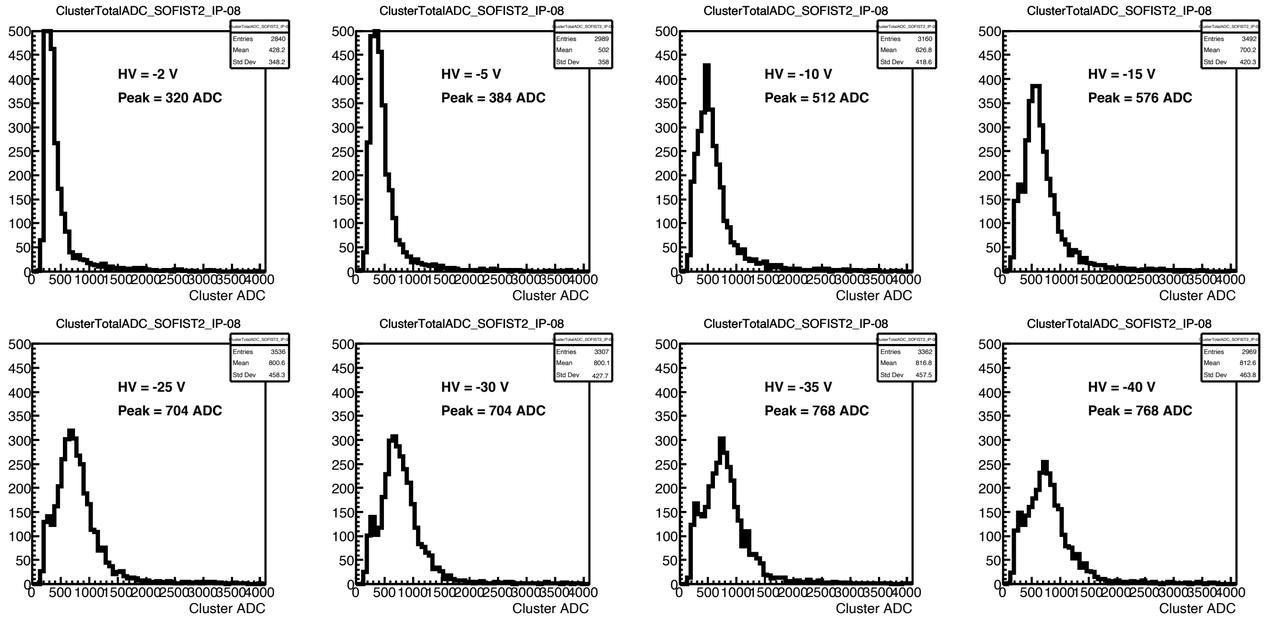
SOFIST setup

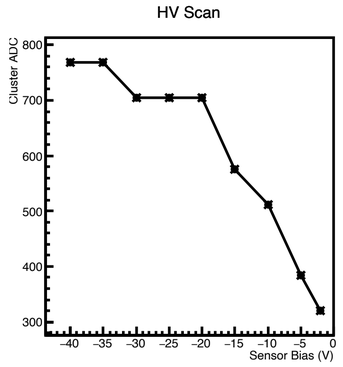
Readout: 12 bit external ADC (on DAQ board)
Sensor bias voltage = -20 V (~1 kΩ·cm)
Sensor thickness 65 μm (Thinned sensor)

Clustering

1) find seed pixel which is ≥ 10 σ
2) add pixels which are ≥ 5 σ to cluster.
3) check 2) for 3 × 3 pixels centered on the seed pixel.

High Voltage Scan





Full depletion voltage is around -30 V.
Cluster charge is ~ 700 ADC for MIP signal.
→ S/N = 700/5 ~140 for the sensor 65 μm thickness.