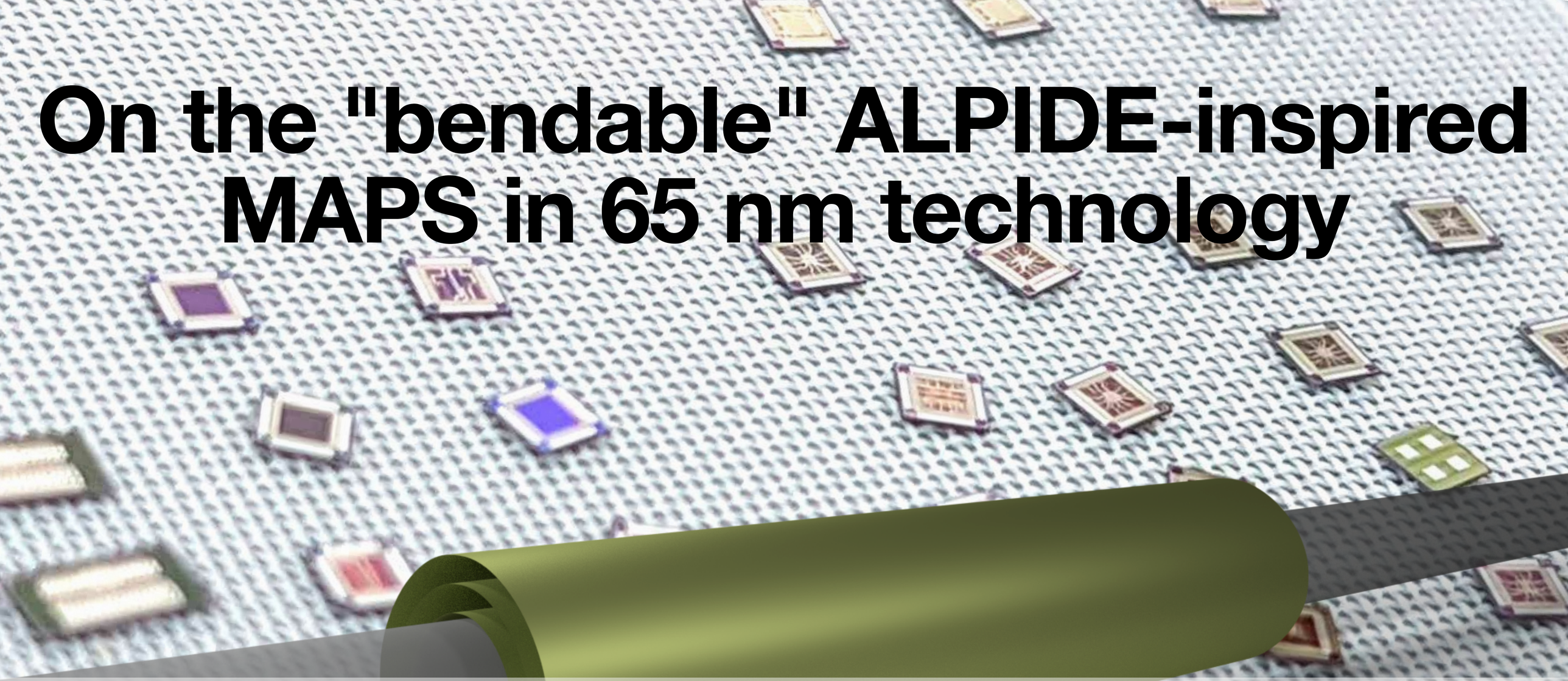
On the "bendable" ALPIDE-inspired MAPS in 65 nm technology



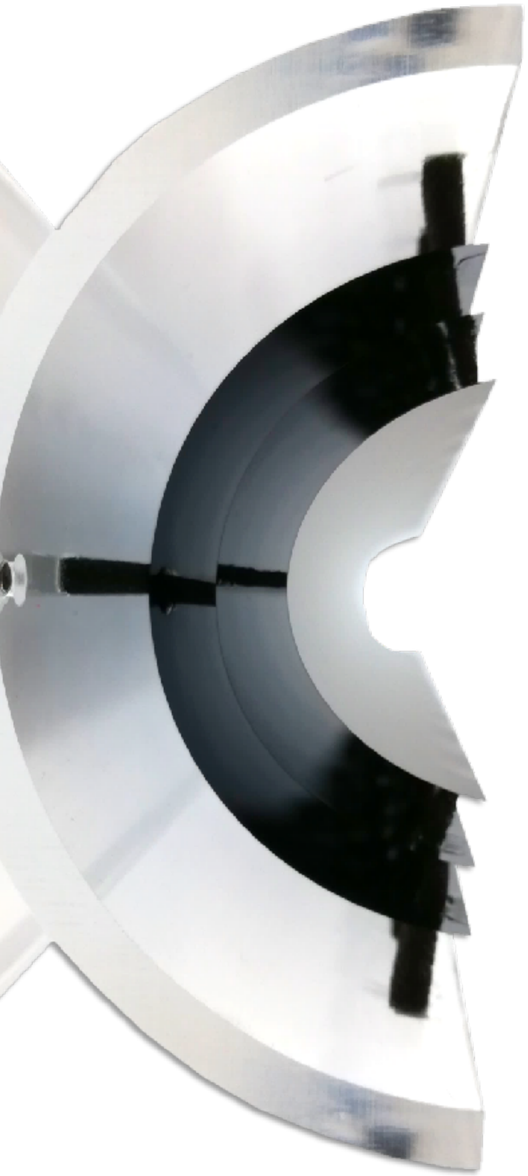
Magnus Mager (CERN)
on behalf of the ALICE collaboration

The 2021 international workshop on the high energy Circular Electron-Positron Collider (CEPC 2021)
8 Nov 2021

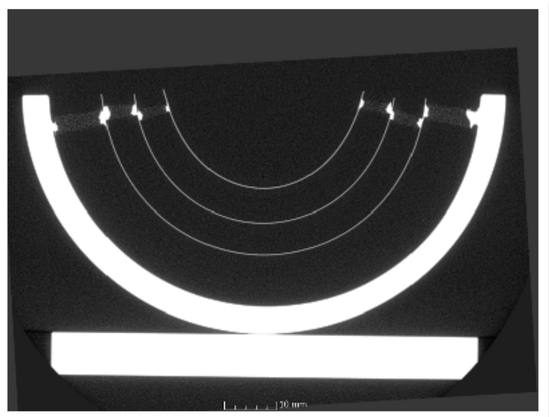
CERN

ALICE

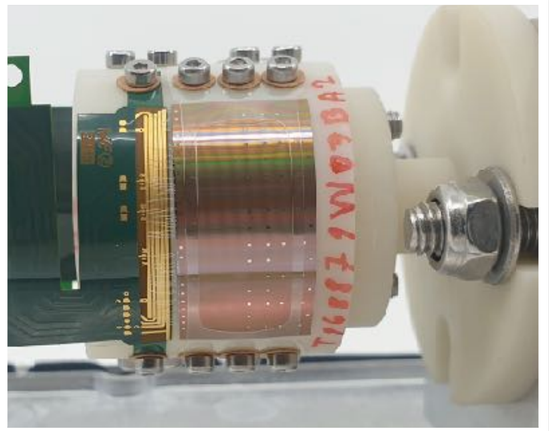
Overview



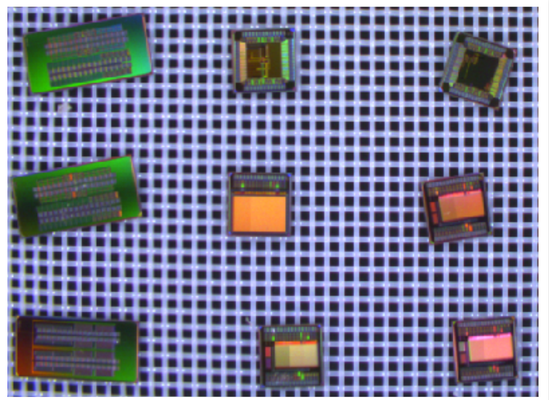
- **Background**
  - material budget breakdown of detectors (ALICE ITS2)
  - thin monolithic sensors
  - proposal for ALICE **ITS3**
- **R&D highlights**
  - bending silicon
  - first prototypes in 65 nm technology
- **Outlook**
  - towards the wafer-scale sensor



[X-ray tomography]



[µITS3 prototype assembly]



[MLR1 chips, 65 nm]

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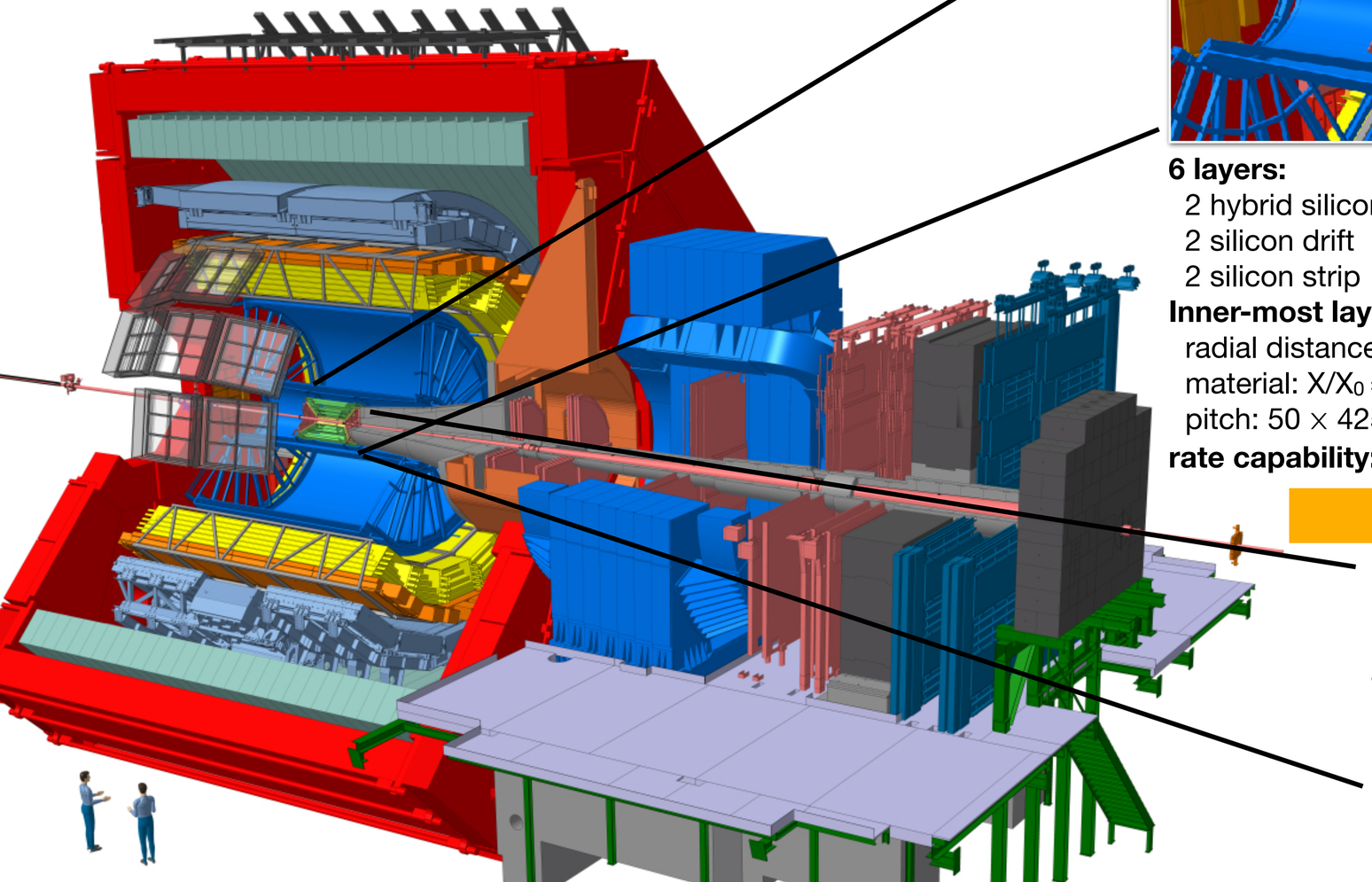
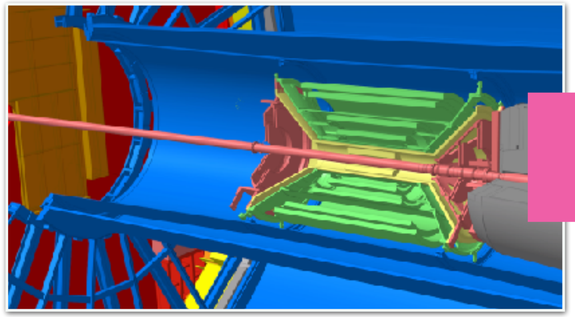
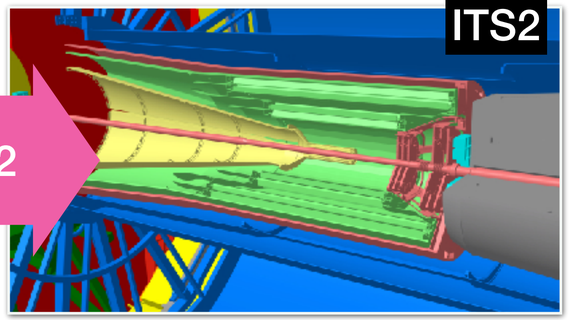
LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)



Inner Tracking System





LS2

6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

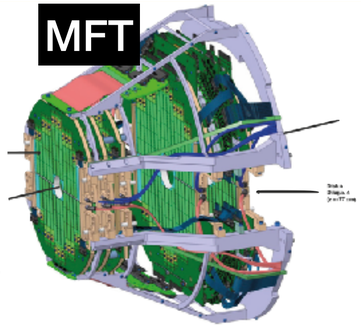
rate capability: 1 kHz

7 layers:
- all MAPS
- 10 m^2, 24k chips, 12.5 Giga-Pixels

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.35\%$
- pitch: $29 \times 27\ \mu m^2$

rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker



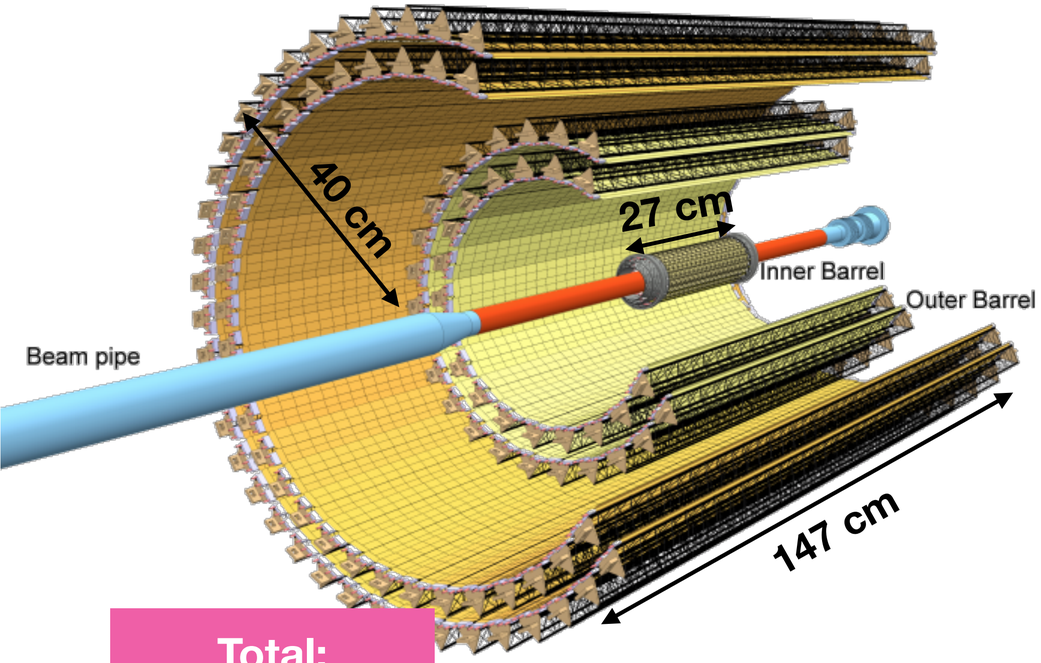
new detector

5 discs, double sided:
- based on same technology as ITS2

ALICE ITS2

state of the art large-scale low material budget detector

Layout



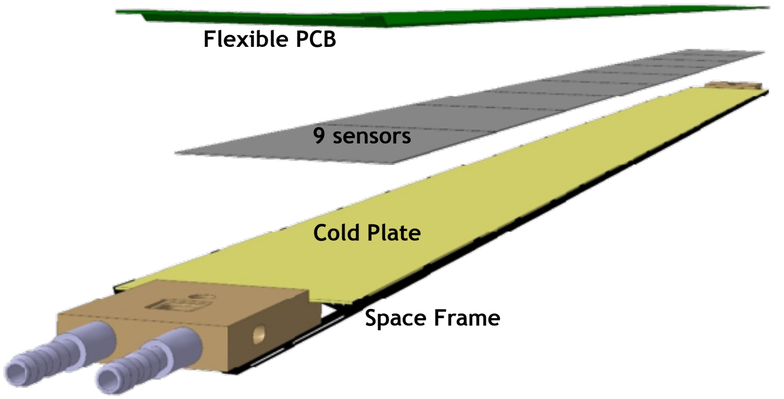
Total:
- 24k chips
- 10 m²
- 12.5 GPixel

Inner Barrel (IB)

3 Inner Layers: 12+16+20 Staves
1 Module / Stave

9 sensors per Module

96 Modules to be produced (including one spare barrel)

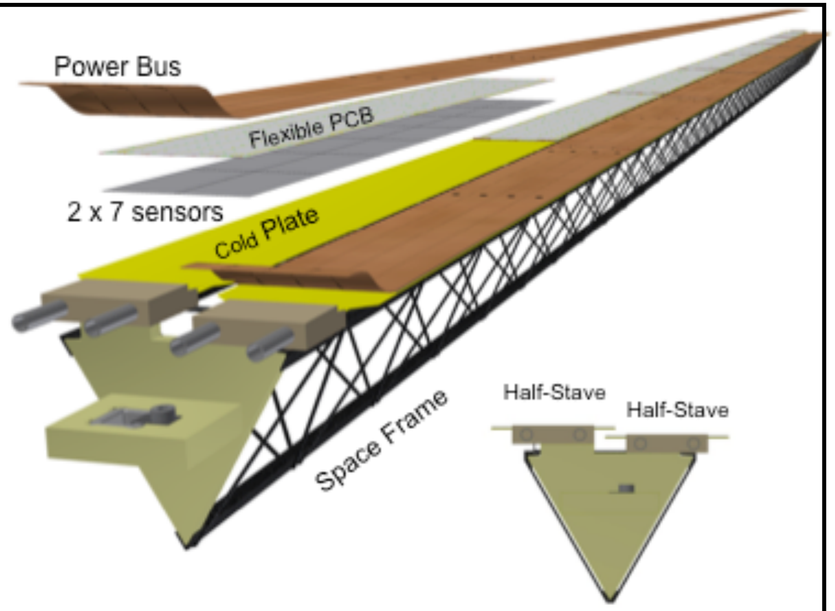


Outer Barrel (OB)

2 Middle Layers: 30+24 Staves
2×4 Modules / Stave
2 Outer Layers: 42+48 Staves
2×7 Modules / Stave

2×7 sensors / Module
(Middle and Outer Layers are equipped with the same Module Type)

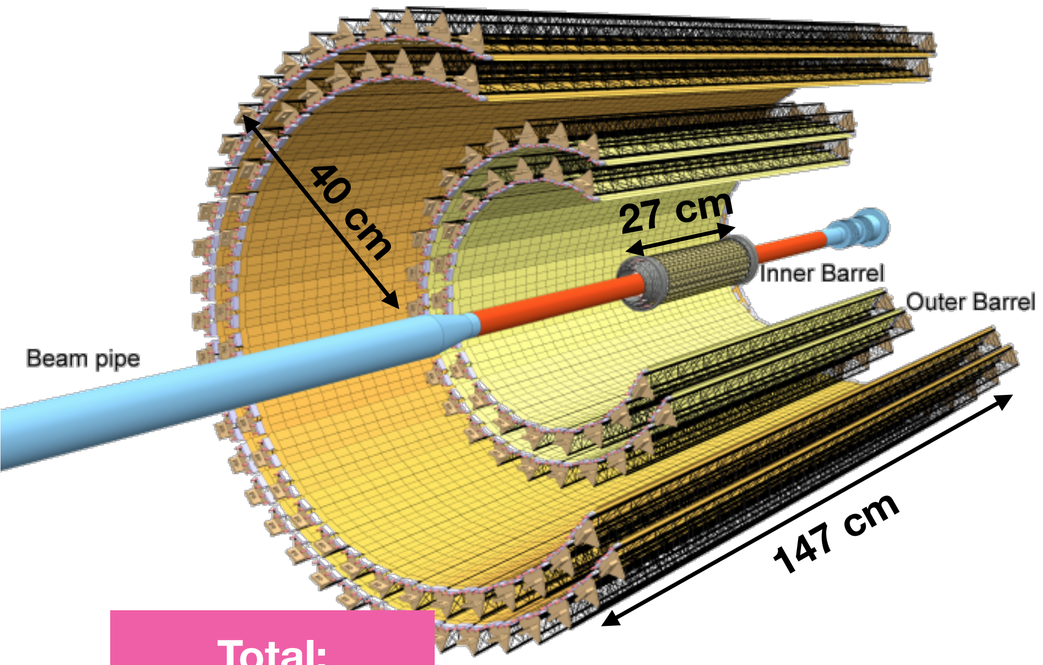
1880 Modules to be produced (including spares)



ALICE ITS2

state of the art large-scale low material budget detector

Layout



Total:
- 24k chips
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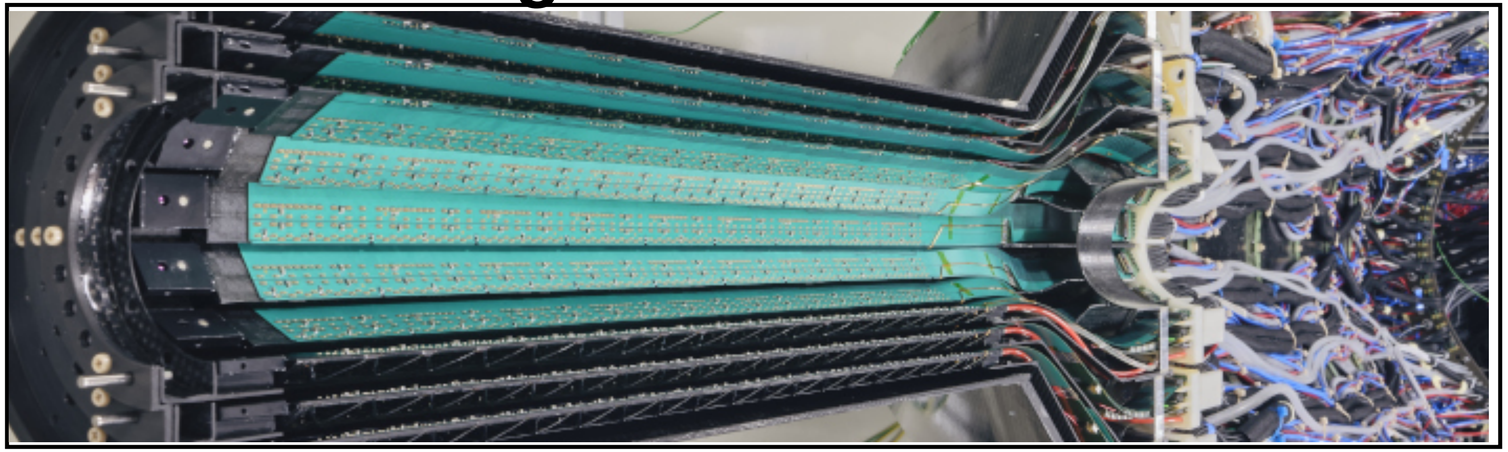
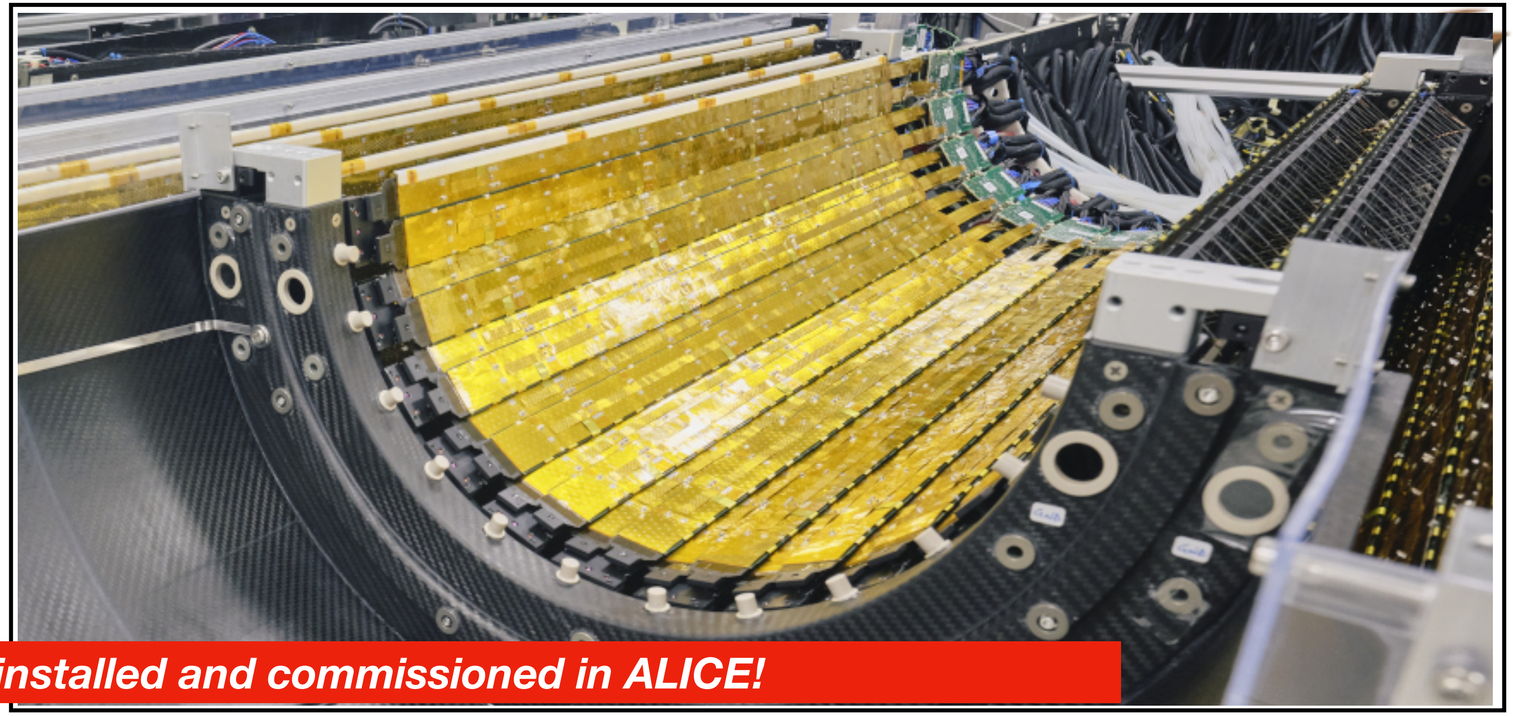
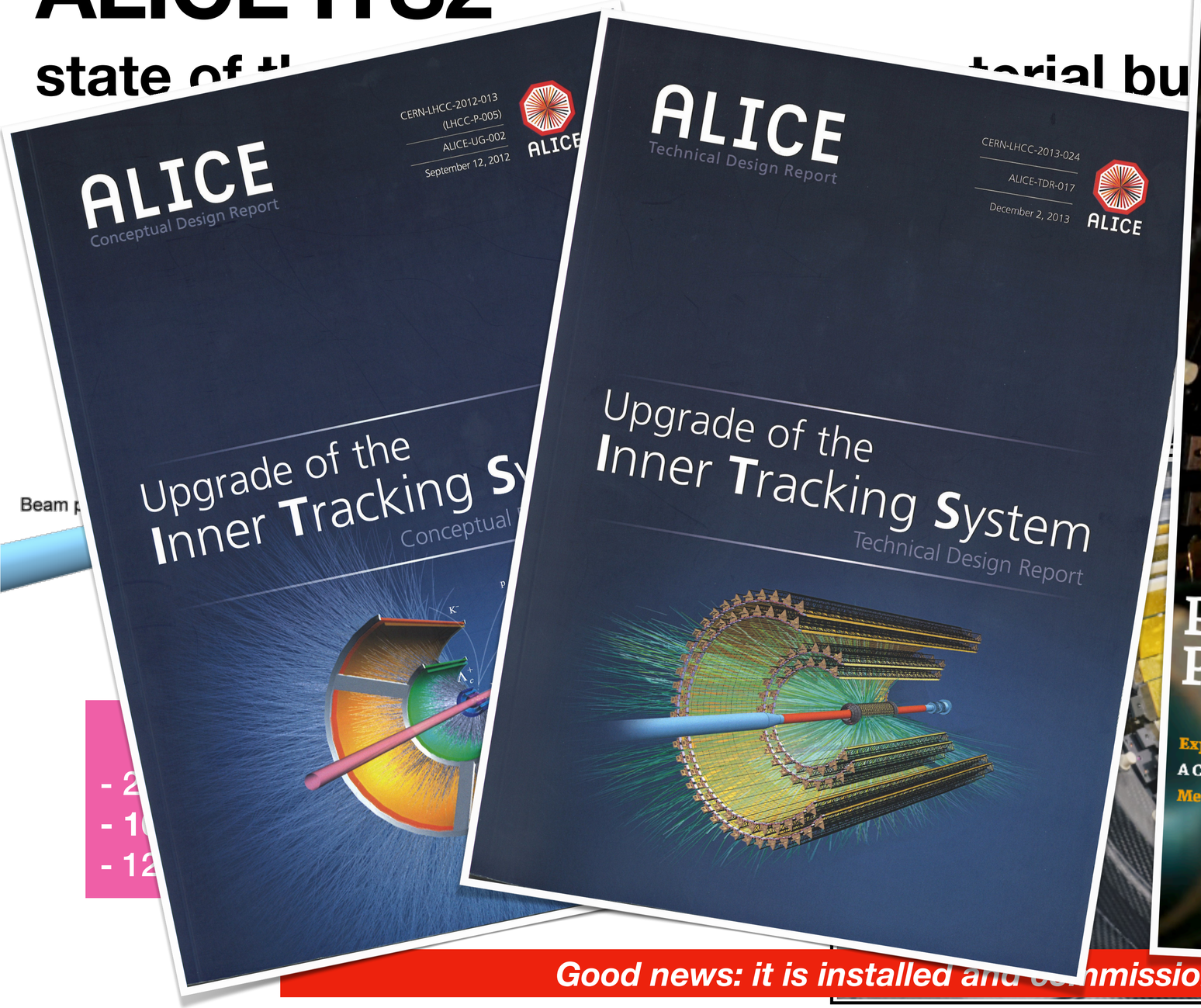




Good news: it is installed and commissioned in ALICE!

ALICE ITS2

state of t… …terial bu…



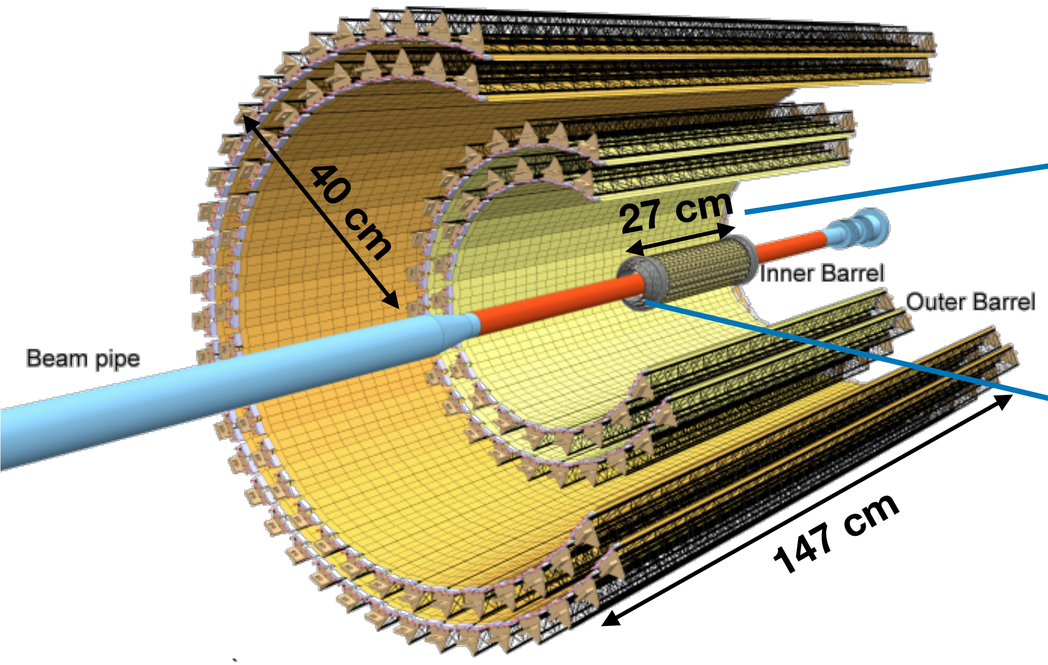
Beam p…

- 2…
- 1…
- 12…

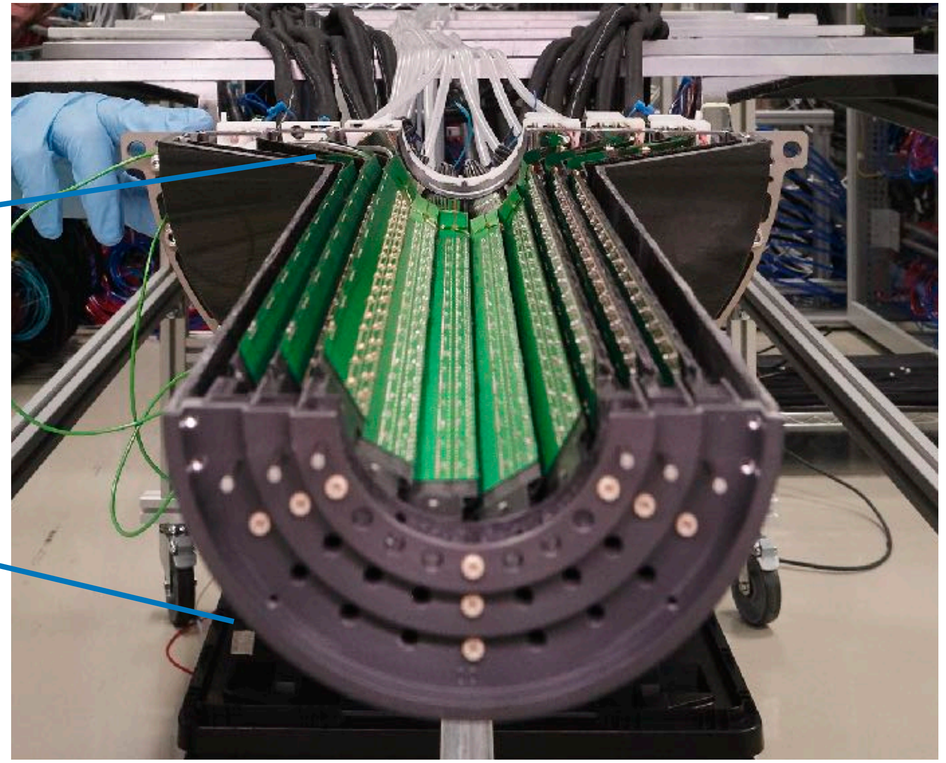
Good news: it is installed and commissioned in ALICE!

ITS2 inner barrel

Layout



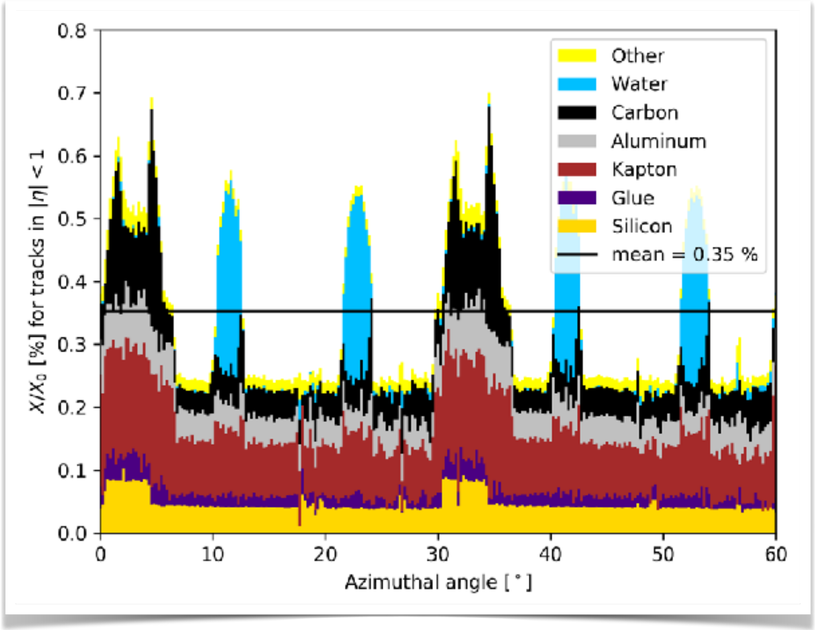
ITS2: assembled three inner-most half-layers

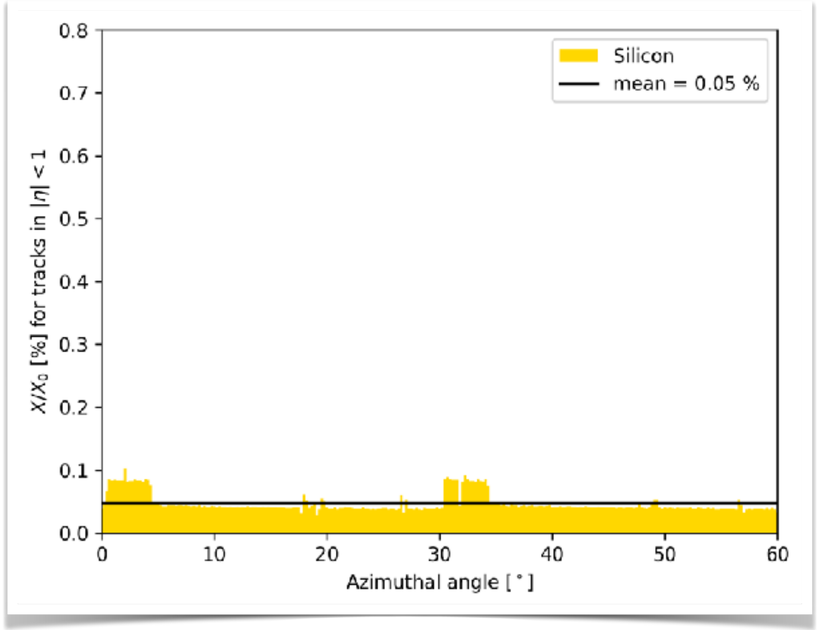


- ITS2 is expected to perform according to specifications or even better
- The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- **Key questions: Can we get closer to the IP? Can we reduce the material further?**

Material budget

a closer look

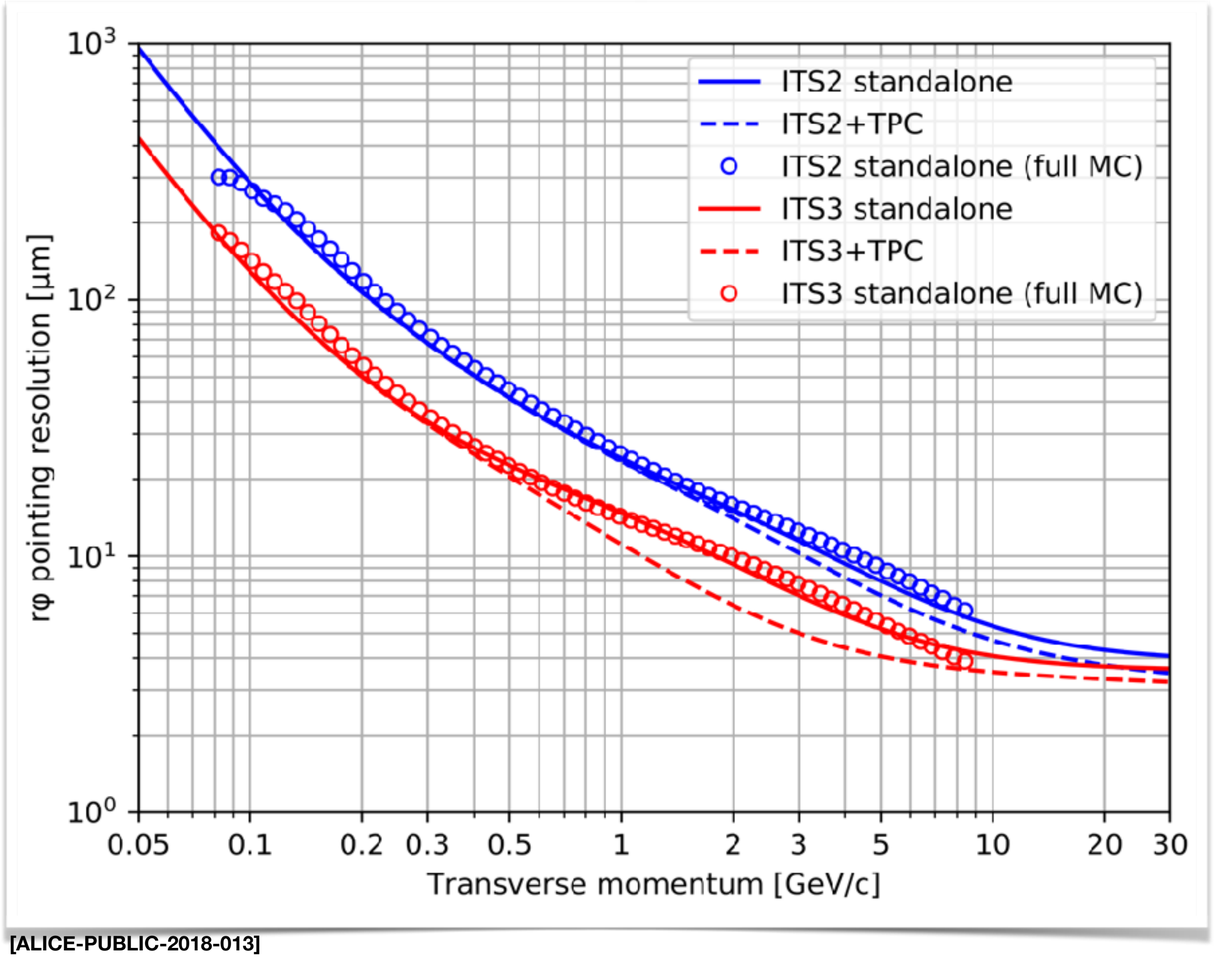




- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/cooling
- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm^2
- Removal of the circuit board (power+data)
  - **possible** if integrated on chip
- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

ITS3 performance figures

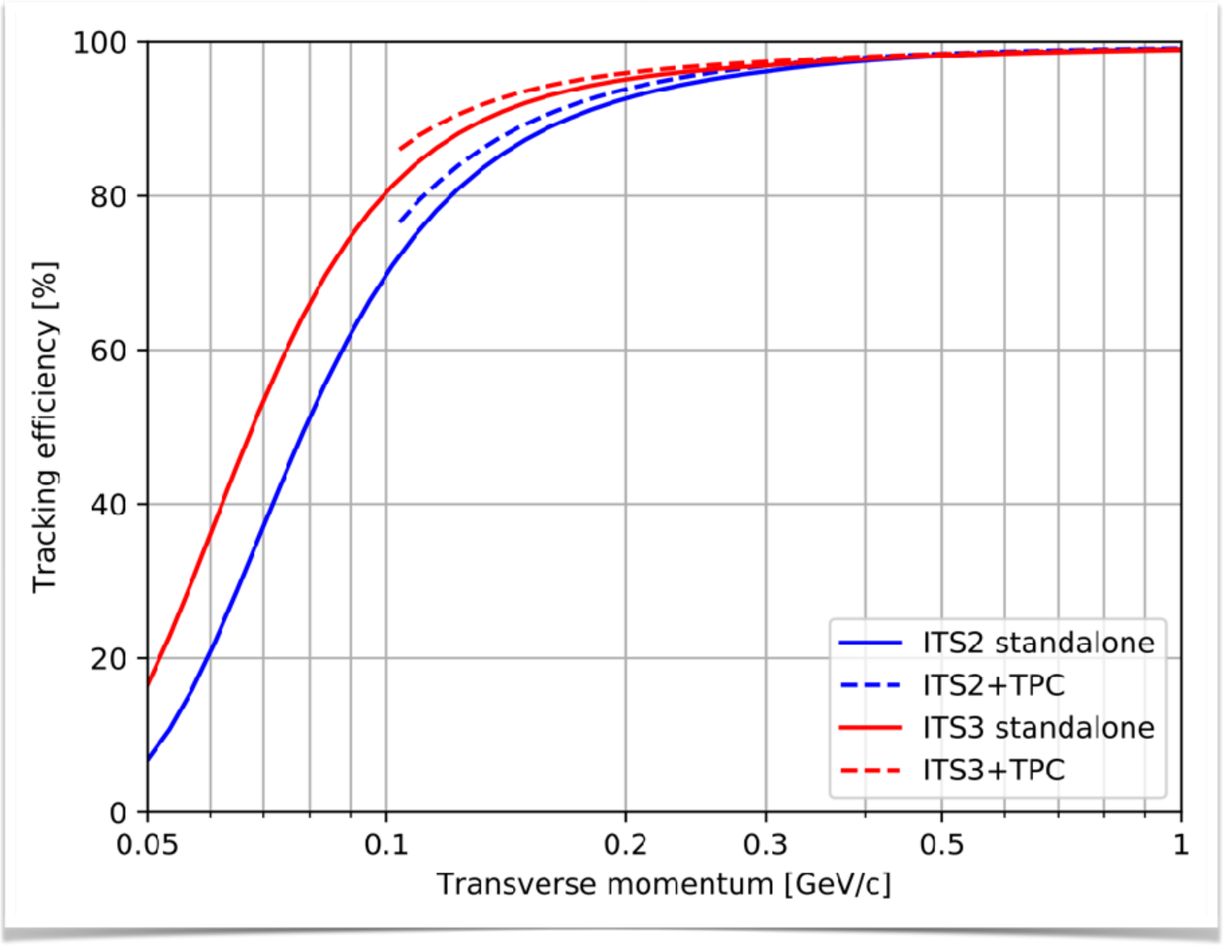
pointing resolution



[ALICE-PUBLIC-2018-013]

improvement of factor 2 over all momenta

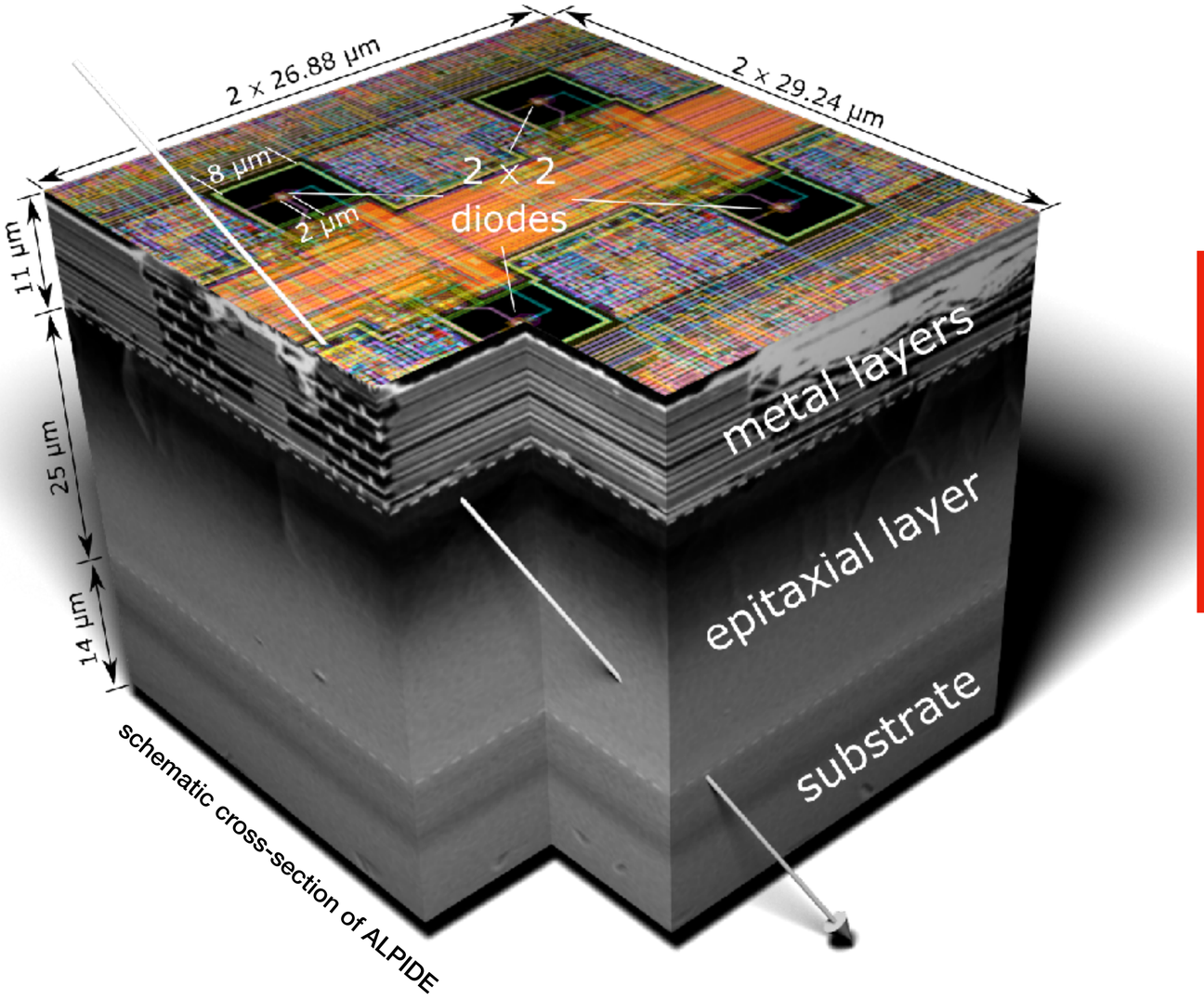
tracking efficiency

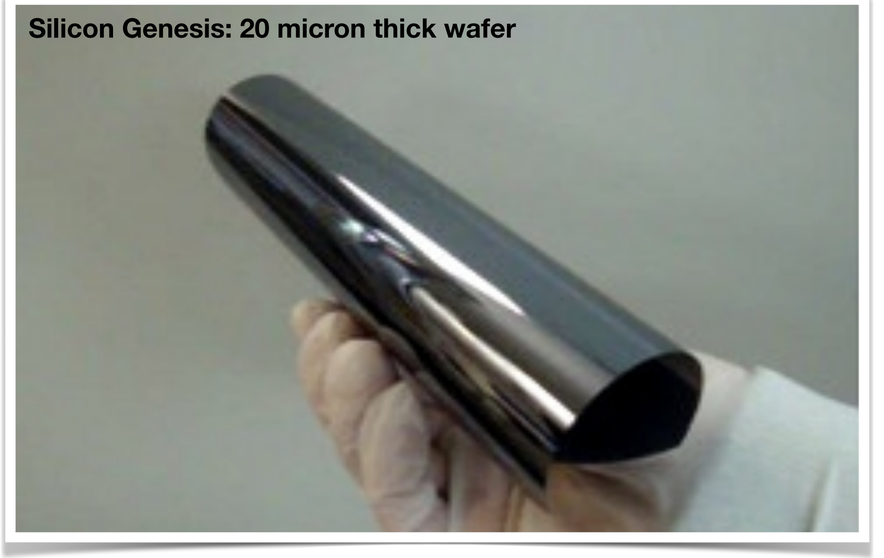


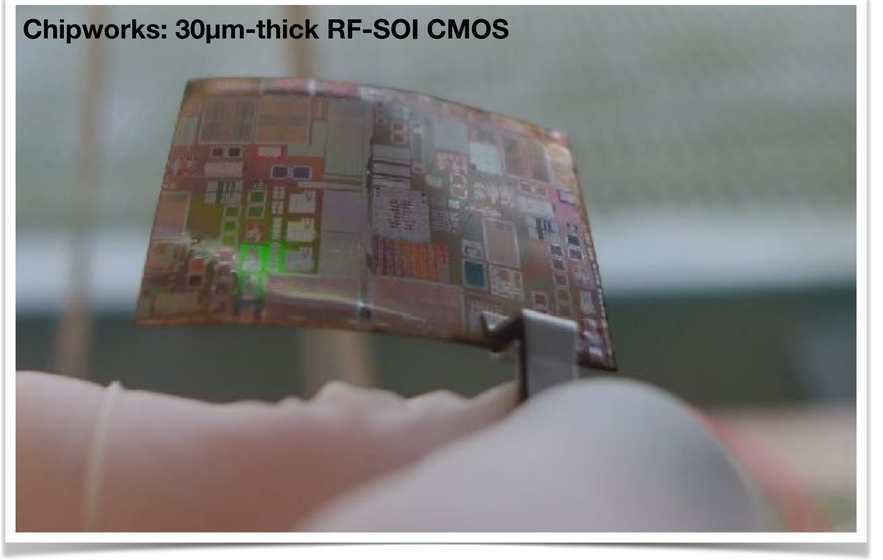
large improvement for low transverse momenta

Monolithic Active Pixel Sensor

Idea (1): make use of the flexible nature of thin silicon

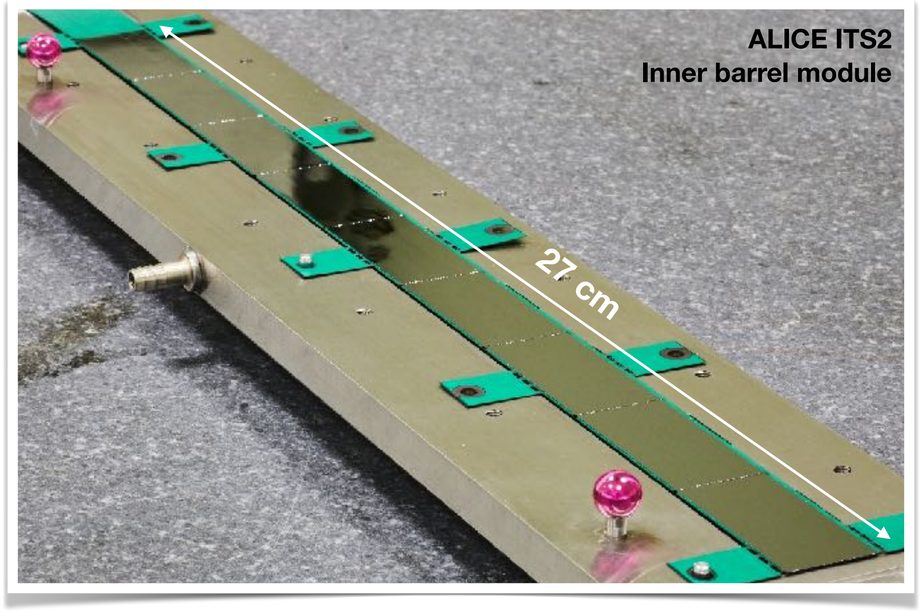


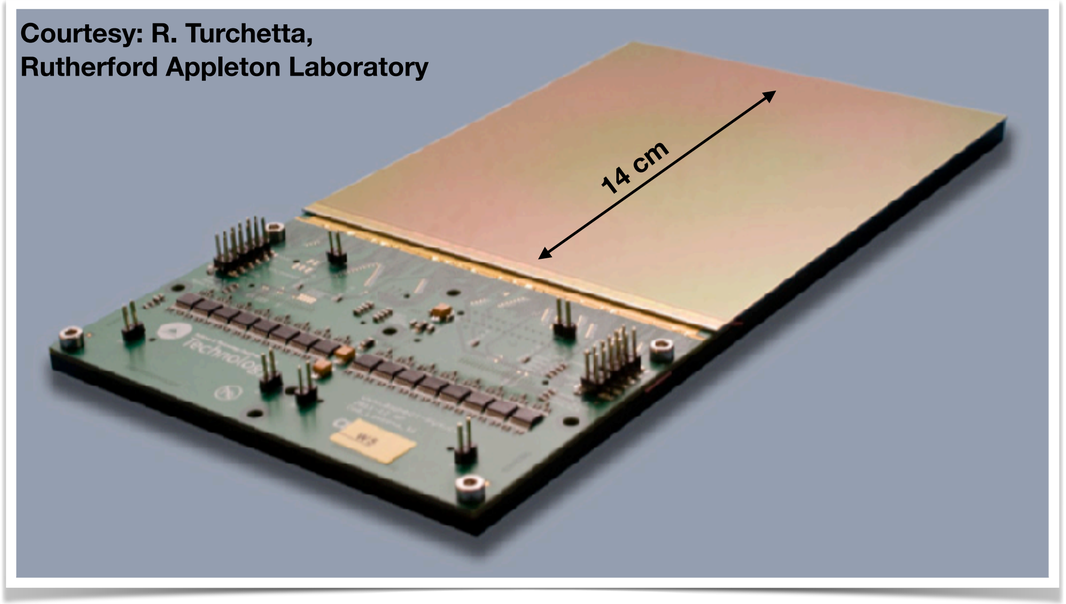




Detector modules

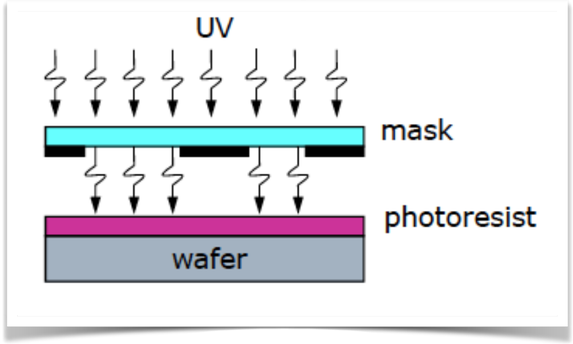
Idea (2): build wafer-scale sensors



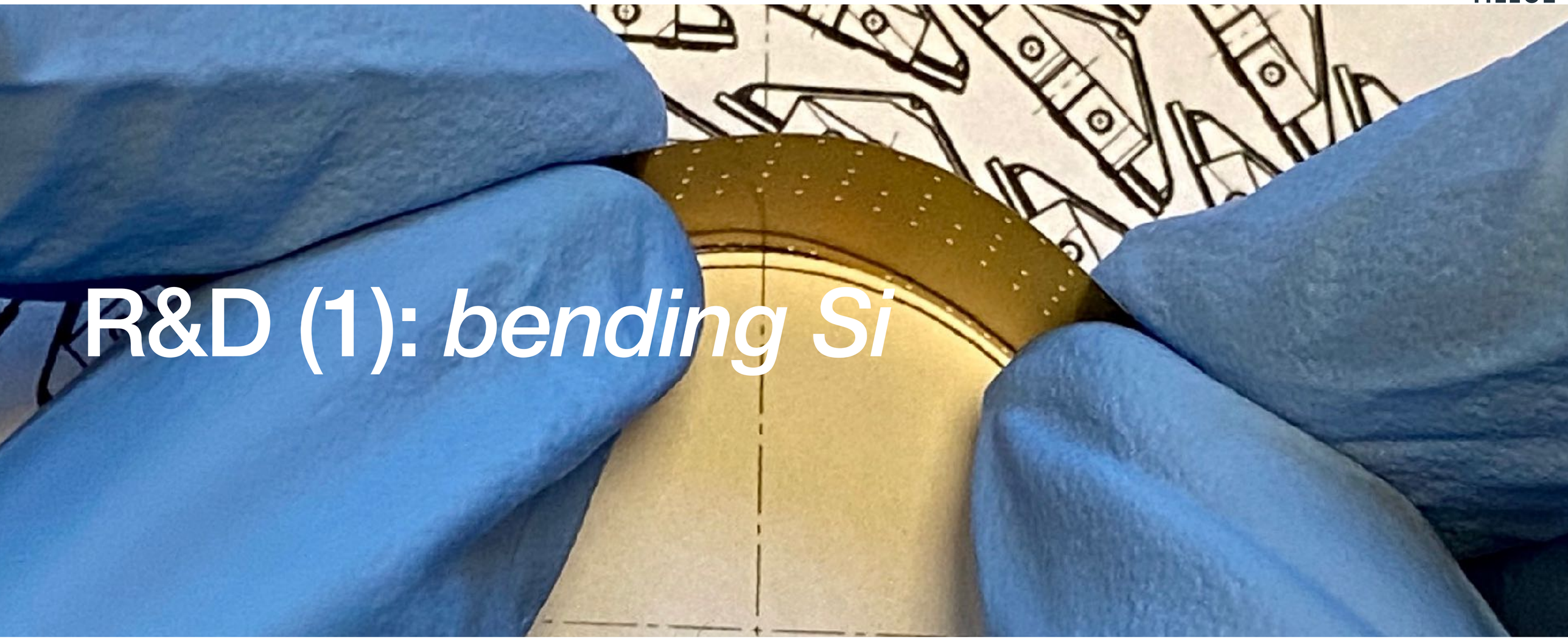


- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a sensor to equip a full half-layer
  - ***requires dedicated sensor design***



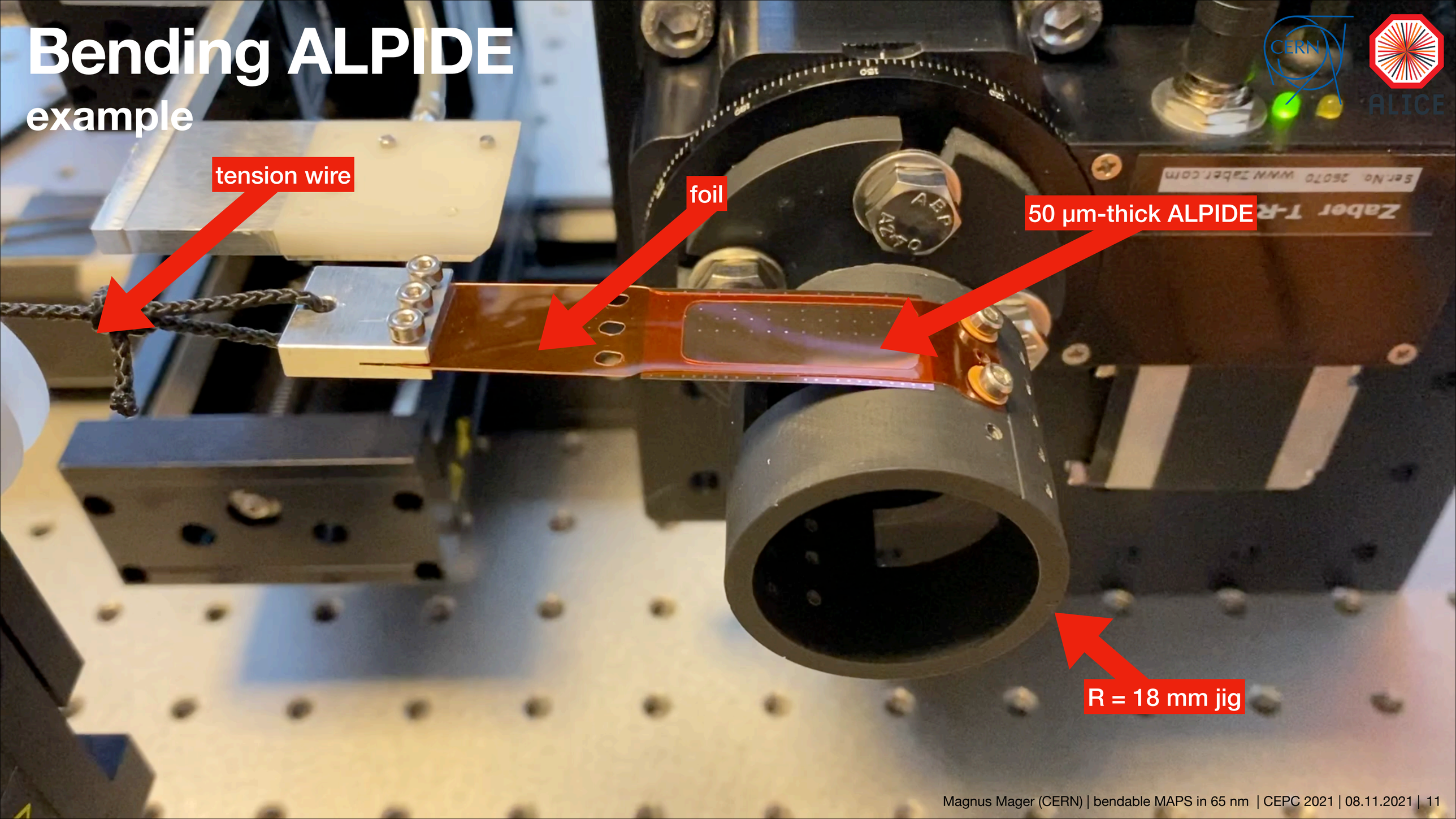
R&D (1): *bending Si*



[“Standard”, 50 µm thick ALPIDEs as used for the ITS2 IB, are already quite flexible!]

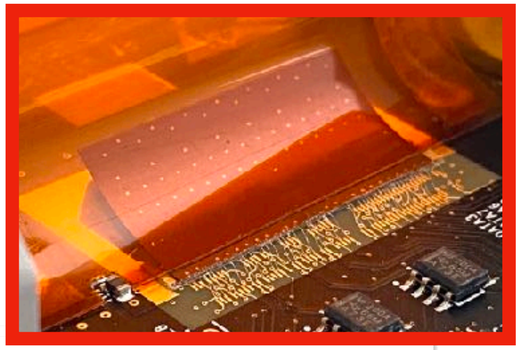
Bending ALPIDE

example



Beam tests

1st paper: arxiv:2105.13000



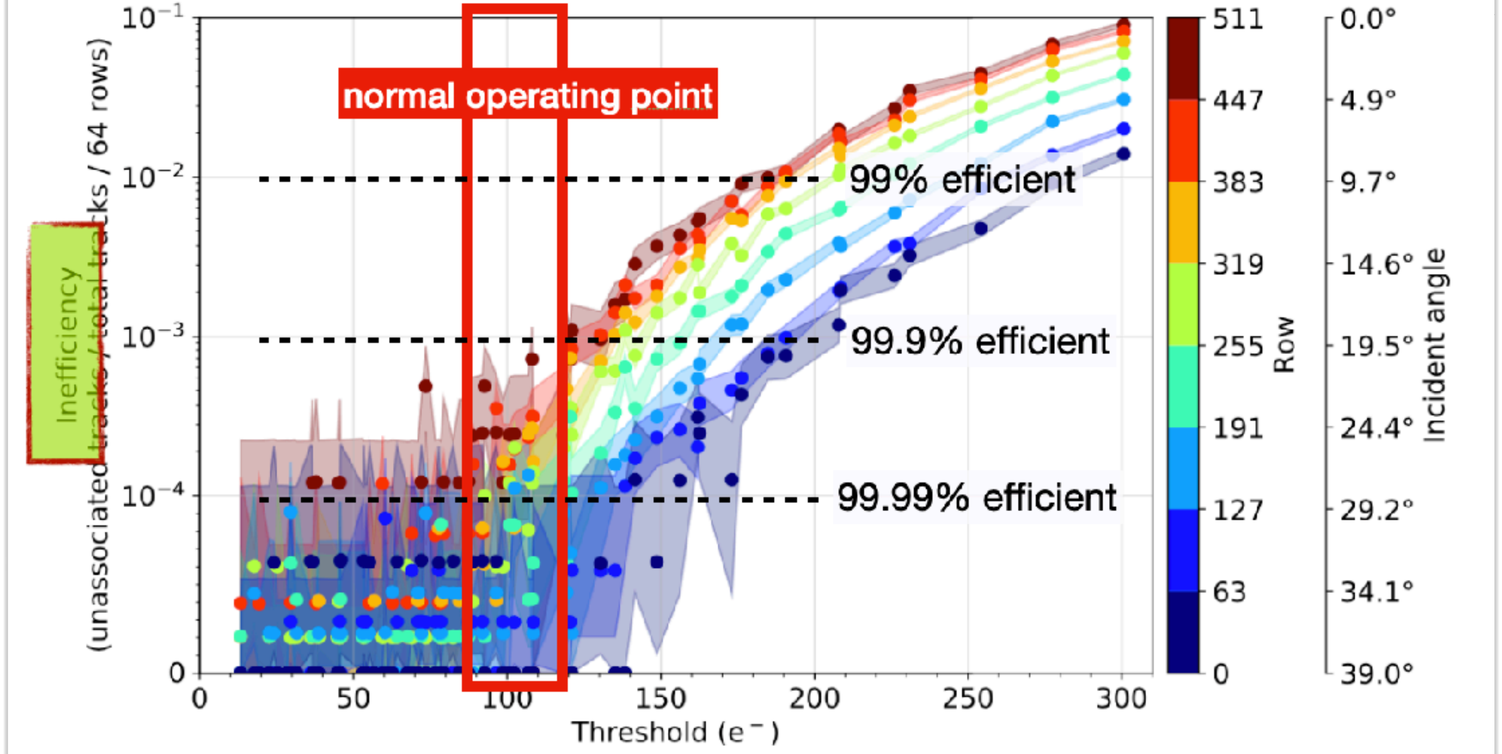


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS3

[a] European Organisation for Nuclear Research (CERN), Geneva, Switzerland
[b] GSI, Darmstadt, Germany
[c] Heidelberg University, Heidelberg, Germany
[d] INFN & University of Trieste, Trieste, Italy

Abstract

A novel approach for designing the next generation of vertex detectors foresees to employ wafer-scale sensors that can be bent to truly cylindrical geometries after thinning them to thicknesses of 20-40 µm. To solidify this concept, the feasibility of operating bent MAPS was demonstrated using 1.5 cm × 3 cm ALPIDE chips. Already with their thickness of 50 µm, they can be successfully bent to radii of about 2 cm without any signs of mechanical or electrical damage. During a subsequent characterisation using a 5.4 GeV electron beam, it was further confirmed that they preserve their full electrical functionality as well as particle detection performance.

In this article, the bending procedure and the setup used for characterisation are detailed. Furthermore, the analysis of the beam test, including the measurement of the detection efficiency as a function of beam position and local inclination angle, is discussed. The results show that the sensors maintain their excellent performance after bending to radii of 2 cm, with detection efficiencies above 99.9 % at typical operating conditions, paving the way towards a new class of detectors with unprecedented low material budget and ideal geometrical properties.

Keywords: Monolithic Active Pixel Sensors, Solid state detectors, Bent sensors

1. Introduction

The precision of barrel vertex detectors is mainly determined by three contributions: their radial distance to the interaction point, their material budget, and their intrinsic sensor resolution. In order to achieve hermiticity, they are typically built out of detector staves placed in layers around the beam pipe. This arrangement effectively sets a practical limit on the first two factors. ALICE,

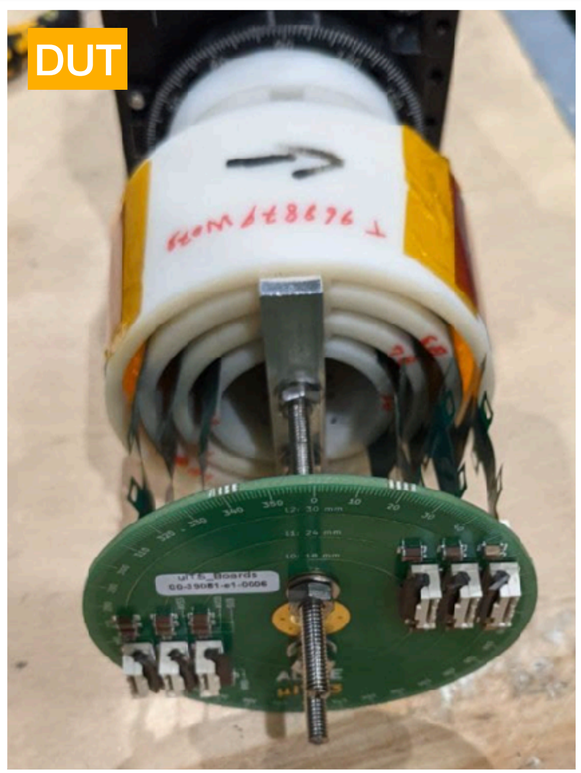
*Corresponding author

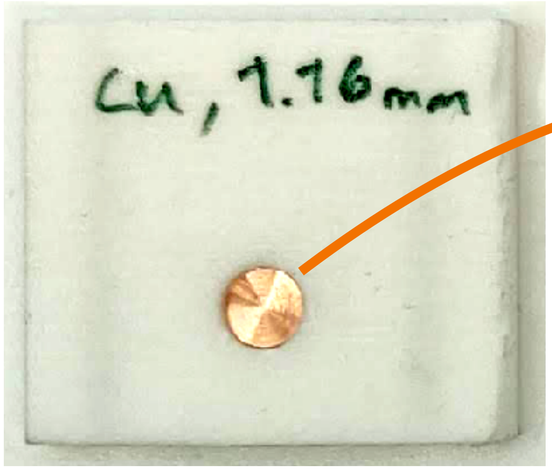
Clearly proving that bent MAPS are working!

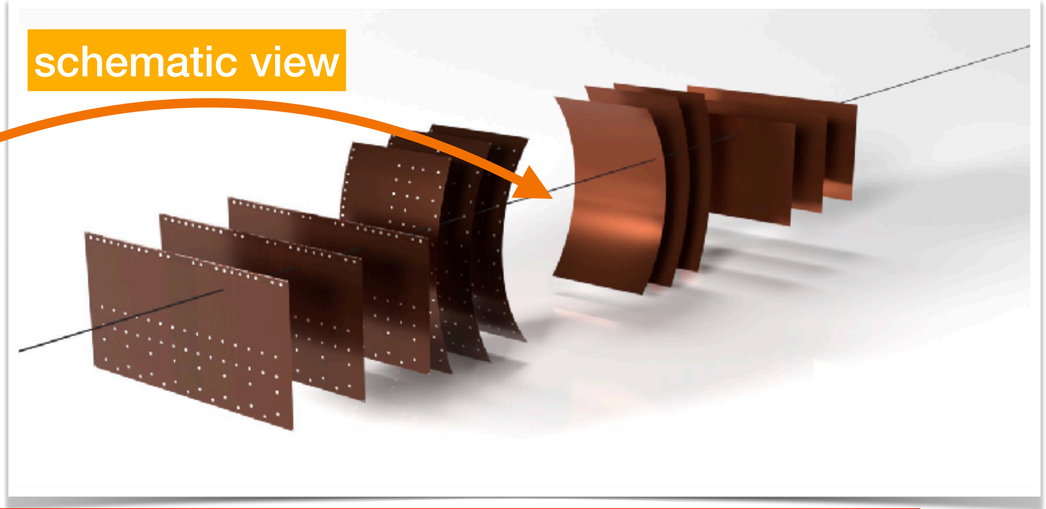
Beam tests

µITS3

- µITS3, i.e. 6 ALPIDEs at ITS3 radii
  - two complete setups based on “gold” quality ALPIDE chips
  - one has a Cu target in the center: expect to see 120 GeV proton/pion–Cu collisions
- Several days of continuous data taking
  - detailed analysis ongoing







First “real” experiment, allows to study tracking/reconstruction

Beam tests

µITS3

- µITS
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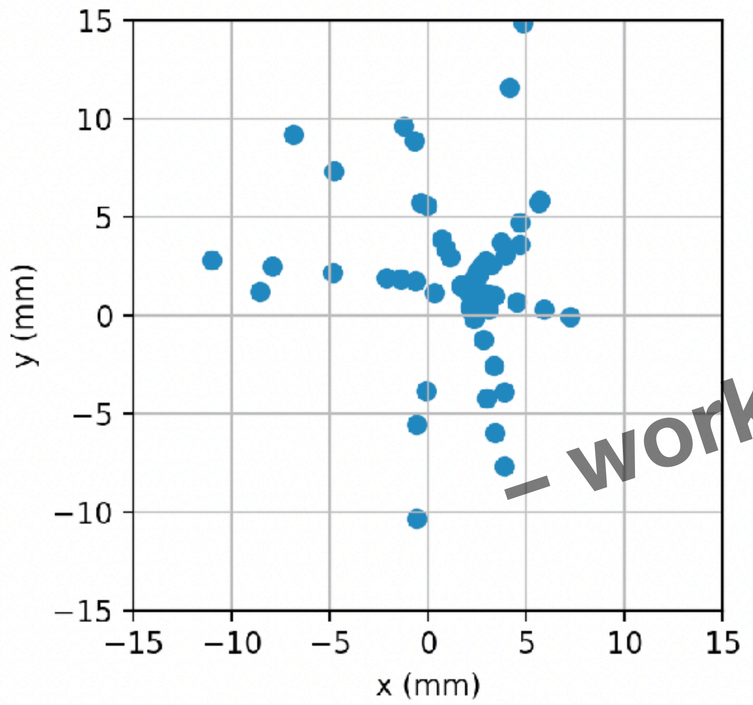
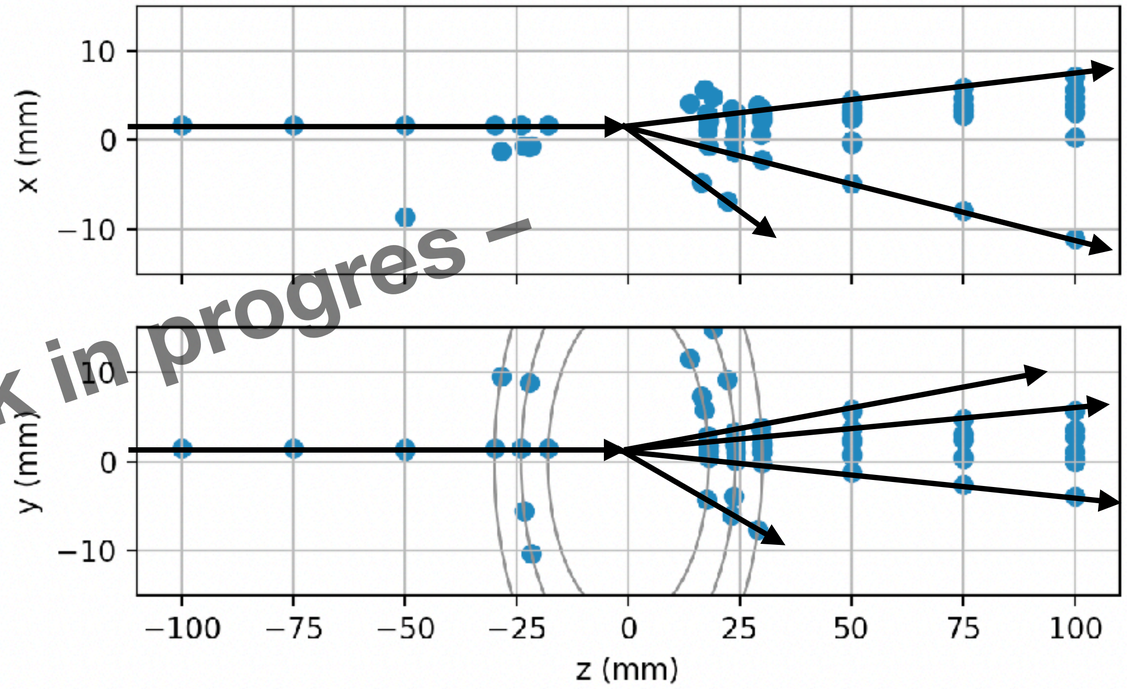
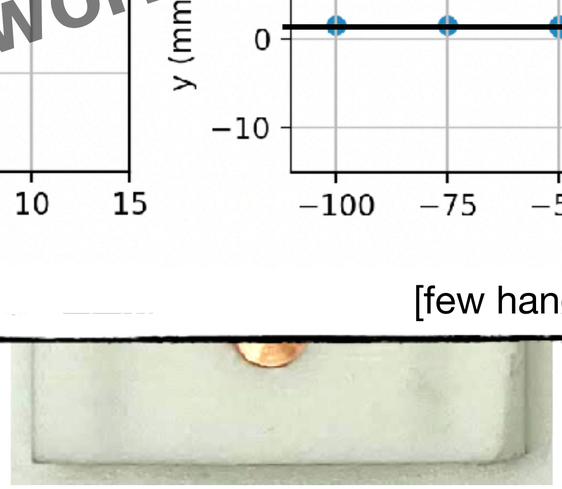
Example event

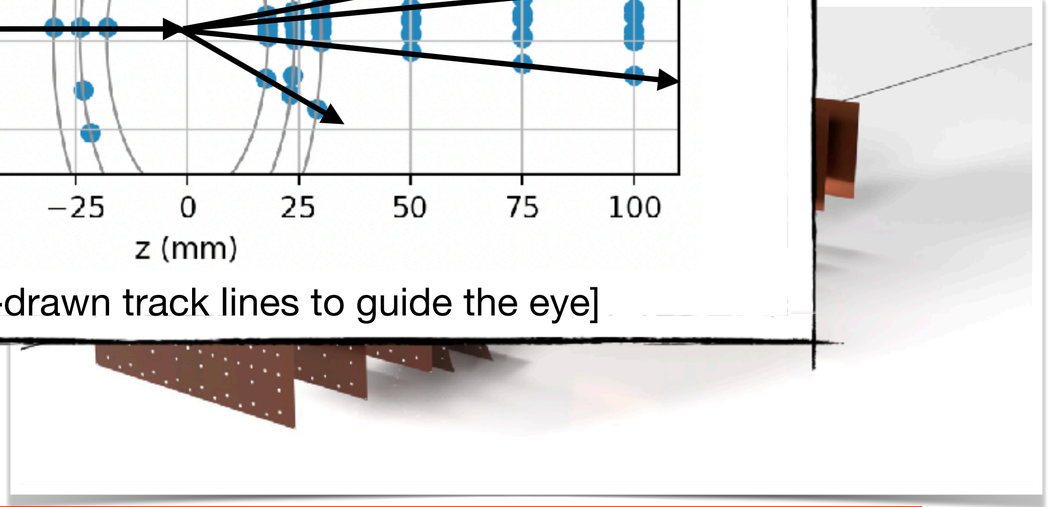




– work in progres –

[few hand-drawn track lines to guide the eye]

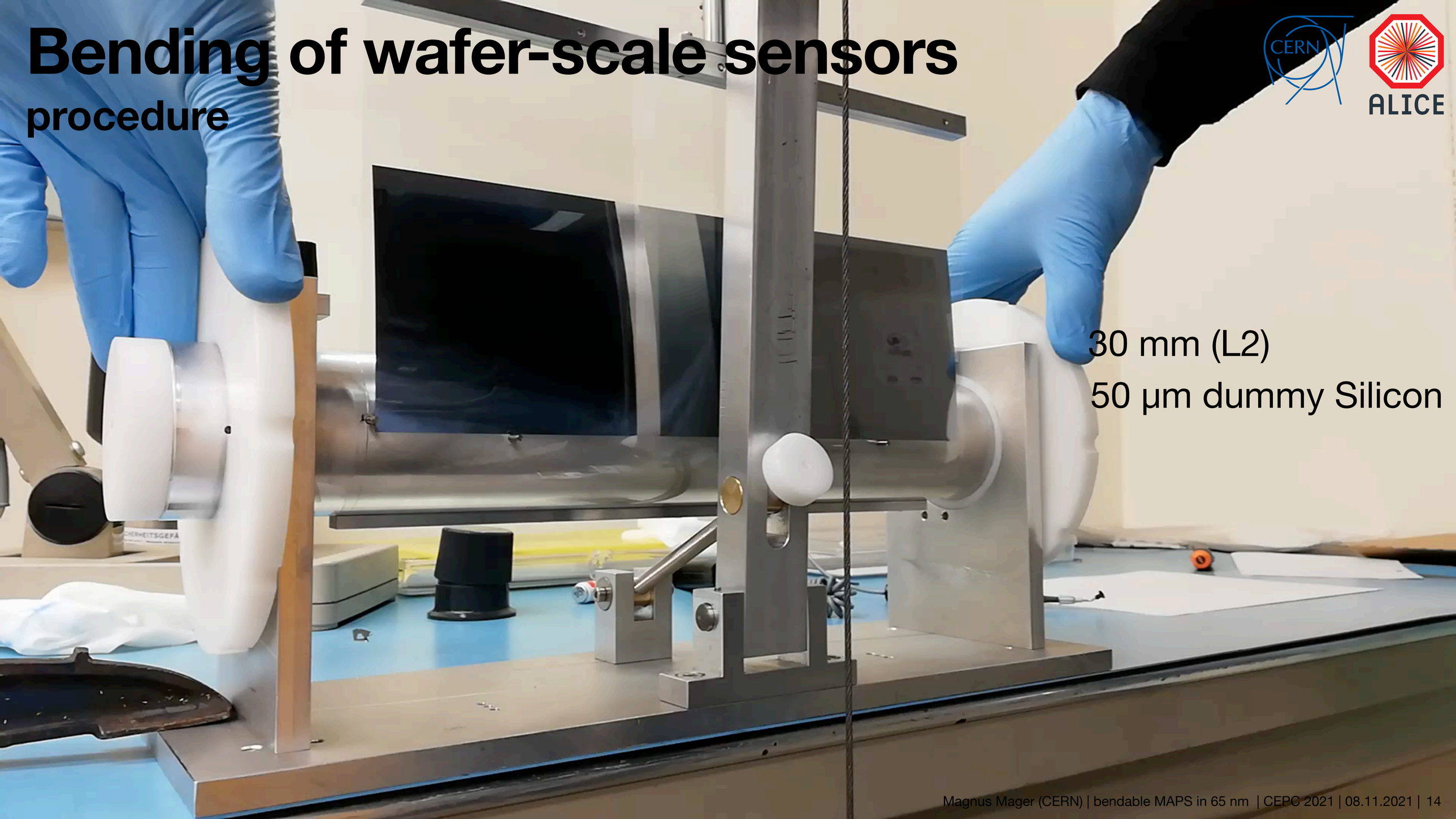




First “real” experiment, allows to study tracking/reconstruction

Bending of wafer-scale sensors

procedure

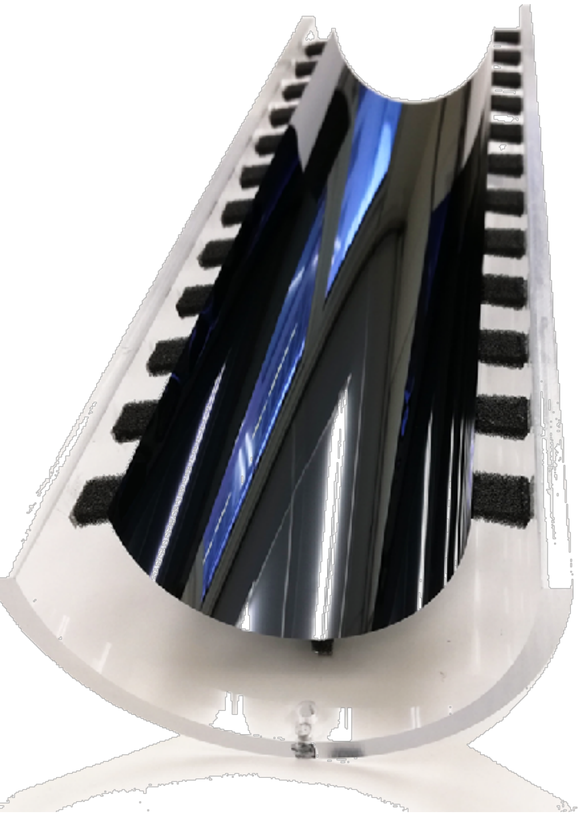


30 mm (L2)

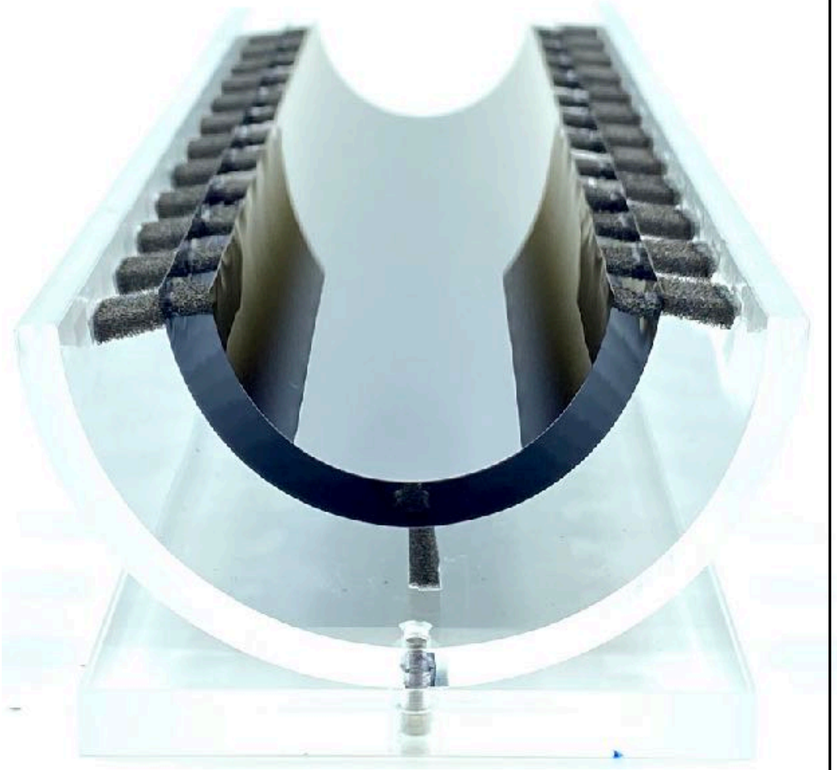
50 µm dummy Silicon

Layer assembly

Layer 2



Layers 2+1

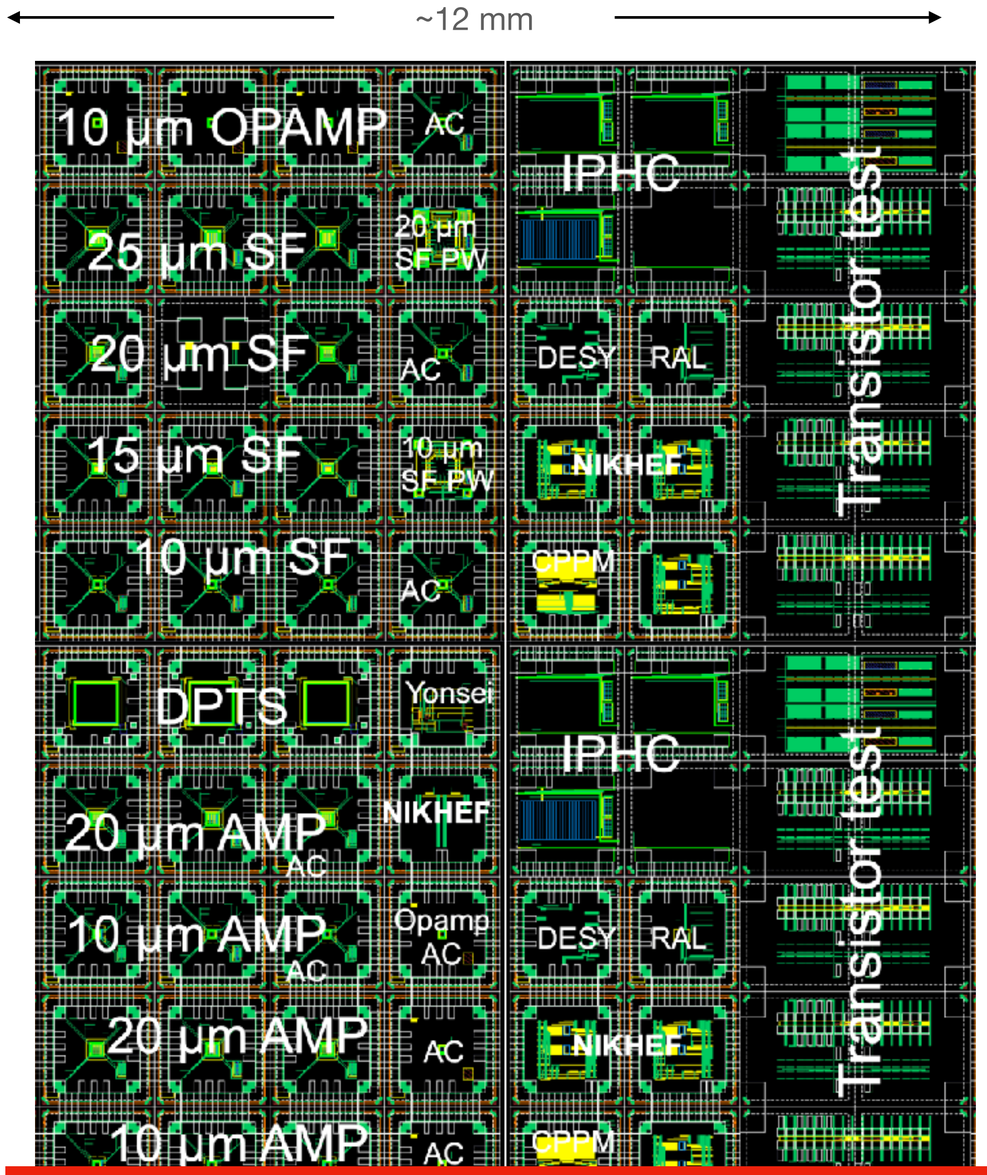


Layers 2+1+0

3-layer integration successful!

R&D (2): MAPS in 65 nm

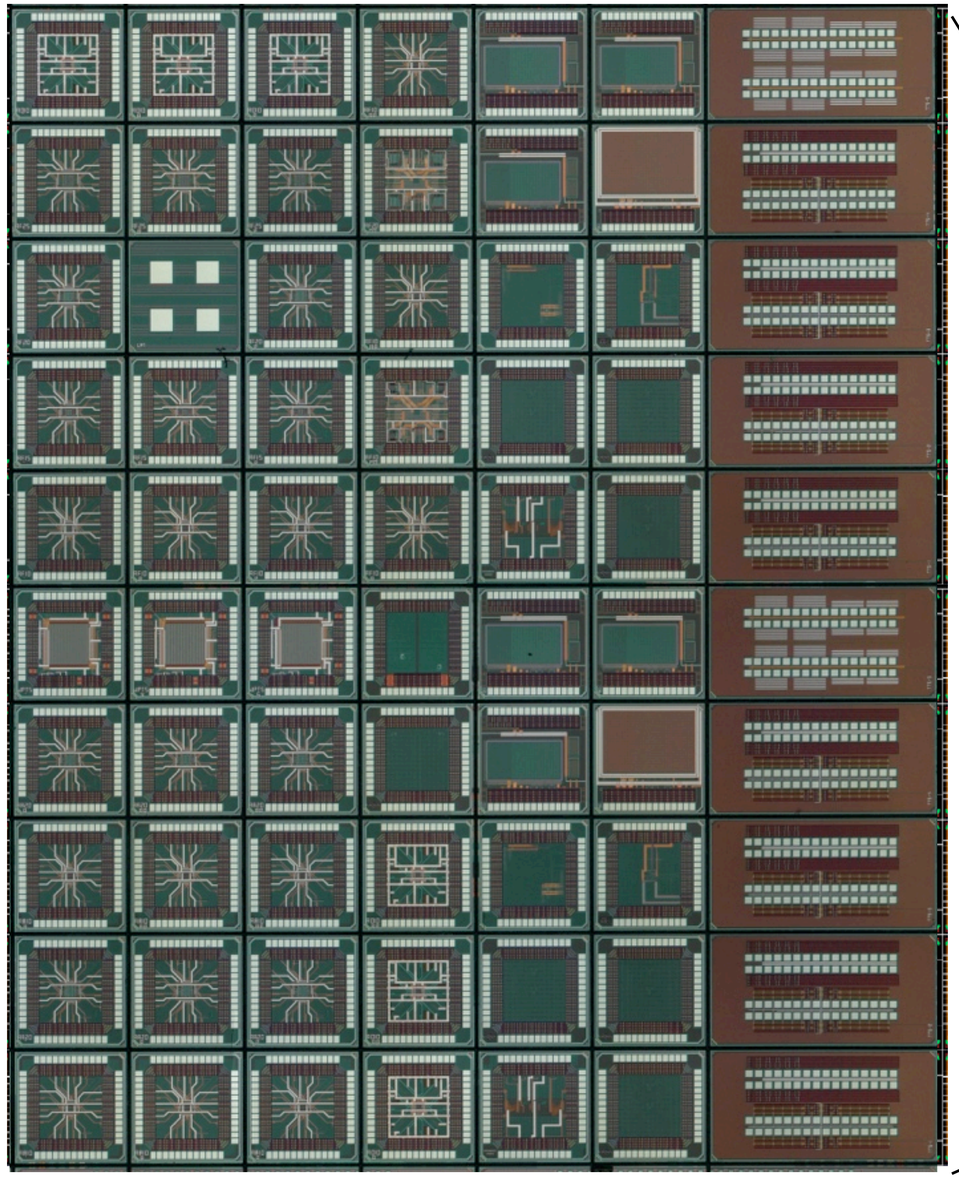
65 nm prototypes, MLR1



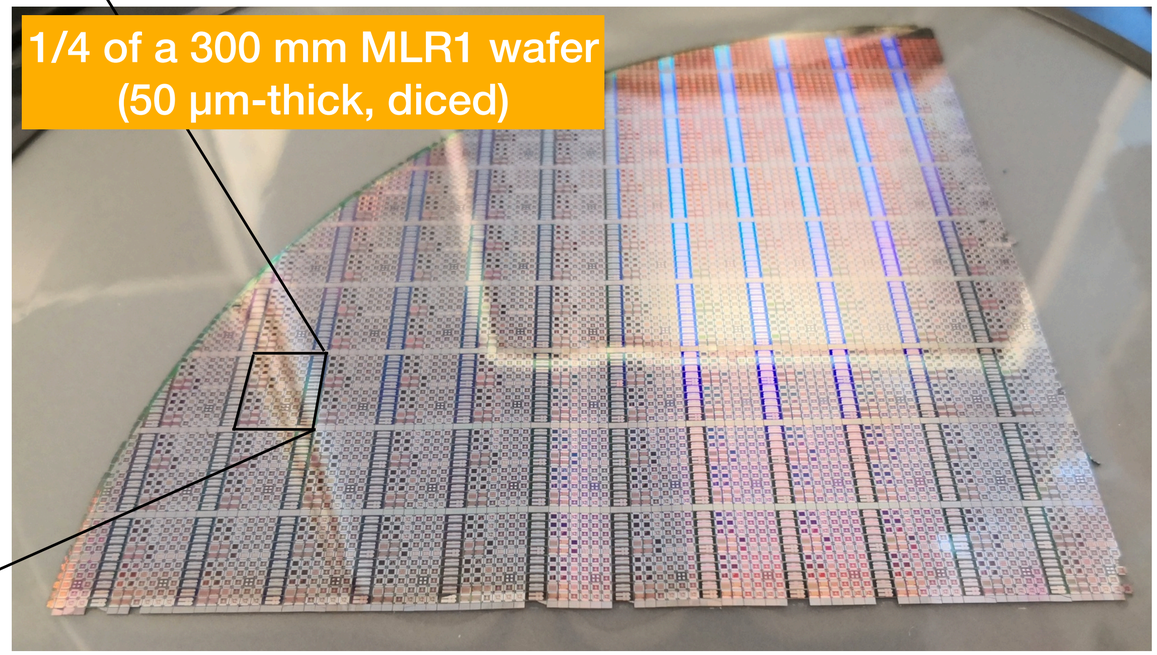
- First submission in TowerJazz 65nm
  - scoped within CERN EP R&D WP1.2
  - significant drive from ITS3
  - + important contributions from outside (not ALICE) groups
- Contained several test chips
  - radiation test structures
  - pixel test structures
  - pixel matrices
  - analog building blocks (band gaps, LVDS drivers, etc)

Very versatile first submission, combining what was initially planned for 2 MPWs

65 nm prototypes, MLR1



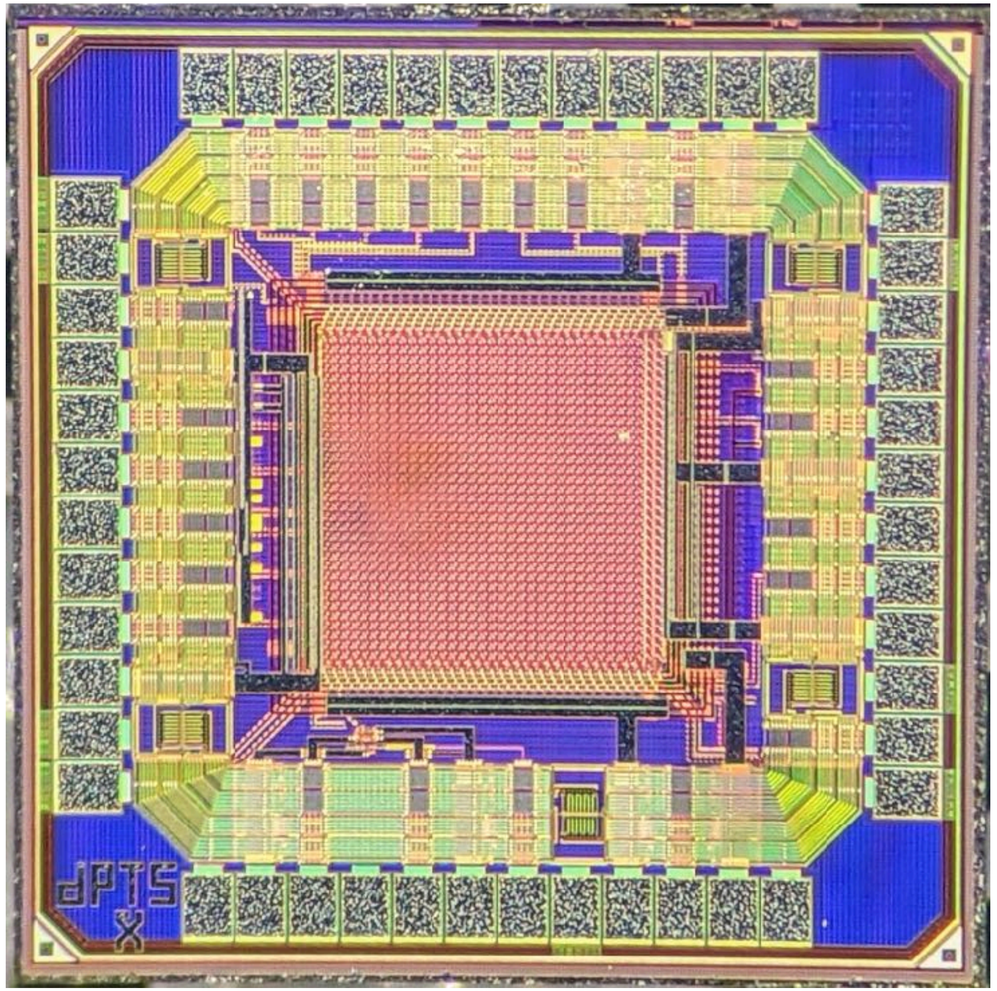
- Fully processed wafers are back by now
  - testing has started at many places
- Produced with 4 different process splits
  - TCAD-guided optimisations in collaboration with foundry, comparable to TJ180nm



65 nm prototypes, MLR1

Digital Pixel Test Structure (DPTS)

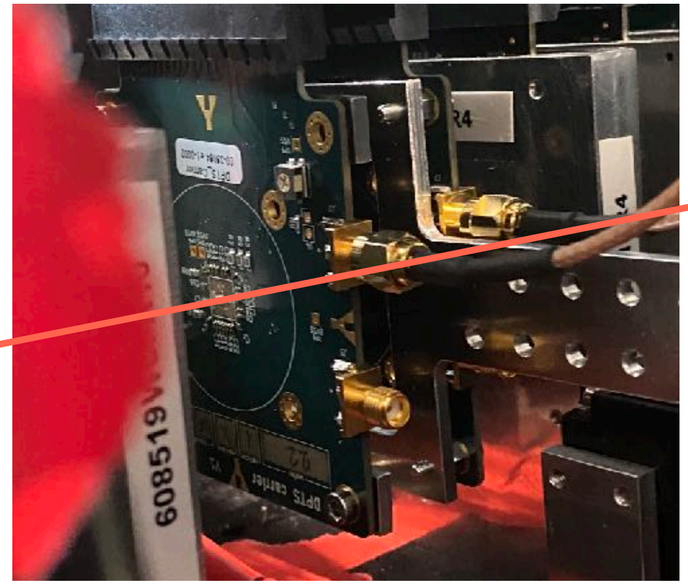
- Most “aggressive” chip in MLR1
- 32 × 32 pixels, 15 µm pitch
  - sizeable prototype, allows for “easy” test beam integration
- Asynchronous digital readout with ToT information
- Allows to verify:
  - sensor performance
  - front-end performance
  - basic digital building blocks
  - SEU cross-sections of registers

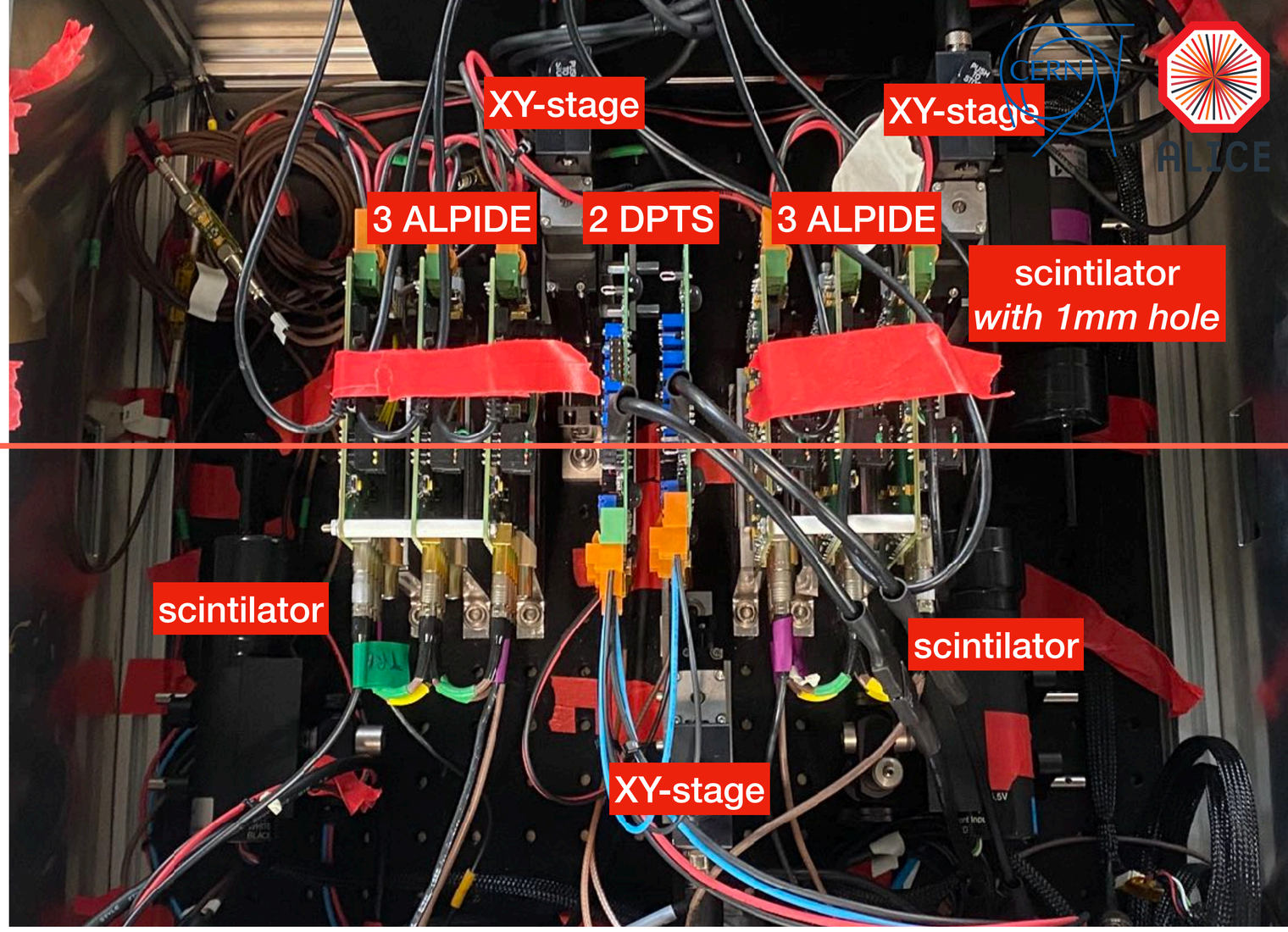


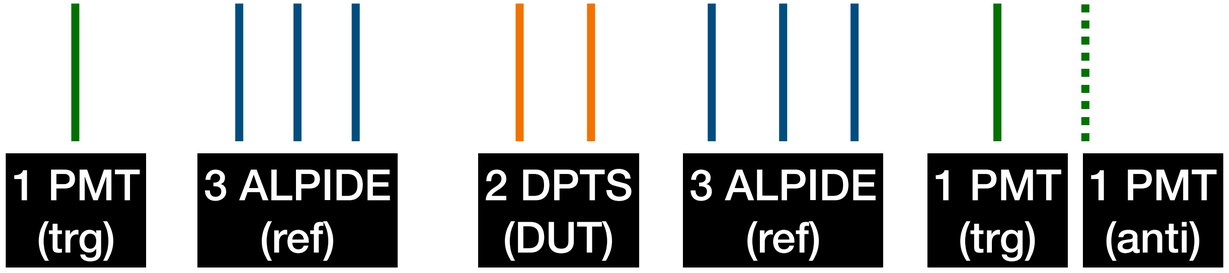
First beam test

Telescope with DPTS

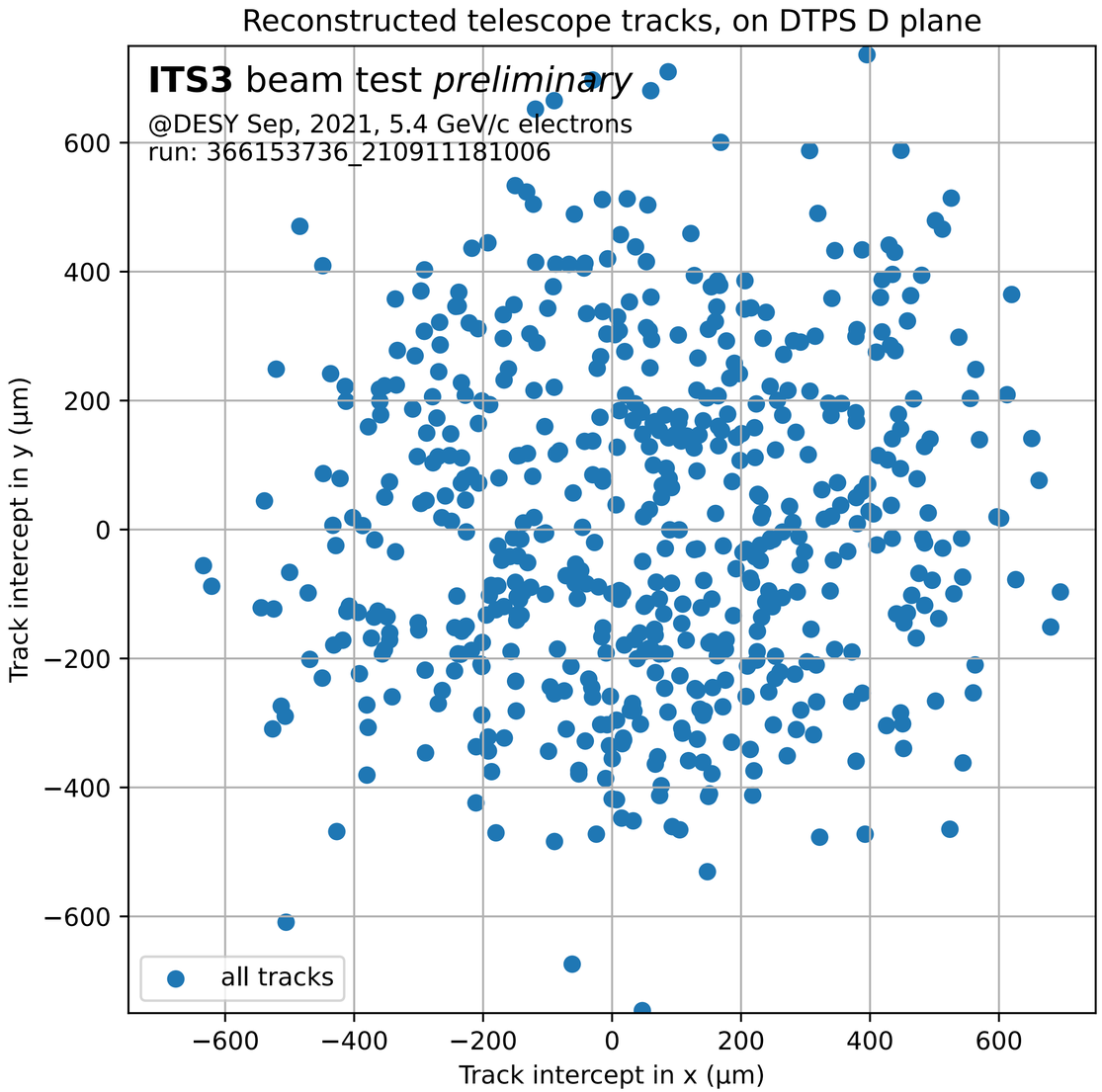
- Scintillator with 1mm hole can be used to trigger on narrow beam spot
- 6 precision linear stages with remote control allow to precisely align 2 DTPS and scintillators







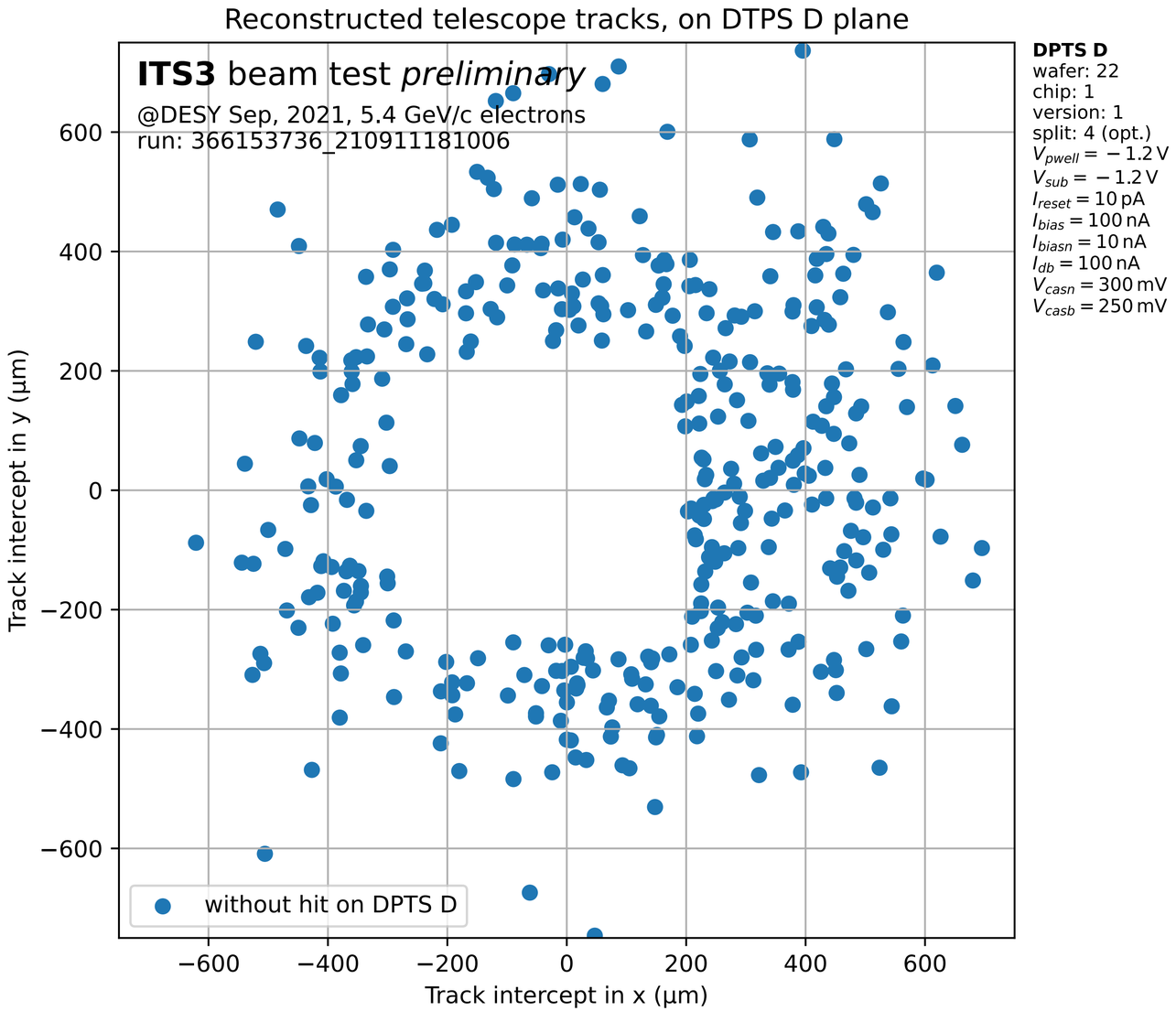
DPTS beam test results



first few % of total statistics analysed

- Beam spot and trigger tuned to illuminate a small area

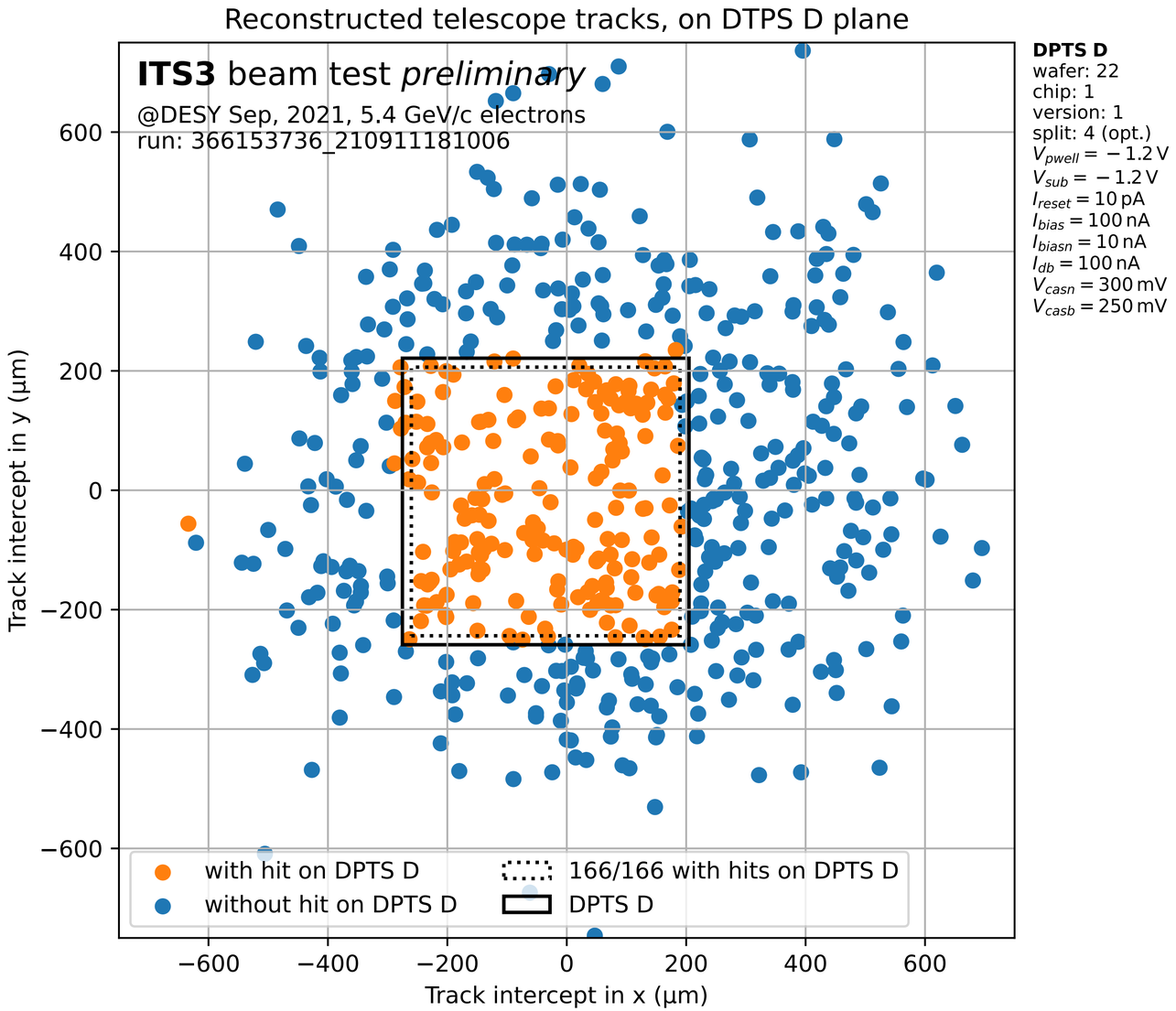
DPTS beam test results



- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen

first few % of total statistics analysed

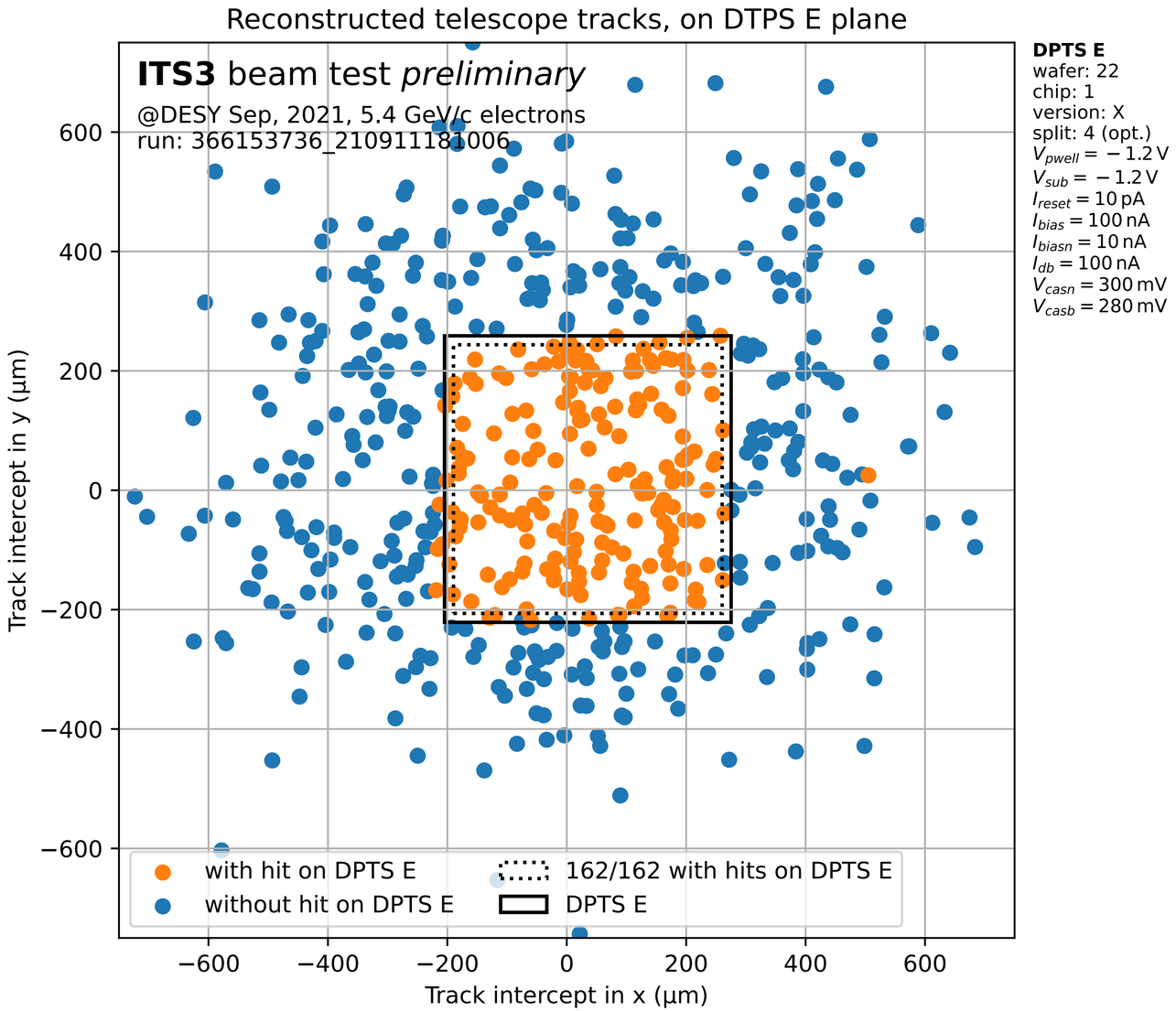
DPTS beam test results



first few % of total statistics analysed

- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest

DPTS beam test results



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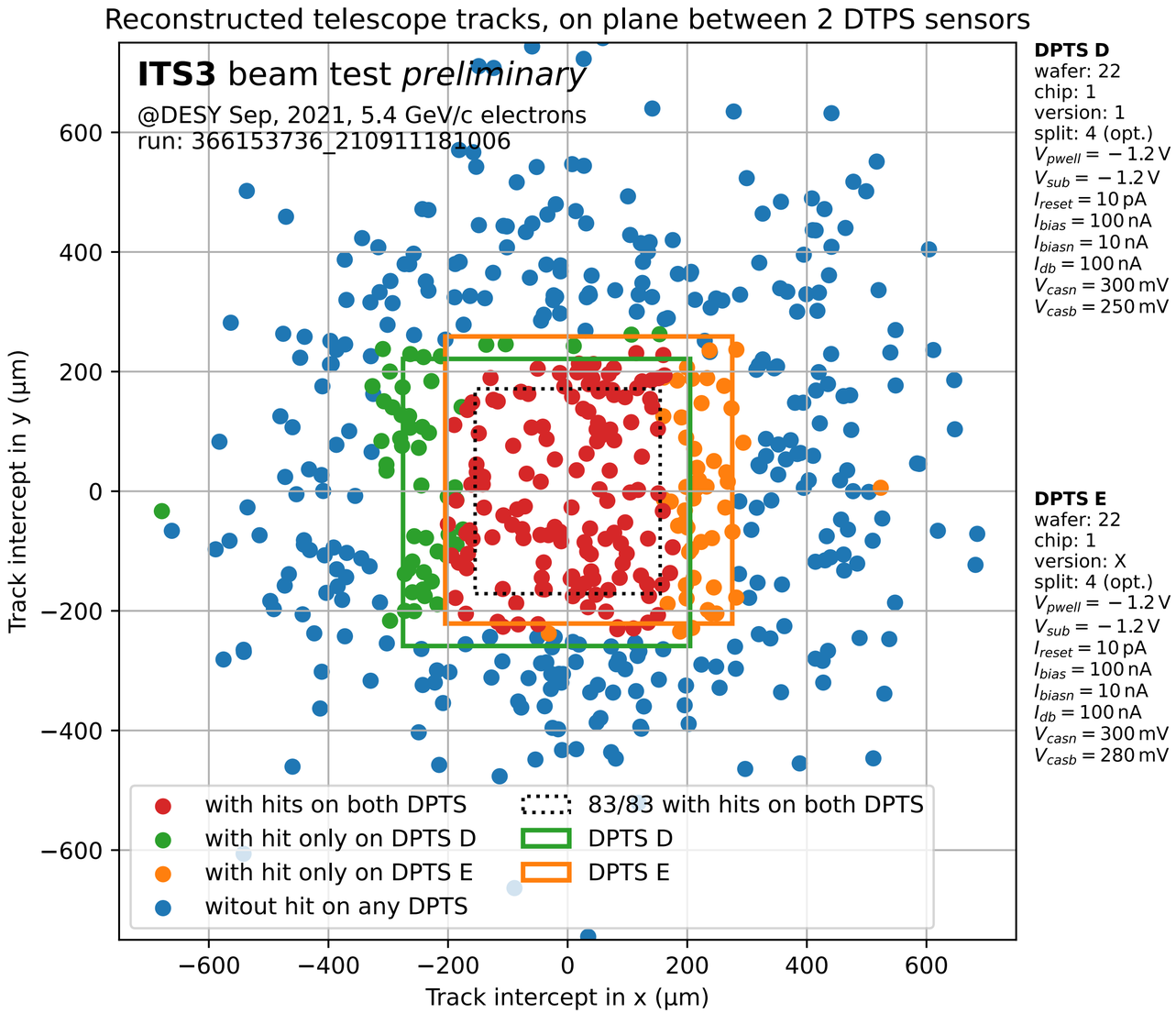
  - similar for second chip **(162/162)**

DPTS beam test results



first few % of total statistics analysed

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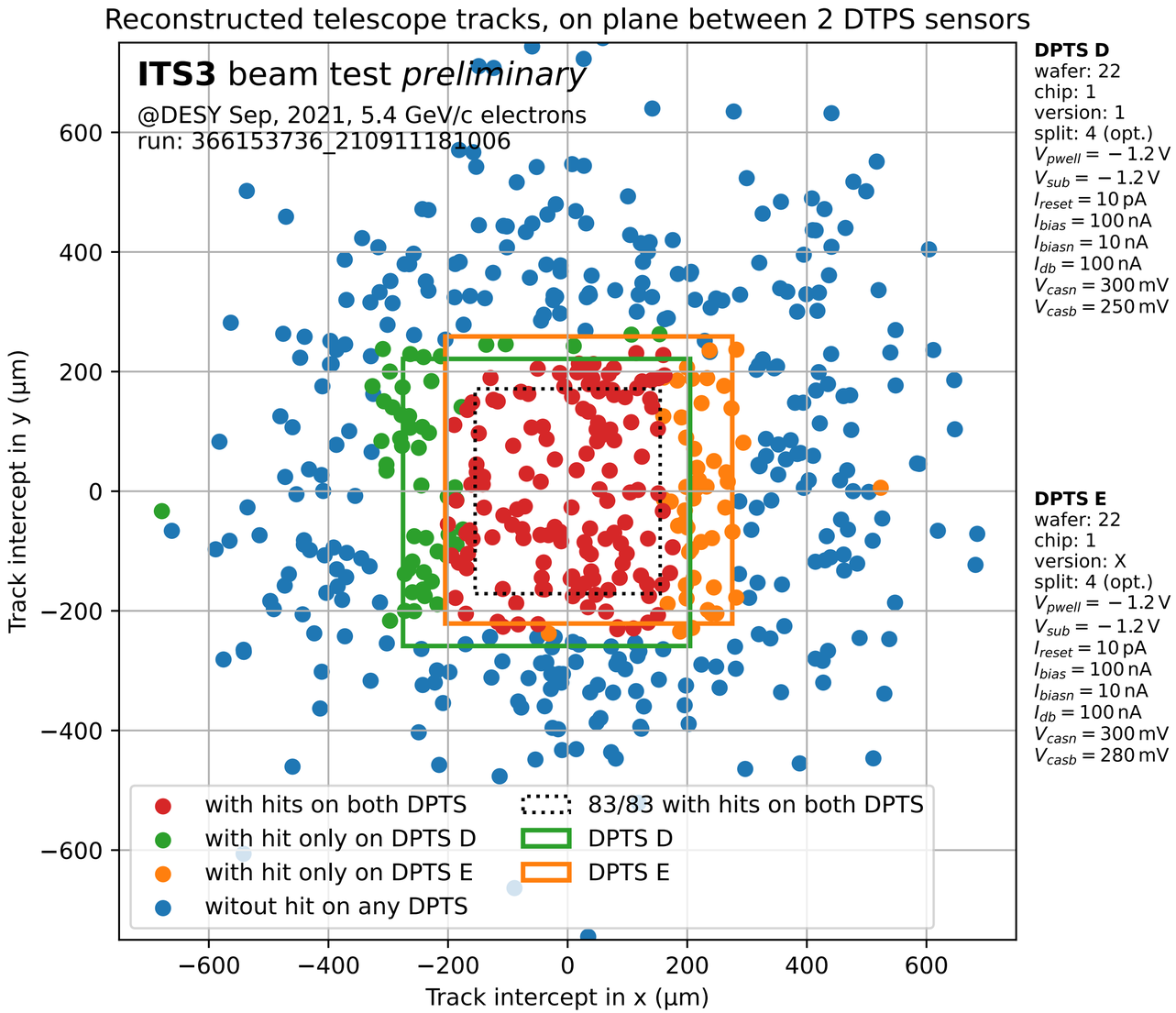
- **166/166** tracks in region of interest
  - similar for second chip **(162/162)**
  - and even for both in coincidence **(83/83)**

DPTS beam test results



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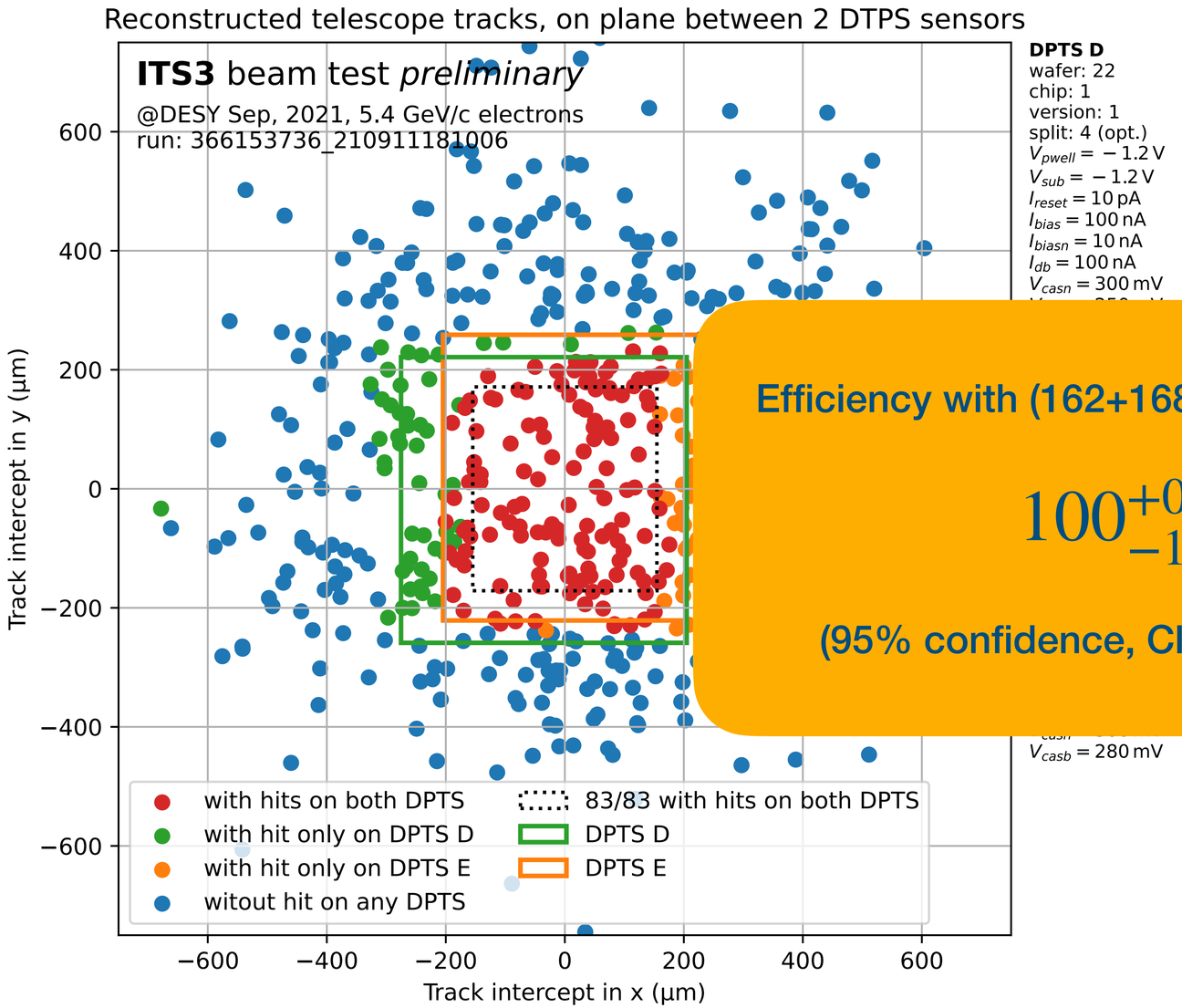
Excellent sensor *and* front-end performance already from *first* 65 nm prototype

DPTS beam test results



Efficiency with (162+168)/(162+168) tracks:

$$100^{+0}_{-1}\ \%$$

(95% confidence, Clopper-Pearson)

- Beam spot and trigger tuned to illuminate a small area
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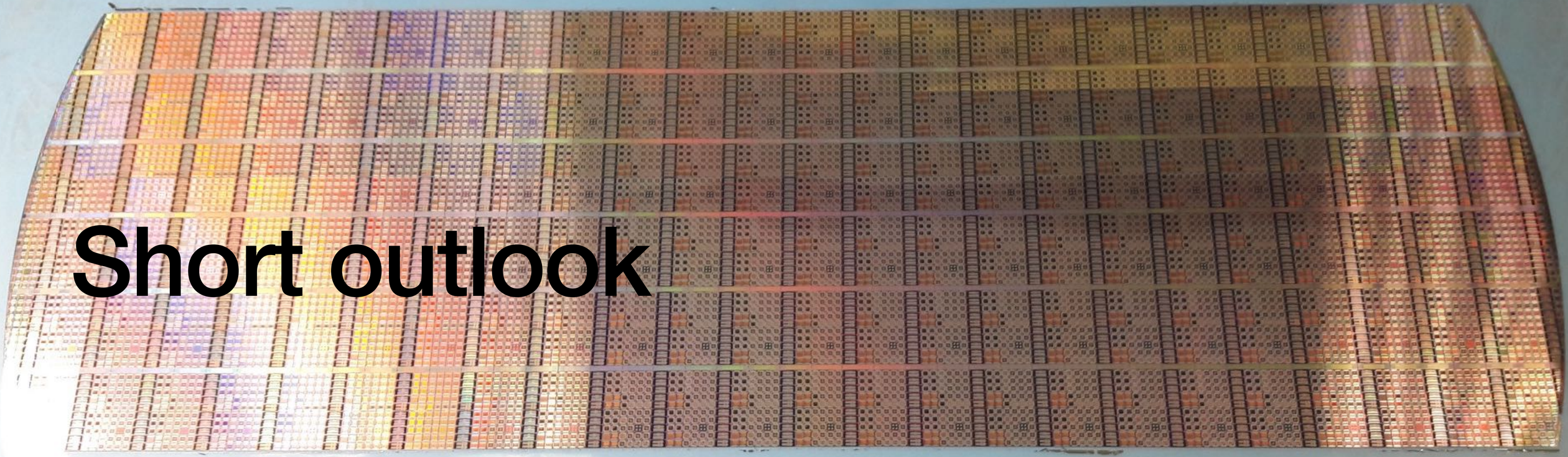
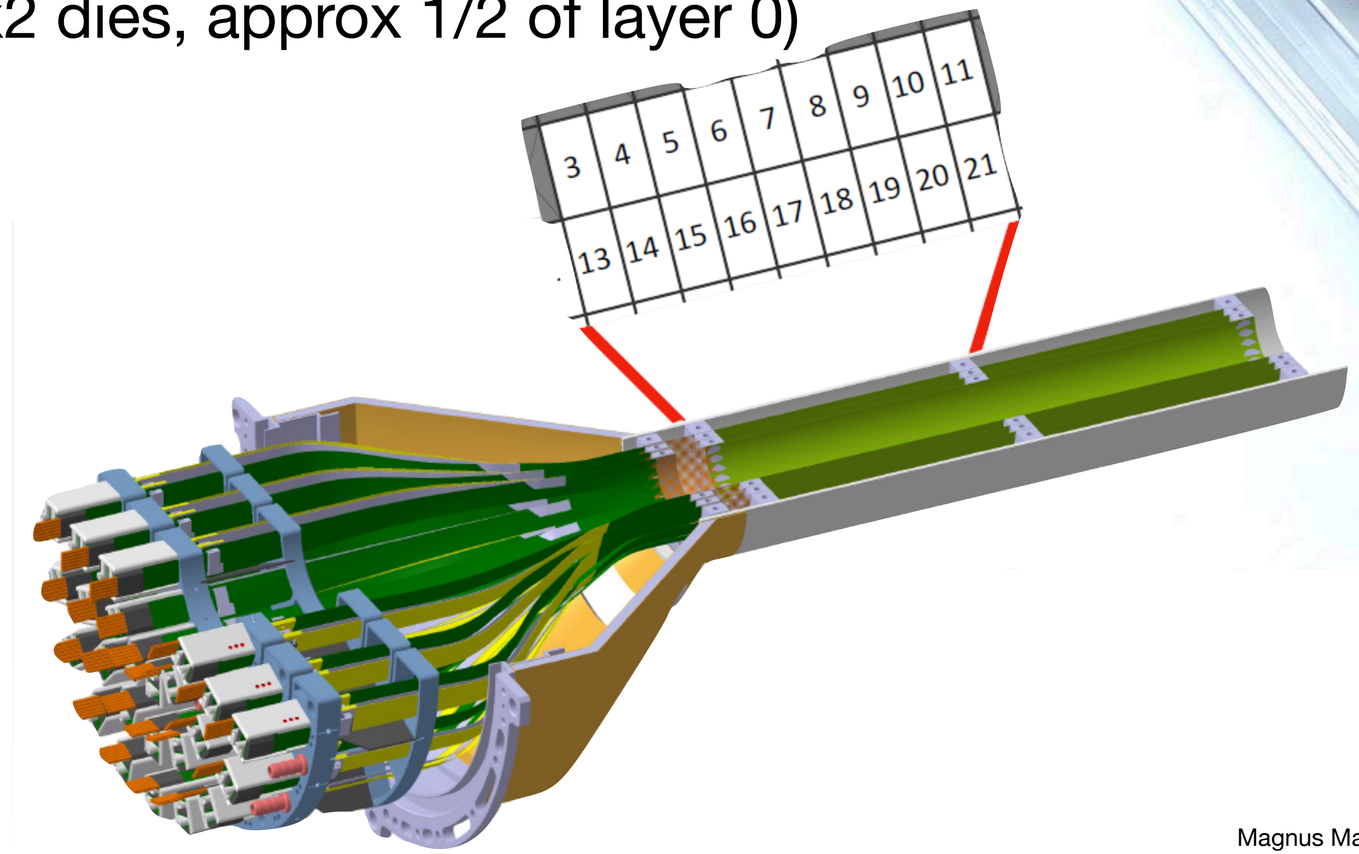
Short outlook

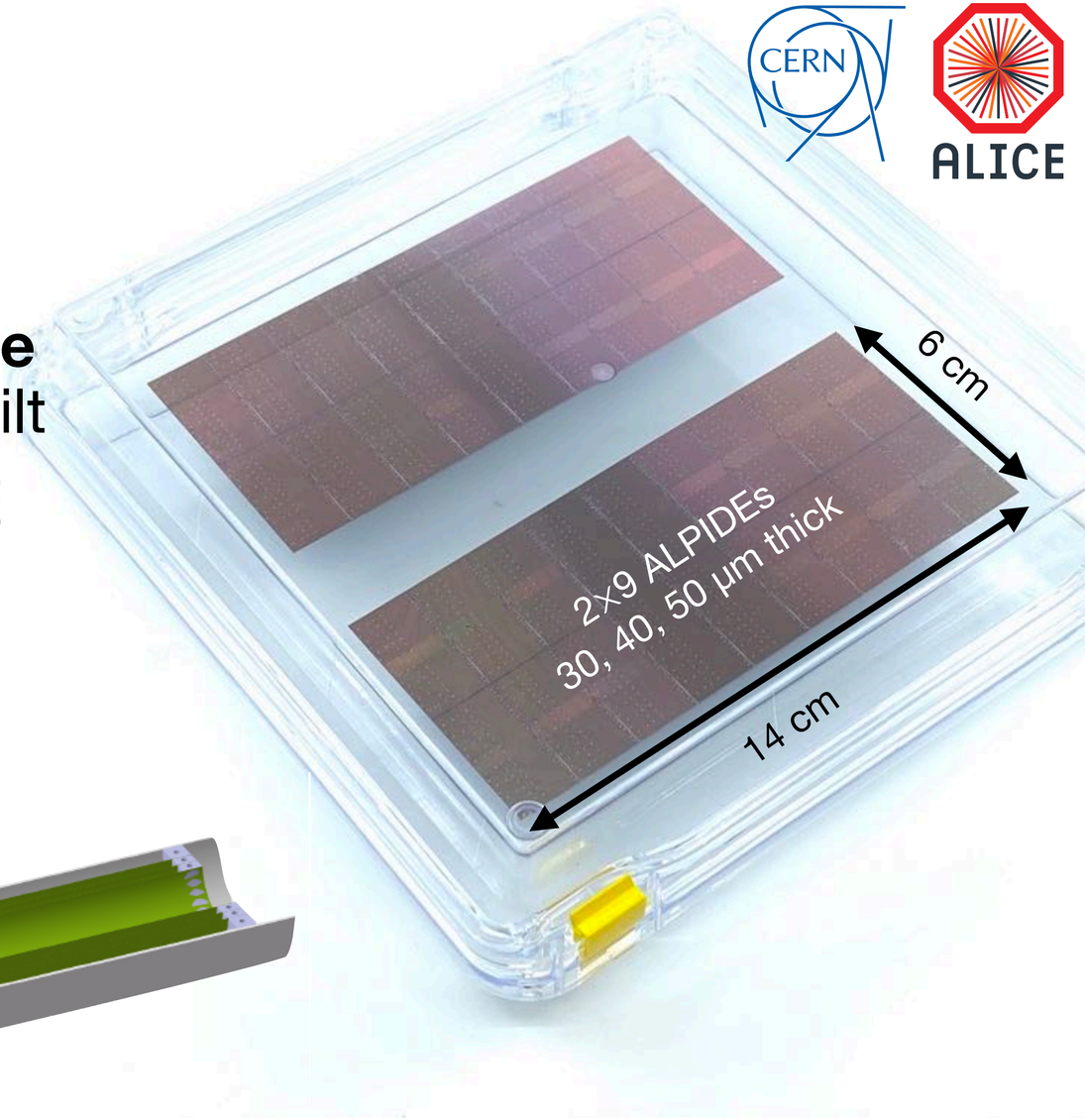


Layer interconnection

“super-ALPIDE”

- To study the bending **and** interconnection of **large** pieces of processed chips, “super-ALPIDE” is built
  - consists of 1 silicon piece cut from an ALPIDE wafer (9x2 dies, approx 1/2 of layer 0)

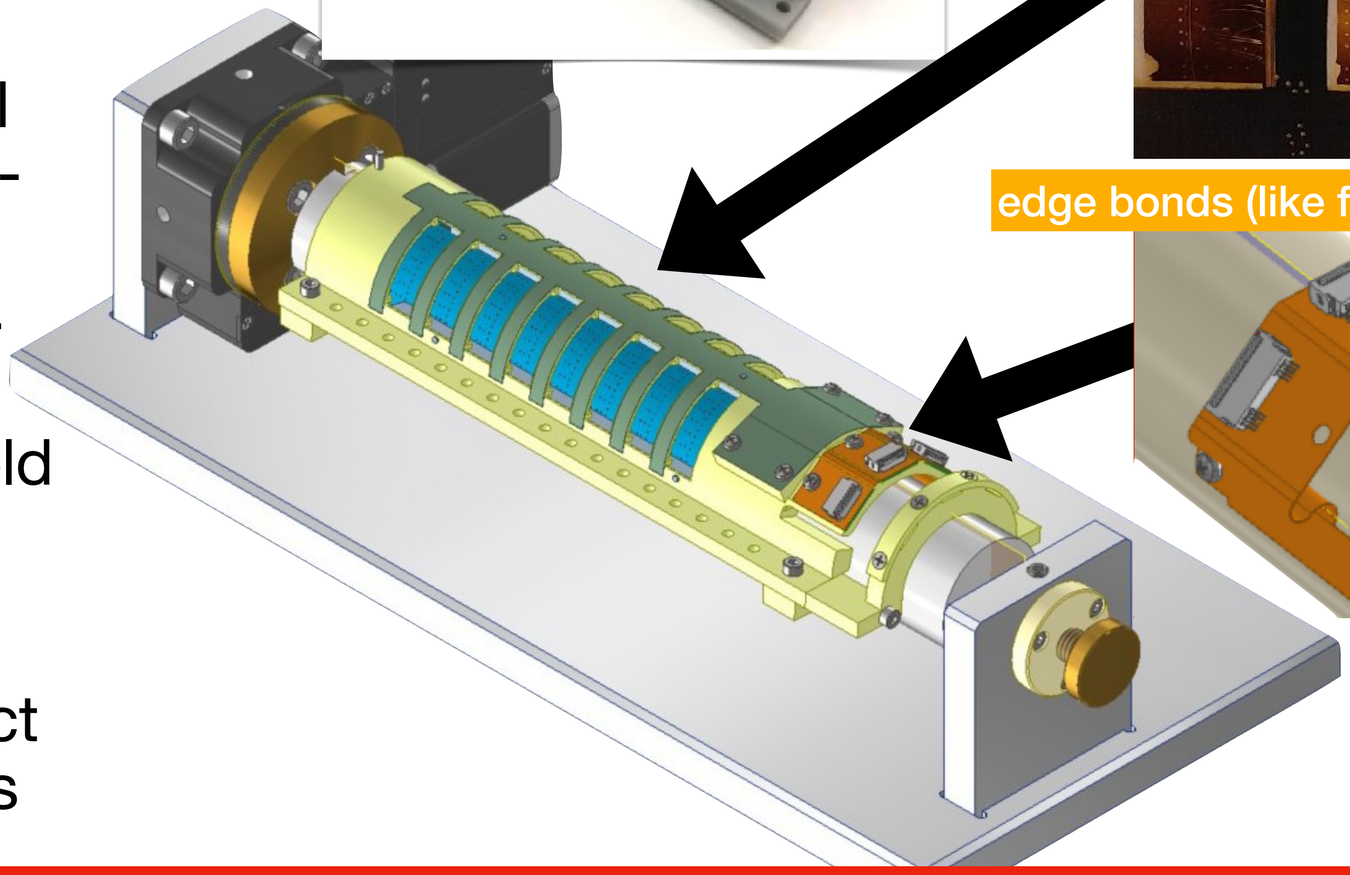




Layer interconnection (2)

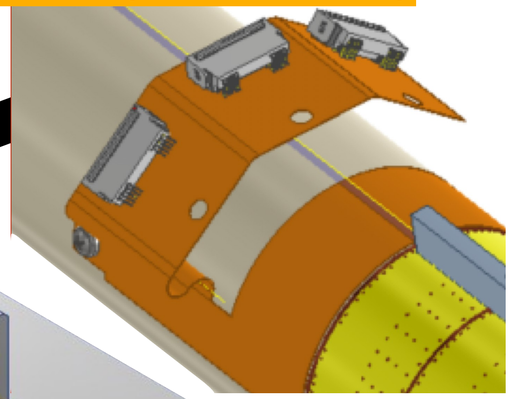
“super-ALPIDE”

- A bonding jig is being prepared
- the first row of ALPIDEs will be wire-bonded to an edge-FPC
  - just like the final detector
- super-ALPIDE/L0 will be held by an exoskeleton that:
  - mimics L1
  - and allows to interconnect all remaining ALPIDE dies



long wires for testing

edge bonds (like final ITS3)



Key R&D for combining electrical and mechanical prototypes

Summary

- **ALICE** proposes to build the next-generation Inner Tracking System, based on **300 mm-wafer-scale**, **20-40 µm-thin**, **bent MAPS**
- R&D on **bent MAPS**:
  - started with existing, thin MAPS within **ALICE ITS3**
  - in-beam verification of bent MAPS: **successful**
  - full-size mechanical mockups: **build and characterised**
- R&D on **65 nm MAPS**:
  - joint effort within CERN EP R&D of several groups with large contribution from the **ALICE ITS3** community
  - first submission (“MLR1”) came back: >50 prototype chips
  - detection efficiency of a 32x32 pixel prototype (“DPTS”): **100%**
- **These newly developed detector technologies have a the potential to be a game changer for several future vertex detectors**

Thank you!