The 2021 International Workshop on the High Energy Circular Electron Positron Collider

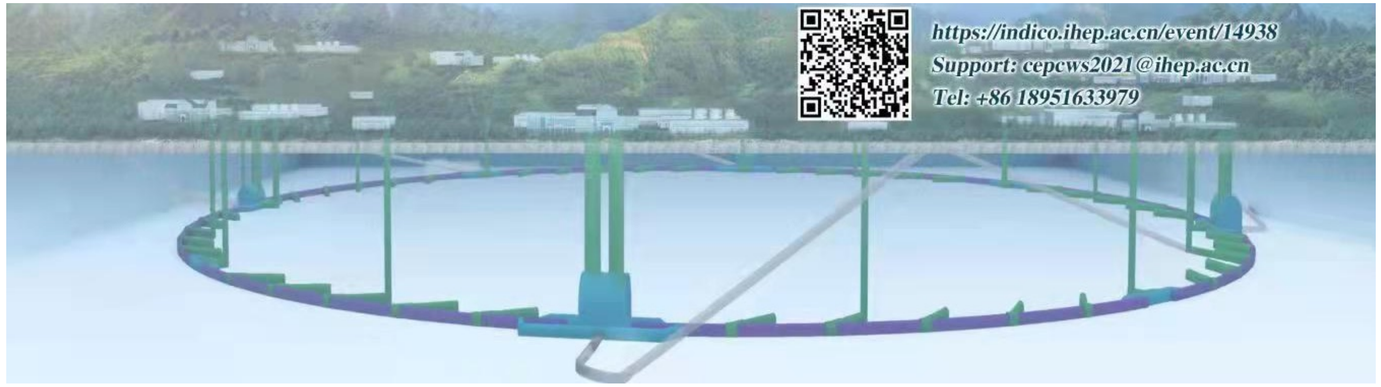
November 8-12, 2021, Nanjing, China

Consolidate the optimization and design of both accelerator and detectors and aim for a TDR in 2 years

Deepen the cooperation between the industry and high energy physics community

Highlights of the detector R&D

Paolo Giacomelli
INFN Bologna



Outline

- Some considerations…
- Silicon trackers
- Timing detectors
- Gas chambers
- Calorimeters
- Muon detectors
- Conclusions

Caveat

All the material presented is from other people's work

All errors and omissions are mine...

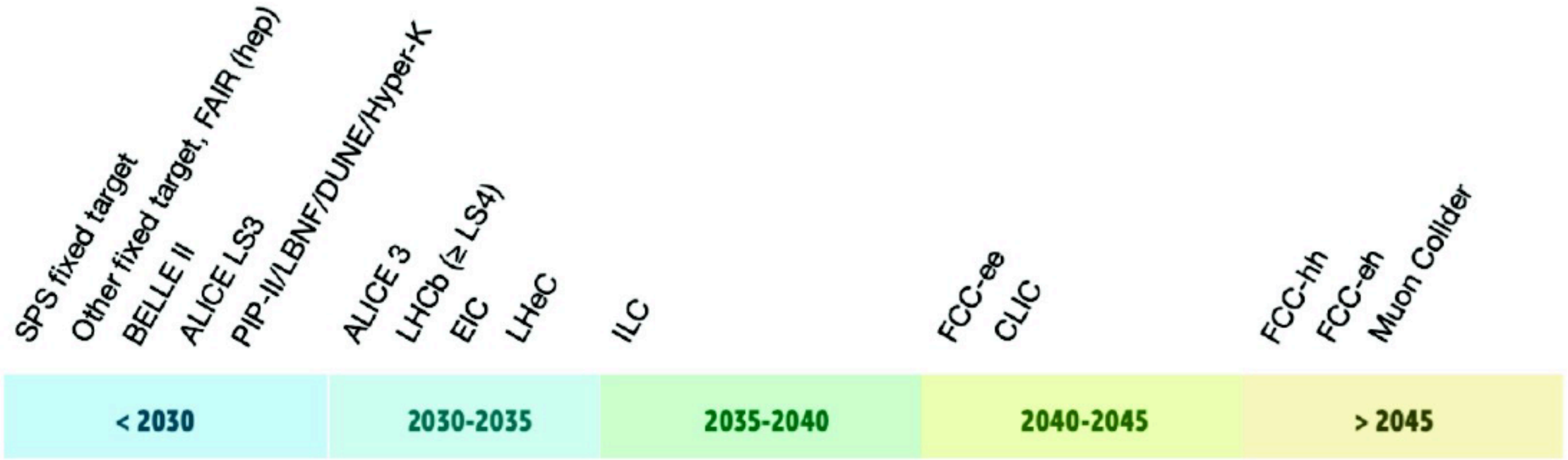
Some considerations

Some considerations

- Higgs factory detector R&D in the global R&D landscape

Future Projects Timeline

Agreed Working Hypothesis



- Funding for “future” projects and “blue sky” R&D is scarce

M. Vos

Some considerations

AIDAinnova project funded by EU H2020 programme
H2020-INFRAINNOV-2020-2, https://cordis.europa.eu/project/id/101004761

focus on Strategic R&D in the pre-TDR phase

++ Forces groups to collaborate with similar projects
-- Specific funding rather limited

Eventually, projects need ear-marked funding

M. Vos

Some considerations

- **Find and exploit synergies**
  - **Ongoing experiments upgrades**
    - **CMS&ATLAS timing detectors, CMS HGCAL, ALICE vertex upgrade, etc.**
  - **Existing detector R&D programs**
    - **AIDAinnova, CERN EP R&D, CALICE, CEPC detector R&D, other international and national funding programs, etc.**
- **Key4HEP is an excellent example of cross-experiment collaboration**
  - **SW experts from ILC, CLIC, CEPC, FCC, SCTF and more, all working together on its development**
- **We could have a similar approach to hardware technologies**
  - **Trackers, calorimeters, gas detectors, timing detectors, muon detectors, electronics, services, …**

Silicon trackers

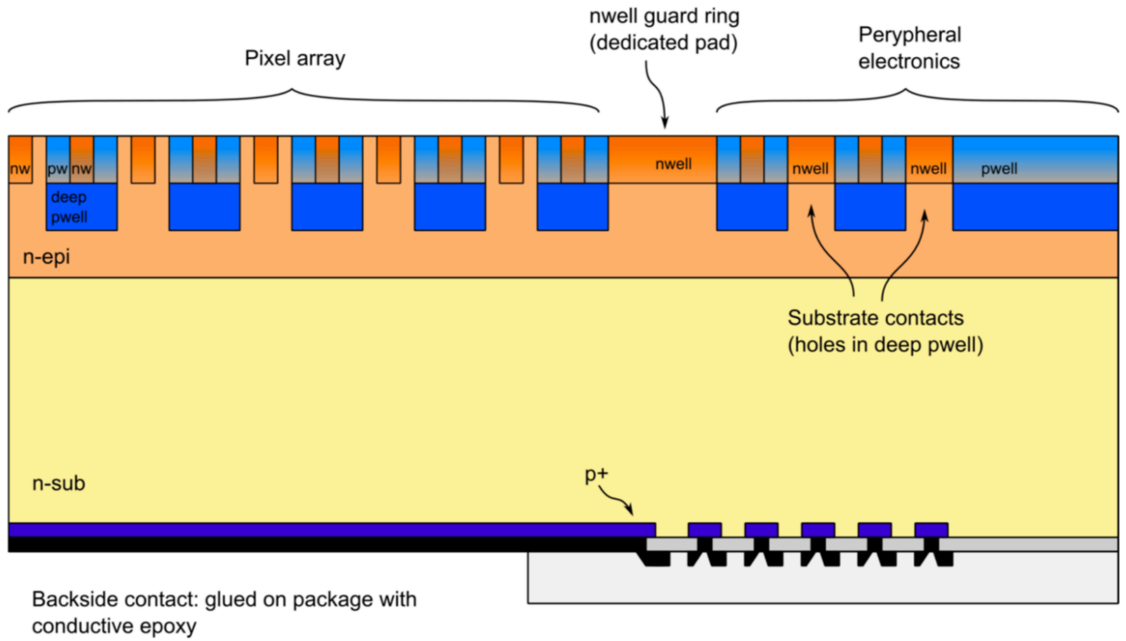
Silicon trackers

- A lot of R&D on MAPS detectors from many different groups
- Profits from some ongoing (or planned) upgrades of current experiments
- Strong move to:
  - Smaller pixel size
  - Thinner detectors (low material)
  - Flexible detectors (bent detectors)
  - Faster and better integrated electronics with low power dissipation
  - Smaller scale technology (55, 65 nm)
  - Very small services (micro-channel cooling, …)

Arcadia

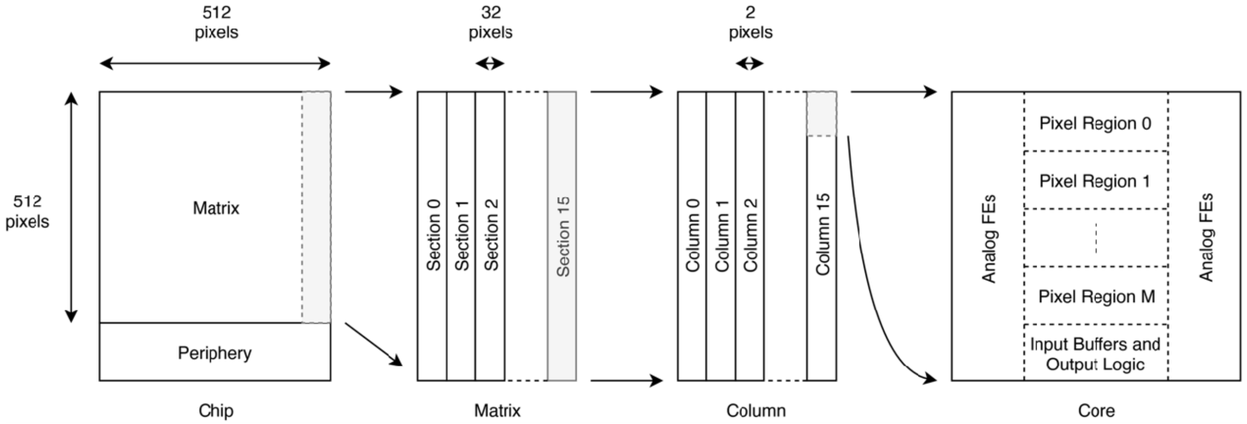
Creation of a novel platform for the implementation of innovative monolithic sensors compatible with standard CMOS fabrication processes

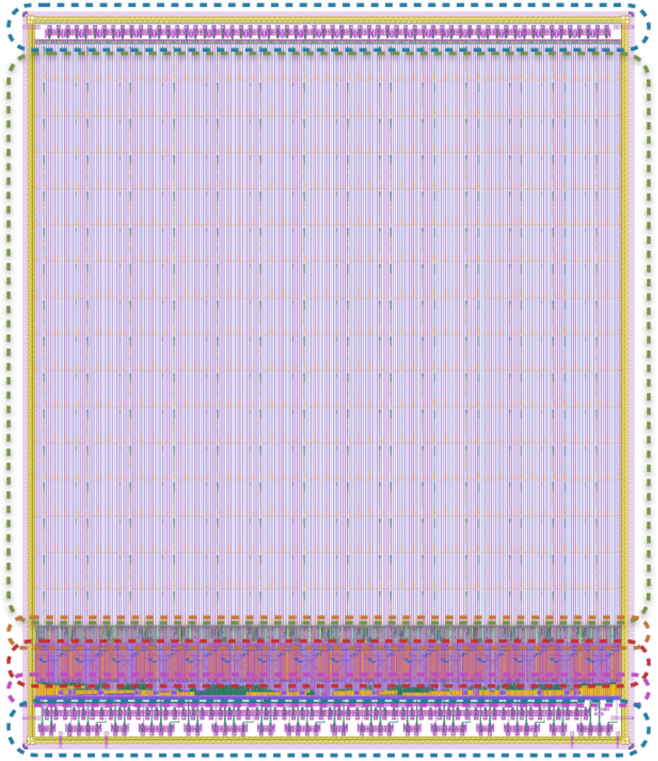
- Challenge: deployment of large-area system-grade CMOS sensors implementing scalable readout architectures with ultra-low power capability (O(10 mW/cm2))
- Technology: LFoundry 110nm CMOS node, quad-well, high-resistivity bulk
- Active sensor thickness in the range 50 µm to 500 µm
- Operation in full depletion with fast charge collection only by drift
- Small charge collecting electrode for optimal signal-to-noise ratio



M. Rolo

Arcadia MD-main demonstrator chip





Top Padframe
Auxiliary supply, IR Drop Measure

Matrix
512x512 pixels, Double Column arrangement

End of Sector (x16)
Reads and Configures 512x32 pixels

Sector Biasing (x16)
Generates I/V biases for 512x32 pixels

Periphery
SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe
Stacked Power and Signal pads

- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm² silicon active area, "side-abuttable"
- Triggerless binary data readout, event rate up to 100 MHz/cm²
- **First Engineering Run** (SPW) takeout 11/2020, **silicon being tested**
- **2nd full CMOS maskset** mid-2021, fab out expected January 2022
- **3rd SPW mid-2022** with design fixes, explorative sensor and CMOS designs, new architectures with higher data throughput, full chip demonstrator for fast timing (R&D on sensors and electronics already started with 2nd SPW)

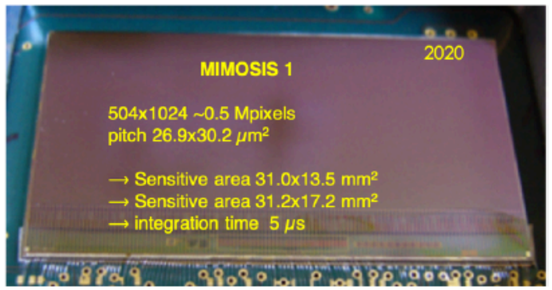
power consumption of 20 mW/cm² seems definitely reachable
demonstrator should provide the experimental confirmation

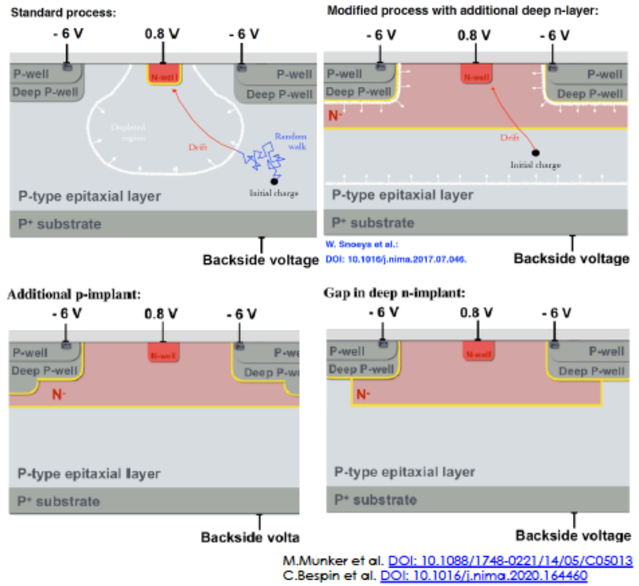
M. Rolo

Mimosis sensor

- Process: Tower 180nm
  - 2020: MIMOSIS-1 fabricated
  - 2021 (late): MIMOSIS-2 submission
  - >2022: final chip, MIMOSIS-3

- Sensing node
  - High resistive epitaxial layer (25 µm for MIMOSIS-1)
  - Benefits from process modification introduced by CERN
  - 2 Couplings collection node - Front-End
    - DC and AC for biasing > 20V (J.Heymes DOI: 10.1088/1748-0221/14/01/P01018)

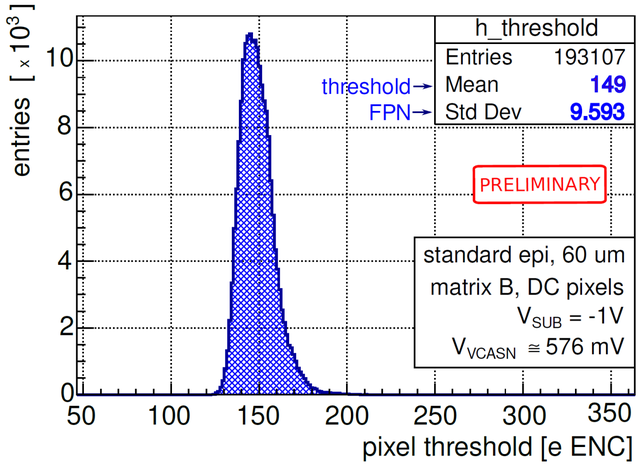




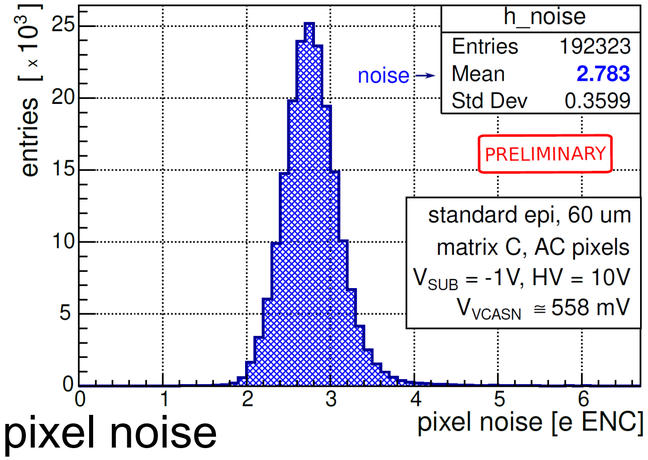
charge diffusion studies

Key studies:
depletion role in trade-off position res. / radiation tolerance

PIXEL THRESHOLD + FPN



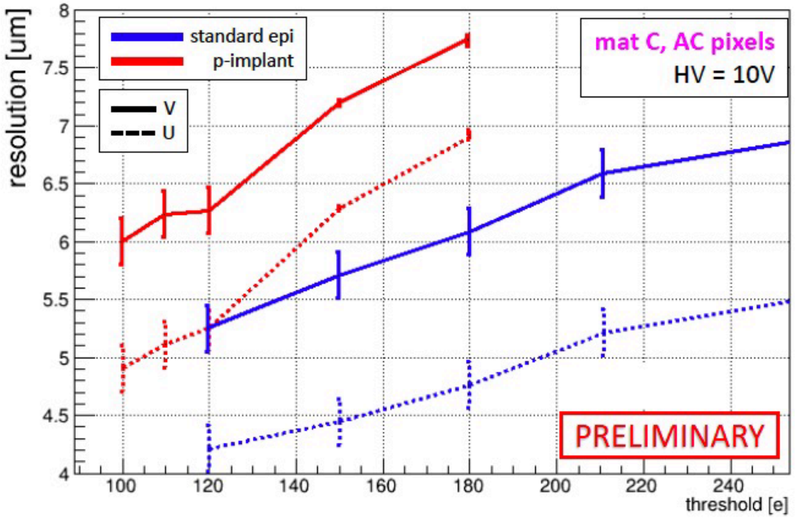
PIXEL NOISE



Low pixel noise

Position resolution

All results PRELIMINARY from R.Bugiel, TWEPP 2021

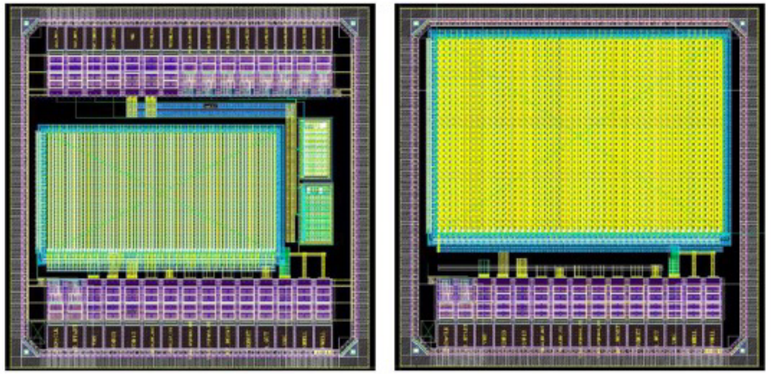


J. Baudot

CE-65nm sensors

Small pixel matrices

- Target: charge collection properties
- Parameter space exploration
  - Pitch 15 & 25 µm
  - Front-ends: source-follower / amplifier
  - Collection diode with
  - Standard and optimised process



Variants A/B/C Variant D

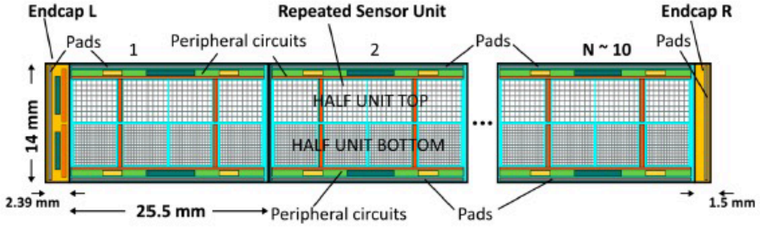
Ongoing studies on stitching

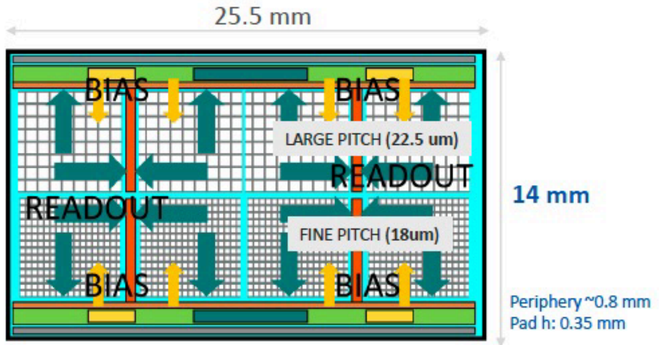
- Engineering run Q1 2022 in Tower-65 n
- Pixel pitch 18 / 23 µm to be confirmed

Very high granularity

MOSS Concept

(From G. Aglieri Rinella)





Key aspects

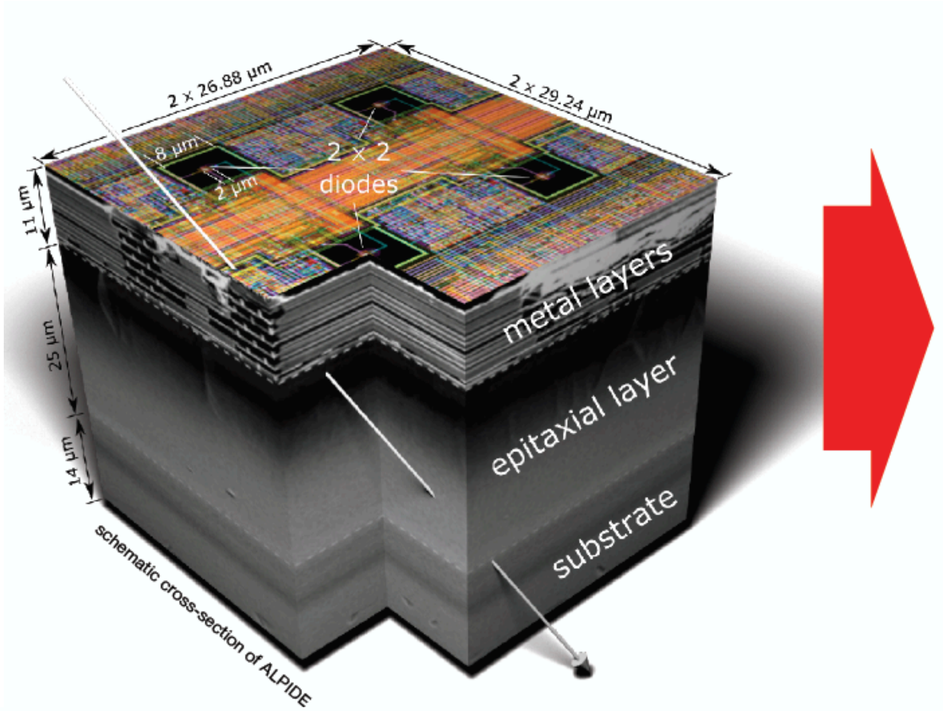
- Yield !
  - Power domain
- Power dissipation
  - 66 pJ to transmit 1 bit over 30 cm

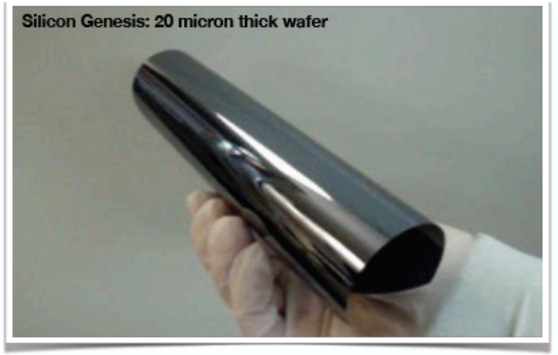
- Implement a large sensor abutting identical but functionally independent sub-units
  - Repeated Sensor Unit, Endcap Left, Endcap Right
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

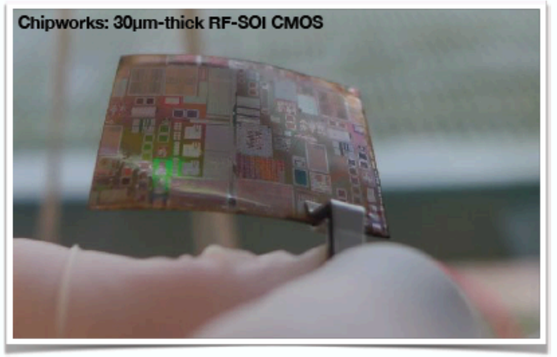
J. Baudot

Bendable MAPS in ALICE

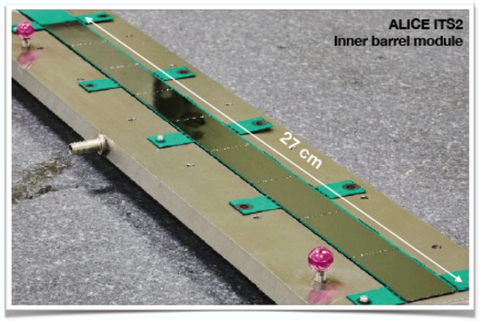
Make use of the flexible nature of thin silicon

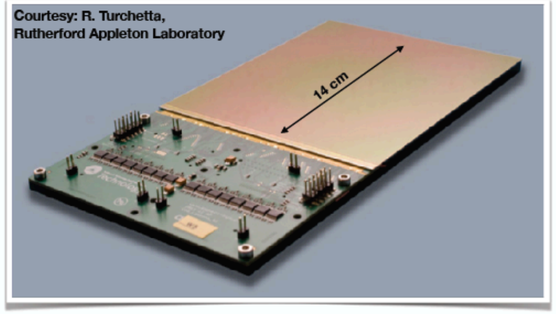




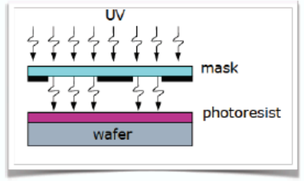


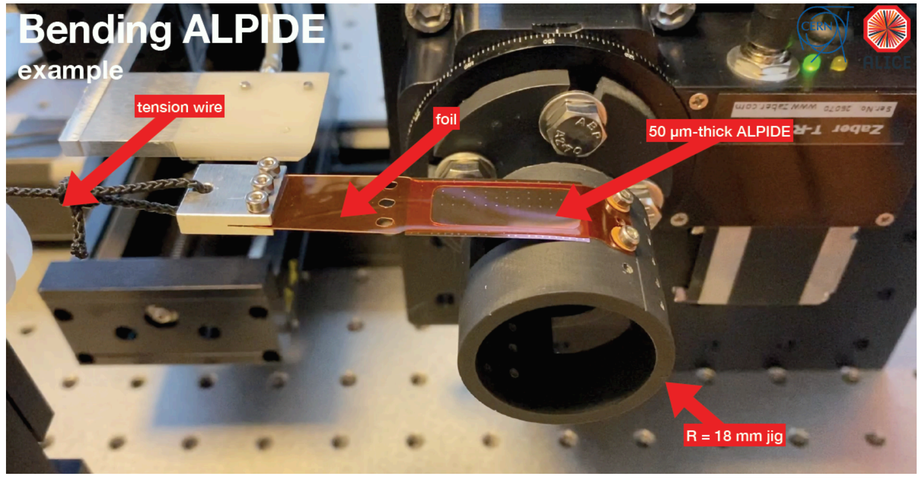
Build wafer-scale sensors





- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm²
  - modules are tiled with chips connected to a flexible printed circuit board
- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a sensor to equip a full half-layer
  - ***requires dedicated sensor design***

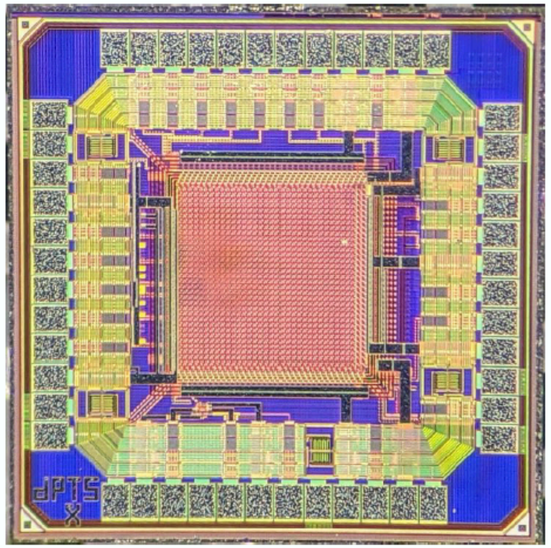




M. Mager

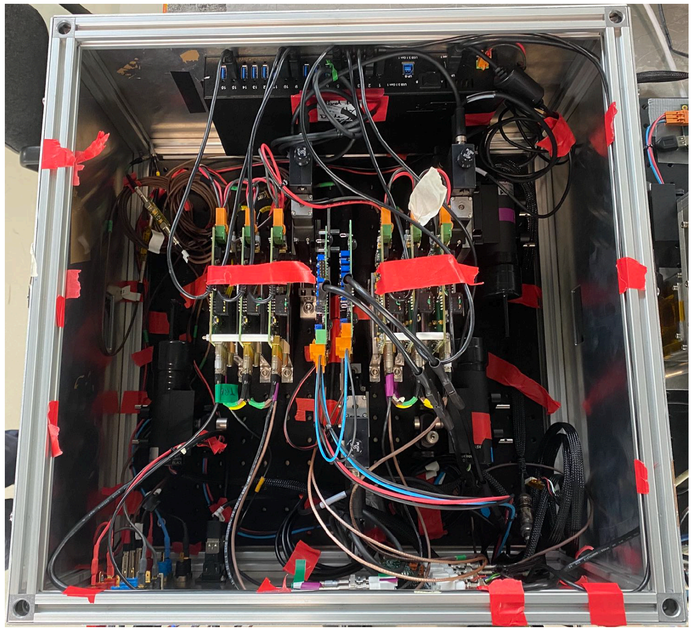
65nm prototypes, MLR1

- Most “aggressive” chip in MLR1
- 32 × 32 pixels, 15 µm pitch
  - sizeable prototype, allows for “easy” test beam integration
- Asynchronous digital readout with ToT information
- Allows to verify:
  - sensor performance
  - front-end performance
  - basic digital building blocks
  - SEU cross-sections of registers

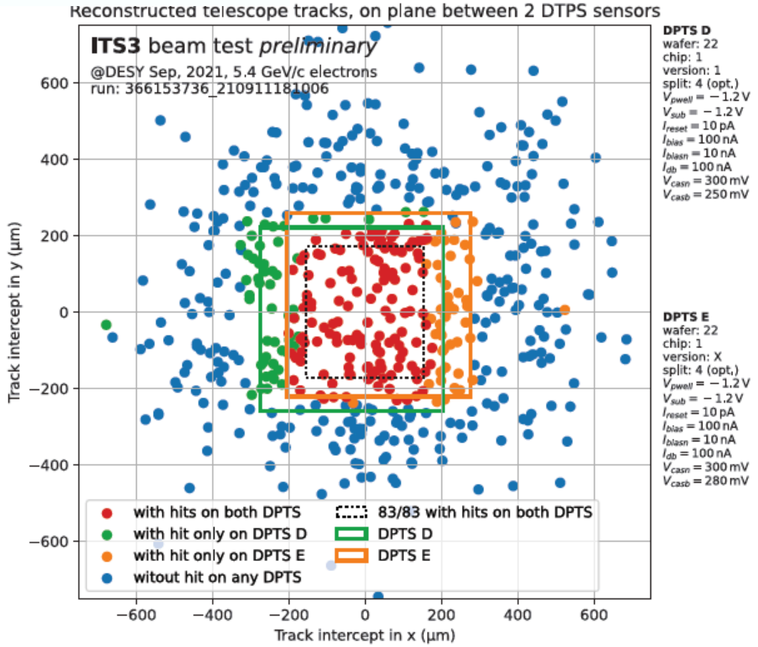


Digital Pixel Test Structure (DTPS)

Telescope with DTPS



DTPS test beam results

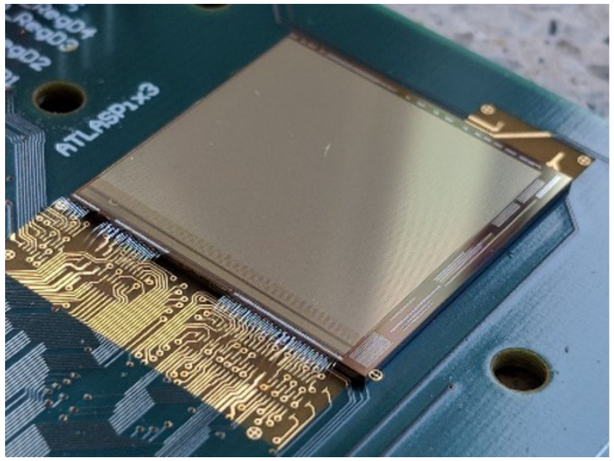


- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest
  - similar for second chip **(162/162)**
  - and even for both in coincidence **(83/83)**

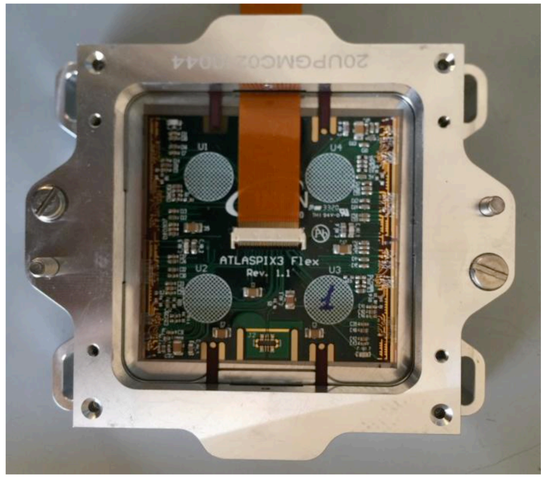
M. Mager

Tracker prototype overview

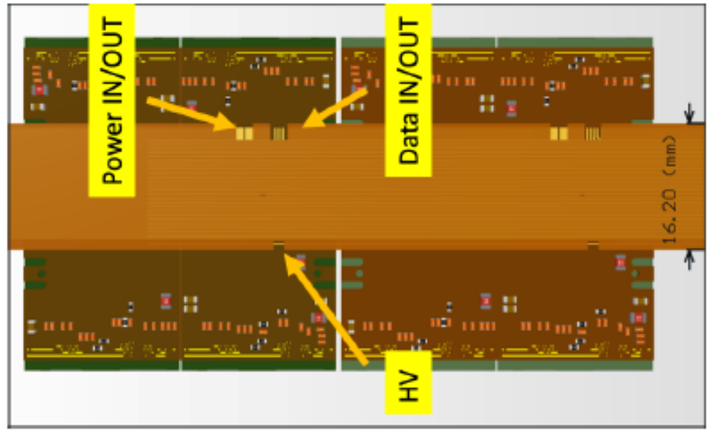
Single chip



Quad module



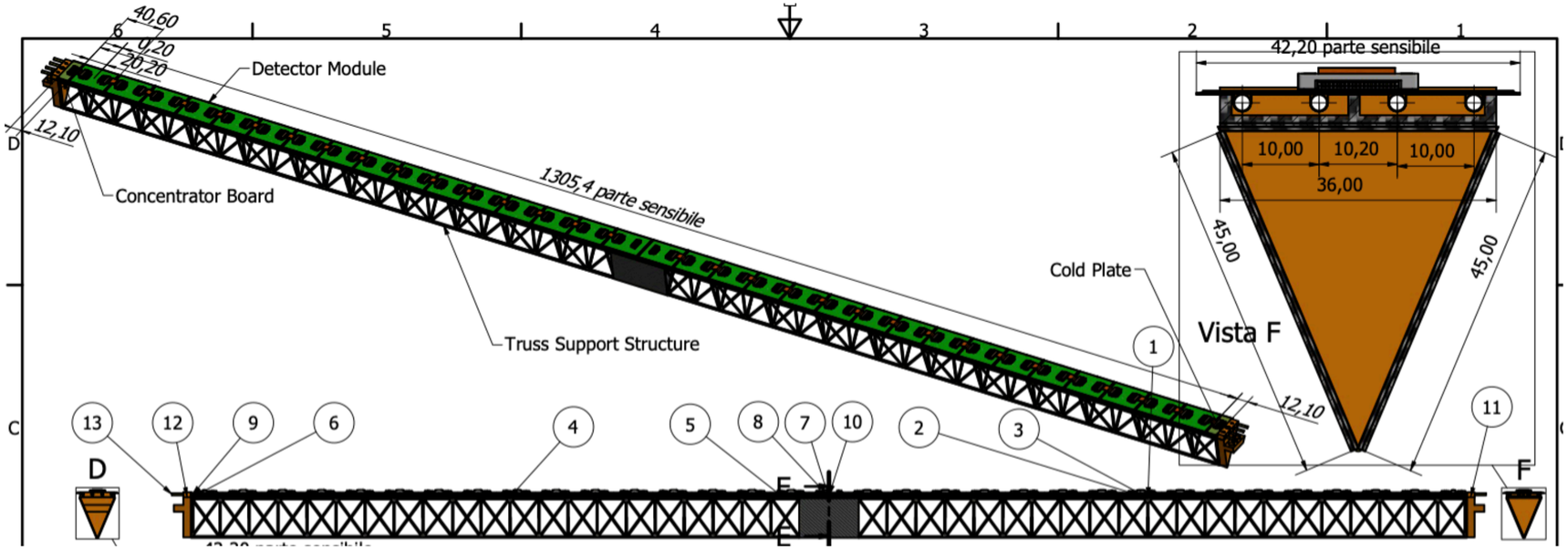
A serial powering chain (up to 16 quads)



ATLASPix3 collaboration

Long stave

~4cm×130cm



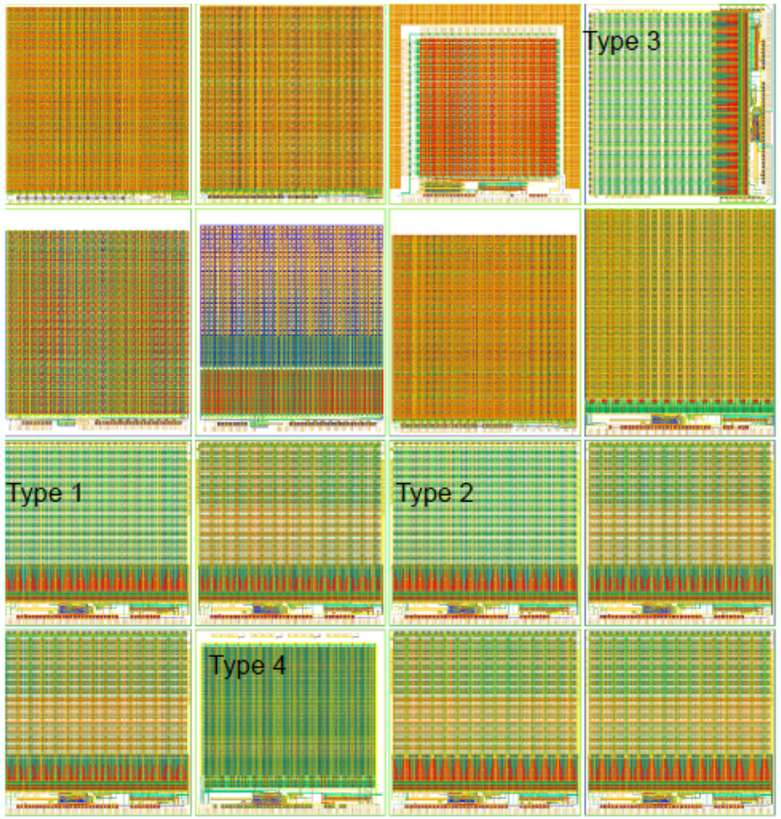
Y. Gao

Sensor design for electron colliders

ATLASPix3 collaboration

- New improved sensor designs suitable for tracking detectors for electron colliders
  - Joint engineering run with LHCb 2020
  - Several designs for CLIC, CEPC, DESY telescope upgrade (TELEPIX)
  - Pixels 25µm X 165µm, 25µm X 35µm
- Key improvements
  - Reduced pixel size
  - Different amplifier and comparator types
  - Reduced power consumption

Matrix	Pixel size µm	Pixel type	Amplifier	Comparator
1	25x165	HVCMOS	N/C MOS	NMOS
2	25x165	HVCMOS	N/P MOS	CMOS
3	25x165	HVCMOS	NMOS	distributed
4	25x35	DMAPS	NMOS	CMOS



Reticle map

Ivan Peric: UK-CEPC tracker workshop

Y. Gao

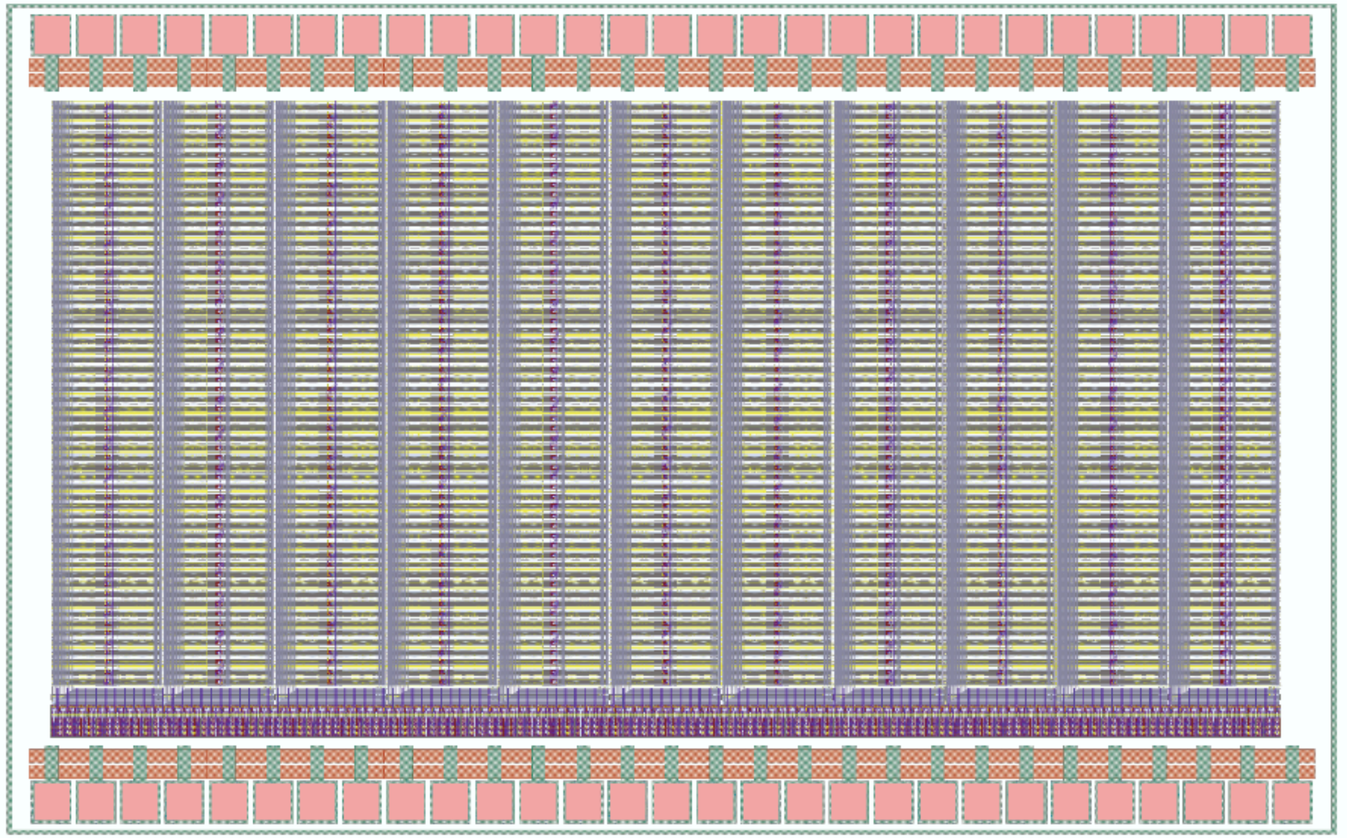
HV-CMOS sensor in 55nm technology

- We have started with design of the dedicated CEPC design in the HLMC 55nm HVCMOS technology
  - HLMC technology offers similar layers as TSI
- The test sensor should be submitted within an MPW run
- The run was originally planned for August 2021, it is postponed to March 2022
- An area of 3 x 2 mm is reserved for our design

ATLASPix3 collaboration

HLMC 上海华力微电子有限公司 Shanghai Huali Microelectronics Corporation

Chip layout

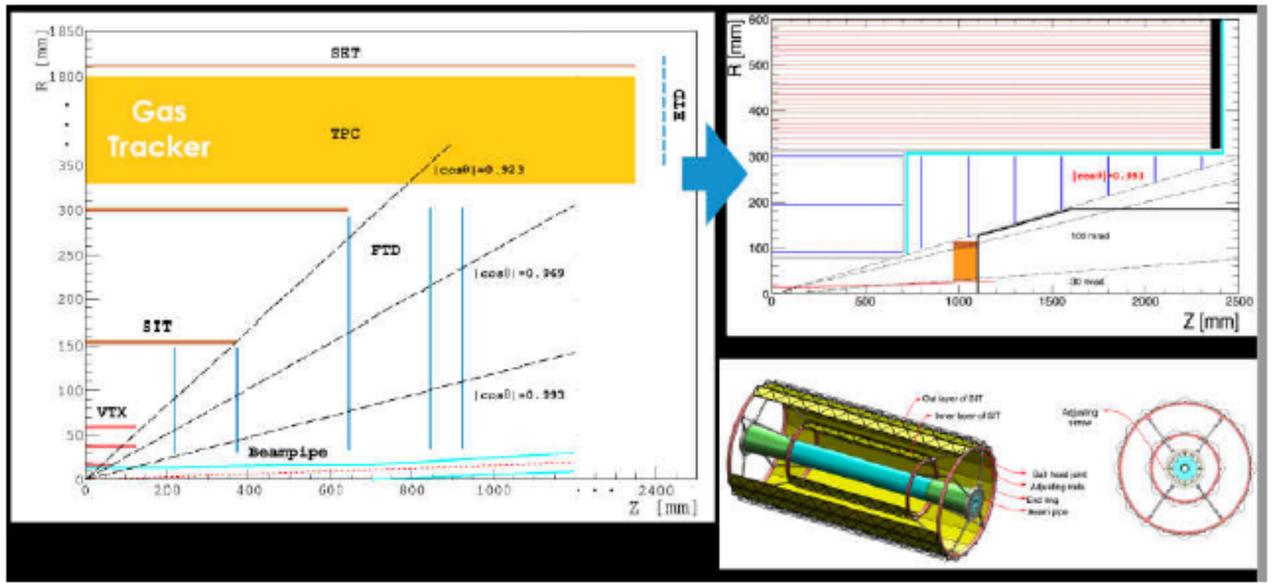


KIT
IHEP

Y. Gao

Silicon Tracker

Silicon tracker layout optimization and structure design

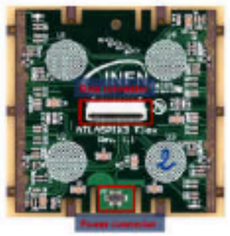


A big international effort

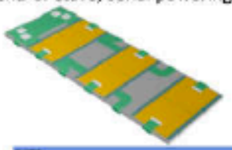
- Australia
  - University of Adelaide
- China
  - Harbin Institute of Technology
  - Institute of High Energy Physics, CAS
  - Northwestern Polytechnical University
  - Shandong University
  - T. D. Lee Institute – Shanghai Jiao Tong University
  - University of Science and Technology of China
  - University of South China
  - Zhejiang University
- Germany
  - Karlsruhe Institute für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisa e Università di Pisa
  - INFN Sezione di Torino e Università degli Studi di Torino
- UK
  - Lancaster University
  - Queen Mary University of London
  - STFC – Daresbury Laboratory
  - STFC – Rutherford Appleton Laboratory
  - University of Bristol
  - University of Edinburg
  - University of Liverpool
  - University of Oxford
  - University of Sheffield
  - University of Warwick

DEMONSTRATOR (SHORT STAVE)

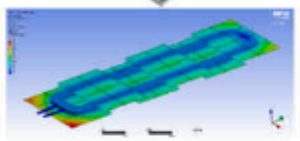
QuadModule Concept

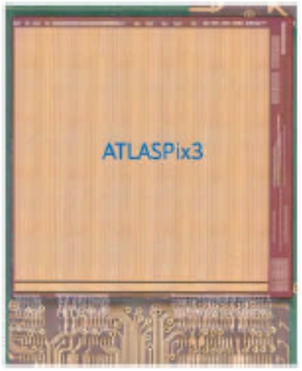


- Multiple modules on light composite support
  - Alternate tile pattern for hermeticity
  - Aggregation of data/optical conversion at the end-of-stave; serial powering

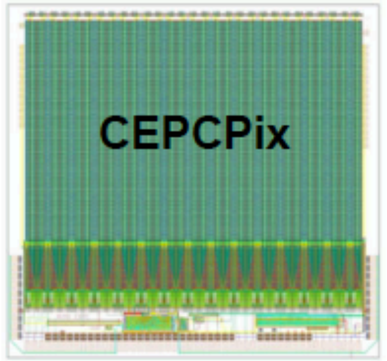


- Readout unit based on 4 chips
  - Shared services among 4 sensors by common power connections and configuration lines
  - Benefits of in-chip regulators to reduce connections





TSI 180 nm HV-CMOS



- Smaller pixel size (25μm) in φ direction
- Lower capacitance
- Amplifier and comparator design
- Electronics in pixel or periphery
- Daisy chain of readout

55 nm HV-CMOS

华虹集团 HUAHONG GROUP

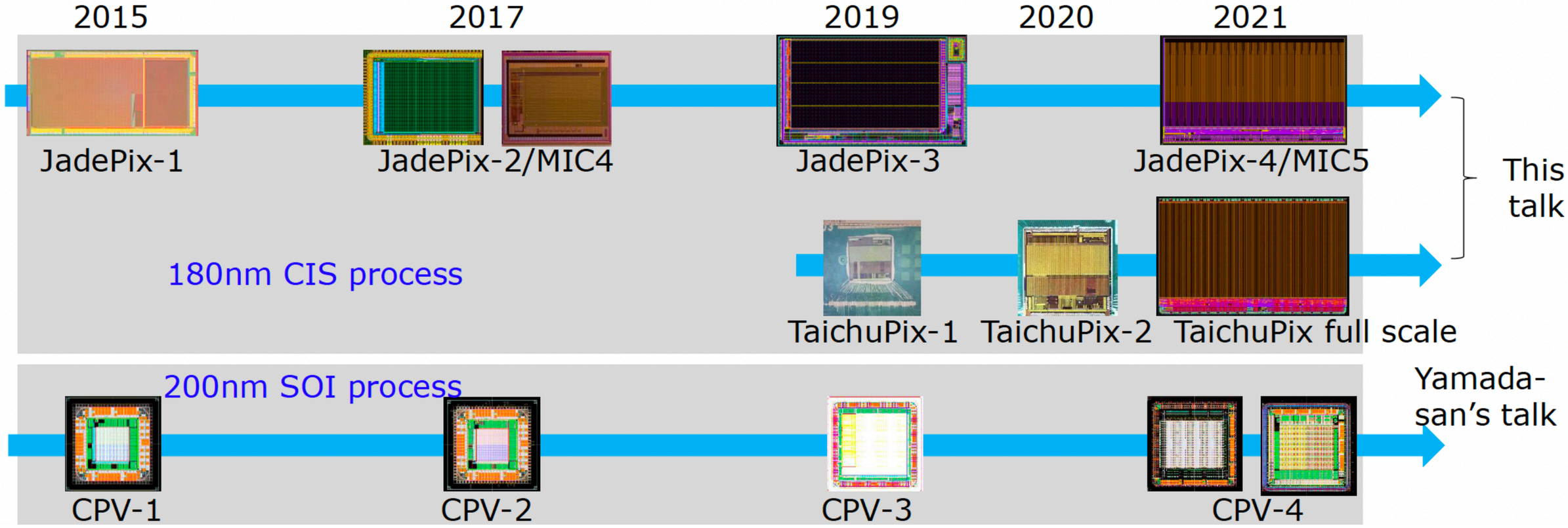
上海华力 HLMC

A Chinese foundry

J. Liu

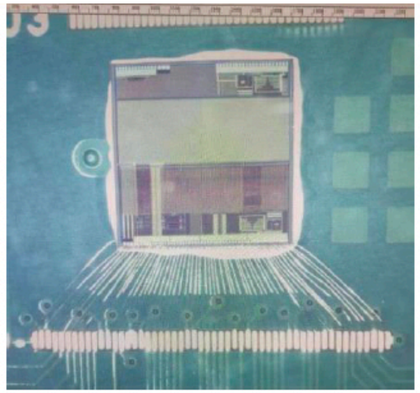
MAPS projects in China

- Development of pixel sensor for CEPC are supported by
  - Ministry of Science and Technology (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation

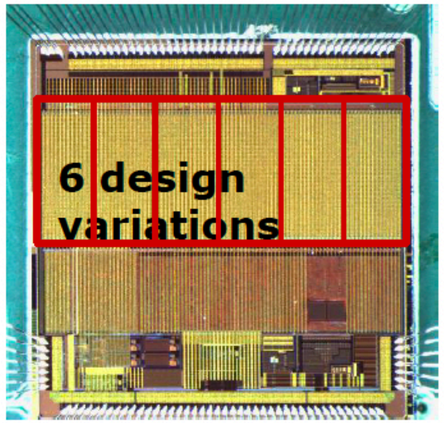


Y. Lu

MAPS project in China



TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm



TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the **data-driven readout**
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - **High speed data interface** up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

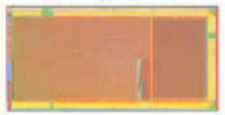
Y. Lu

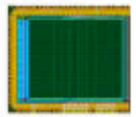
CMOS pixel sensors

	JadePix1 (2015)	JadePix2 (2017)	MIC4 (2017)	JadePix3 (2019)
Architecture	Roll. Shutter + Analog output	Roll. Shutter + In pixel discri.	Data-driven r.o. + In pixel discri.	Roll. shutter + end of col. priority encoder
Pitch (μm²)	33 × 33 /16 × 16	22 × 22	25 × 25	16 × 26 16 × 23.11
Power con. (mW/cm²)	--	--	150	~ 55* / <100
Integration time (μs)*	--	40-50	~3	~100
Prototype size (mm²)	3.9 × 7.9 (36 individual r.o)	3 × 3.3	3.1 × 4.6	10.4 × 6.1
Main goals	Sensor optimization	Small binary pixel	Small pixel + Fast readout+ nearly full functional	Smaller pixel + Low power + fully functional

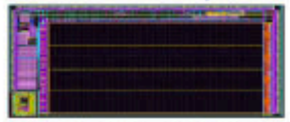
*Assuming a matrix of 512 ×1024 pixels

All prototypes in TowerJazz 180 nm process

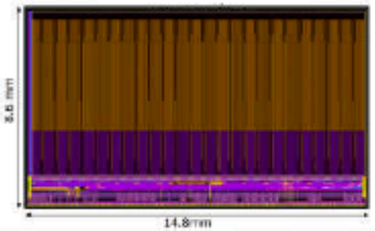

JadePix1 (IHEP)


JadePix2 (IHEP)


MIC4 (CCNU & IHEP)


JadePix3 (IHEP, CCNU, Dalian Minzu Univ., SDU)

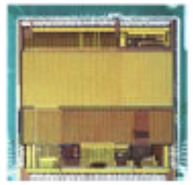
JadePix4



	S.P. resolution	Integration time	Average power
JadePix-4	<5 μm	~1 μs	< 100 mW/cm²
JadePix-3	<3 μm	<100 μs	< 100 mW/cm²

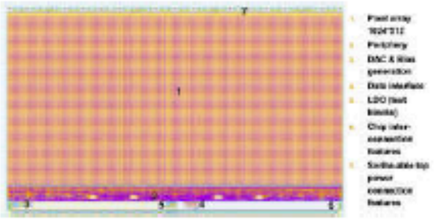
Optimized for fast readout

Taichupix1 / Taichupix2



Chip size: 5 mm × 5 mm
Pixel size: 25 μm × 25 μm

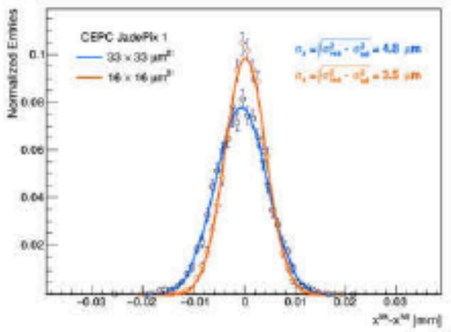
Full-size Taichupix



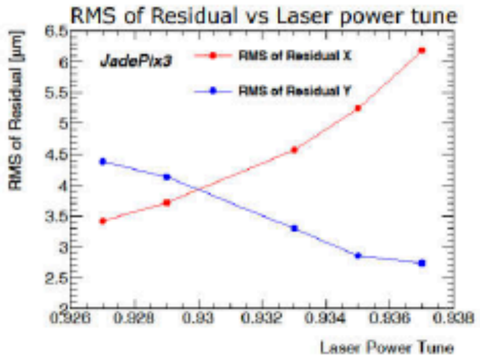
1024*512 pixel array, FE-I3-like

High speed, deadtime~50ns@40MHz,
time stamp precision 25/50ns

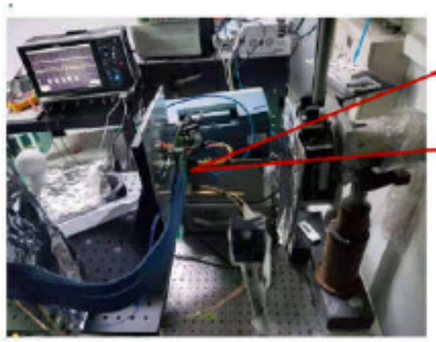
Beam test



Laser test



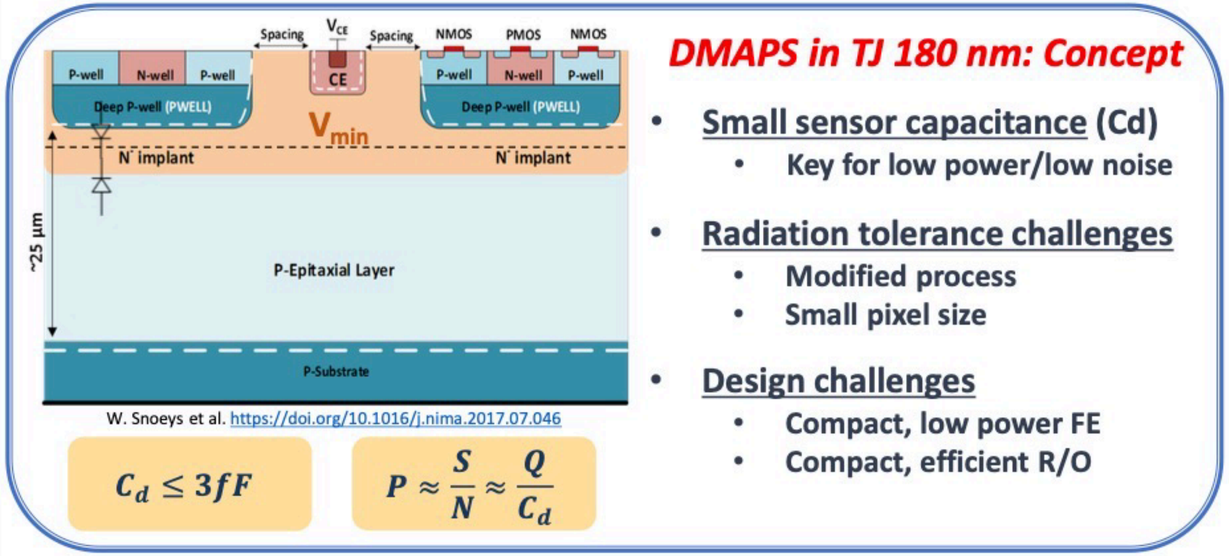
Radiation test



TaichuPix-2 exposed to 6 keV X-ray up to 2.5 Mrad and beyond

J. Liu

BELLE II vertex detector upgrade



W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

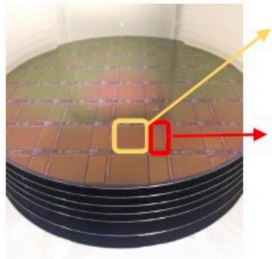
$C_d \leq 3fF$

$P \approx \frac{S}{N} \approx \frac{Q}{C_d}$

DMAPS in TJ 180 nm: Concept

- Small sensor capacitance (Cd)
  - Key for low power/low noise
- Radiation tolerance challenges
  - Modified process
  - Small pixel size
- Design challenges
  - Compact, low power FE
  - Compact, efficient R/O

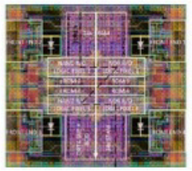
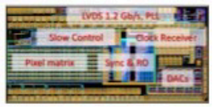
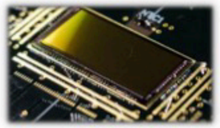
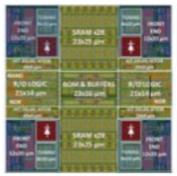
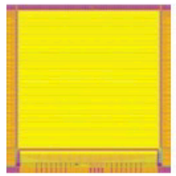
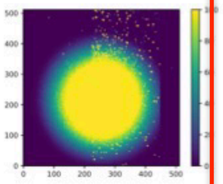
Large scale demonstrator chip development



- MALTA **Previous talk**
  - Asynchronous readout
- TJ-Monopix1
  - Synchronous column-drain R/O

- Process modification enhancements, Cz substrate ⟹ improved efficiency
- TJ-Monopix2: Improved full-scale DMAPS

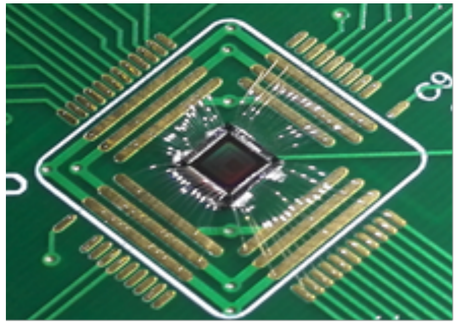
We are here now

TJ-Investigator characterization	*TJ-Monopix1* & MALTA Design	*TJ-Monopix1* & MALTA Submission	Mini-MALTA sub. with process fixes	*TJ-Monopix1* resub. process fixes & Cz	*TJ-Monopix2* & *MALTA2* Design	*TJ-Monopix2* & MALTA2 Submission	*TJ-Monopix2* Characterization	*"OBELIX"* Design
								Full scale System-ready: LDO, CDR, memory etc.
Q2 2016	Q4/2016	Q3/2017	Q3/2018	Q2/2019	Q2/2019	Q3/2020	Present	Future plans

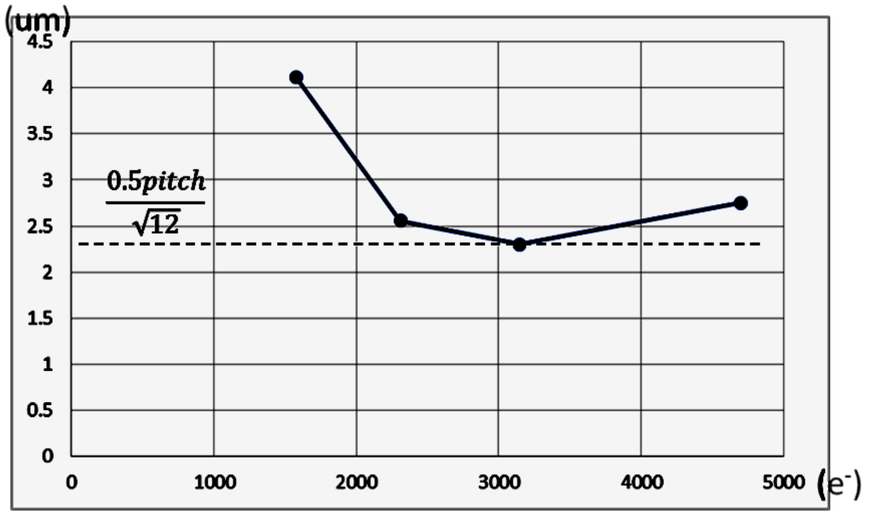
Tested several technologies: Thin DSSD, upgraded DEPFET pixel, SOI pixel, CMOS pixel

K. Nakamura

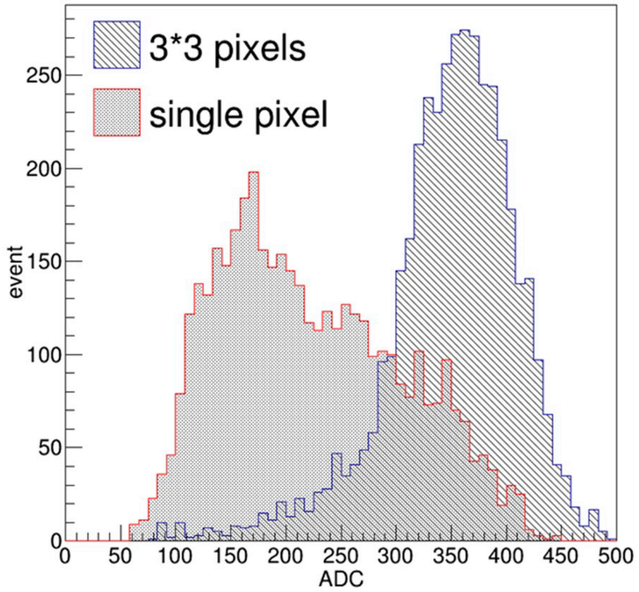
Silicon-On-Insulator (SOI) development



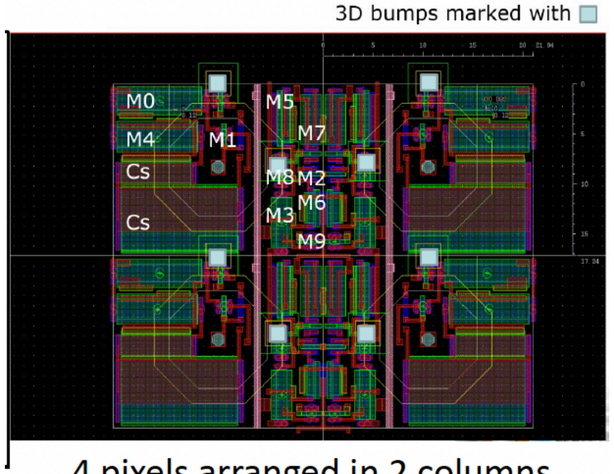
CPV-2 (2.9 x 2.9 mm^2) mounted on the PCB



σ of position residual at different laser beam intensity



Exploring the 3D technology with the CPV4 design



4 pixels arranged in 2 columns

pixel: 17 x 21 μm^2

M. Yamada

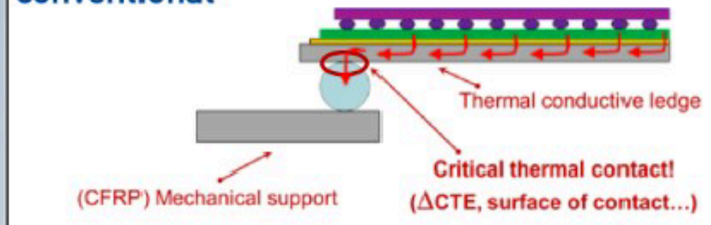
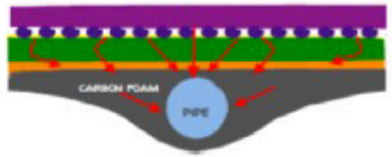
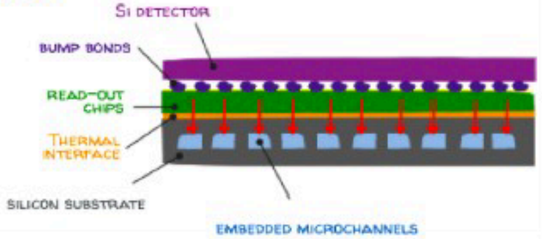
Micro-channel cooling

Minimize thermal resistance between heat source and heat sink

Crucial to keep FCChh detectors feasible within CO2 temperature range

Can also reduce the material involved in systems based on liquid or bi-phase coolant

$$TFM = \frac{(\Delta T \text{ fluid - sensor})}{\text{power density}}$$

approach	TFM
conventional 	20
integrated 	12
microchannels 	5-8 liquid 3 bi-phase

see P.Petagna, presentation, EIC tracking Workshop, Jul 24th 2018, A. Mapelli, presentation, 3rd FCC Physics and Experiments Workshop

M. Vos

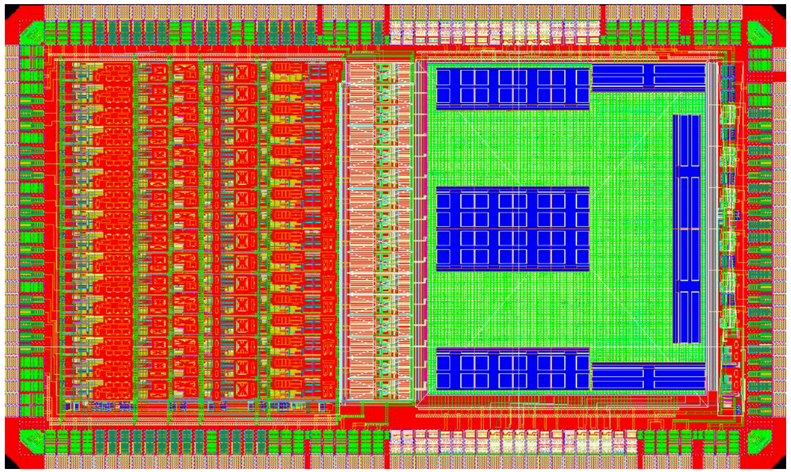
Gas Chambers

Gas central trackers

- The name of the game is low material
  - Achieve excellent momentum resolution
- TPC
  - Trying to solve the issues with the high-luminosity Z run
- Drift chambers
  - Gas mixtures lighter than air…
  - Offer also outstanding PID, especially using dN/dx
- 4th detector concept has a bit of both worlds:
  - Silicon tracker complemented with a
  - Drift chamber for improved PID

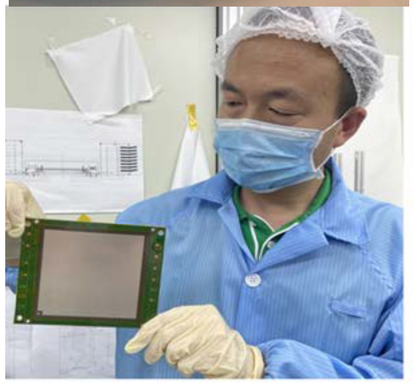
TPC R&D

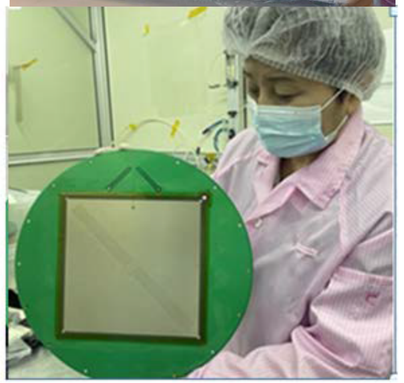
WASA_V1 ASIC layout



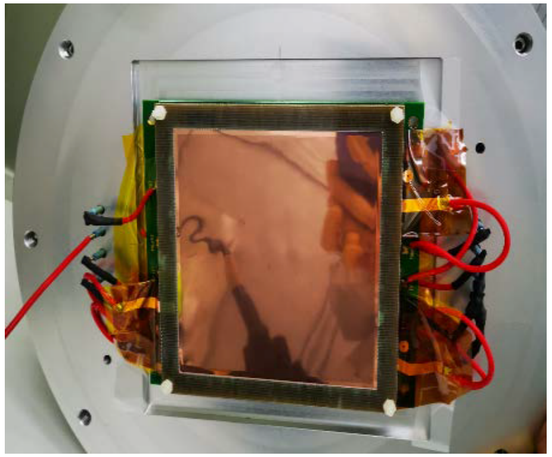
The power consumption is 2.33 mW/channel

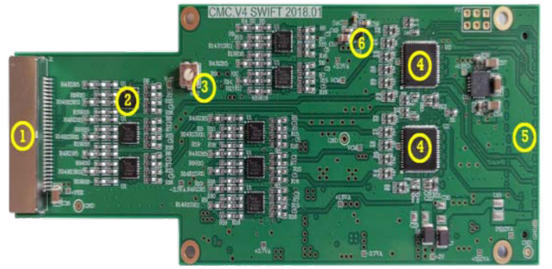
MicroMegas production in 2021





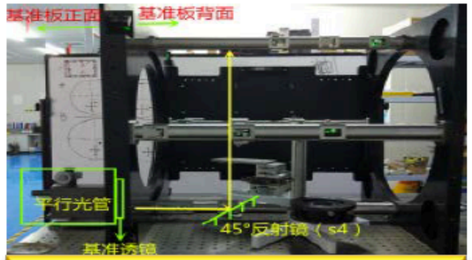
Detector and ASIC





Motivation for pixelated TPC

- Cluster counting
- Improved measurements for low angle tracks
- Improved double track separation
- Reduced hodoscope effect
- Lower occupancy
- Fully digital readout



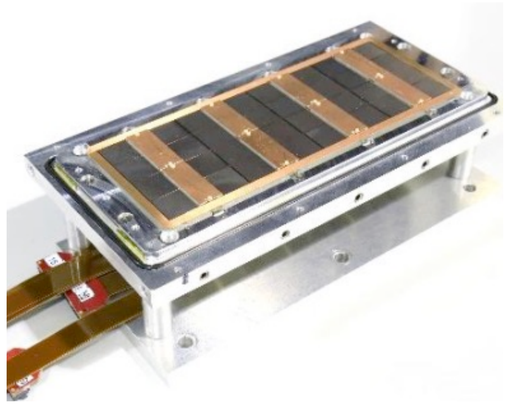
Pad TPC Prototype at IHEP 2015-2021

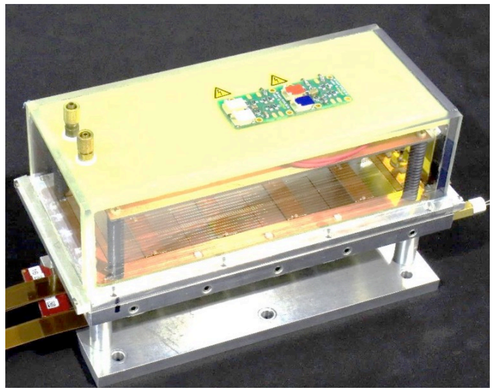
R&D

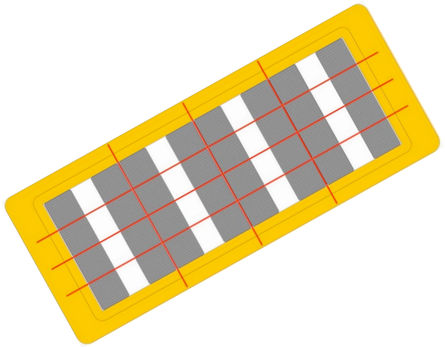
J. Liu

Pixelated TPC

8-QUAD module with field cage

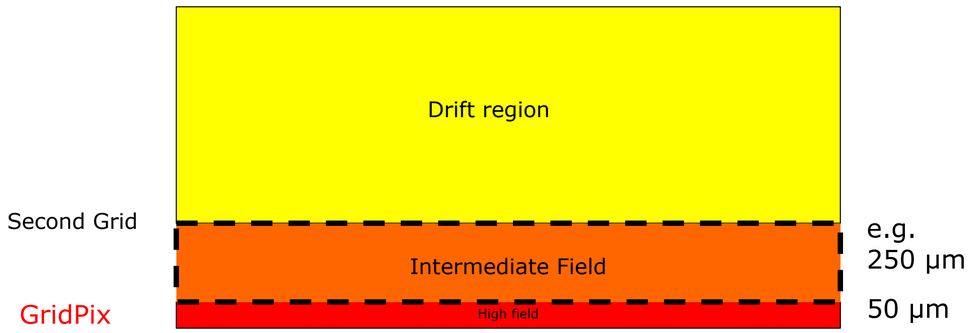






The Ion back flow can be reduced by adding a second grid to the device.
It is important that the holes of the grids are aligned. The Ion back flow is a function of the geometry and electric fields. Detailed simulations – validated by data - have been presented in LCTPC WP #326.
With a hole size of 25 μm an IBF of 3×10^{-4} can be achieved and the value for IBF*Gain (2000) would be 0.6.
Well below the specifications (<4).

Plan to test this idea



Ion backflow	Hole 30 μm	Hole 25 μm	Hole 20 μm
Top grid	2.2%	1.2%	0.7%
GridPix	5.5%	2.8%	1.7%
Total	12 10^{-4}	3 10^{-4}	1 10^{-4}
transparency	100%	99.4%	91.7%

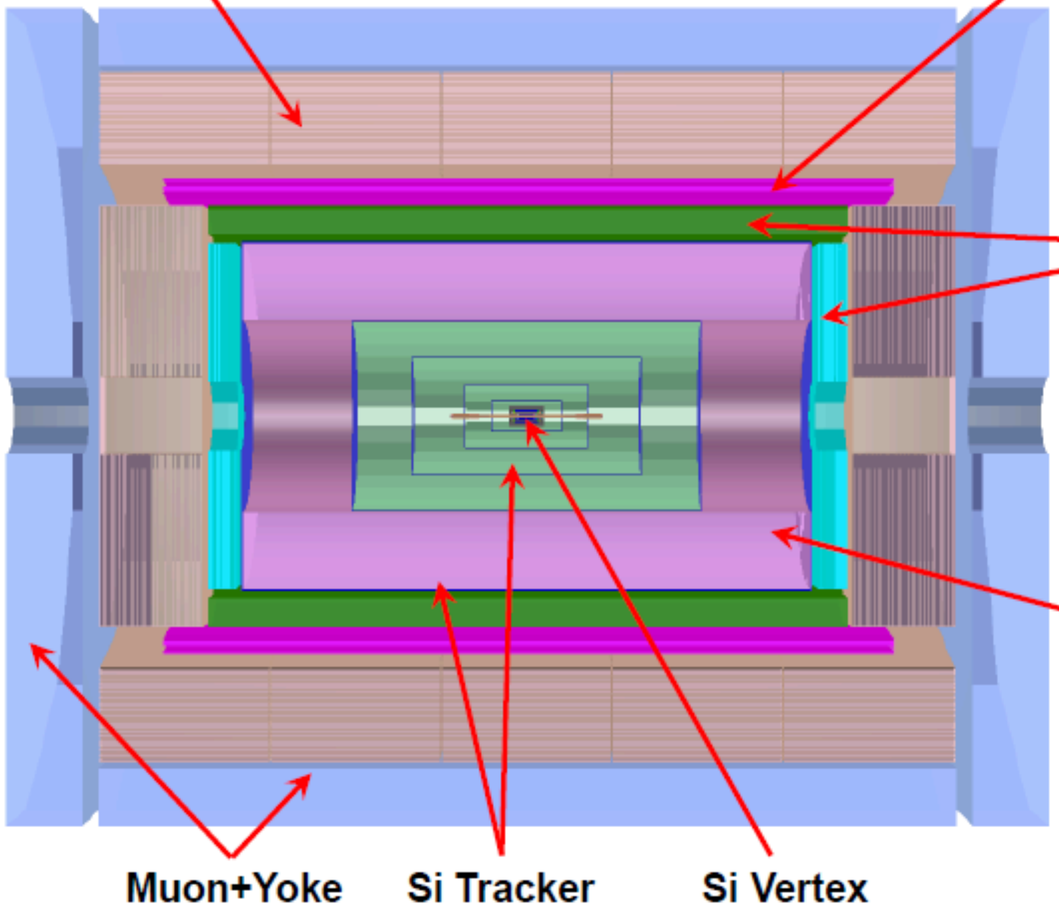
P. Kluit

The 4th detector concept

Scint Glass PFA HCAL

Advantage: Cost efficient, high density

Challenges: Light yield, transparency, massive production.



Solenoid Magnet (3T / 2T) Between HCAL & ECAL

Advantage: the HCAL absorbers act as part of the magnet return yoke.

Challenges: thin enough not to affect the jet resolution (e.g. BMR); stability.

Transverse Crystal bar ECAL

Advantage: better π^0/γ reconstruction.

Challenges: minimum number of readout channels; compatible with PFA calorimeter; maintain good jet resolution.

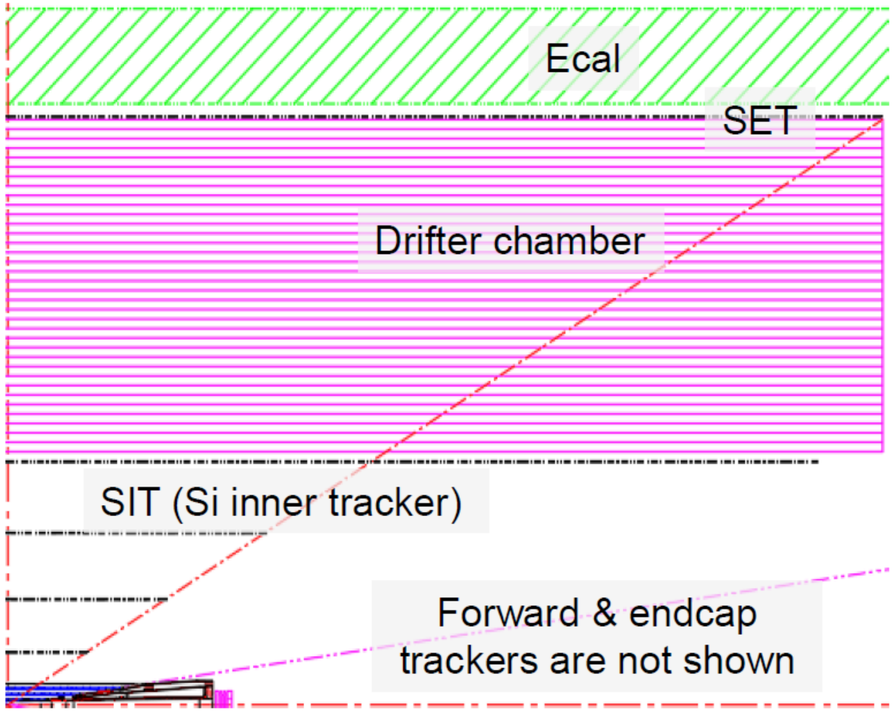
A Drift chamber that is optimized for PID

Advantage: Work at high luminosity Z runs

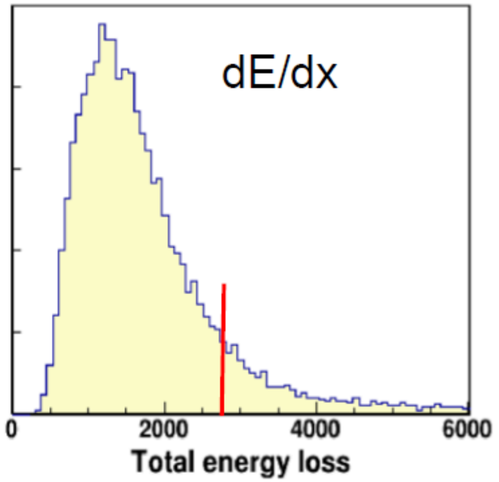
Challenges: sufficient PID power; thin enough not to affect the moment resolution.

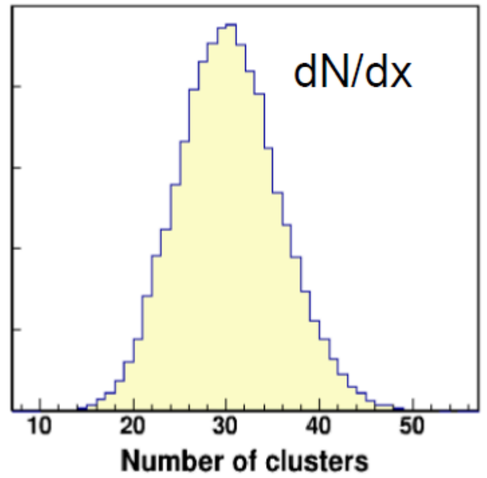
S. Xin

4th detector concept's Drift chamber



A drift chamber (DC) placed between the Full Silicon Tracker (FST) layers, optimised for PID

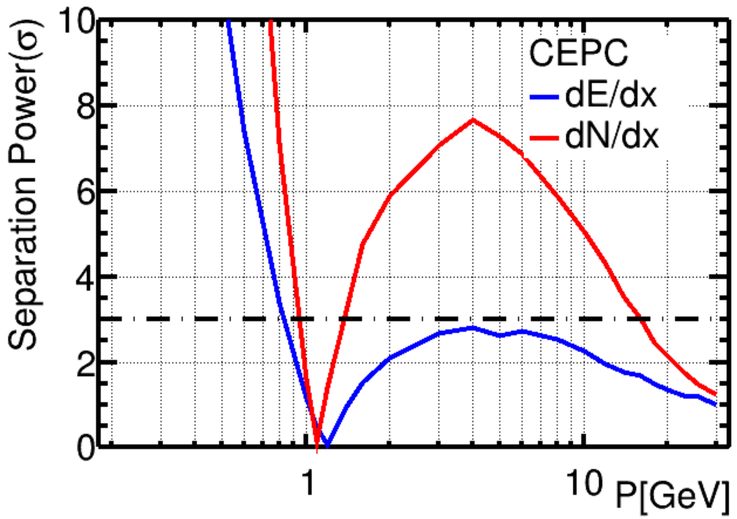




- PID optimization requirement:
  - Low sampling track length L
  - Large primary ionization density ρ_{cl}
  - High cluster counting efficiency ε

dN/dx resolution

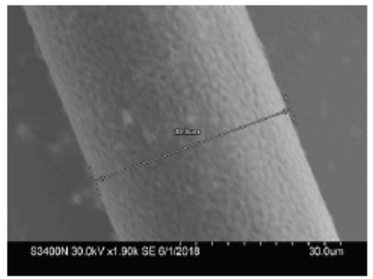
$$\frac{\sigma_{dN/dx}}{dN/dx} \propto \frac{1}{\sqrt{L * \rho_{cl} * \varepsilon}}$$



S. Xin

IDEA Drift chamber: R&D program

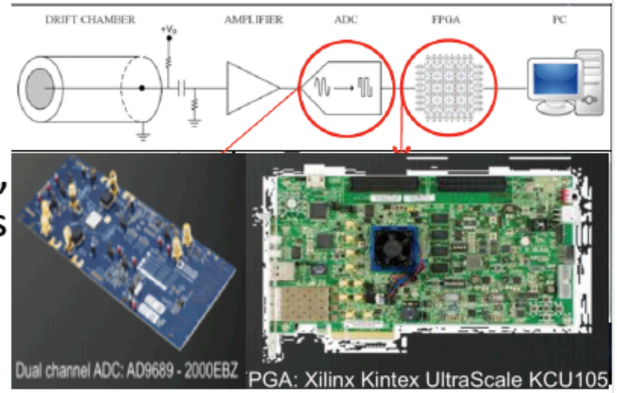
35 µm C wire – Cu coated



- Studies on new materials for DCH wires → metal coated Carbon monofilaments to operate with safer wire tensions far away from the elastic limit (e.g. : a tension $T_c \geq 250$ N needs to be applied to 35µm C monofilament, but elastic limit is 830 N)

- Studies on new polymeric fibers for DCH envelopes → (e.g. conductive polymeric matrices) to strongly reduce gas permeability (Helium), to enhance electrical conductivity for electrostatic and radiofrequency shielding, to improve the transparency

- Front-end, DAQ and pre-processing electronics for cluster counting → FEE: wideband (1 GHz) amplifier (25 dB) low mass, low power, low noise, multichannel (×8) ASIC, 12 bit & 2 GSa/s digitizers, multi-channel (16/32) FPGA for filtering and data reduction



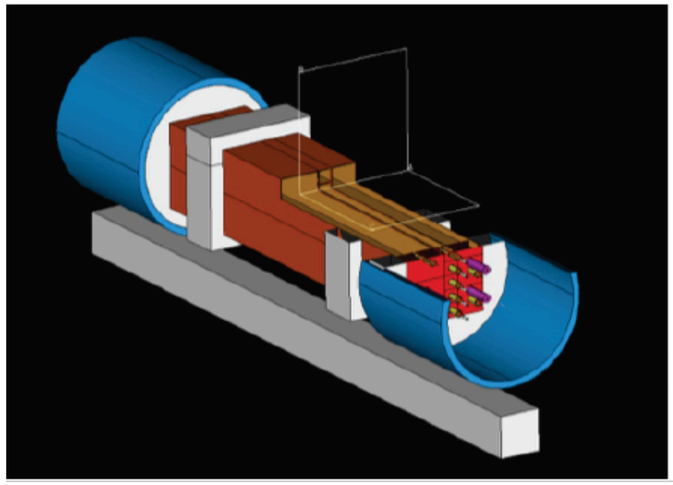
- Construction of scale 1:1 prototypes → to test the proposed innovative solutions for new materials

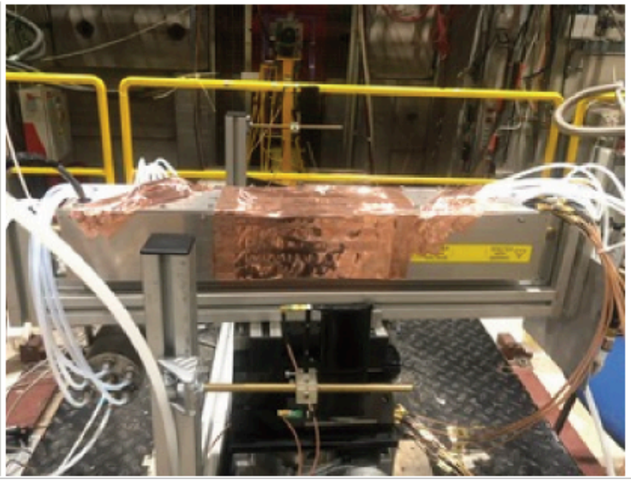
- Test beam facilities with identified beams of $e/\mu/\pi/K/p$ in the range 1-50 GeV/c → to experimentally determine the particle identification capabilities in the relativistic range

M. Primavera

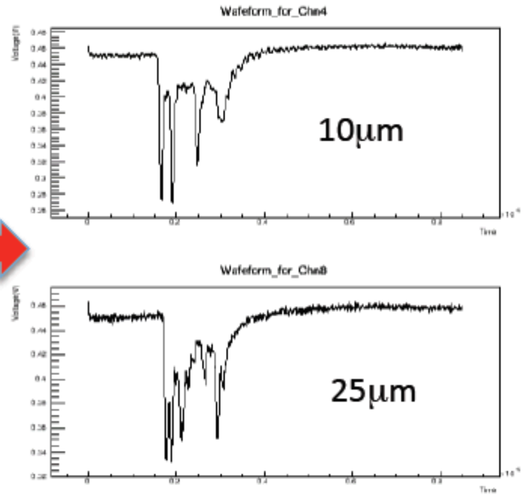
IDEA Drift chamber: R&D program

- Beam test in parasitic mode (we could be main user in spring 2022) now ongoing at CERN (H8) with drift tubes :
  - @fixed muon momentum → N_{cl} versus cell size (1x1cm^2, 2x2cm^2, 3x3cm^2), gas mixture (90/10 to 75/25 He/iC_4H_{10}), gas gain (1x10^5 to 5x10^5), sense wire diameters (15, 20, 25, 30 μm), angle between track and wire (0°, 30°, 45°, 60°) → **measure counting efficiency vs cluster density, estimate cluster size distribution, study number of clusters versus space charge effects**
  - @muon momentum scan (few GeV/c to about 250 GeV/c, $\beta\gamma = 40 \div 1800$) and having chosen optimal conditions (gas mixture, gain, sense wire diameter, etc.) → **measure relativistic rise** both for dE/dx and dN_{cl}/dx and use the experimental results to fine tune simulation for flavor physics and for jet flavor tagging (both in fast and in full simulation)
  - test and optimize counting algorithms





1x1cm^2



M. Primavera

Timing detectors

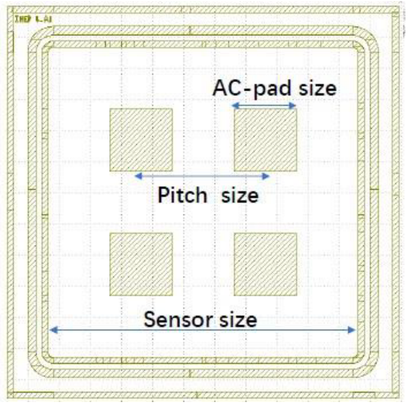
Timing detectors

- Timing detectors are used to improve PID
- Timing resolutions once unthinkable (<30 ns) are becoming a reality
- CMS and ATLAS are paving the way with large timing detectors for their Phase 2 upgrades
- Fast detectors under consideration at CEPC:
  - LGAD
  - MRPCs

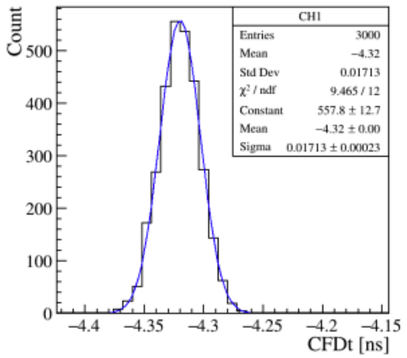
LGAD development at IHEP

AC-LGAD sensors developed by IHEP

Sensors	Sensor size [μm]	AC-pad size [μm]	Picth size [μm]
1-A7	1000	100	450
2-A2	2000	300	1200
2-A1	2000	600	1200
2-A3	2000	750	1000
4-A1	4000	1000	2000



- The timing resolution is about 15-17 ps (Laser testing)
- Almost no difference for different size of the pads



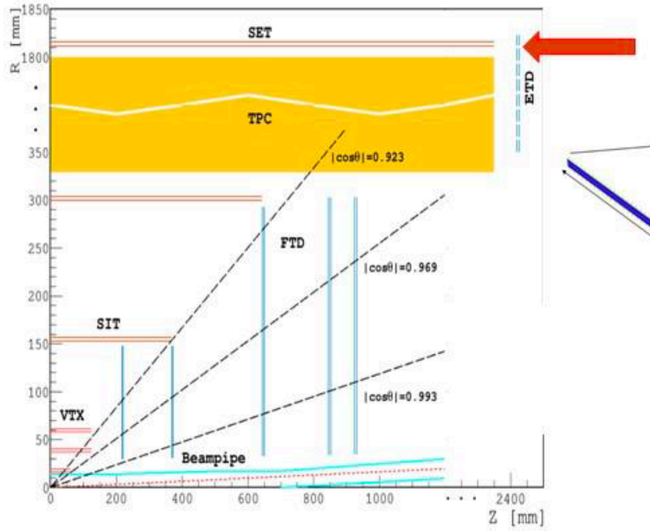
Sensors	Pad-pitch (μm)	Timing resolution (ps)
1-A7	100-450	15
2-A2	300-1200	16
2-A1	600-1200	17
2-A3	750-1000	17
4-A1	1000-2000	17

From laser test results, the pad size may not affect the time resolution of the AC-LGAD.

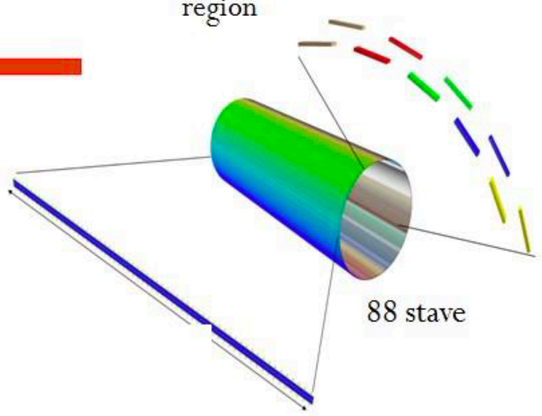
Beam testing should be done to check the real spatial and timing resolution.

Outer Si tracker for CEPC?

Baseline detector concept in CDR

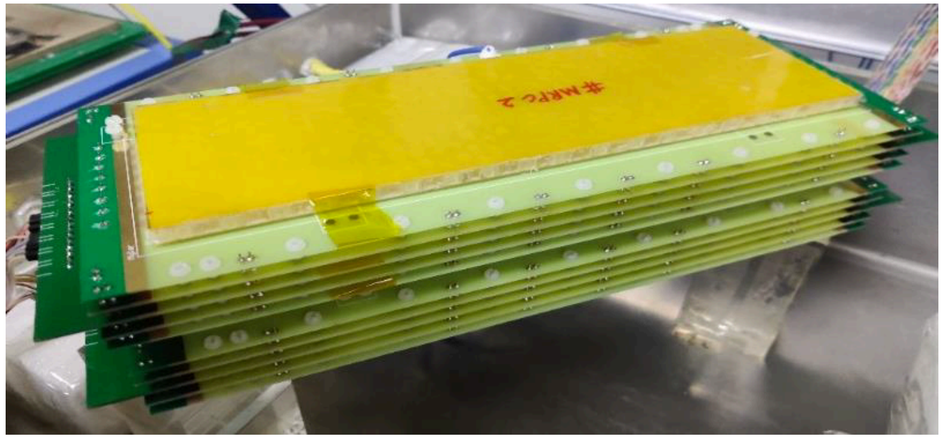


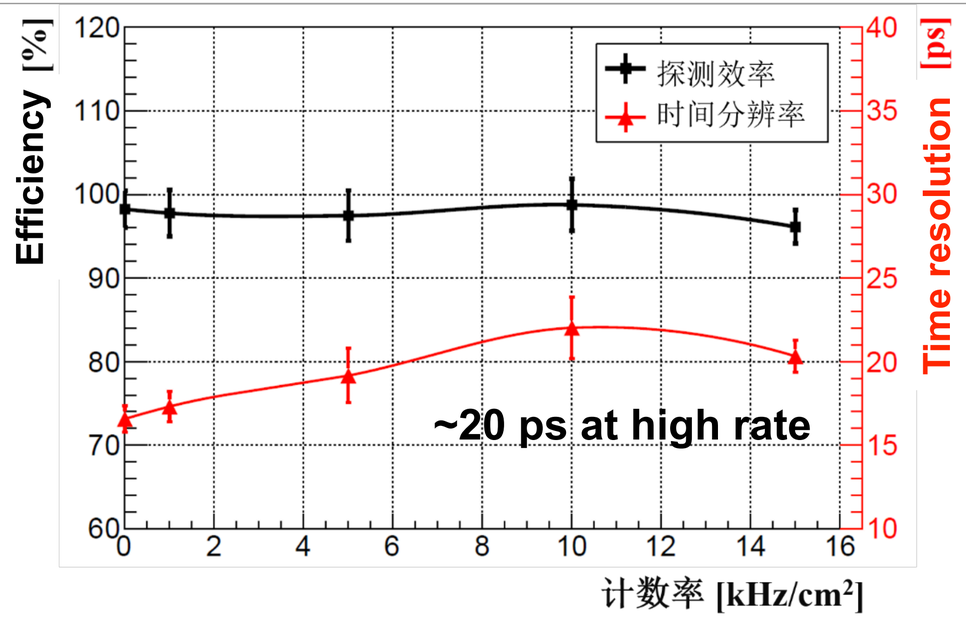
Timing detector in Barrel region



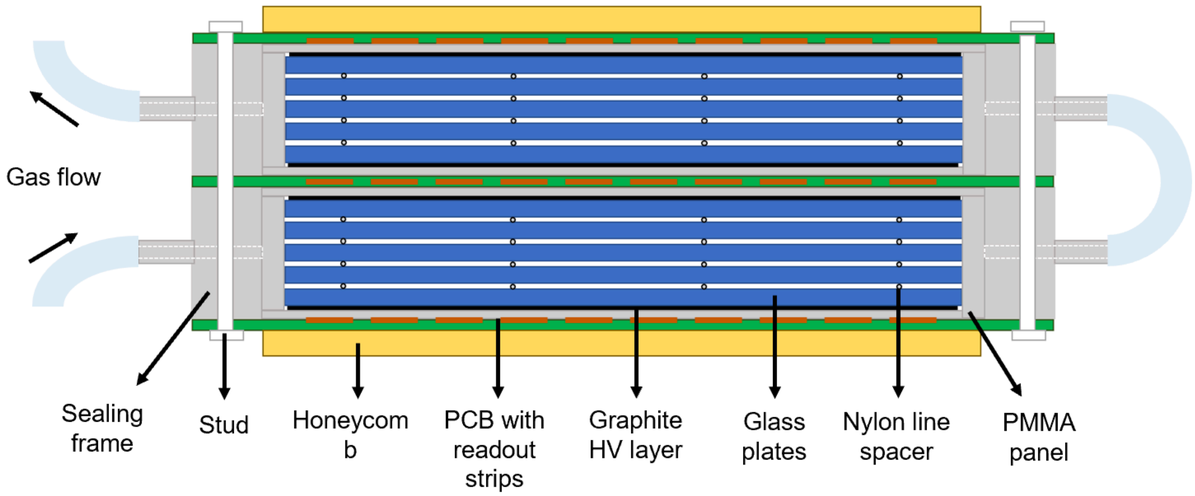
M. Zhao

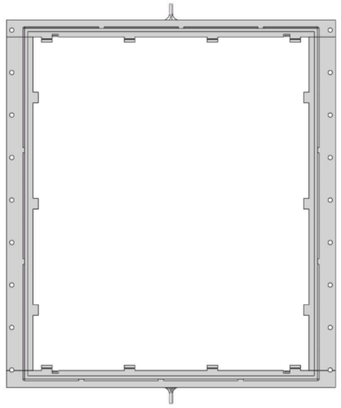
MRPCs

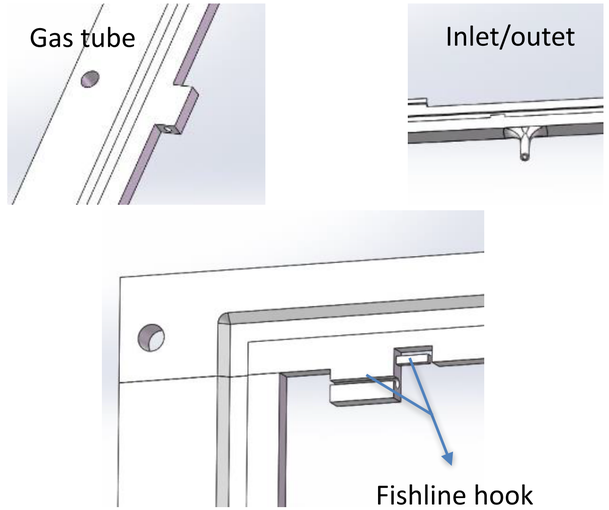




Sealed MRPC







Sealed MRPC will be used for CEE-e TOF (2024)

B. Wang, W. Yi

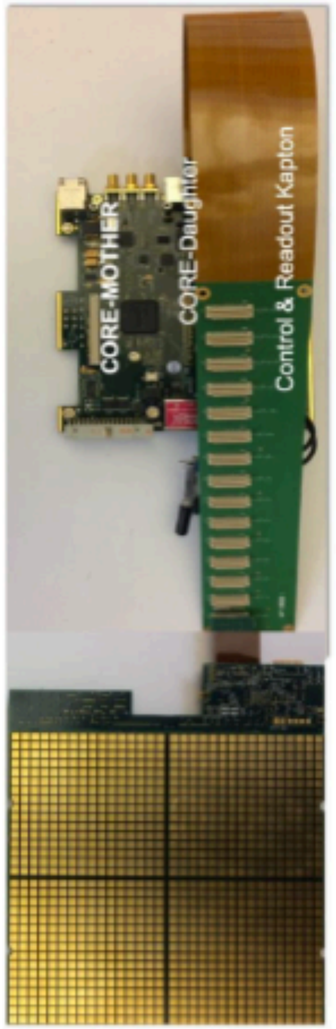
Calorimeters

Calorimeters

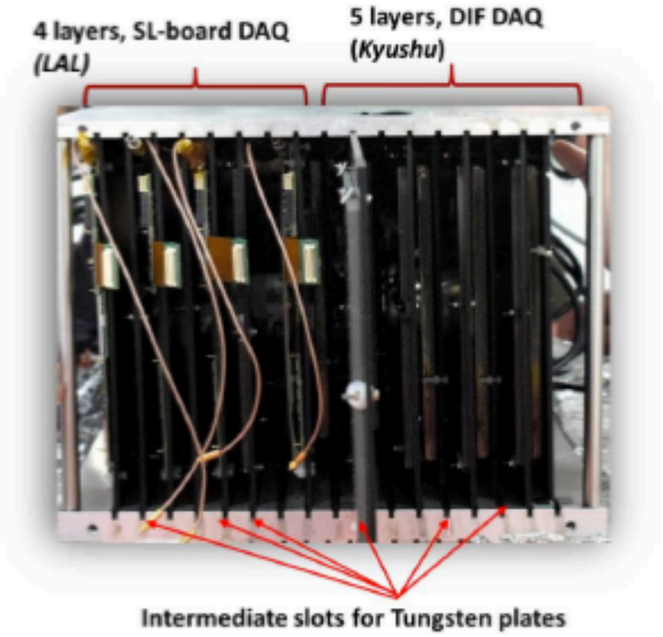
- Very sophisticated calorimeters are proposed for CEPC
- High granularity calorimeters of various types, using the CALICE experience:
  - SiW
  - SDHCAL
  - T-SDHCAL
- Dual readout calorimeter placed outside of the magnet for IDEA
  - Very good hadronic energy resolution
  - Can be complemented with a crystal ECAL, placed inside the coil, for an exquisite e.m. energy resolution
- Also here a lot of R&D is ongoing

SiW ECAL: ready for 2021 test beam

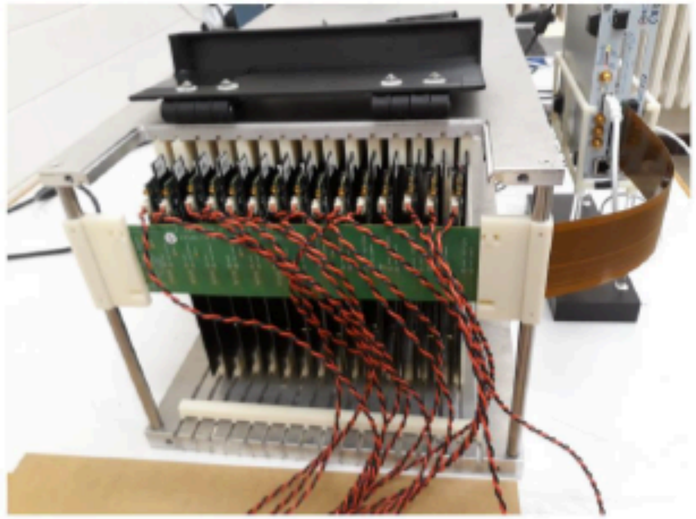
Test bench 2018



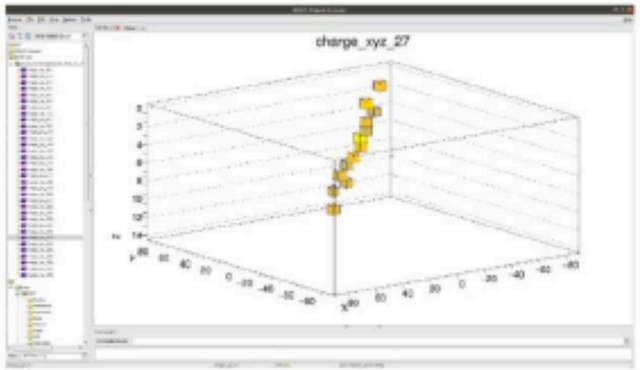
Beam test 4 layers in 2019



15 layers in 2020:
15000 cells in readout



First cosmic (Adrian Irles)



- Rapid development of compact readout electronics
- For the first time all components at hand that could be installed in a lepton-collider detector
- Beam test at DESY is ongoing: Nov. 1-15, 2021

Over 15 layers ready for beam test (FEV10, 11, 12, 13 and COB)

Y. Liu

SiW ECAL: ready for 2021 test beam

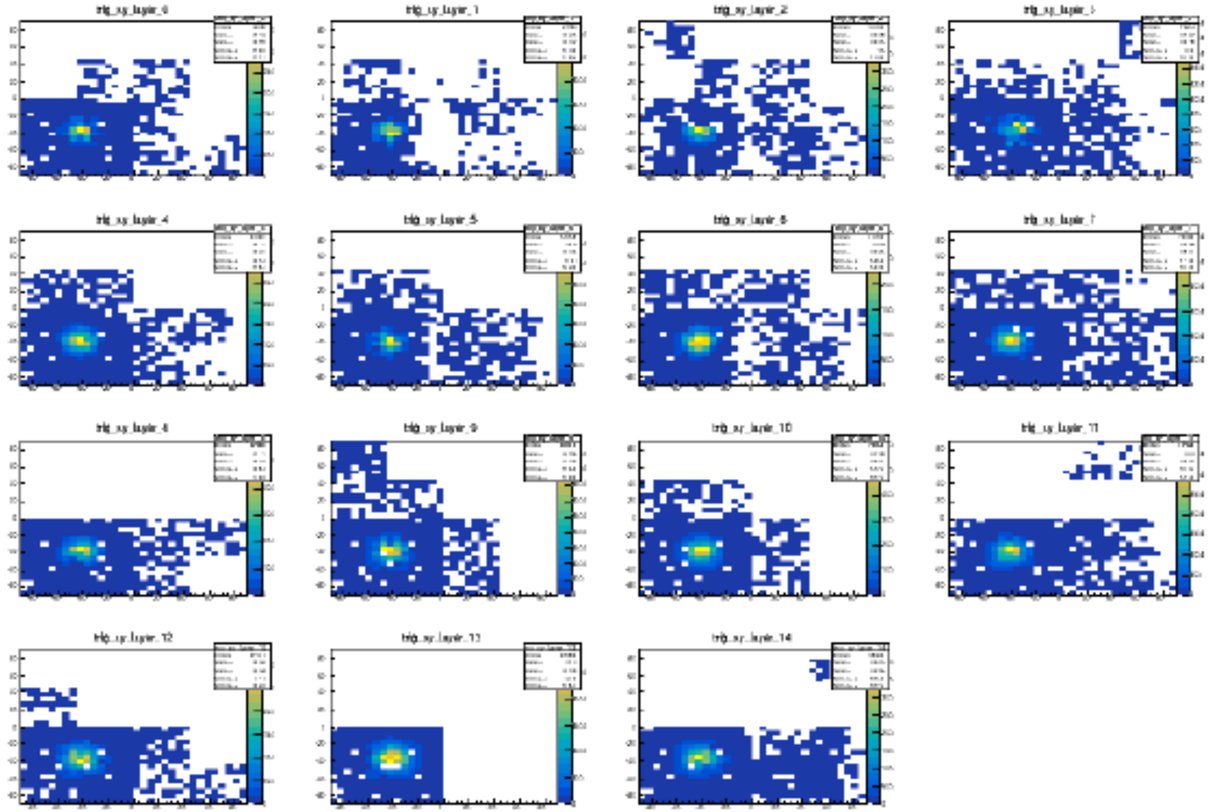
"Live" from the DESY Beam Test

Fresh results (Nov. 8) from Roman Pöschl (IJCL

Detector Setup

Detector in beam position

Hit maps of all 15 layers



- DESY Beam Test 1/11/21 – 15/11/21
  - Successful operation of the prototype composed of 15 layers (15360 cells)
  - Smooth data taking as we speak
  - Exciting and important results can be expected

Y. Liu

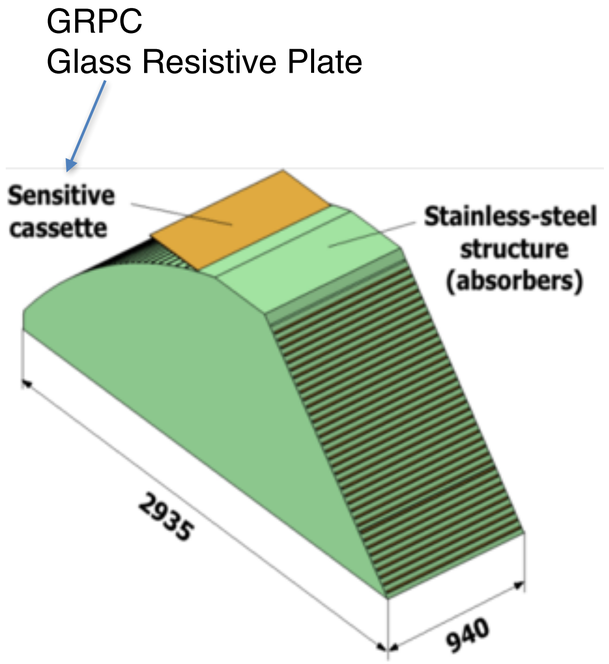
SDHCAL R&D for future colliders

Detectors as large as 3m X 1m need to be built

Electronic readout should be the most robust with minimal intervention during operation.

Mechanical structure with minimal dead zone

Include time information SDHCAL → T-SDHCAL



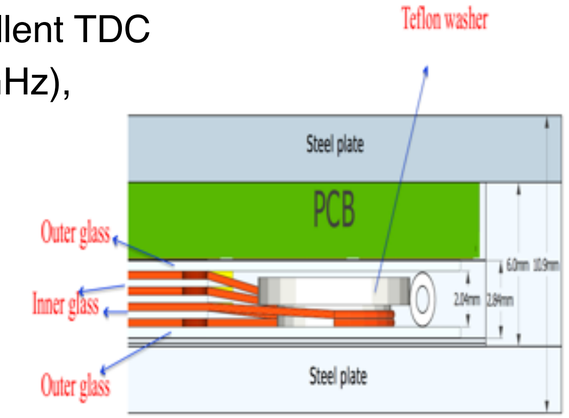
T-SDHCAL

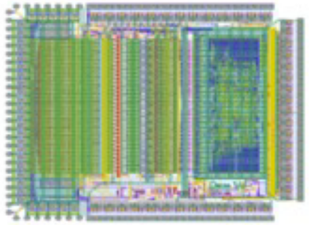
Timing is an important factor to identify delayed neutrons and better reconstruct their energy

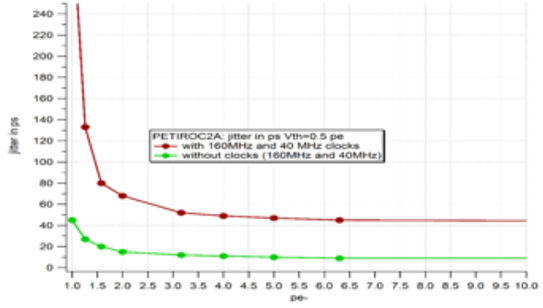
How to achieve an excellent time resolution:

An ASIC with a fast preamplifier, precise discriminator and excellent TDC
→PETIROC 32-channel, high bandwidth preamp (GBWP> 10 GHz), <3 mW/ch, dual time and charge measurement (Q>50 fC)
→ TDC either internal or external

A fast-time DETECTOR
→ MultiGAP RPC is an excellent candidate
4-5 gaps of 250 µm each can provide 100 ps time resolution



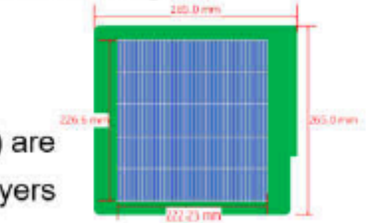


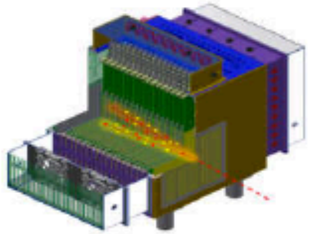


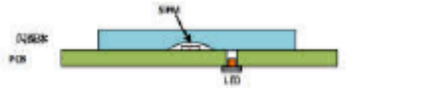
S. Li

PFA ECAL prototype

- 16 super-layers with each super-layer consisting of 2 EBUs and 2 tungsten layers.
- The total radiation length ~ 23.4 X_0
- Scintillator strips (45mm*5mm*2mm) are arranged in alternating orthogonal layers and read out with SiPM
- 210 channels per EBU
- 12 fans at two ends for air cooling



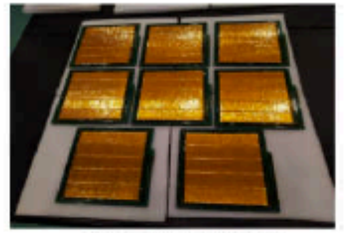




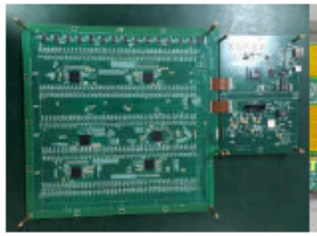
质量检查

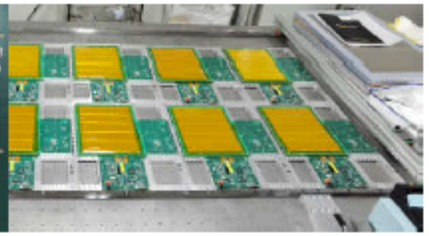
部件清洗

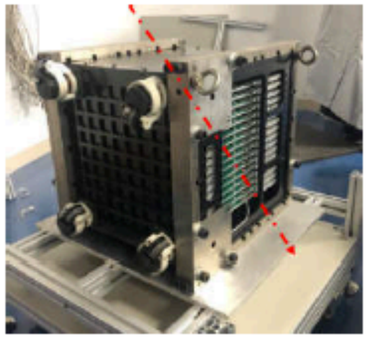
单元组装



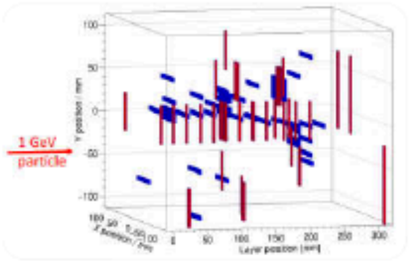
探测器与电子学集成



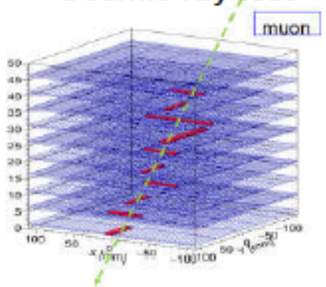


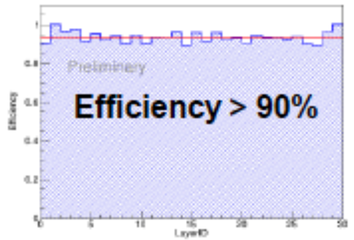


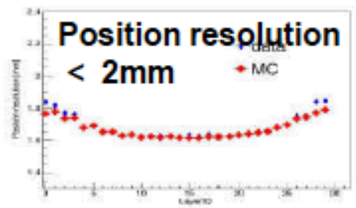
Beam test at IHEP



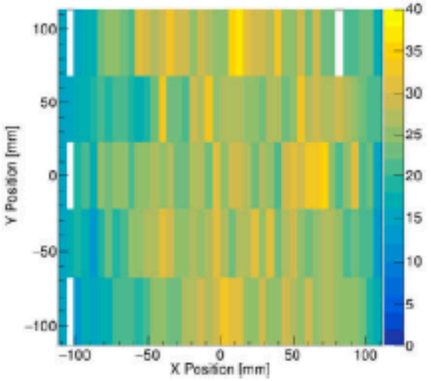
Cosmic-ray test







Light yield ~ 20 ph.e./MIP

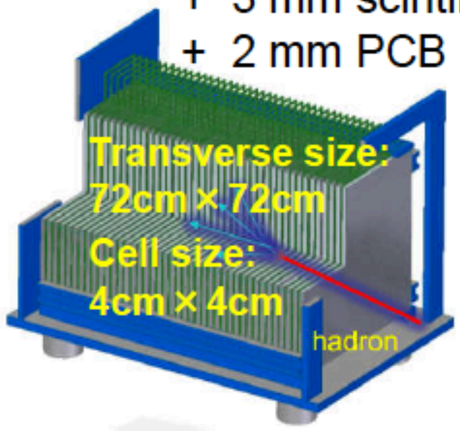


J. Liu

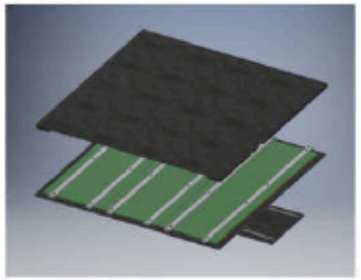
PFA HCAL

A full-size AHCAL prototype is being built

40 layers of 20 mm steel
+ 3 mm scintillator
+ 2 mm PCB

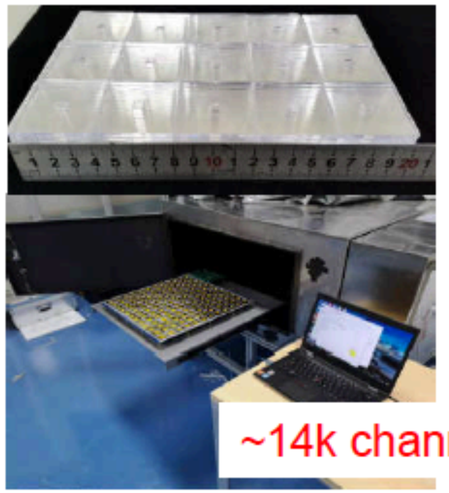


Mechanical design

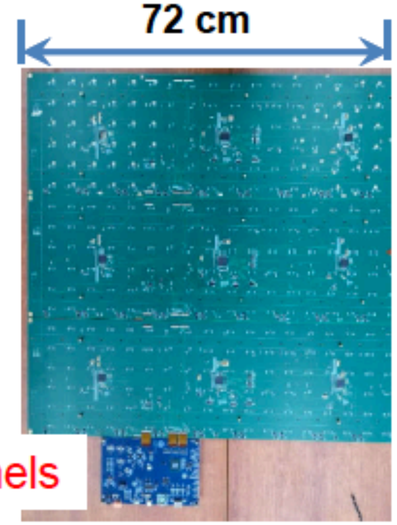


Cooling design and simulation

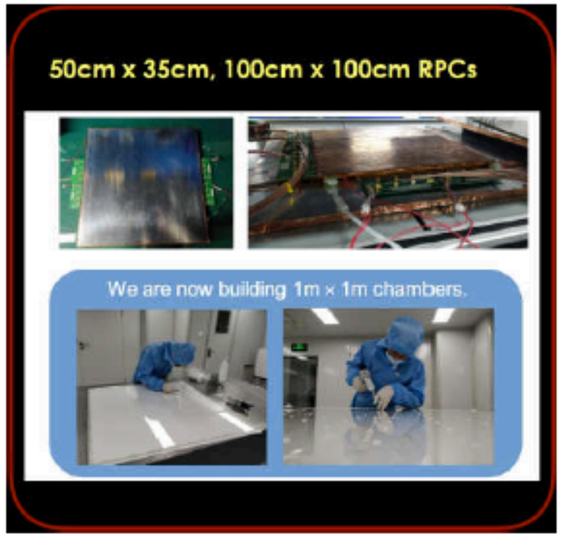
Scintillator tiles production and quality control

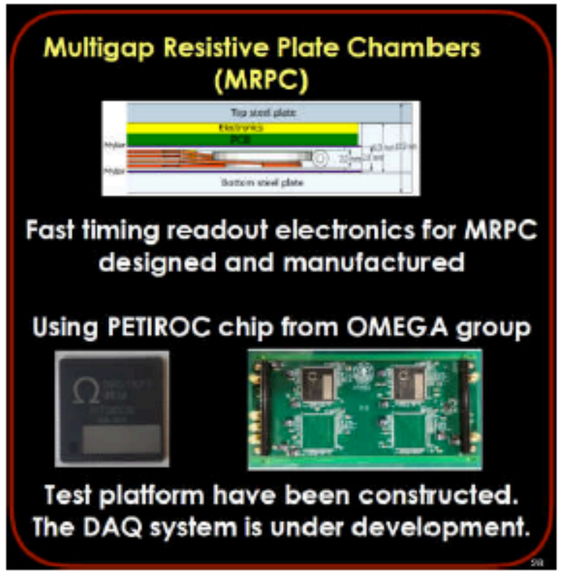


Readout board development



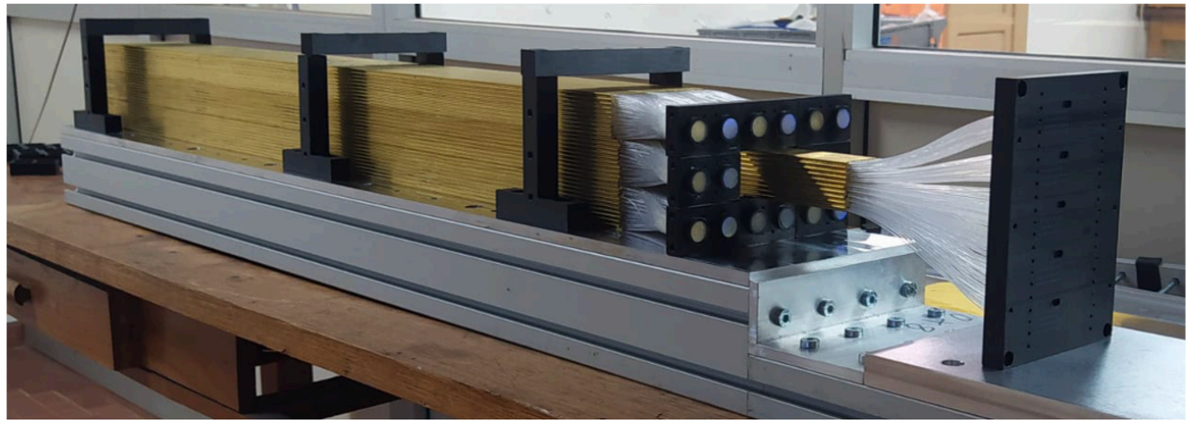
RPC-SDHCAL





J. Liu

2020 Dual Readout prototype

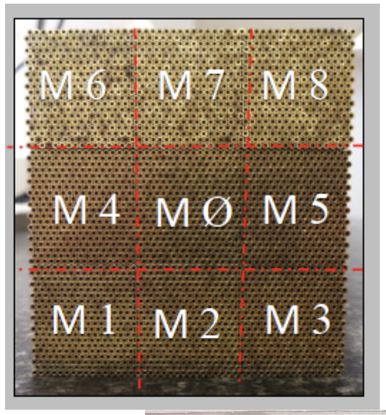


Electromagnetic dimensions of 10x10x100 cm^3

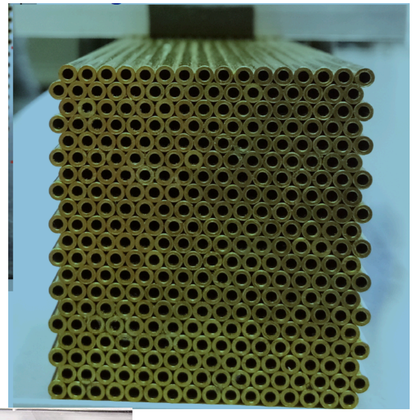
9 towers containing 16x20 capillaries (160 C and 160 S)

Capillary tube with outer diameter of 2 mm and inner diameter of 1.1 mm
1-mm-thick fibers

Full prototype - 9 towers



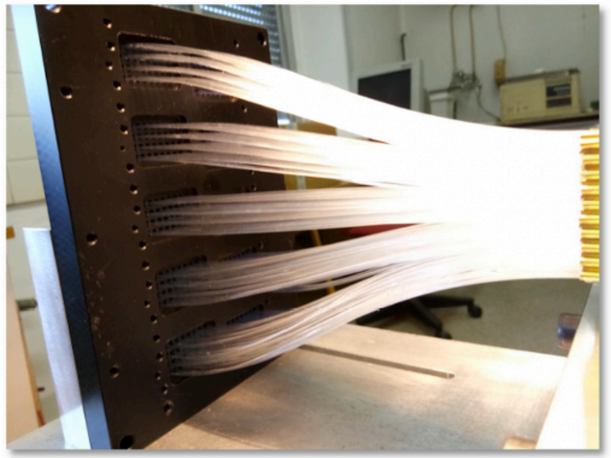
Single tower

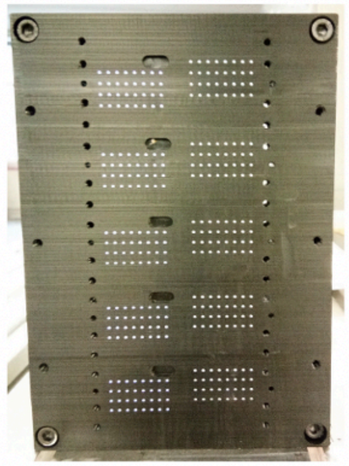


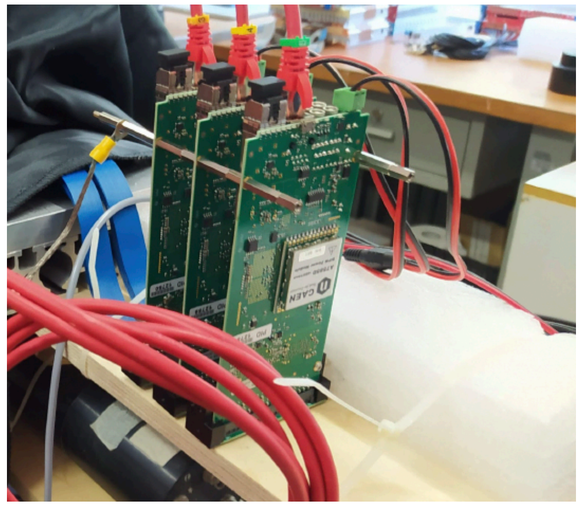
“Bucatini calorimeter”

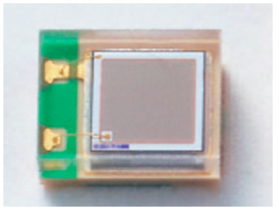
Front end board housing 64 SiPM

Fiber guiding system









Hamamatsu SiPM: S14160-1315
PS Cell size: 15 μm

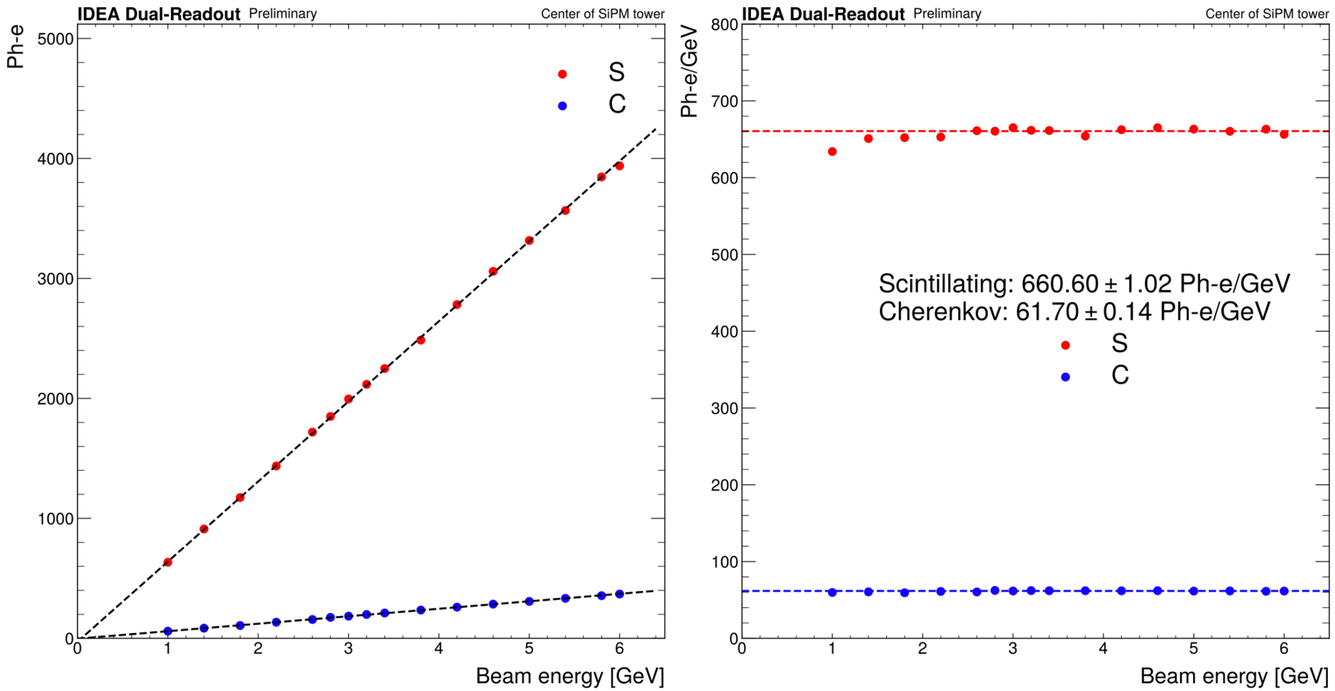
Readout Boards CAEN A5202

L. Pezzotti

2020 Dual Readout prototype

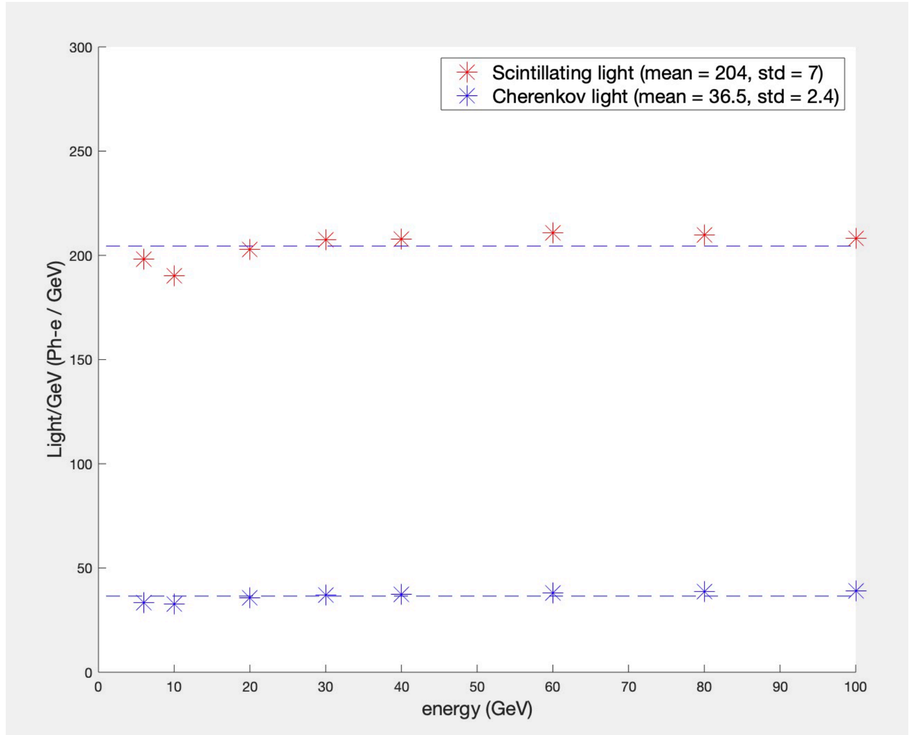
Two test beams in 2021: DESY and CERN

DESY with e^- 1-6 GeV



Preliminary - no filters used

SPS with e^+ 10-125 GeV

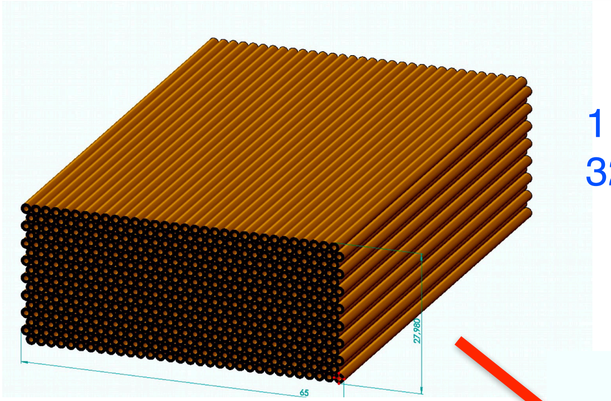


Preliminary

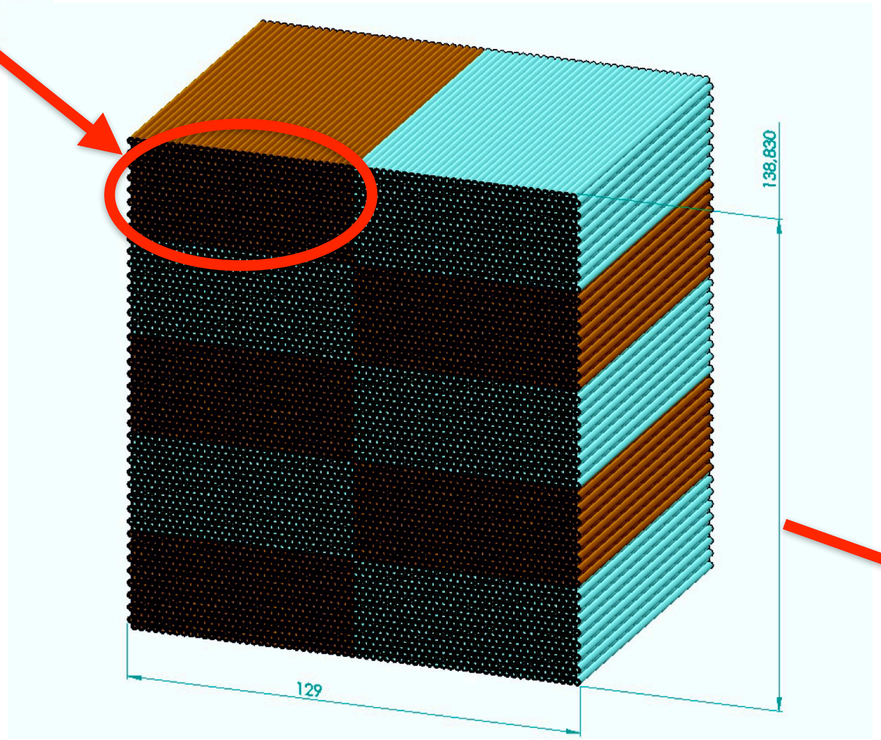
yellow filters used over scintillating fibers, neutral filters used over clear fibers

L. Pezzotti

DR future prototypes



1 Mini-Module (MM):
32 x 16 channel (512 ch)



1 Module:

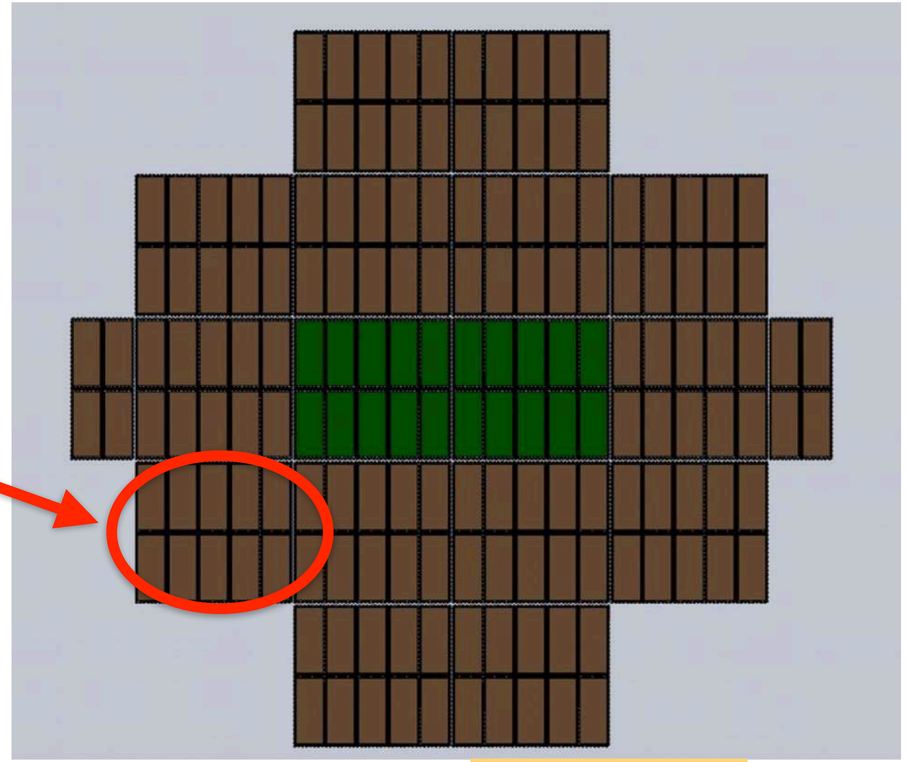
2 x 5 MMs
→ 10 FEE boards
(8-channel grouping)
~ 13 x13 x 200 cm^3

HiDRa2

Full hadronic shower containment calorimeter

17 modules, ~ 65 x 65 x 200 cm^3

- 2 central modules with SiPMs
→ ~ 10 k SiPMs, ~ 20 FEE boards
- all others with PMTs
→ ~ 150 PMTs

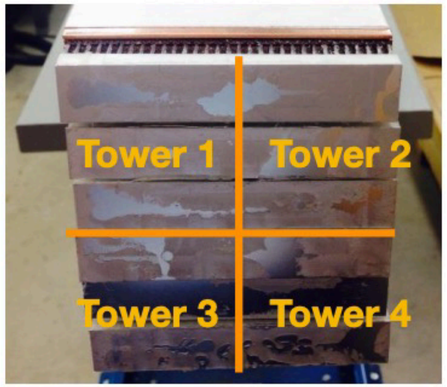


G. Gaudio

Plate based + 3D printing calo (Korea)

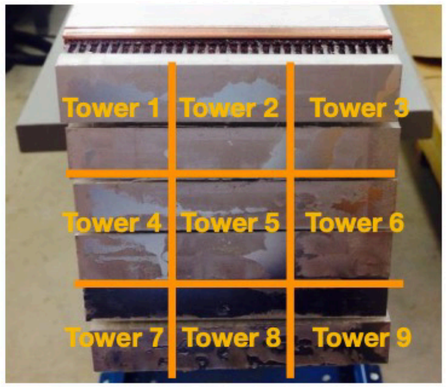
"Short-term plan"

Module #1 (2x2)

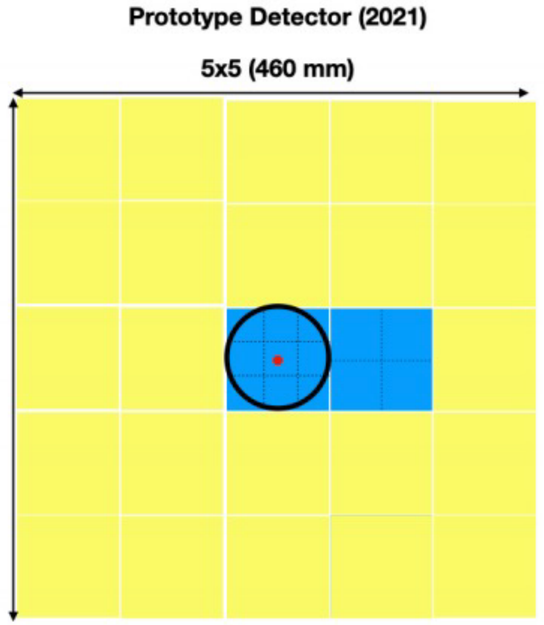


Tower#1	Tower#2
Tower#3	Tower#4

Module #2 (3x3)

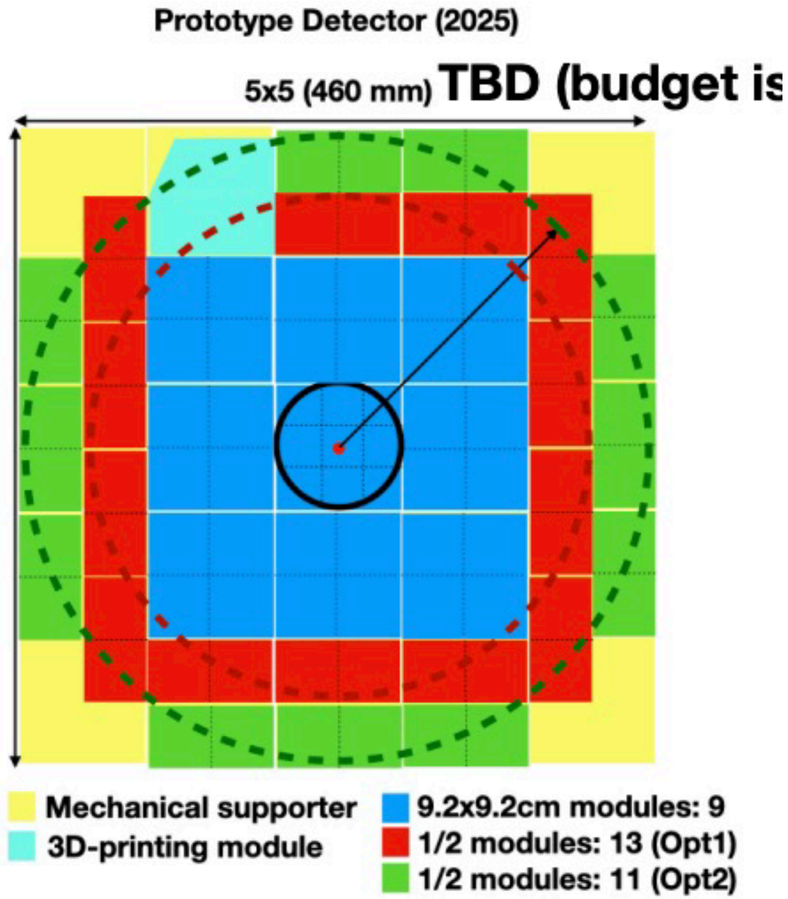


Tower#1	Tower#2	Tower#3
Tower#4	Tower#5	Tower#6
Tower#7	Tower#8	Tower#9



Building more and more modules 2022-2025

"Mid-term plan"



Strong collaboration on DR calorimetry between INFN, Korea and USA

G. Gaudio

DR calorimeter

Dual-readout fiber-sampling calorimeter

- Longitudinally unsegmented fiber-sampling calorimeter
  → measure both EM & hadronic components simultaneously
  → fine unit structure with a high granularity
- Projective geometry with a uniform sampling fraction
  → more fibers in the rear than the front

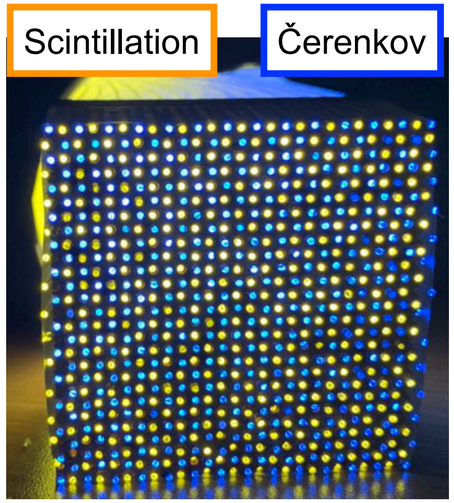
$$S = E[f_{em} + (\frac{h}{e})_S (1 - f_{em})],$$

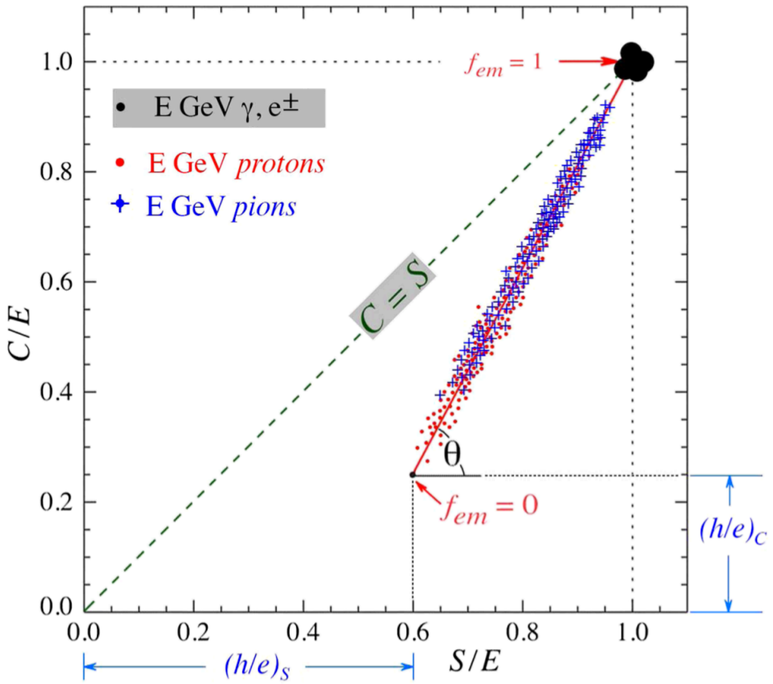
$$C = E[f_{em} + (\frac{h}{e})_C (1 - f_{em})]$$

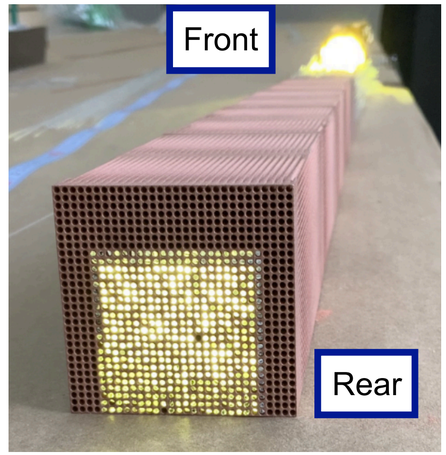
$$f_{em} = \frac{(h/e)_C - (C/S)(h/e)_S}{(C/S)[1-(h/e)_S] - [1-(h/e)_C]}$$

$$\cot\theta = \frac{1-(h/e)_S}{1-(h/e)_C} \equiv \chi,$$

$$E = \frac{S - \chi C}{1 - \chi}$$

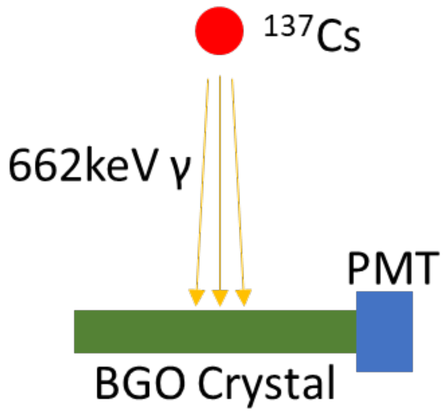


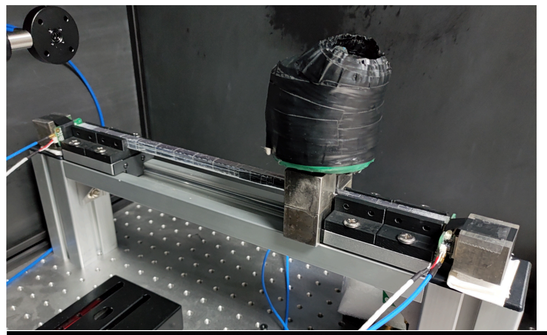


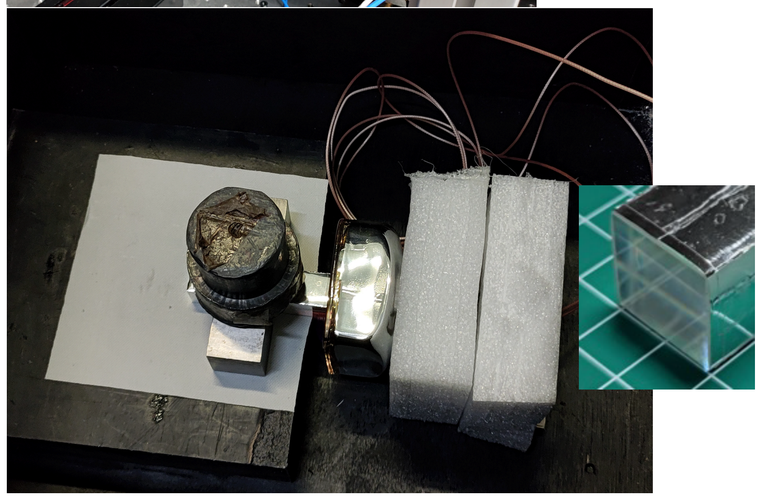


S. Ko

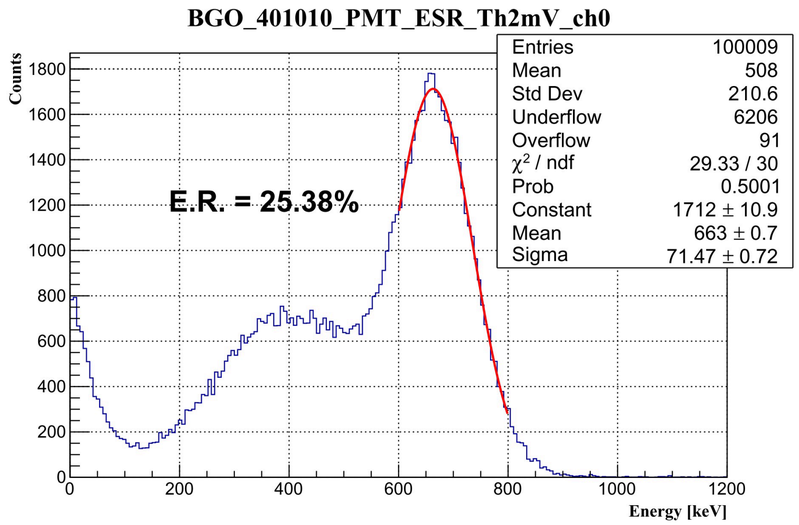
High granularity crystal ECAL

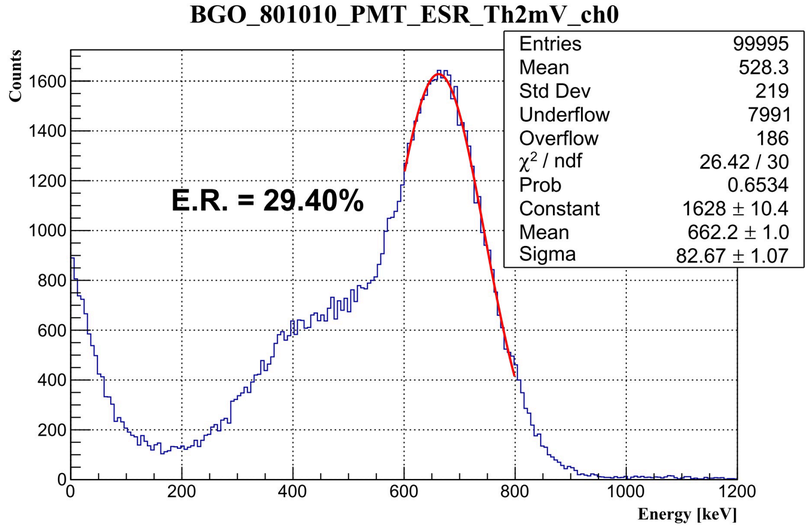




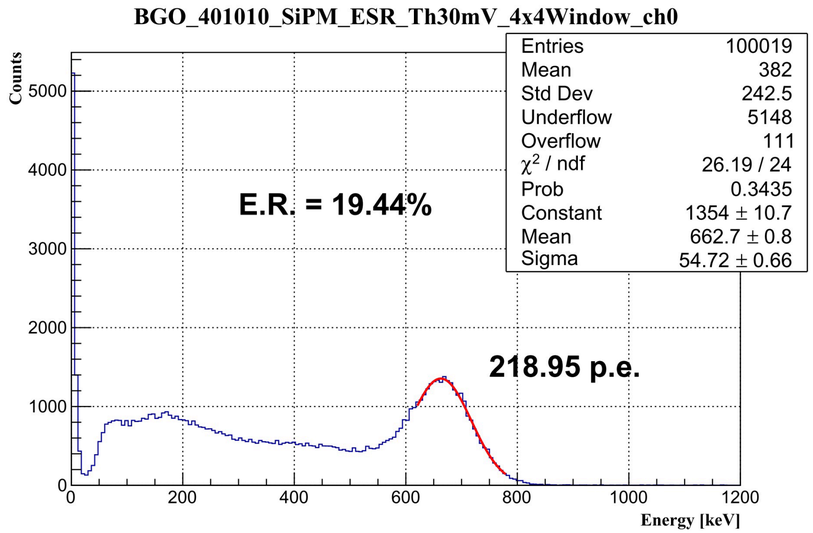


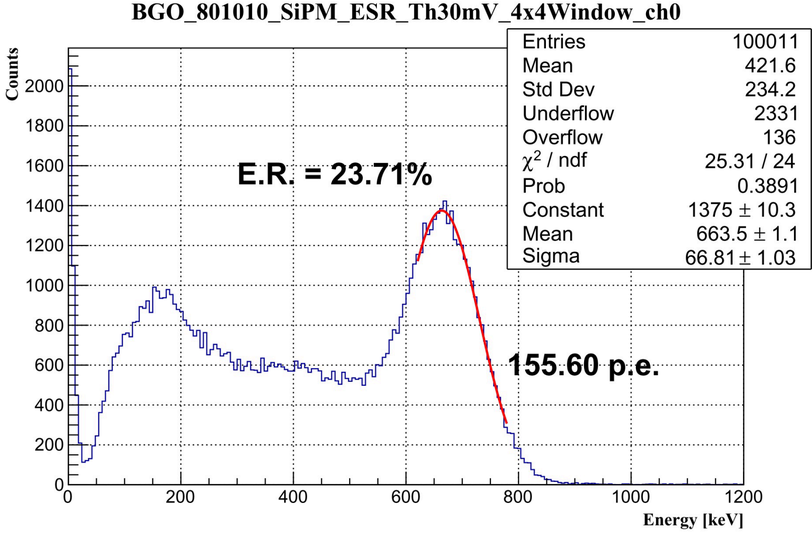
PMT





SiPM





PMT has better acceptance (full coverage of crystal transverse area) than SiPM, to be updated with larger SiPMs

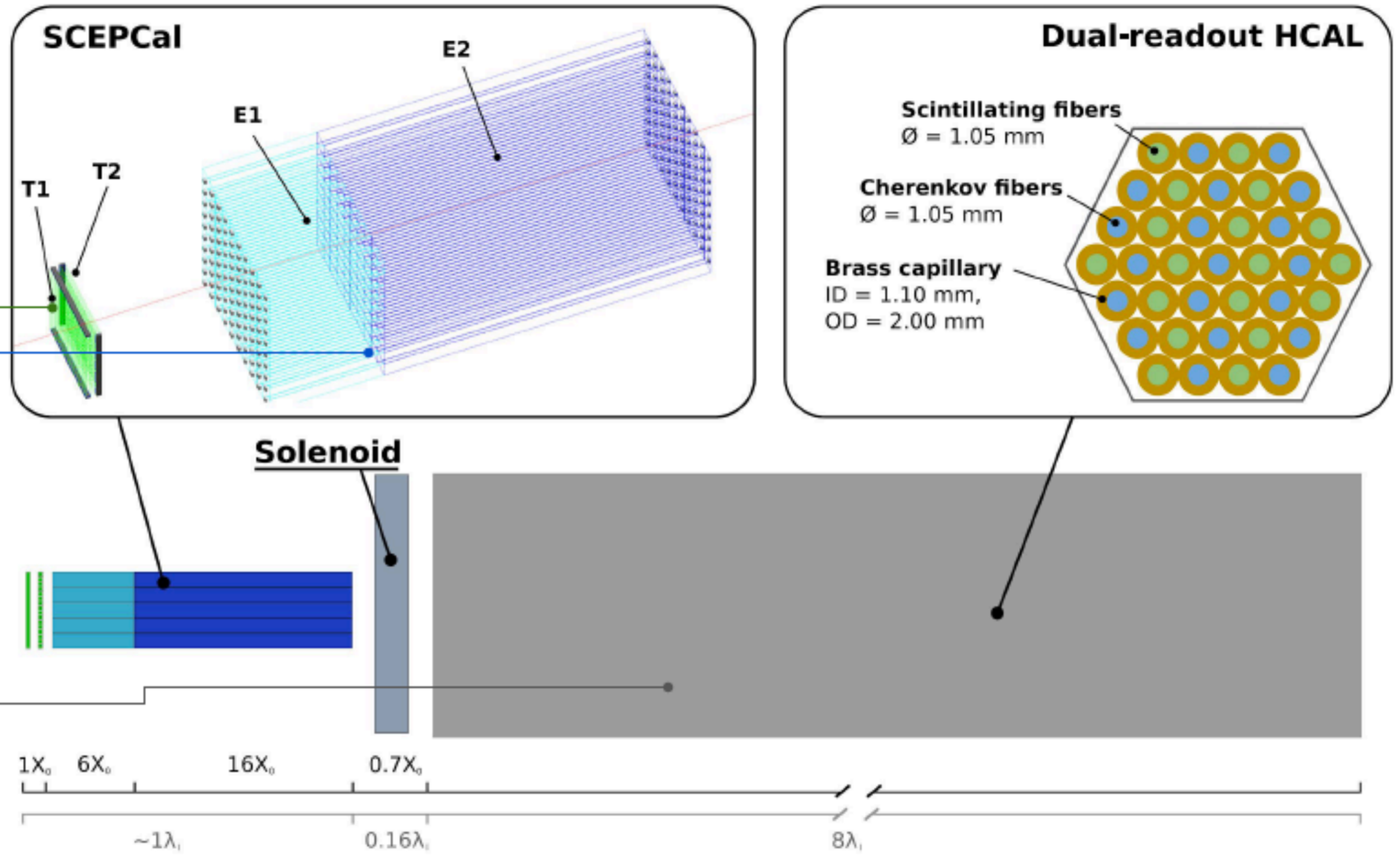
F. Guo

Crystal ECAL with IDEA's DR calorimeter

Layout overview

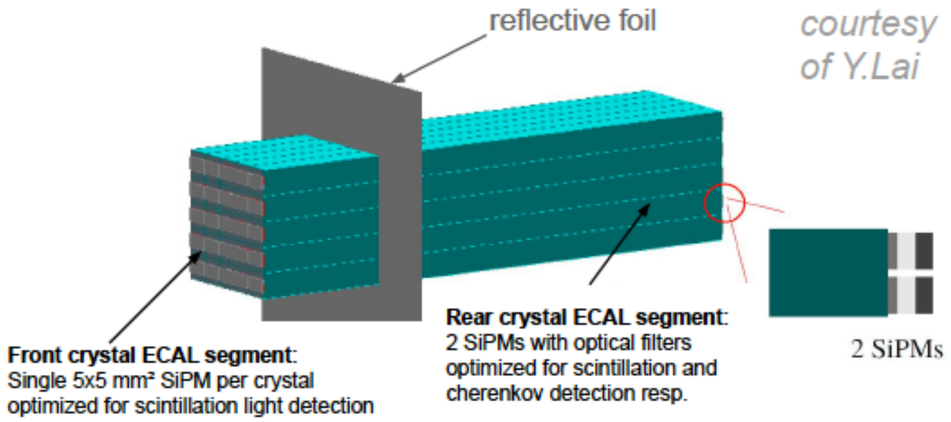
- **Transverse and longitudinal segmentations** optimized for particle identification and particle flow algorithms
- Exploiting **SiPM readout** for contained cost and power budget

- **Timing layers** — $\sigma_t \sim 20$ ps
  - LYSO:Ce crystals (~$1X_0$)
  - 3x3x60 mm³ active cell
  - 3x3 mm² SiPMs (15-20 um)
- **ECAL layers** — $\sigma^{EM}_E/E \sim 3\%/\sqrt{E}$
  - PWO crystals
  - Front segment (~$6X_0$)
  - Rear segment (~$16X_0$)
  - 10x10x200 mm³ crystal
  - 5x5 mm² SiPMs (10-15 um)
- **Ultra-thin IDEA solenoid**
  - ~$0.7X_0$
- **HCAL layer** — $\sigma^{HAD}_E/E \sim 26\%/\sqrt{E}$
  - Scintillating and "clear" PMMA fibers (for Cherenkov signal) inserted inside brass capillaries

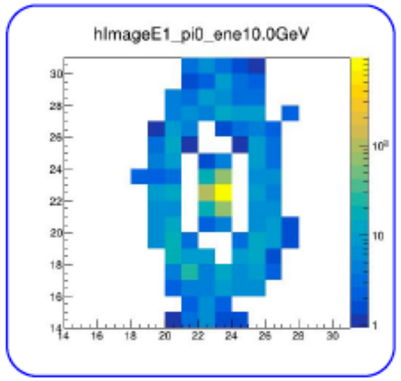


M. Lucchini

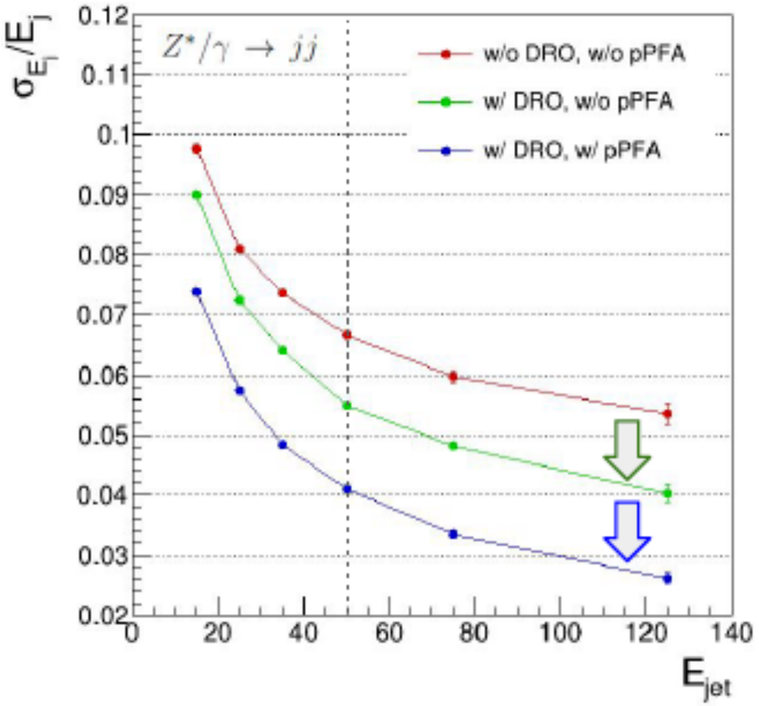
Crystal ECAL with IDEA's DR calorimeter



$\pi^0 \to \gamma\gamma$ events



Jet resolution

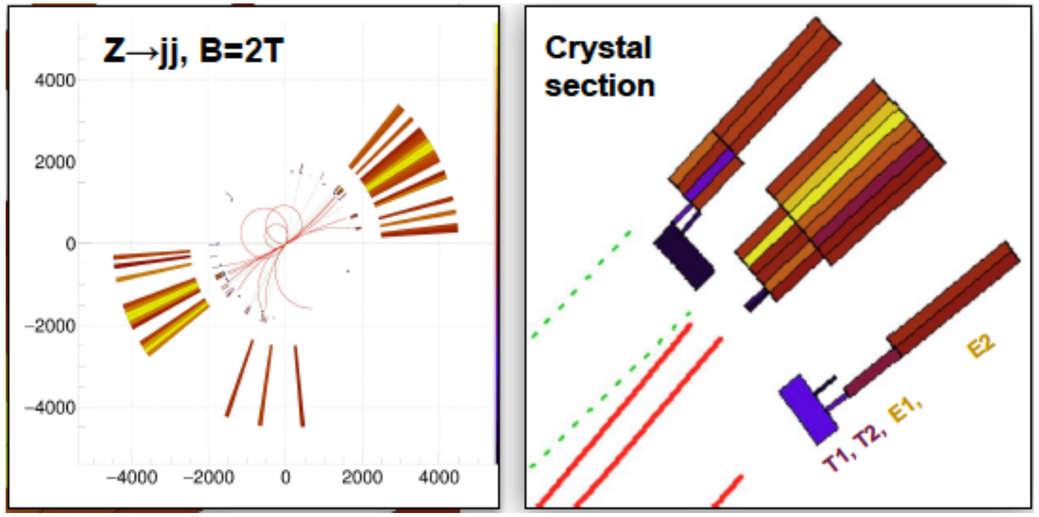


crystals + IDEA w/o DRO

crystals + IDEA w/ DRO

crystals + IDEA w/ DRO + pPFA

Event display



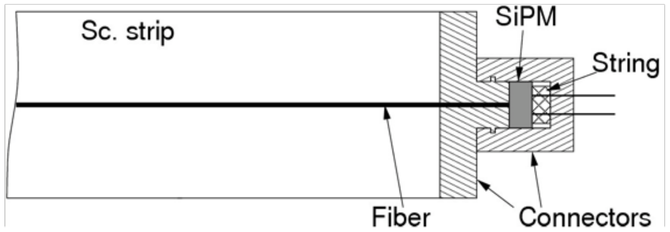
Sensible improvement in jet resolution using dual-readout information combined with a particle flow approach → 3-4% for jet energies above 50 GeV

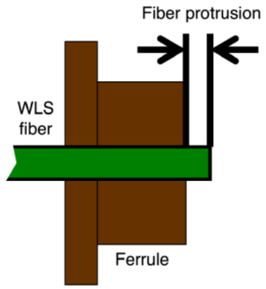
M. Lucchini

Muon detectors

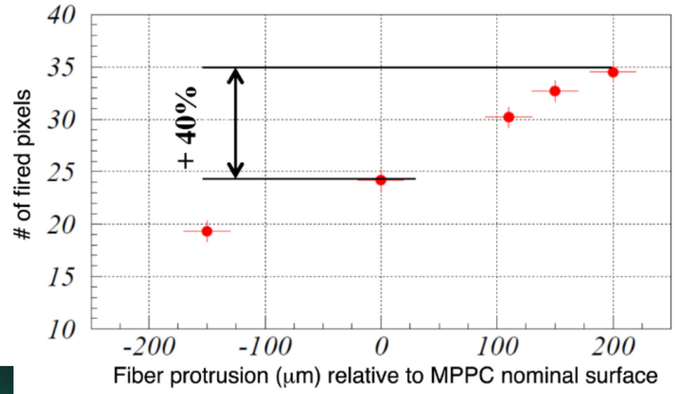
Scintillator-based detector

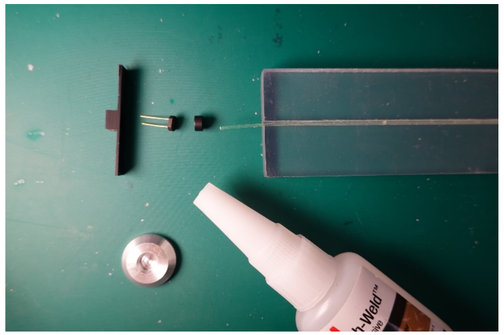
Optical coupling

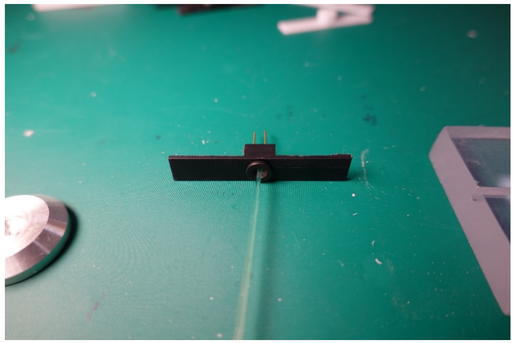


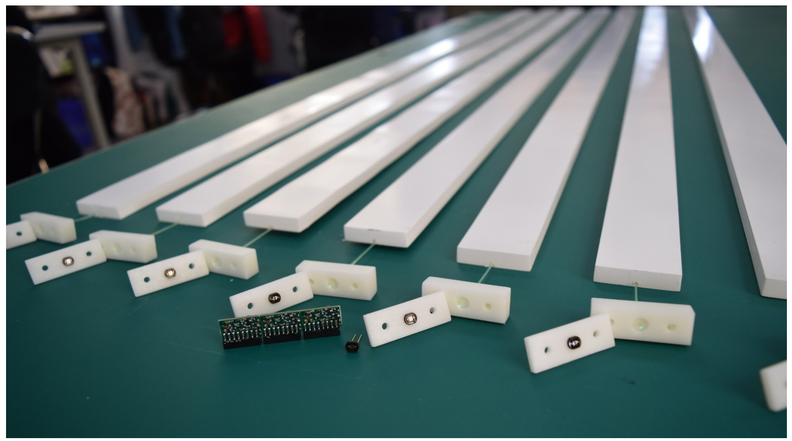


From Belle II







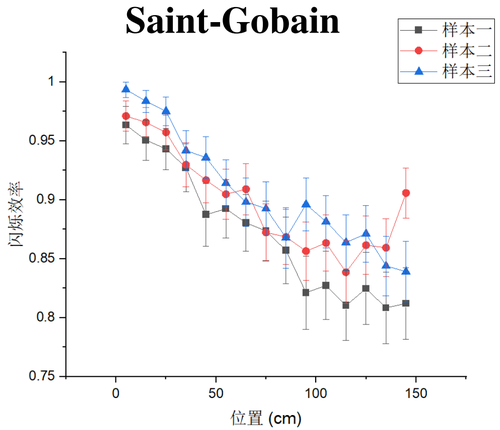


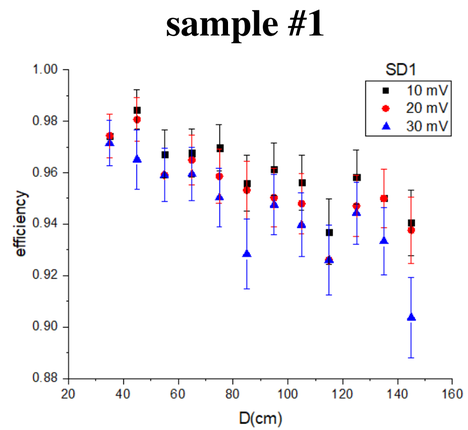
Fiber comparison

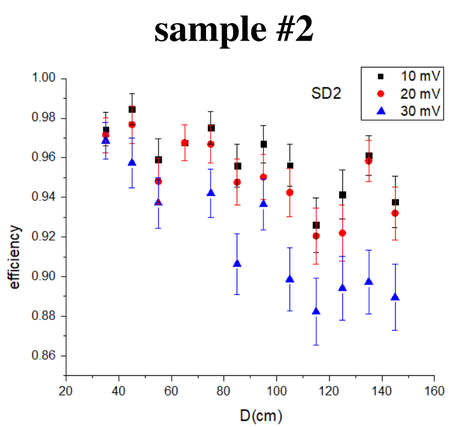
			Saint_Gobain			Kuraray		
Position	Time	Scintillation sample	Entries	Mean	Entries×Mean (×10^7)	Entries	Mean	Entries×Mean (×10^7)
0-150 cm	1h	#1	10820	2617	2.83	12520	4892	6.12
		#2	10657	2462	2.62	12507	5260	6.58
70-80 cm	10h	#1	5872	1883	1.10	6031	4216	2.54
		#2	5838	2108	1.23	5998	4608	2.76

X. Wang

Silicon-based detector



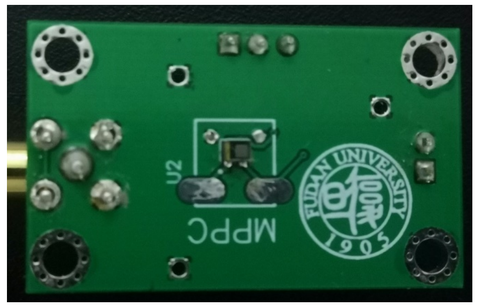


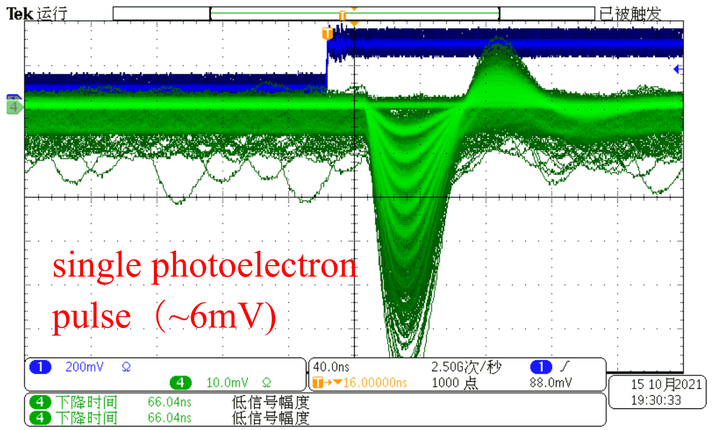


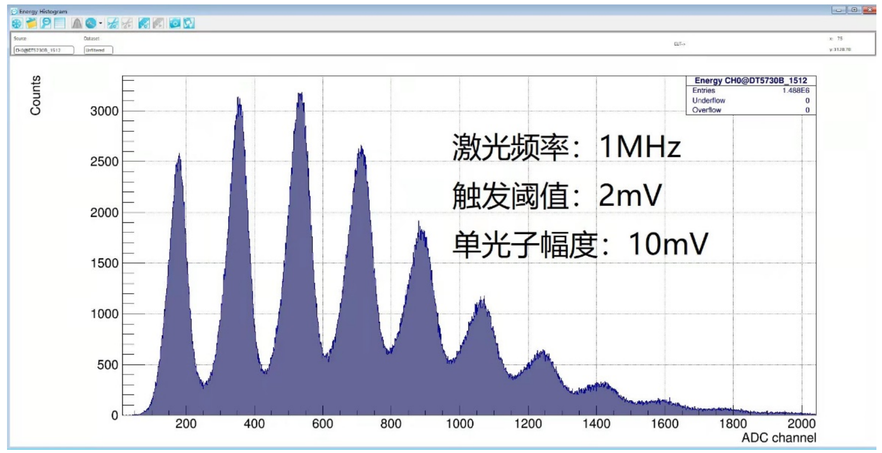
Good improvement on fiber efficiency!

- Design new preamp
- Study with NDL SiPM
- Performance is good, but the 1*1 size is too small, while 3*3 is too large.

Study on NDL SiPM

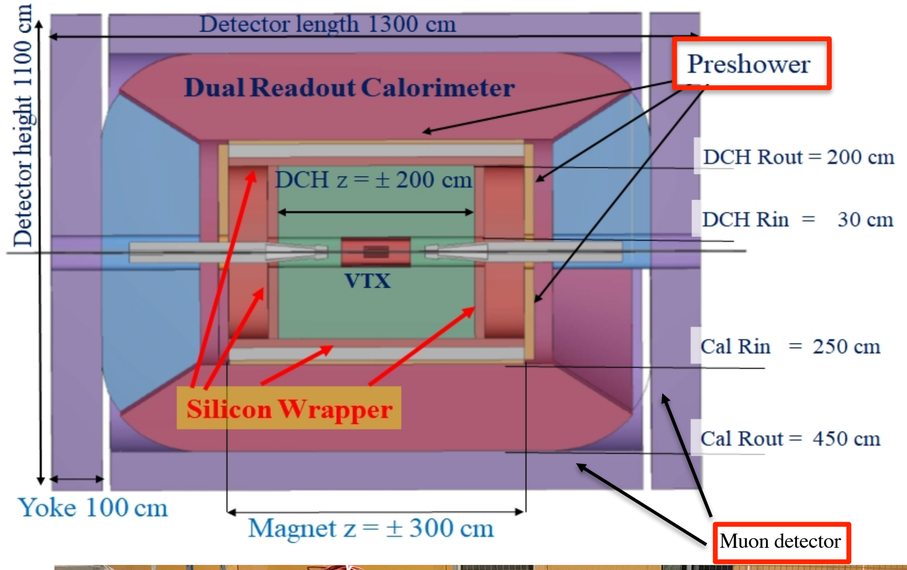


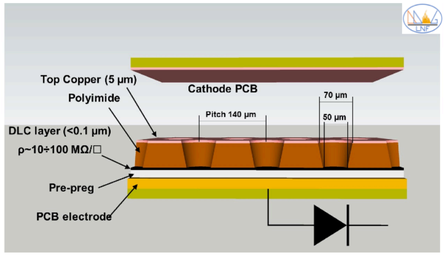


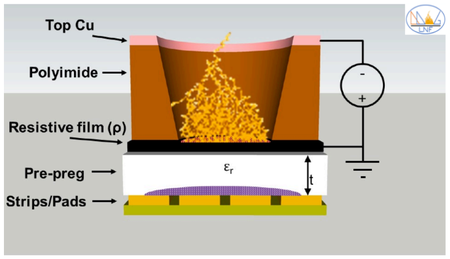


X. Wang

μRWELL-based detectors

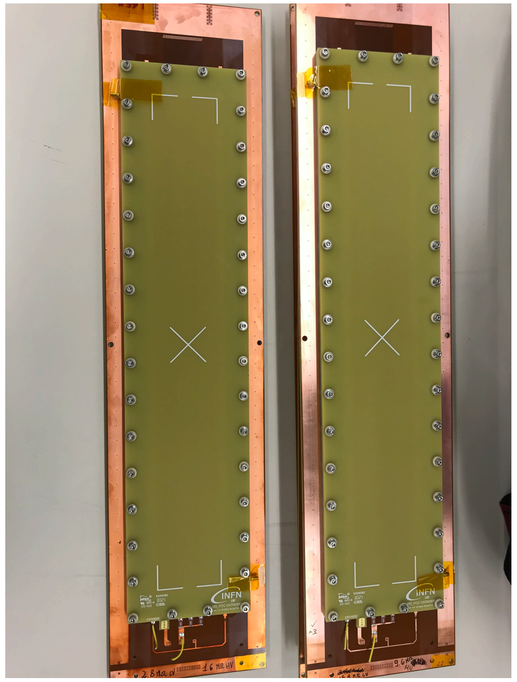


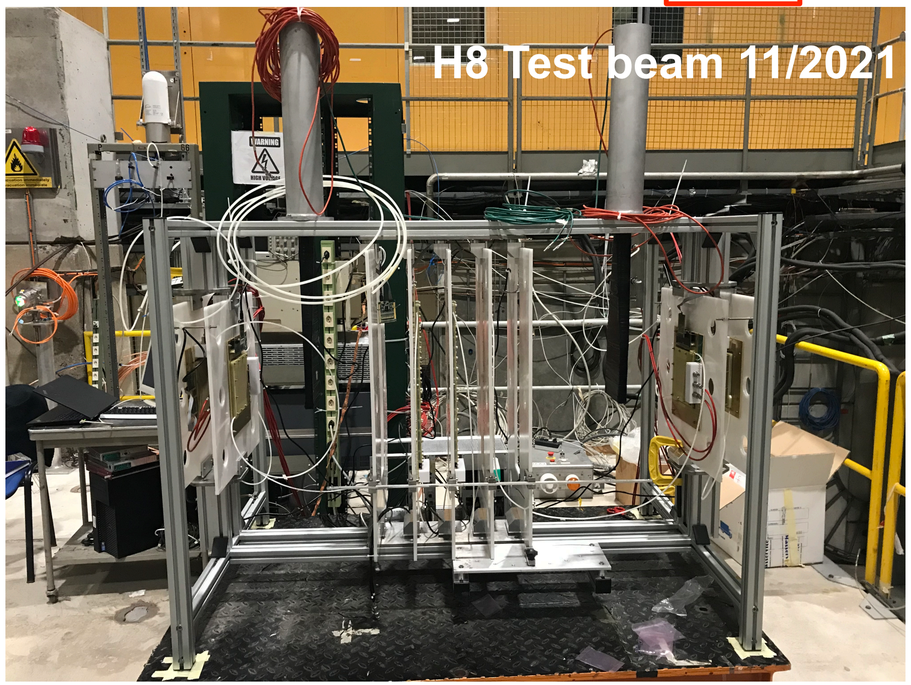


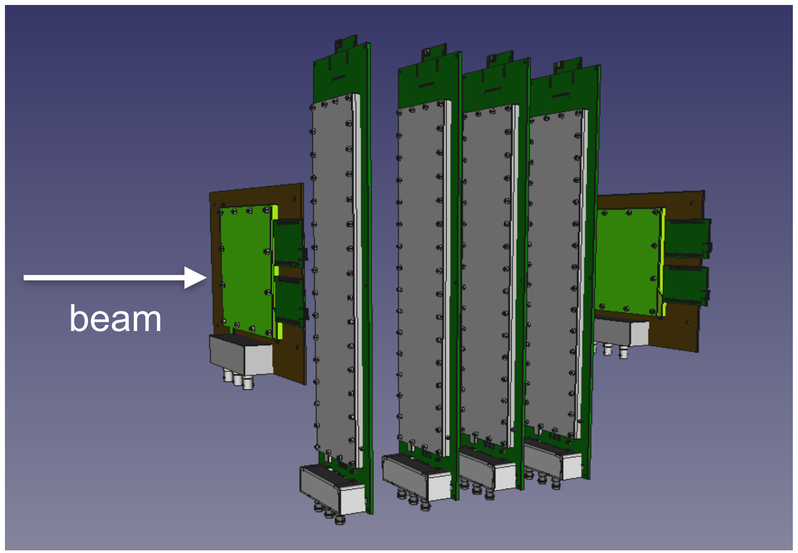


New μRWELL prototypes with 50cm long strips

strips







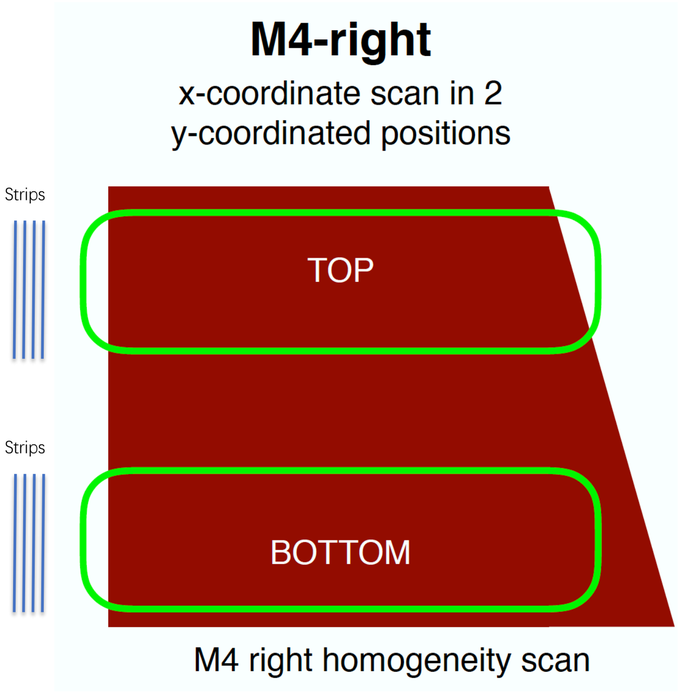
7 μRWELL prototypes with resistivity varying between
10 and 80 MOhm/□
Will allow to define best resistivity for final 50x50 cm^2 detector

X. Wang

μRWELL-based detectors

2022-2024 R&D program

- Define the best resistivity of the DLC for both μRWELL fundamental tiles and build the 50×50 cm^2 prototypes for the pre-shower and muon systems.
- Optimize the engineering mass construction process together with the ELTOS industry.
- Develop a custom-made ASIC for the μRWELL with the experience obtained from the TIGER chip and to test the μRWELL prototypes.
- Develop a new reconstruction algorithm, ML-based, to improve the resolution of μRWELL.
- Simulation of the CEPC decay channels of interest to optimize the detector design with special emphasis on Long Lived Particles to show the impact of a performing tracked in the muon system instead of a tagger.



Development of a new ASIC

- Two large microRWell chambers M4 in Bologna;
- Ferrara has procured the Tiger electronics;
- Plan to start equipping the M4s with the TIGER next spring;
- Use a cosmic telescope to characterize the detector and the electronics and later to expose the chamber with the TIGER electronics to a test beam;
- Funding received to develop a new ASIC starting from the experience of the TIGER.

X. Wang

Common R&D

- We are living in a stimulating but uncertain situation: no consensus on the post-LHC accelerator, if not in general on a Higgs and EW factory
- Limited manpower to work on future projects
- Limited financial resources available for R&D for future experiments
- Small number of young detector experts
  - Even smaller number of young detector experts working on R&D for future experiments

Detector requirements for the various Higgs and EW factories (circular or linear) have more similarities than differences

Why not use the good example of key4HEP and take advantage and exploit the synergies between R&D plans for FCC-ee, ILC, CLIC, CEPC?

Conclusions

- A lot of material presented at this workshop
- Despite the limited resources a lot of R&D is ongoing on many of the technologies of interest to CEPC
- Need for significant R&D in the next 4-5 years
  - Should try to use at best all the synergies between R&D programs for CEPC, FCC-ee, ILC, CLIC, current experiment upgrades, EU grants, other International and/or national grants, etc.
- We know how to build detectors for high energy e^+e^- collisions, but
  - CEPC poses additional challenges
    - Higher physics rates
    - Very large datasets at the Z^0 peak
    - Large datasets make CEPC the ultimate heavy flavour factory (b, c, τ)
    - Search for extremely rare events: LLPs, ALPS, HBL, ...
- We should prepare up to four detector concepts
  - These concepts should include also engineering solutions
  - Final detectors will likely be a mix-and-match of the various technologies discussed

Backup