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ORIGINAL PAPER

Research and development of the back-end electronics for the two-dimensional improved resistive plate chambers in CMS upgrade

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Abstract

Purpose To complement and ensure redundancy in the endcap muon system of the Compact Muon Solenoid (CMS) detector and to extend the Resistive Plate Chamber (RPC) system coverage, improved RPCs (iRPCs) with either orthogonal layer strips with one-end electronics or single layer strips with two-end electronics providing more precise time measurement will be installed in the very forward pseudorapidity region of $|\eta| < 2.4$. The iRPC readout system needs to support two-dimensional (2D) or two-end readout. In addition, it must combine detector data with Timing, Trigger and fast Control (TTC) and Slow Control (SC) into one data stream over a bi-directional optical link with a line rate of 4.8 Gb/s between the Front-End Electronics (FEE) and the Back-End Electronics (BEE). To fulfill these requirements, a prototype BEE for the iRPC 2D chamber has been researched and designed.

Methods A Micro-Telecommunication and Computing Architecture (μTCA)-based processing card was designed in this study to establish a prototype system together with a μTCA crate. The Giga-Bit Transceiver (GBT) protocol is integrated to provide bi-directional communication between the FEE and BEE. A server is connected with the BEE by a Gigabit Ethernet (GbE) link for SC and a 10-GbE link for Data AcQuisition (DAQ).

Results The Bit Error Rate (BER) test of the back-end board and a joint test with the iRPC 2D prototype chamber were performed. A BER of less than 1.331×10^{-16} was obtained. The time measurement with a resolution of 3.05 ns was successfully realized, and detector efficiencies of 97.7% for longitudinal strips and 96.0% for orthogonal strips were measured. Test results demonstrate the correctness and reliability of the prototype BEE.

Conclusion The BEE prototype satisfies the requirements for the iRPC 2D chamber, and it worked stably and reliably during a long-term joint test run.

Keywords CMS · iRPC · TTC · SC · BEE · μTCA · GBT · DAQ

Introduction

In the roadmap of the Phase-2 upgrade project in the Compact Muon Solenoid (CMS) experiment, the center-of-

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mass energy of proton-proton collisions will be increased to 14 TeV from the current 13 TeV, with a luminosity of $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and ultimate value reaching $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, at the price of a pile-up rate of 200 interactions per 25 ns [1]. The improved Resistive Plate Chamber (iRPC) system will be added to the vacant part of the RPC region to deal with the more challenging conditions in terms of higher background rate and pile-up. By improving the time and spatial resolutions, the iRPCs together with Cathode Strip Chambers, which are also located in the same high pseudorapidity region, will improve the identification accuracy of triggered events [2].

Two possible options for iRPC readout have been considered: The baseline is two-end readout, while the alternative is two-dimensional (2D) readout. Figure 1 shows the structures of the two options of iRPC. In the two-end case, strips are in one-layer layout and read out from both ends by Front-End Boards (FEBs), the hit position along the strip is calculated from the time difference between the signals from both ends. While in the 2D case, strips are in two-layer layout and read out from one end by on-detector ASICs and data collectors, both the X and Y numbers of each fired strip are provided. In both cases, accurate time is provided in addition to the hit strips like the original RPCs.

This paper describes mainly the research and development work on the BEE and joint tests with iRPC 2D chamber. A prototype system consisting of two Giga-Bit data Formatter (GBF) boards as the data collectors and Micro-Telecommunication and Computing Architecture (μTCA) compliant Back-End Board (BEB) was designed. To verify the feasibility of the designed BEB and the overall readout system, the hardware tests and joint tests with a CMS iRPC 2D prototype chamber were performed and the test results are discussed in this paper.

System architecture

How a full-functionality demo system to fulfill the high bandwidth, low latency, and accurate time requirements of the iRPC readout has been deeply discussed and approved within the CMS and RPC groups [3–5]. The demo system consists of iRPC 2D prototype chamber, on-detector ASICs, data collector, and the BEE. The data collector, consisting of two GBF boards, measures the arriving time of the hits and converts into detector data and then transmits to the BEE via a high-speed fiber link. As shown in Fig. 2, the prototype BEE, consisting of a Micro-Telecommunication and Computing Architecture (μTCA) crate, an Advanced Mezzanine Card (AMC13) [6], a MicroTCA Carrier Hub (MCH) [7], a μTCA compliant BEB, and also a server PC, provide Data AcQuisition (DAQ), Slow Control (SC), and Timing, Trigger and fast Control (TTC) functionalities.

The chosen μTCA crate is VT892 [8], a commercial 7U chassis that provides 12 full-size double-width AMC slots as well as three clocks for each slot. By offering a flexible,

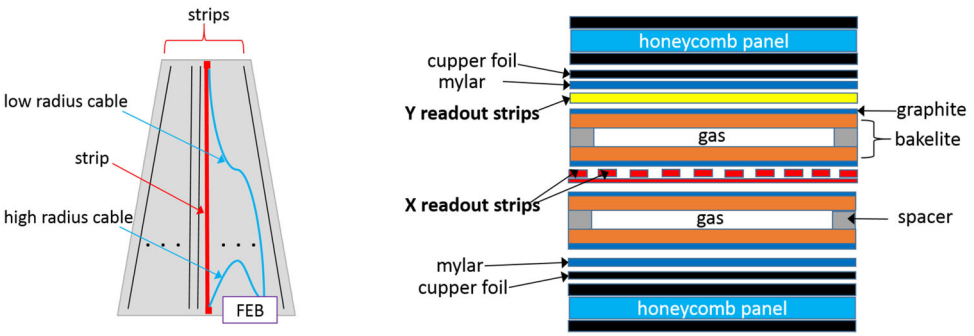


Fig. 1 Diagram of the two options of the iRPC. Left: Two-end iRPC, strips are one-layer layout and read out from both ends. Right: 2D iRPC, strips are two-layer layout and read out from one end

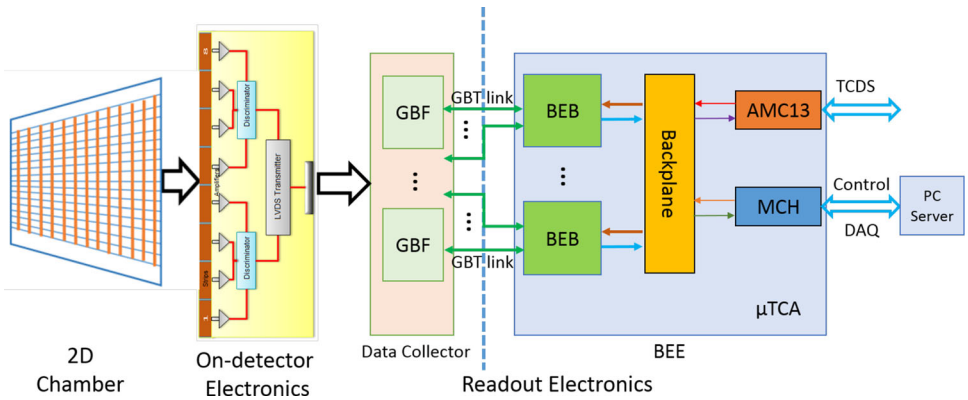


Fig. 2 Block diagram of the readout system connected to an iRPC 2D chamber

high-density, high-performance backplane which supports a bandwidth of up to 10 Gb/s for each channel, this crate provides support for the AMC13 DAQ. The AMC13 is a customized MCH module that was designed entirely by CMS. In addition to DAQ, it is used to interface with the Trigger and Control Distribution System (TCDS) [9] as a slave partition in the BEE and FEE to obtain the fast control commands (RESET, BC0, SYNC, etc.) and trigger accept signal. Moreover, the AMC13 delivers its readout status to the TCDS to reduce the trigger rate if the readout path of any subsystem is 'busy' and to resume triggering when all subsystems are 'ready.' The VadaTech UTC002 is feature-rich MCH and integrated for managing the whole system, including for SC purposes as the Ethernet switch.

Details regarding the GBF board and the BEB are provided in the next section.

Hardware design

The IHEP trigger group was responsible for the design and development of the Concentration Pre-Processing and Fan-out (CPPF) board [10] for the Phase-1 CMS L1-Trigger upgrade. The CPPF module was successfully commissioned in the CMS data-taking path during Run 2 (2015–2018) of the Large Hadron Collider. The new full-height double-width μTCA standard BEB for the Phase-2 muon upgrade and iRPC readout was modified from the CPPF board by adding a clock fan out daughter board. A block diagram and photograph of the module are shown in Figs. 3 and 4, respectively. The core components on this board are two Field-Programmable Gate Arrays (FPGAs): Kintex-7 for system controlling and clock management and Virtex-7 for

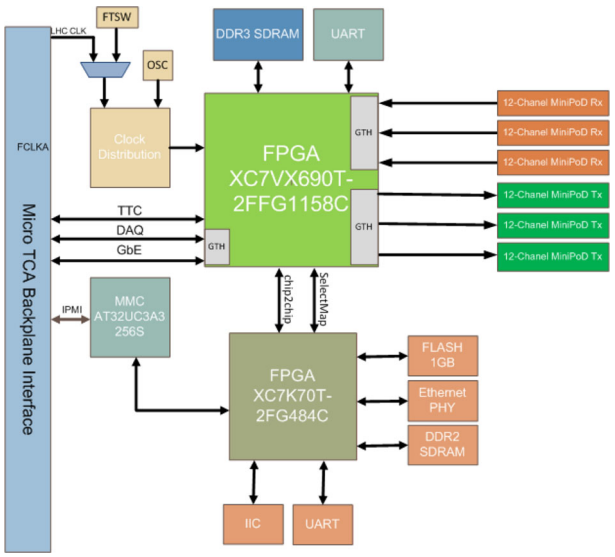


Fig. 3 Block diagram of the BEB

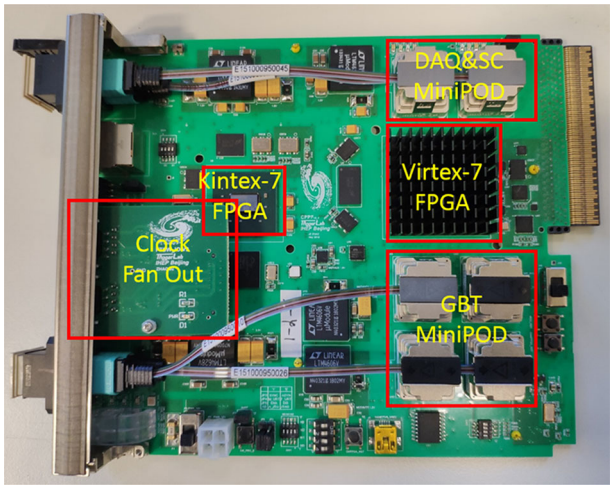


Fig. 4 Photograph of the BEB

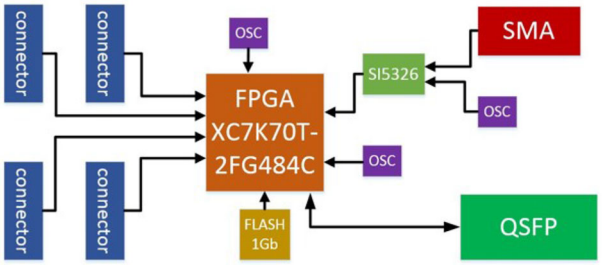


Fig. 5 Block diagram of the GBF board

TTC, SC distribution, and DAQ implementation. A 128MB flash drive was chosen for automatic firmware loading after board power-up. Six Avago MiniPods, three for transmitting and three for receiving, are used. As each minipod integrates 12 fiber links and each fiber supports a line rate of up to 11.3 Gb/s that meets the requirement of 4.8 Gb/s for this system, a total bandwidth of 400 Gb/s is supported by each board.

The GBF was designed to receive the output of discriminator from the on-detector ASICs and provide the time information (coarse time) together with time stamp (bunch counter) and fired strips as input to the GBT block. A hardware block diagram and photograph of this board are shown in Figs. 5 and 6, respectively. The main components on the board are a Xilinx Kintex-7 FPGA, Quad Small Form-factor Pluggable (QSFP) transceiver, jitter cleaner, and flash drive. The main role the FPGA plays is as a Time-to-Digital Converter (TDC) and Giga-Bit Transceiver in FPGA (GBT-FPGA) [11]. The QSFP is a 4-channel high-speed optical fiber interface, compatible with the 4-channel GTH transceivers with a line rate of 4.8 Gb/s in this application. The SI5326 is a configurable clock chip capable of jitter cleaning. It is used to provide a flexible and stable clock distribution solution for both the internal and external clock

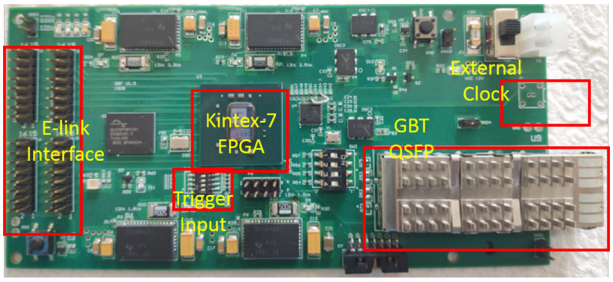


Fig. 6 Photograph of the GBF board

source inputs. Additionally, the flash drive is used to store the firmware and ensure automatic FPGA firmware loading after power-up.

Firmware development

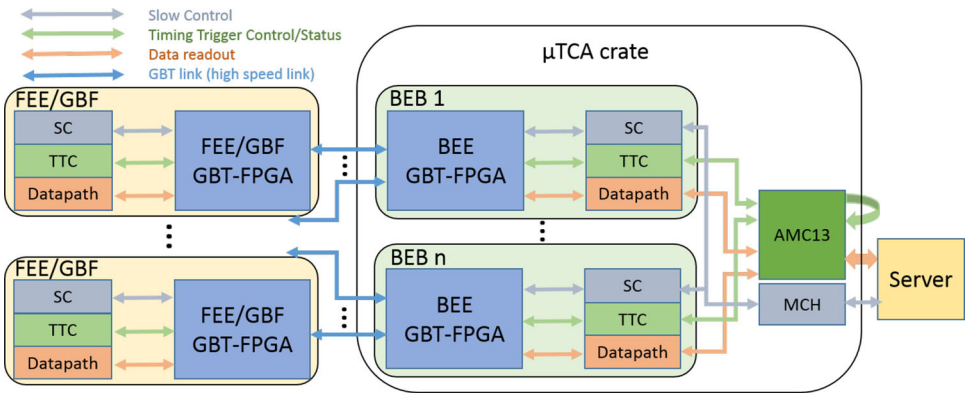
In this research work, the GBF was designed for signal sampling, time measurement, and communication with the BEE which perform the tasks of TTC distributing, SC dispatch, and detector data packing and storage [12]. A unified GBT-FPGA interface was chosen to ensure communication between the GBF and BEE through a bi-directional optical fiber with a line rate of 4.8 Gb/s. All the TTC, SC, and detector data are transferred through this versatile link; a system clock distribution path is also established to ensure a synchronous working mode. Figure 7 shows the functional block diagram of the firmware modules.

Transmission link

The GBT protocol [13] provides an optimized solution for high energy physics experiments with a bi-directional versatile transmission link. In this work, we used the GBT-FPGA Intellectual Property (IP) in both GBF and BEB to implement the combination of detector data, TTC, and SC into one optical link (2 fibers). The GBT frame was chosen for encoding and decoding based on its capability of error detection and correction.

As is shown in Fig. 8, the GBT frame is defined with a 120-bit format at a 40 MHz user clock domain. The 4-bit header is always transmitted at the beginning of each frame to synchronize the serial data. The valid value is defined as '0110' for an idle frame and '0101' for a data frame, keeping the Direct Current (DC) balance under consideration. The 4-bit SC region is dedicated to the execution of control operations, a Time Division Multiplexing method-based SC frame for the user is additionally customized due to the limited bandwidth in each GBT frame [14]. The 80-bit data region is fully customizable by the user; the first 16 bits are used for TTC dispatch, while the remaining 64 bits are defined for the detector data. A 32-bit Forward Error Correction (FEC) trailer is added at the end of the frame to protect the other regions of the frame against transmission errors due to link noise and single event upsets, taking advantage of double error detection and single error correction.

Figure 9 presents the internal dataflow of the GBT-FPGA. On the transmitter side, the data and SC are accepted by a scrambler to ensure the DC balance of the transmission link. The Reed Solomon (RS) encoder was used to provide protection against possible errors during transmission by double error detection and single error correction. The serializer is



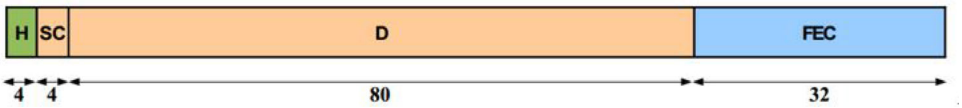


Fig. 7 Block diagram of the firmware modules. Each BEB can be connected with multiple GBF boards

Fig. 8 The GBT frame applied in this readout electronics system. H depicts the bits reserved for the Header, SC is the bit region for slow control, D represents the bits for data, and FEC is for the trailer

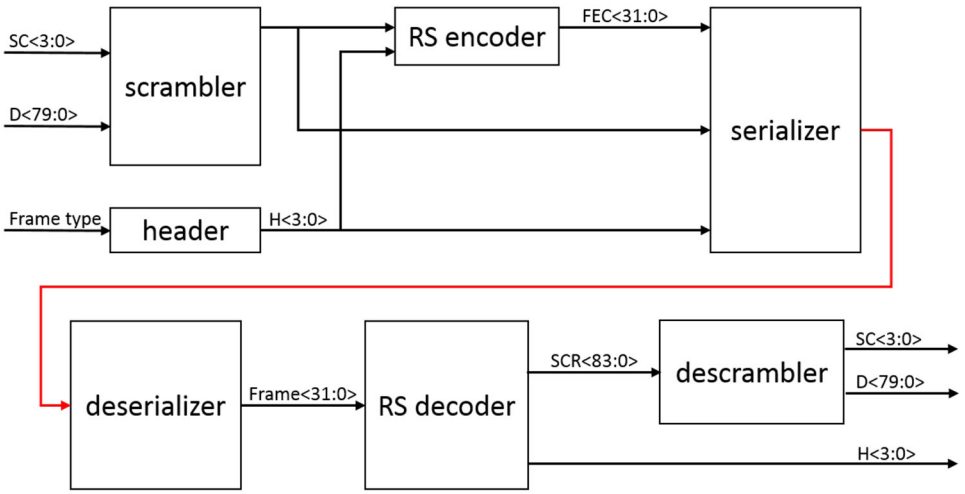


Fig. 9 Internal dataflow of the GBT-FPGA. The top half represents the transmitter, and the bottom represents the receiver

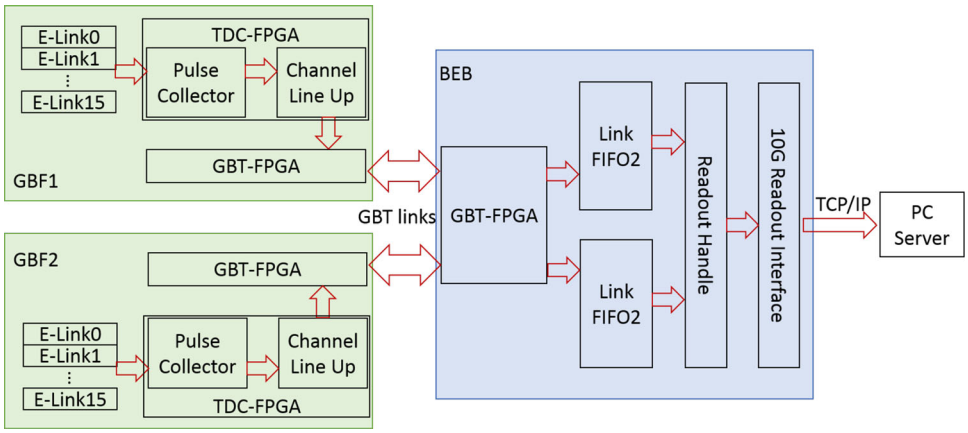


Fig. 10 Functional block and data flow of the readout architecture. The data stream starts from the E-link on the GBF and ends with a server for storage. The two GBF boards interface with the on-detector ASICs of each coordinate, respectively

Table 1 Data format definition for detector data collection with a total of 32 bits. Both the rising and falling edges share the same format but have a different value set for 'edge'

Edge	Board ID	Channel number	Coarse time	Fine time
[31]	[30:29]	[28:24]	[23:8]	[7:0]

responsible for serializing the frames and dividing the 120-bit frame into three parts, leaving the header unchanged, to meet the data width constraint of the GTH IP core. On the receiver side, after being processed by the deserializer, RS decoder, and descrambler, the original data and SC are restored.

Data formatting, packing and saving

The test system readout path, consisting of two GBF boards, a BEB, and a PC server, is sketched in Fig. 10.

A 64-bit data structure is defined in this system to encode the data of the iRPC 2D chamber. Table 1 shows the common 32-bit format for each edge of the signal. The 1-bit edge indicates the rising or falling edge of one signal. The two GBF boards are distinguished by the 2-bit board ID. Five bits are used for the channel number of the 32 input links. The coarse time is composed of a 12-bit bunch crossing number and a 4-bit number of the precise time in a precision of 2.5 ns. The 8-bit fine time region is defined to provide a more precise time resolution in steps of 1/256 ns for the two-end readout, but not for the 2D readout.

The differential signal is generated from the on-detector amplifier and discriminator and then delivered to each GBF board through a 16-channel flat cable. The GBF's clock source is the external 40 MHz system clock distributed by the BEE. A 400 MHz sampling clock is obtained by multiplying the source clock with a well-configured Phase-Locked Loop (PLL), which will be used in the TDC-FPGA to digitize the time with a precision of 2.5 ns. The TDC-FPGA in the GBF records the arrival times of both the rising and falling edges of the input trigger and strip signal in the clock domain of the sampling clock and then lines up all the signals that are captured in a given trigger window in a sequence of channel numbers, regarding the time information of trigger as the header.

The BEE aims to pack the raw data from the two input links (for the joint test) and then store them on a disk. Two

links in the GBT-FPGA are enabled to receive and align the data from each GBF board. After being decoded from the GBT frame, the raw data are temporarily stored in the link FIFO, waiting for concentrating and event packing, which are handled by the readout handle procedure. If they share the same trigger information, data from the two input links are packed together link by link, in spite of the time difference. Finally, the packed event is transmitted by the 10 GbE module via an optical fiber, and stored on a disk for further offline analysis. Figure 11 presents a timing chart of the packing procedure that demonstrates this function.

Fast and slow control

As shown in Fig. 12, the fast control (BC0, RESET, SYNC, etc.) via the AMC13 through the backplane is merged in the BEB together with the slow control command (trigger window set, delay set, etc.) via the MCH respectively, and then transmitted to the processor in the GBF. In the other direction, the status of the fast control (RDY, BSY, ERR, etc.) and the slow control information (trigger window size, delay value, etc.) are delivered via the AMC13 and MCH respectively after being separated by the BEB.

For the fast control, the AMC13 was chosen for the standalone joint test setup; it sends fast control commands to the BEB and then to the GBF through the GBT link. For the slow control, registers on both the GBF and BEB are configured before data taking. The SC frame is defined based on High-level Data Link Control (HDLC) [15] as shown in Fig. 13 and then is separated by the Time Division Multiplex method to the SC region of the GBT frames. To provide the required A8D8 read and write mode between the BEB and the server, a GbE link based on the SiTCP protocol [16] is used. An online SC state machine is defined and several SC transactions, such as E-link polarity set, trigger window size set, desired width set for strip signal, start of data taking, stop of data taking, and delay value setting are executed in sequence from the server to the BEB and then to the GBF via the GBT link. In the other direction, the expected SC responses are collected.

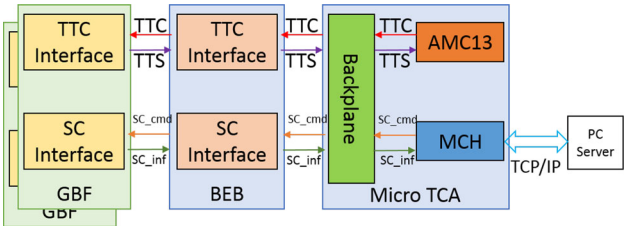


Fig. 12 The loop path for the fast and slow controls in this system

System clock distribution

In-source and in-phase clocks are necessary to ensure the system works synchronously. As illustrated in Fig. 14, the 40 MHz source clock is generated in the AMC13 and delivered to the BEB via the backplane to be fanned out. One of the clocks goes directly to the BEB FPGA as the BEB system clock; the other acts as the input clock for the jitter cleaner to produce the 120 MHz GTH reference clock required by the GBT link. The system clock of the GBF is then generated by a PLL with this GTH reference clock as input and distributed from the clock interface on the BEB. The bit slip provided by the GTH is used to synchronize the clocks. After this procedure that references the 120 MHz clock produced by the jitter cleaner on the GBF is done, the recover clock from the GBF receiver will have the same phase as the BEB reference clock.

By the above distribution method, the data from the two GBF boards may still not be sent out at the same time due to the different lengths of the transmission links. To solve this problem, a measurement of the loopback duration for each link is made and half of the duration time is used to calibrate the time difference by delaying the clock for the shorter link in the BEB.

Hardware tests

The reliability of the hardware interface for high-speed transmission in this design is expressed by Bit Error Rate (BER), which stands for the error bits with respect to the total bits received during a transaction and is a key indicator to evalu-

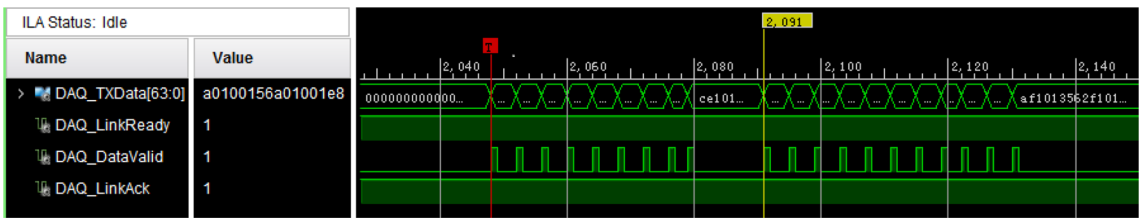


Fig. 11 An ILA capture of a single event readout through the 10 GbE module. By default, data from the orthogonal strips are read out before the longitudinal strips. The Data Valid signal indicates that the strip signals are captured within the trigger window

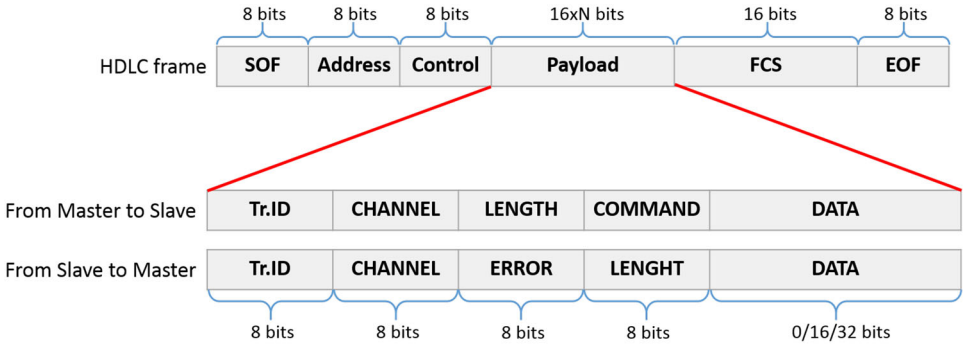


Fig. 13 Diagram of the HDLC-based SC frame. 'From Master to Slave' means from the server PC to the BEB and FEE, while 'From Slave to Master' means from the FEE or BEB to the server

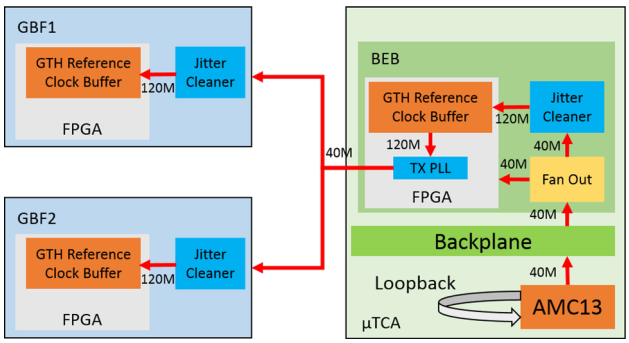


Fig. 14 Diagram of the clock distribution from back-end to front-end

ate the accuracy of data transmission per unit time. During a 167-hour loopback Integrated Bit Error Ratio Tester (IBERT) [17] run, a BER of less than 1.331×10^{-16} with the line rate of 11.3 Gb/s per channel making a total bandwidth of 406 Gb/s per board was obtained, indicating a reliable performance of the hardware. Figures 15 and 16 show the 36-channel BER test results from the IBERT tool in BEB and the eye scan of one of the channels.

A customized method is realized to verify the performance of the applied GBT link. Two 32-bit test data are applied in one GBT frame in the transmitter side and are cross-checked in the receiver side, no error occurred after a 24-hour run, indicating the GBT link is reliable and stable in this research work.

Joint tests

Joint tests with a full-size iRPC 2D prototype chamber were performed [18,19] to verify the functionalities of the readout electronics system, including fast control, slow control, data packing, data saving, and the BEE control capability to the GBF via the GBT link of 4.8 Gb/s. Tests were also made for a detector performance study. Figure 17 shows the joint test setup of the readout system with an iRPC 2D prototype chamber. On the left is the iRPC 2D chamber with 16 strips in the longitudinal direction and 10 strips in the orthogonal direction. Cosmic triggers were provided by two scintillators located above and below the chamber. The trigger rate of the chosen area is around 0.1 Hz. On the right is the testing readout system, including two GBF boards as the data collectors, a BEB, and a server.

Basic tests

To create a working system, efforts were made to locate and remove interference in the experimental hall. Several tests of the low voltages for the on-detector ASICs and high voltage for the chamber were performed to find the appropriate settings. With a high voltage of 7200 V applied to the chamber, the timing profiles of the rising and falling edges of the strip signal, the hit profile along the strips, the 2D profile of the time and hits, and the profile of the signal width were measured for both the longitudinal and orthogonal strips to get an overview of the signal distribution.

After the basic tests were performed, data were taken for the studies of the slow control test and time measurement and muon efficiency, as described in sections "Slow control test and time measurement" and "Efficiency study," respectively.

Slow control test and time measurement

Slow control commands including E-link polarity set, trigger window size set, board ID set, and the desired width of strip signal set have been tested being correct as shown below in the delay adjustment. As the time measurement of the GBF requires the trigger to arrive in advance, the delay adjustment has to be made through a slow control command by delaying the signals respect to the trigger. As shown in Fig. 18, the signal's peak moves corresponding to the delay setting parameters, indicating the slow control of delay setting works correctly. For the left plot, the fitted delay agrees with a setting value of 22.5 ns. For the right plot, the fitted delay agrees with a setting value of 47.5 ns.

For the time measurement, data collected around 2 hours within a trigger window of 100 ns have been used for analysis. A resolution of 3.05 ns has been measured, corresponding to the clock precision of 2.5 ns as shown in Fig. 18.

Name	Status	BER	Loopback Mode
Link Group 0 (18)			None
Link 0	11.300 Gbps	1.331E-16	None
Link 1	11.300 Gbps	1.331E-16	None
Link 2	11.300 Gbps	1.331E-16	None
Link 3	11.300 Gbps	1.331E-16	None
Link 4	11.300 Gbps	1.331E-16	None
Link 5	11.300 Gbps	1.331E-16	None
Link 6	11.300 Gbps	1.331E-16	None
Link 7	11.300 Gbps	1.331E-16	None
Link 8	11.300 Gbps	1.331E-16	None
Link 9	11.300 Gbps	1.331E-16	None
Link 10	11.300 Gbps	1.331E-16	None
Link 11	11.299 Gbps	1.331E-16	None
Link 12	11.300 Gbps	1.331E-16	None
Link 13	11.300 Gbps	1.331E-16	None
Link 14	11.300 Gbps	1.331E-16	None
Link 15	11.300 Gbps	1.331E-16	None
Link 16	11.300 Gbps	1.331E-16	None
Link 17	11.300 Gbps	1.331E-16	None

Name	Status	BER	Loopback Mode
Link Group 0 (18)			None
Link 18	11.300 Gbps	1.331E-16	None
Link 19	11.300 Gbps	1.331E-16	None
Link 20	11.300 Gbps	1.331E-16	None
Link 21	11.300 Gbps	1.331E-16	None
Link 22	11.300 Gbps	1.331E-16	None
Link 23	11.300 Gbps	1.331E-16	None
Link 24	11.300 Gbps	1.331E-16	None
Link 25	11.300 Gbps	1.331E-16	None
Link 26	11.300 Gbps	1.331E-16	None
Link 27	11.300 Gbps	1.331E-16	None
Link 28	11.300 Gbps	1.331E-16	None
Link 29	11.300 Gbps	1.331E-16	None
Link 30	11.300 Gbps	1.331E-16	None
Link 31	11.300 Gbps	1.331E-16	None
Link 32	11.300 Gbps	1.331E-16	None
Link 33	11.300 Gbps	1.331E-16	None
Link 34	11.300 Gbps	1.331E-16	None
Link 35	11.300 Gbps	1.331E-16	None

Fig. 15 BER results from the IBERT tool. A BER of less than 1.331×10^{-16} is obtained. 36 high-speed links in BEB with the GTH maximum line rate of 11.3 Gb/s per channel are achieved, indicating a total bandwidth of 406 Gb/s per board

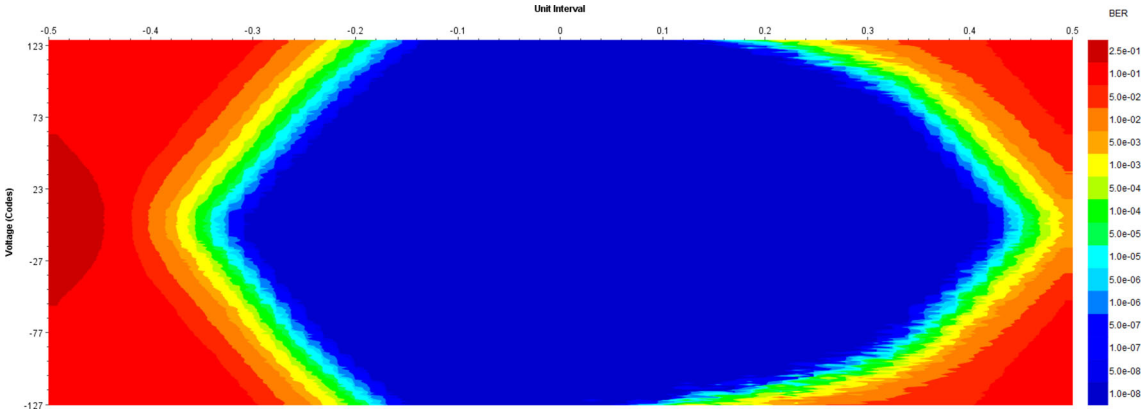


Fig. 16 Eye scan of one of the channels in BEB with an open Unit Interval (UI) of 70.77%. Both the horizontal and vertical increment settings are 1, and the horizontal range is from -0.5 UI to 0.5 UI

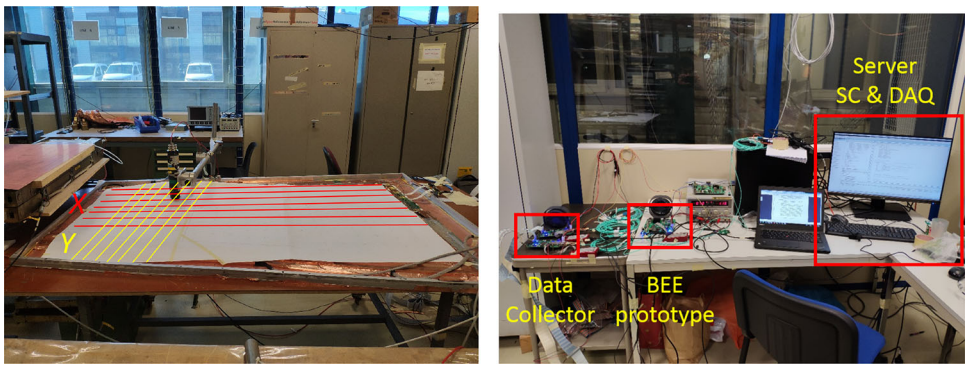


Fig. 17 Joint test setup of the readout system (right) with an iRPC 2D prototype chamber (left). The lines marked with X (Y) denote the longitudinal (orthogonal) strips. Scintillators located above and below the strip overlap region provided cosmic triggers

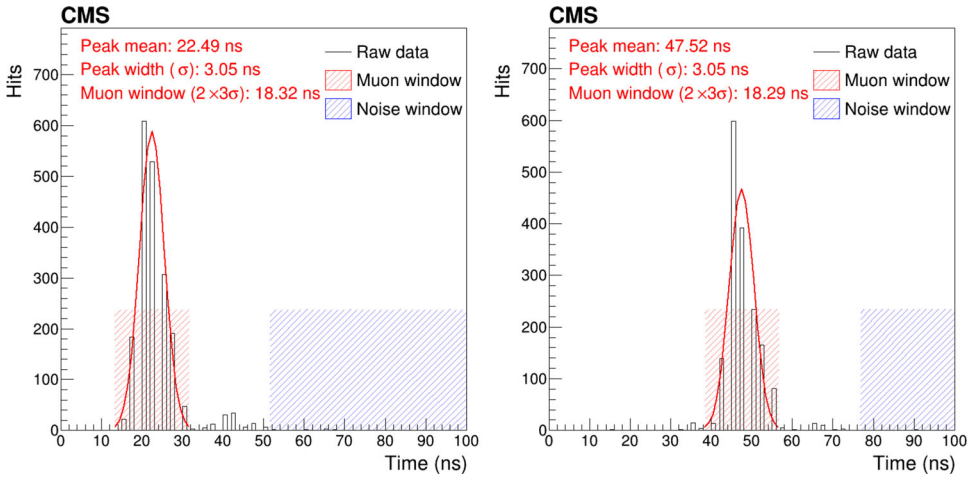


Fig. 18 Slow control with delay adjustment. In the left plot, the fitted delay agrees with a setting value of 22.5 ns. In the right plot, the fitted delay agrees with a setting value of 47.5 ns. The resolution of 3.05 ns is in accordance with the clock precision of 2.5 ns

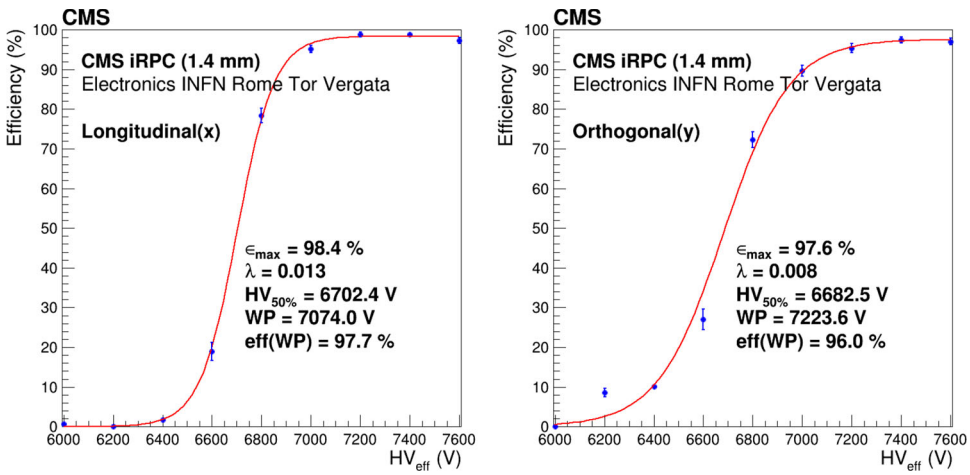


Fig. 19 Muon efficiency curves with fitted parameters obtained by a high voltage scan

Efficiency study

Since at least one hit is expected to be detected for every trigger, the efficiency, which is the ratio between the total number of detected hits and the number of triggers, is a good measurement for evaluating the readout path and, in addition, studying the performance of the 2D chamber. To find out the best Working Point (*WP*) of the chamber, we measured the efficiency with a high voltage scan and fitted the efficiency curve based on the sigmoid function in Eq. (1) [20] to extract the needed parameters. In this formula, λ and $HV_{50\%}$ respectively represent the slope of the curve and the applied high voltage at the point where the experimental efficiency (*Eff*) is half of the maximum value ($Eff_{\max}$). The recommended *WP* is then calculated by Eq. (2) [20], indicating the applied high voltage where *Eff* is 95% of $Eff_{\max}$.

$$Eff = \frac{Eff_{\max}}{1 + e^{-\lambda(HV_{\text{eff}} - HV_{50\%})}} \tag{1}$$

$$WP = \frac{\ln(19)}{\lambda} + HV_{50\%} + 150V \tag{2}$$

Figure 19 presents the muon efficiency curves with fitted parameters obtained by a high voltage scan for both longitudinal and orthogonal strips.

All the active strips of the chamber were successfully read out. For the two-dimensional longitudinal (orthogonal) strips, a working point of 7074.0 (7223.6) V was measured with an efficiency of 97.7 (96.0)%. The result is in accordance with the previous CAEN TDC readout system [20] applied to this iRPC prototype 2D chamber, indicating the reliability of the readout electronics.

Conclusions

The research and development of a prototype Back-End Electronics (BEE) for the two-dimensional (2D) improved Resistive Plate Chambers (iRPCs) in the CMS Phase-2 Upgrade study has been introduced in this paper. The test system has the capabilities of time measurement, timing trigger and fast control, slow control, system clock distribution, and data acquisition with the integrated giga-bit transceiver link. Test result of the bit error rate of less than 1.331×10^{-16} for

the line rate of 11.3 Gb/s per channel providing a total bandwidth of more than 400 Gb/s per board is obtained, proving the new hardware is suitable for the BEE application. Time measurement of a resolution of 3.05 ns and efficiency study scan result demonstrate the BEE fulfill the iRPC 2D readout in the research and development period.

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