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SHANDONG UNIVERSITY

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Status of the Silicon Tracker Project

Sensor proposal: ATLASPix

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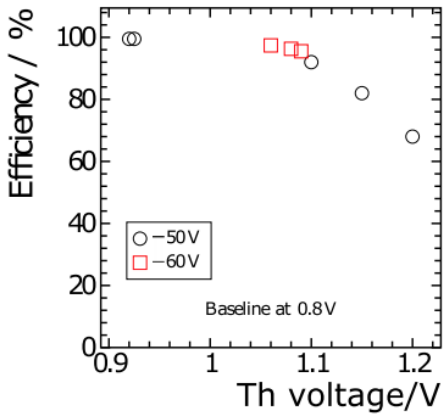
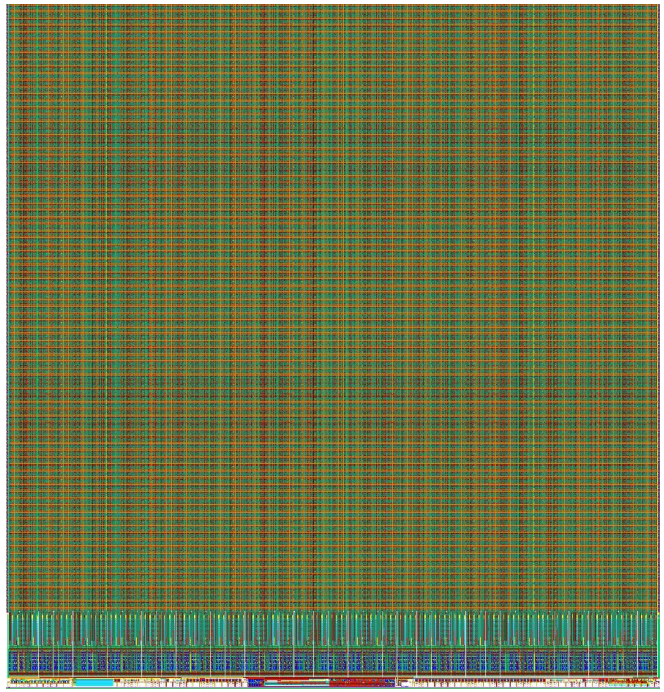
ATLASPix is a CMOS sensor developed to fulfil the requirements for the ATLAS upgrade

- Not strictly an ATLAS development
- **Monolithic CMOS** allows to produce **large** areas **fast** and **cheap**
- No hybridisation – wirebonds or C4NP bumps possible
- **25ns timing** compliant
- Hit efficiency 99.5% (ATLASPix1)
- Pixel size **150 µm by 50 µm** (or smaller)
- Triggered or triggerless readout possible
- 1.28 GBit/s downlink

I. Peric et. al., NIM A924 (2019) 99-103



ATLASPix3



ATLASPix3

- Reticule size: **2.02 cm by 2.1 cm**
- Full-size sensor, ATLASPix3 (TSI, 200Ωcm, 180nm) **available**
- 132 columns with 150µm pixel
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two **end of column (EoC) blocks**. EoC1 is attached to hit buffers and EoC2 to trigger buffers.

Readout Systems: KIT single chip board

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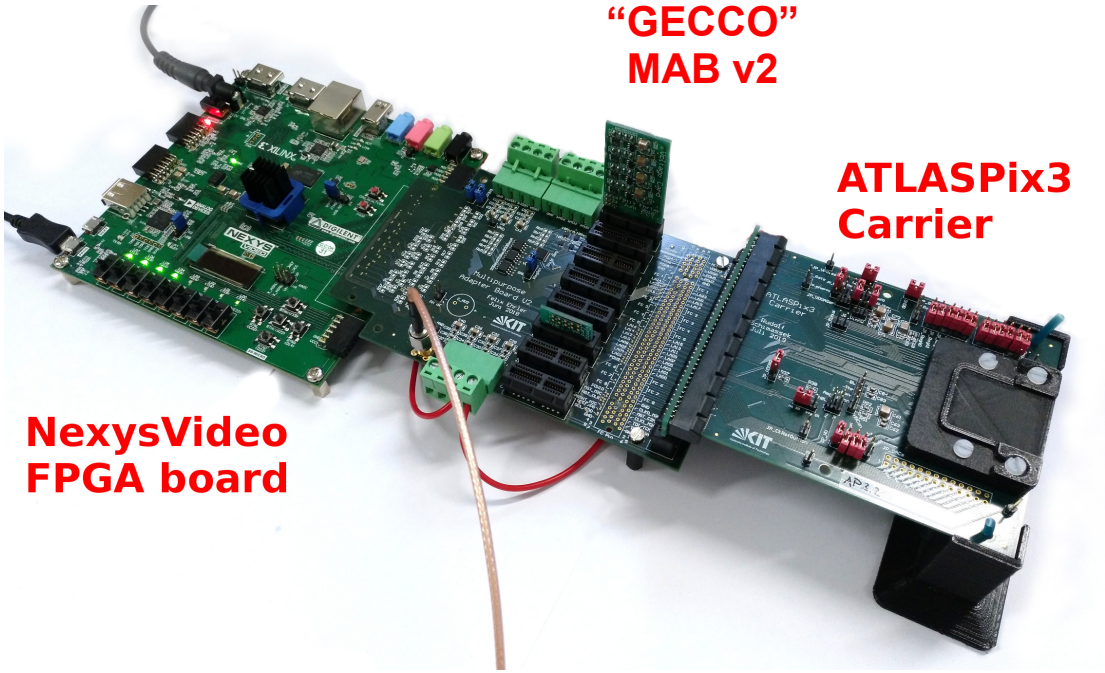
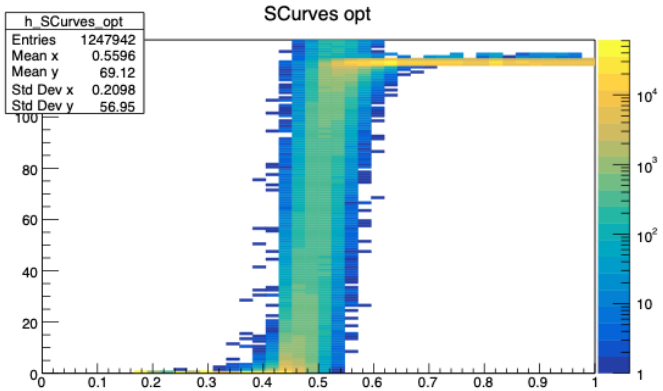
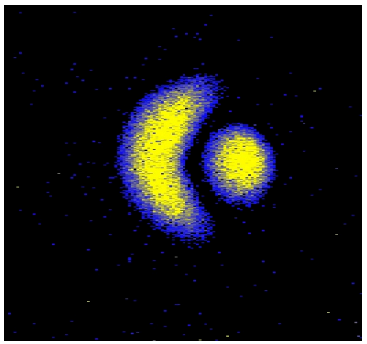
Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests

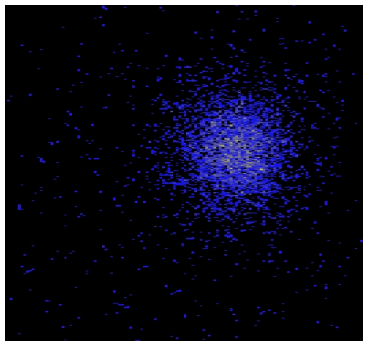




Calibration with S-Curves (injections)

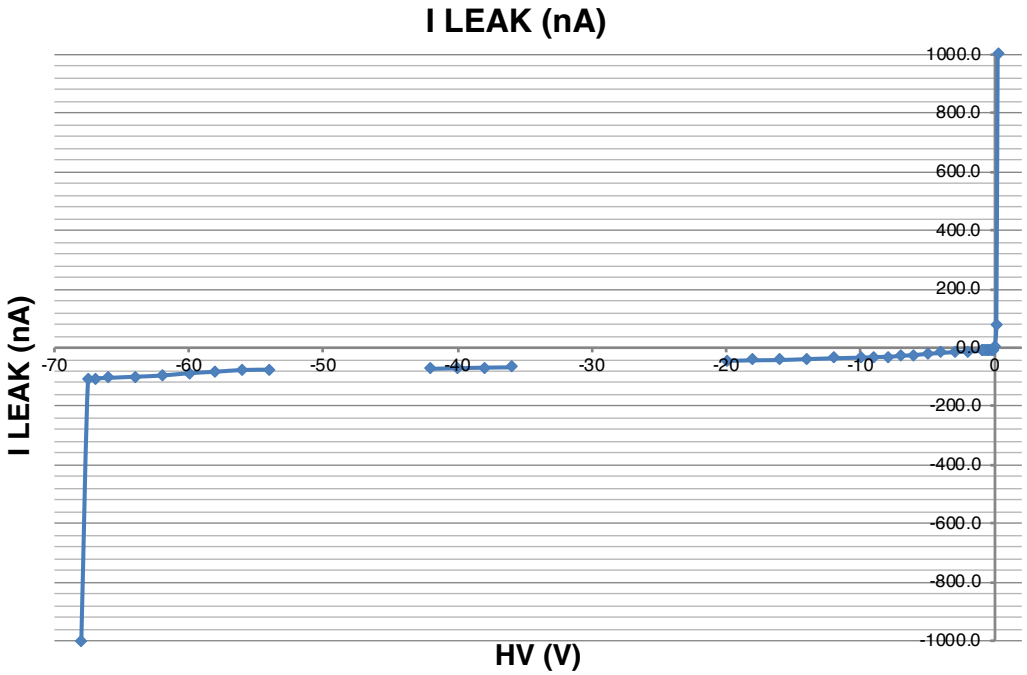


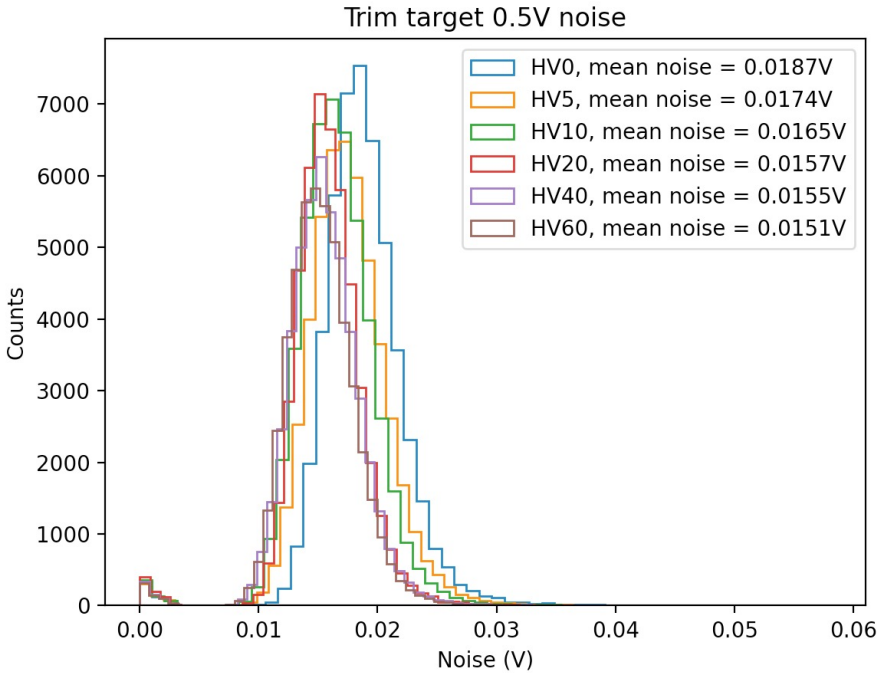
Fe-55 with collimation

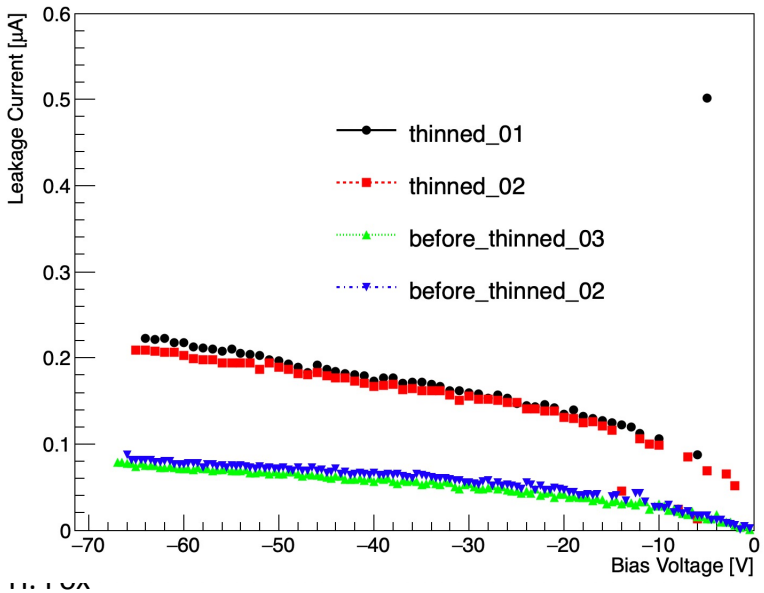


Sr-90 with collimation

IV-curve


I LEAK (nA)
I LEAK (nA)
HV (V)
1000.0
800.0
600.0
400.0
200.0
0.0
-200.0
-400.0
-600.0
-800.0
-1000.0
-70
-60
-50
-40
-30
-20
-10
0


Trim target 0.5V noise
HV0, mean noise = 0.0187V
HV5, mean noise = 0.0174V
HV10, mean noise = 0.0165V
HV20, mean noise = 0.0157V
HV40, mean noise = 0.0155V
HV60, mean noise = 0.0151V
Counts
Noise (V)
7000
6000
5000
4000
3000
2000
1000
0
0.00
0.01
0.02
0.03
0.04
0.05
0.06


Leakage Current [μA]
thinned_01
thinned_02
before_thinned_03
before_thinned_02
Bias Voltage [V]
0.6
0.5
0.4
0.3
0.2
0.1
0
−70
−60
−50
−40
−30
−20
−10
0

Detector calibration

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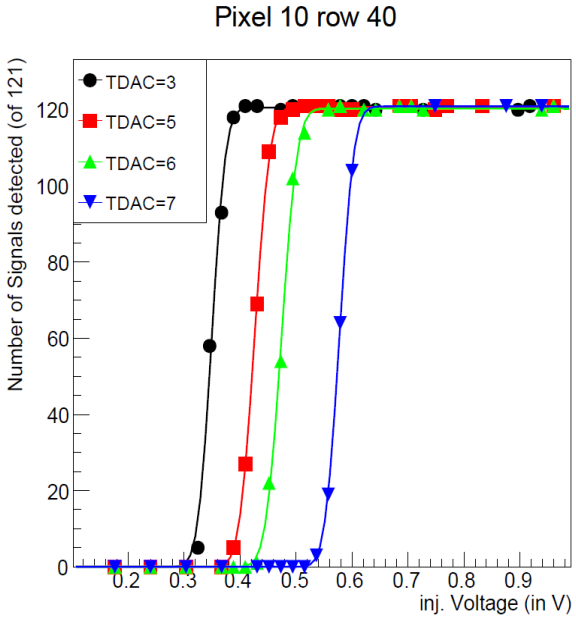
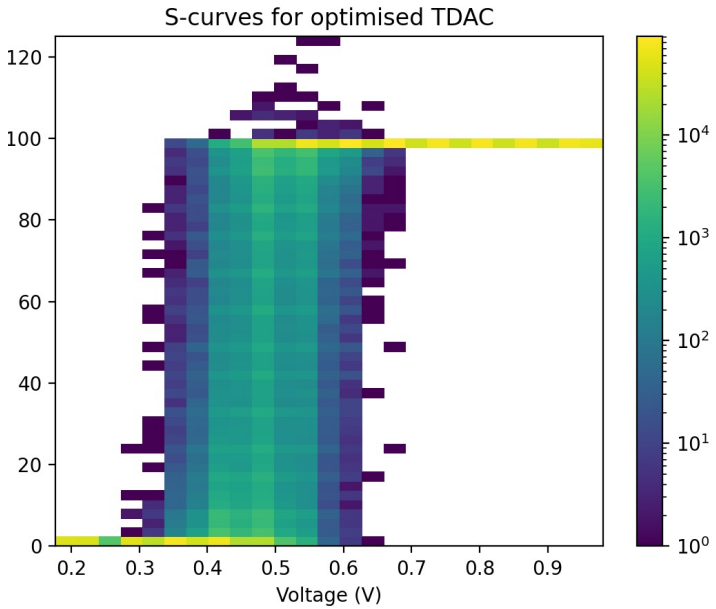
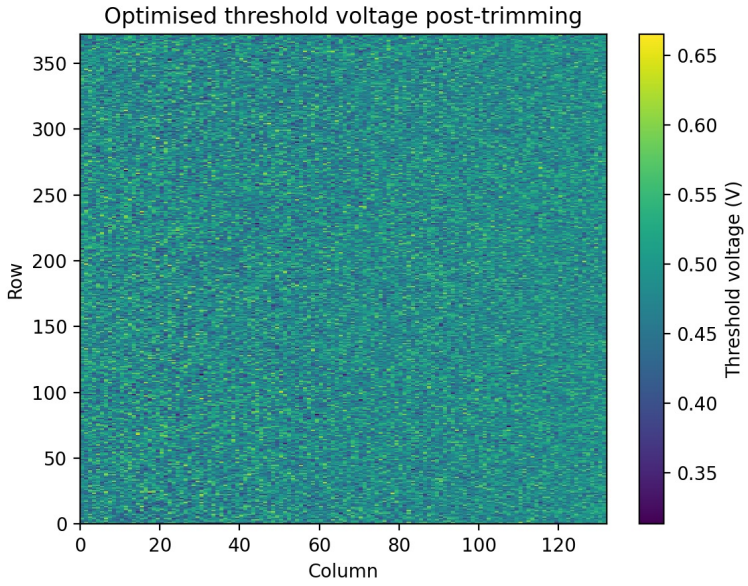
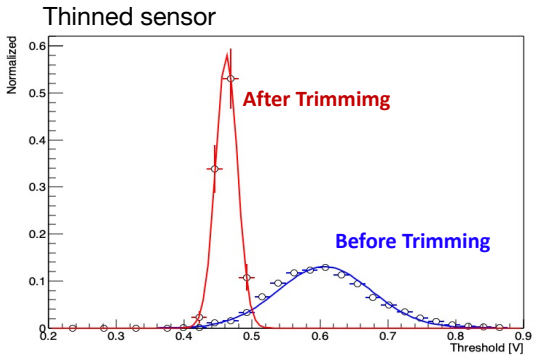
Calibrate the threshold for each pixel relative to a global value, 3-bit TDAC value

Take a number of S-curves (hits above threshold vs injection voltage)

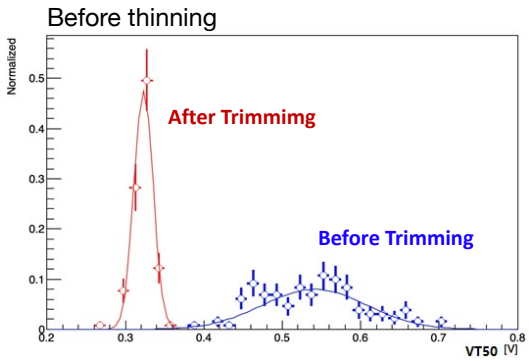




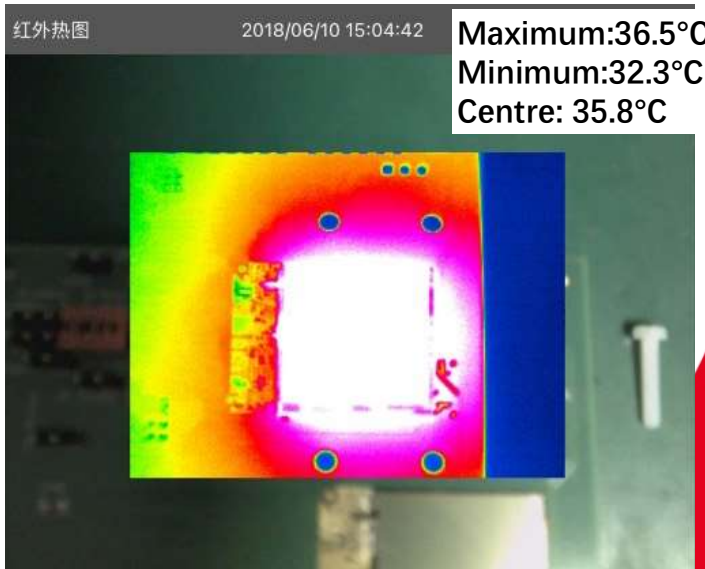




Sigma: **69.30 mV** -> **16.08 mV**



Sigma: **66.31 mV** -> **12.17 mV**



Source Test: γ from Am-241; 150µm thinned chip

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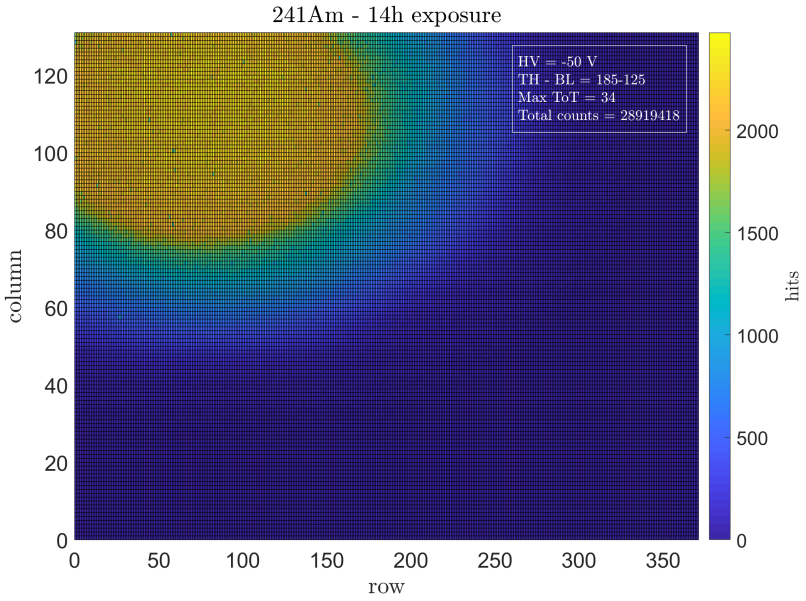
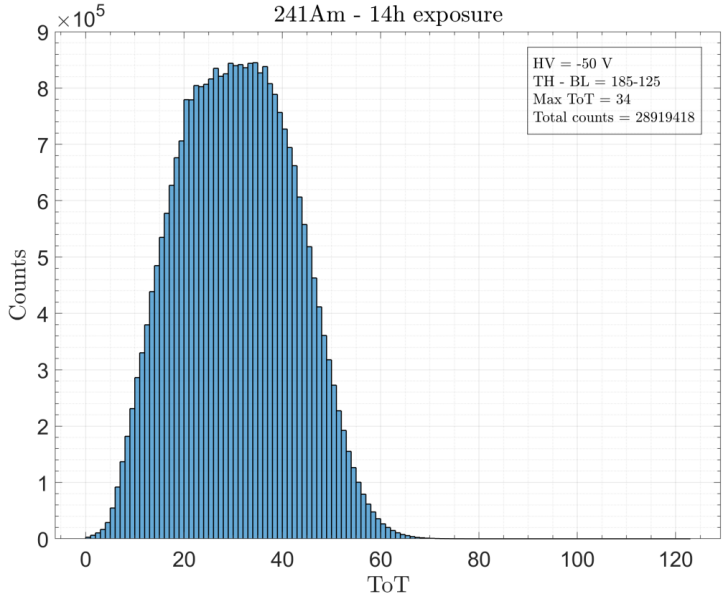
Hit map shows excellent pixel efficiency.

Time over Threshold (ToT) shows a smooth distribution of energy deposits

- No clustering yet
- Threshold target can be lowered closer to the noise level
- ToT needs to be calibrated between pixels.





Source Test: β from Sr-90 (MIP)

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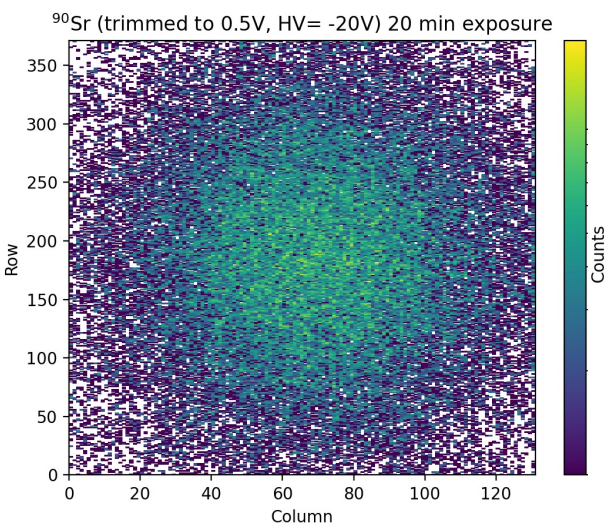
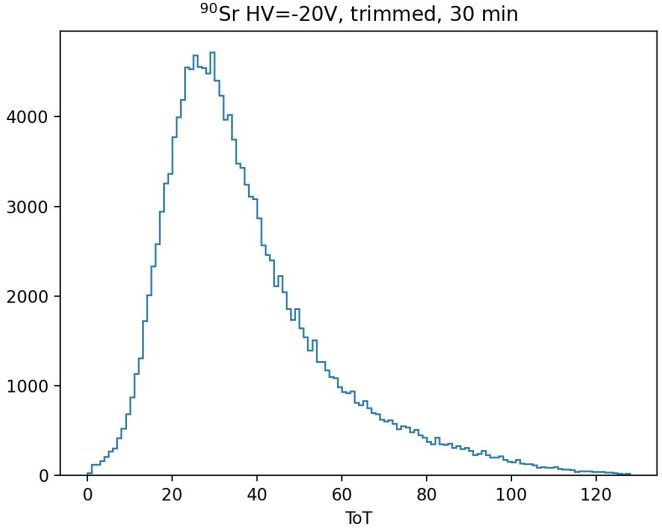
No problems seen in hit map

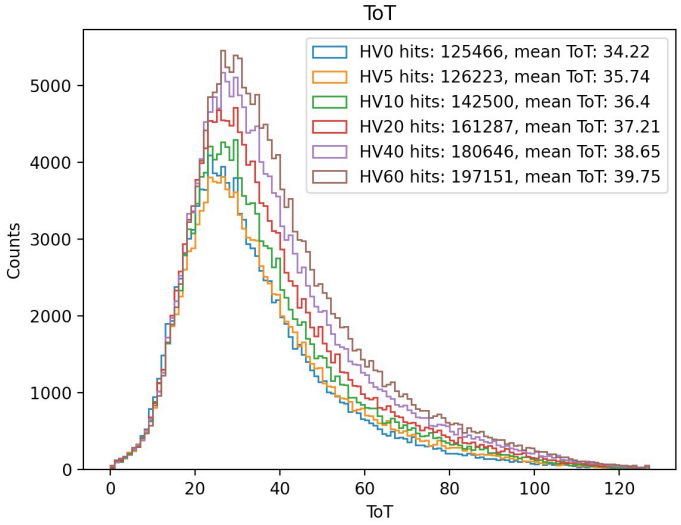
Energy distribution (ToT) has the expected Landau distribution (convoluted with Gaussian)

Behaviour with increasing HV is as expected

No clustering yet



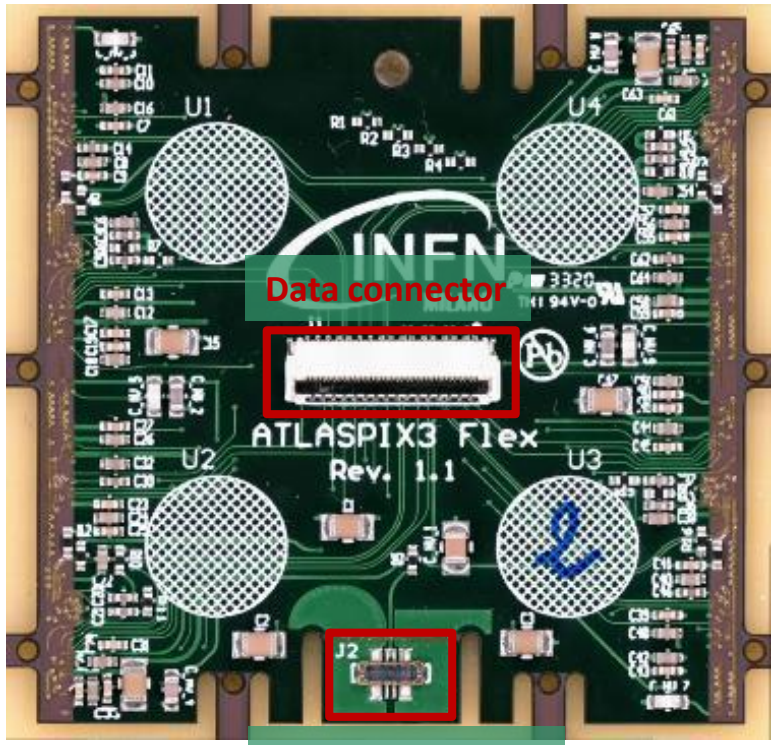


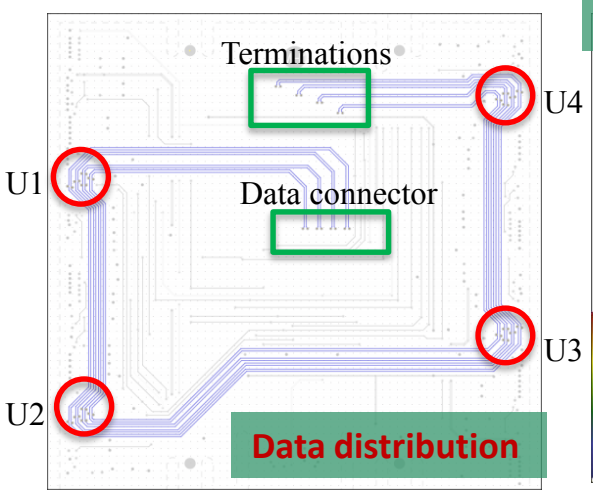


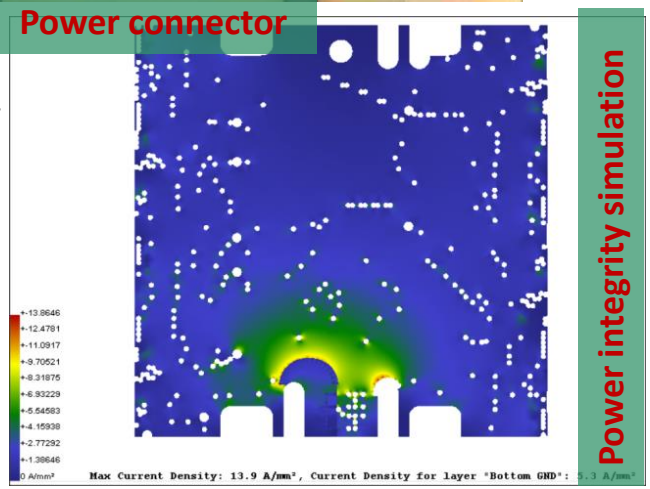
Module concept

- **Readout unit based on 4 chips**
  - shared services among 4 sensors by common power connections and configuration lines
  - benefits of in-chip regulators to reduce connections
  - avoids complications with stitching
- **Two configuration options**
  - command decoder (LVDS, default)
  - SPI (backup)
- **4-layer flex hybrid**
  - 2 power layers
  - 2 signal layers, impedance-matched lines

PCB received
now under verification







Module flex tests (Milano): Setup

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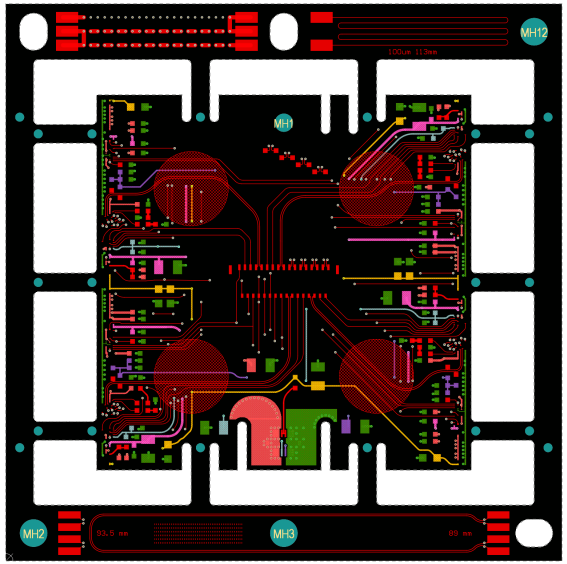
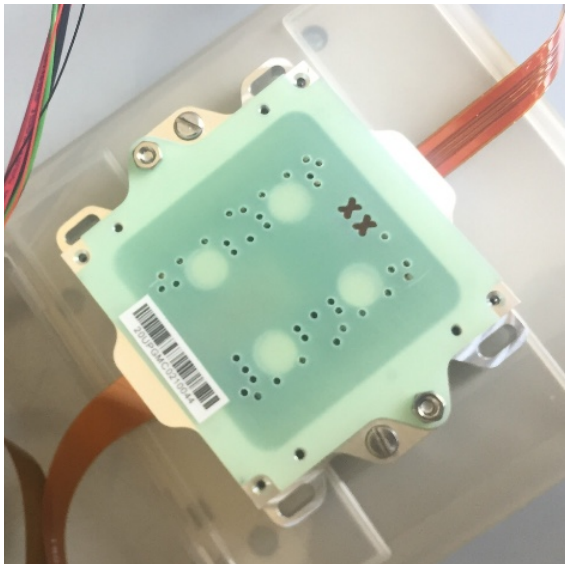
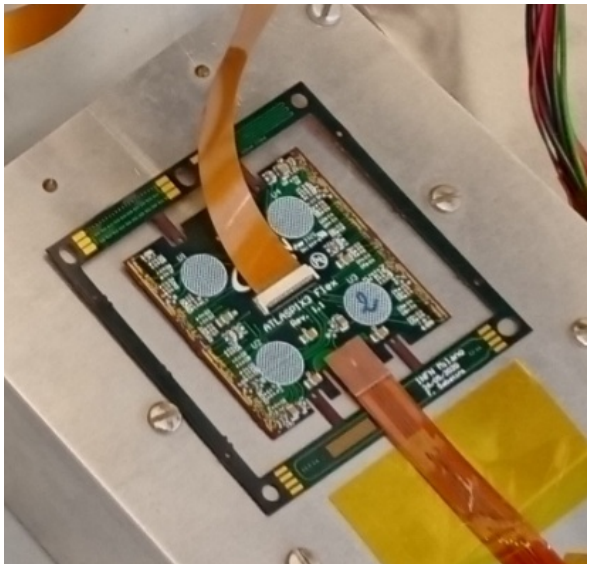
4 chips glued, 2 chips bonded

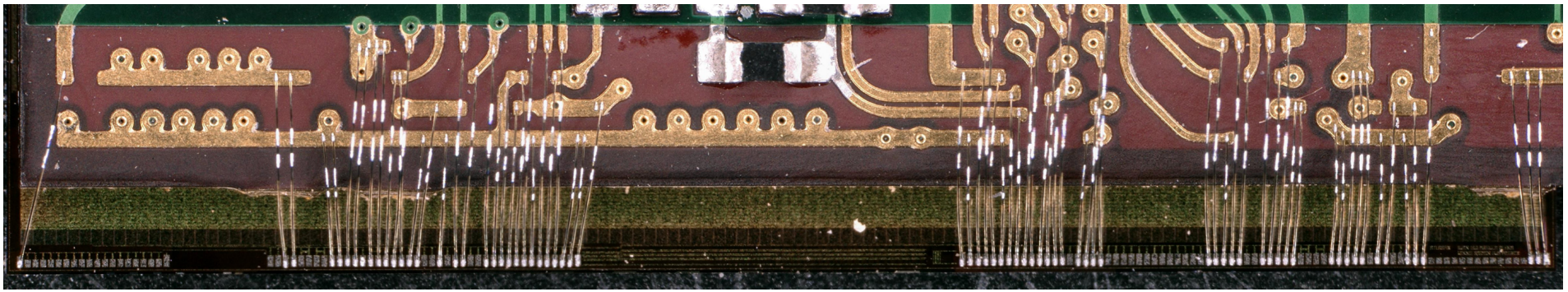
data pig-tail and power pig-tail

config / readout with SPI interface









Module flex tests (Milano): Source test

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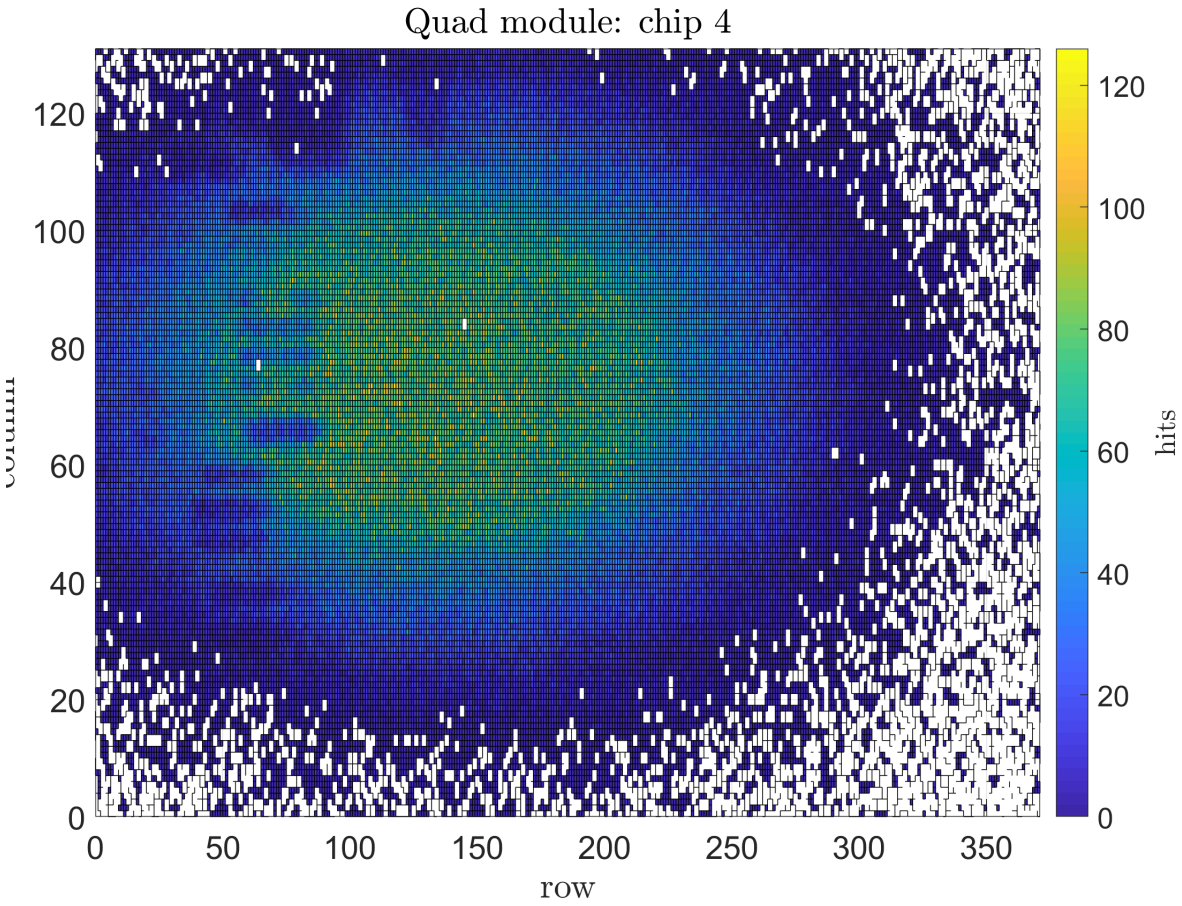
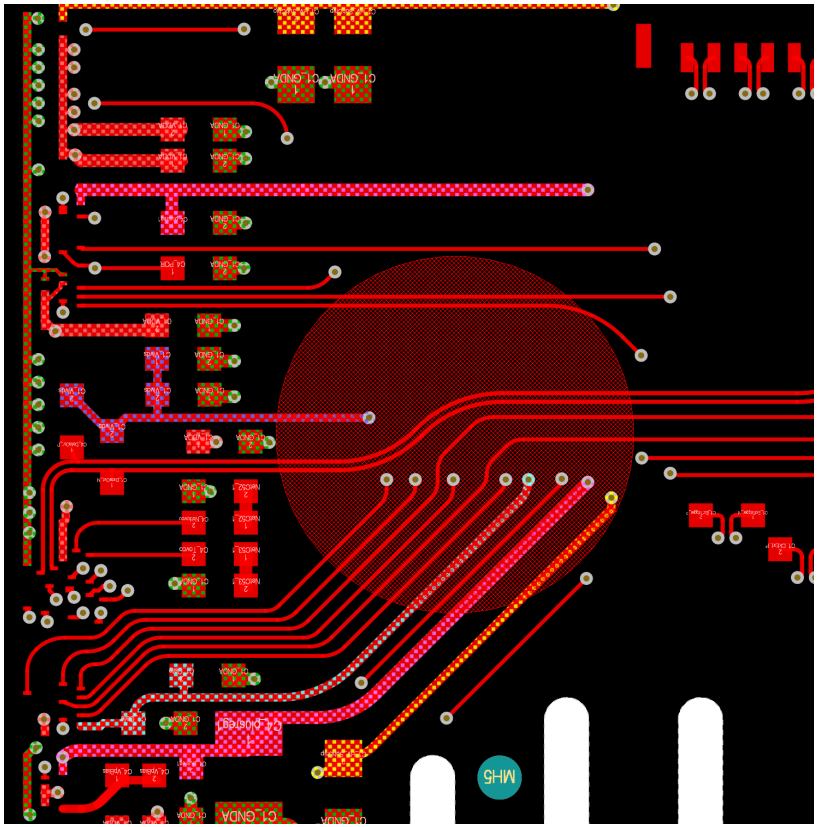
Power characteristics as expected (HV=0). 10 minute source scan with Am-241





Next iteration:

Serial powering using on-chip regulators

Command decoder (clock recovery)

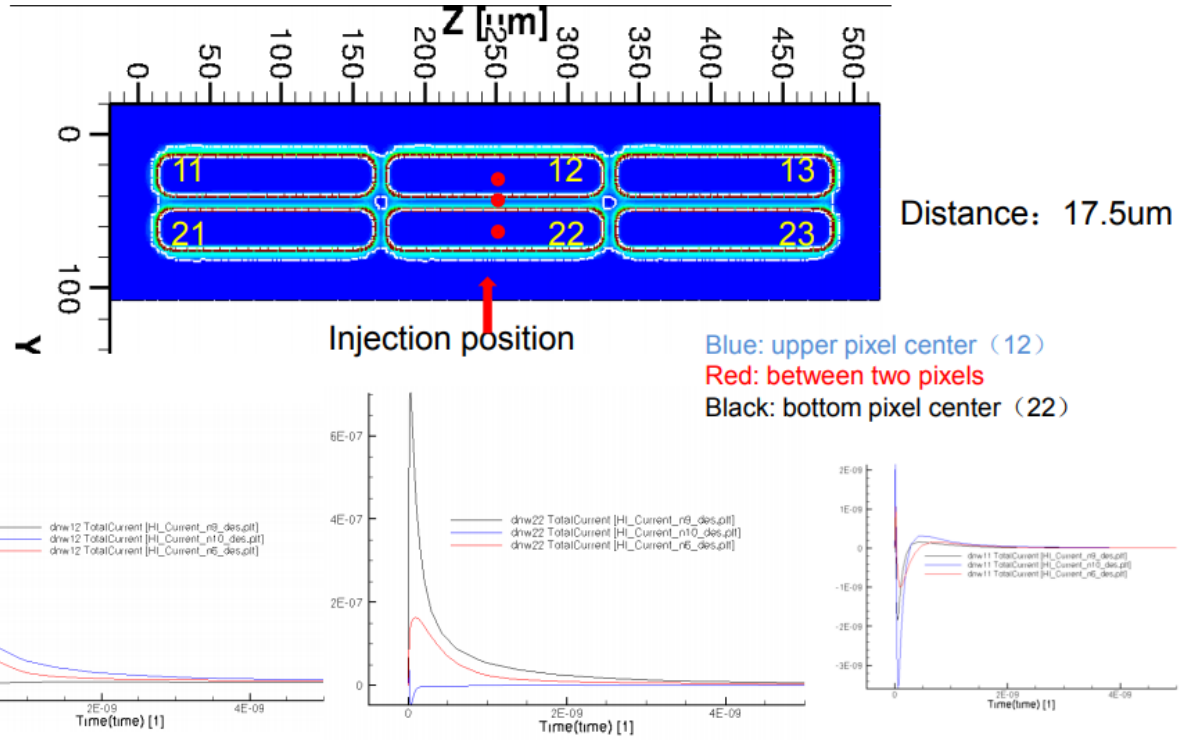
3 ATLASPix3.1 wafers on the way to thinning and dicing

Added stability capacitor to the power regulators

⇒ Needed for serial powering

55nm CMOS Devlopment: Simulation

- 3D Simulation of 6 pixels
  - –25um*100um pixel size, 10um gap, 10Ωcm resistivity
  - –CV simulation, ~100fF per pixel
  - –MIP signal injected sim
- Further sim going on with 3*3 pixel arrays
  - –Different gap size
  - –With or without pstop



55nm CMOS development: Pre-amp design

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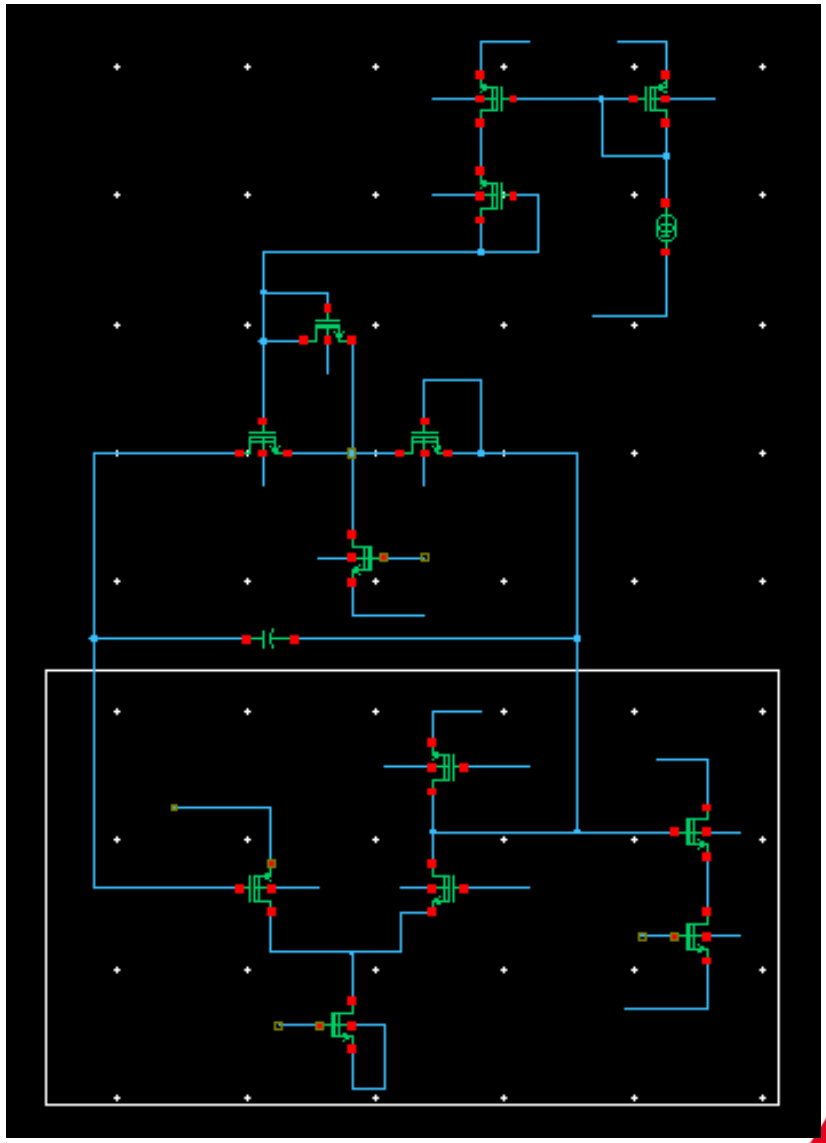
- Two types of pre-amp proposed, one is with 3.3V transistors, the other with standard 1.2V
- Charge Sensitive Amplifier
  - –Classic folded-cascode amplification stage
  - –Active feedback circuit
  - –Leakage current compensation
- Schematic almost fixed, layout and further sim ongoing



Conclusion and Outlook

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Made good progress on understanding and operating ATLASPix3

Work in progress / todo:

- Clustering of pixel hits
- Threshold optimisation and ToT calibration
- Laser test; Temperature dependence
- Radiation hardness
- Beam test with telescope

Moving towards a module that is a building block for larger units

- Work on full module readout
- Serial powering
- Command decoder

Bespoke development of 55nm HV-CMOS with Chinese foundry

- Finalise design choices and implementation
- Next submission possible in December

Backup