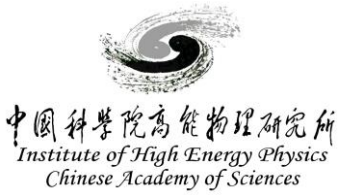
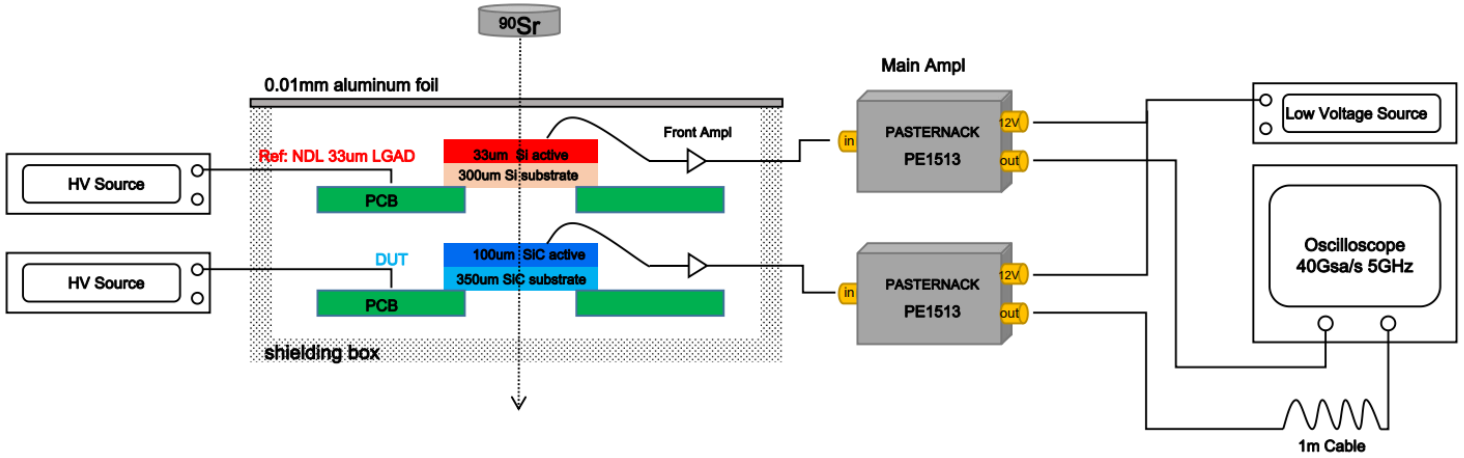
Introduction of IHEP Beta source system



Tao Yang

2021-9-27

Beta source system setup to measure time resolution



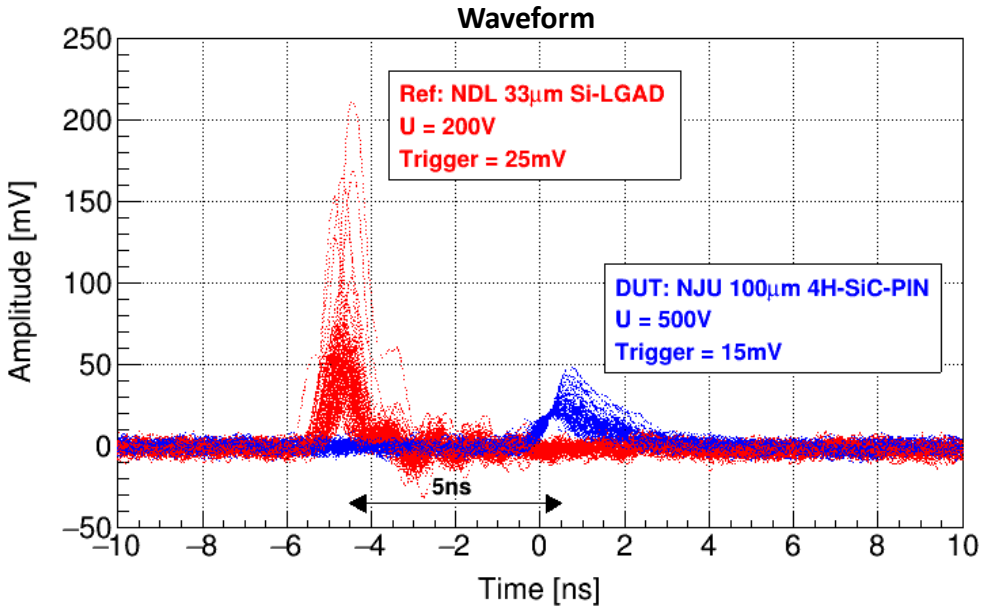
Ref: NDL 33 μm Si-LGAD $\sigma_T = 34$ ps U=200V at room temperature

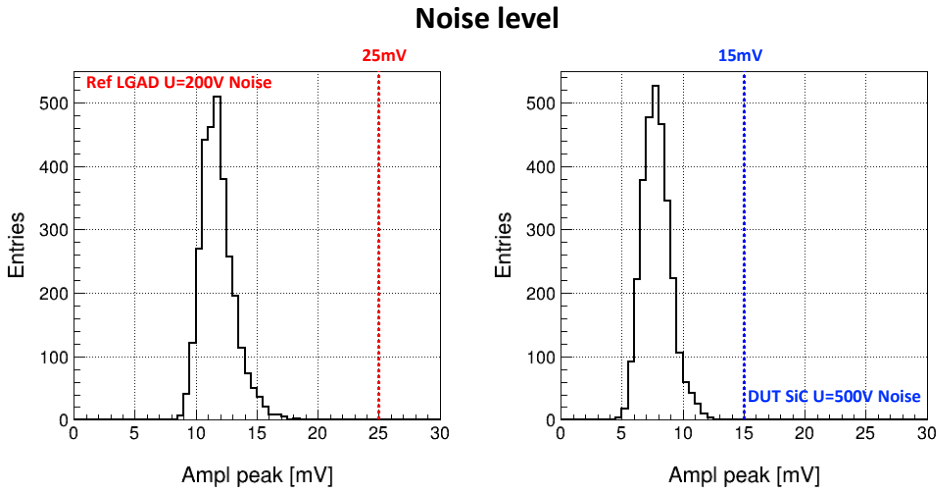
DUT: NJU 100 μm 4H-SiC-PIN 5mm×5mm, 1.5mm×1.5mm

System configuration:

- 2 channels trigger mode: $Trigger_{LGAD}$=25mV, $Trigger_{SiC}$=15mV which depend on noise level.
- DUT time delay: ~ 5 ns from 1 meter cable to enhance trigger efficiency.
- Sampling: 20 Gsa/s each channel where $\sigma_{TDC} = \frac{50ps}{\sqrt{12}} \sim 14ps$
- Timer: Constant Fraction Descriminator (CFD ratio = 50%)
- Amplifier: 100 times from (UCSC board + Broad Band Amplifier)

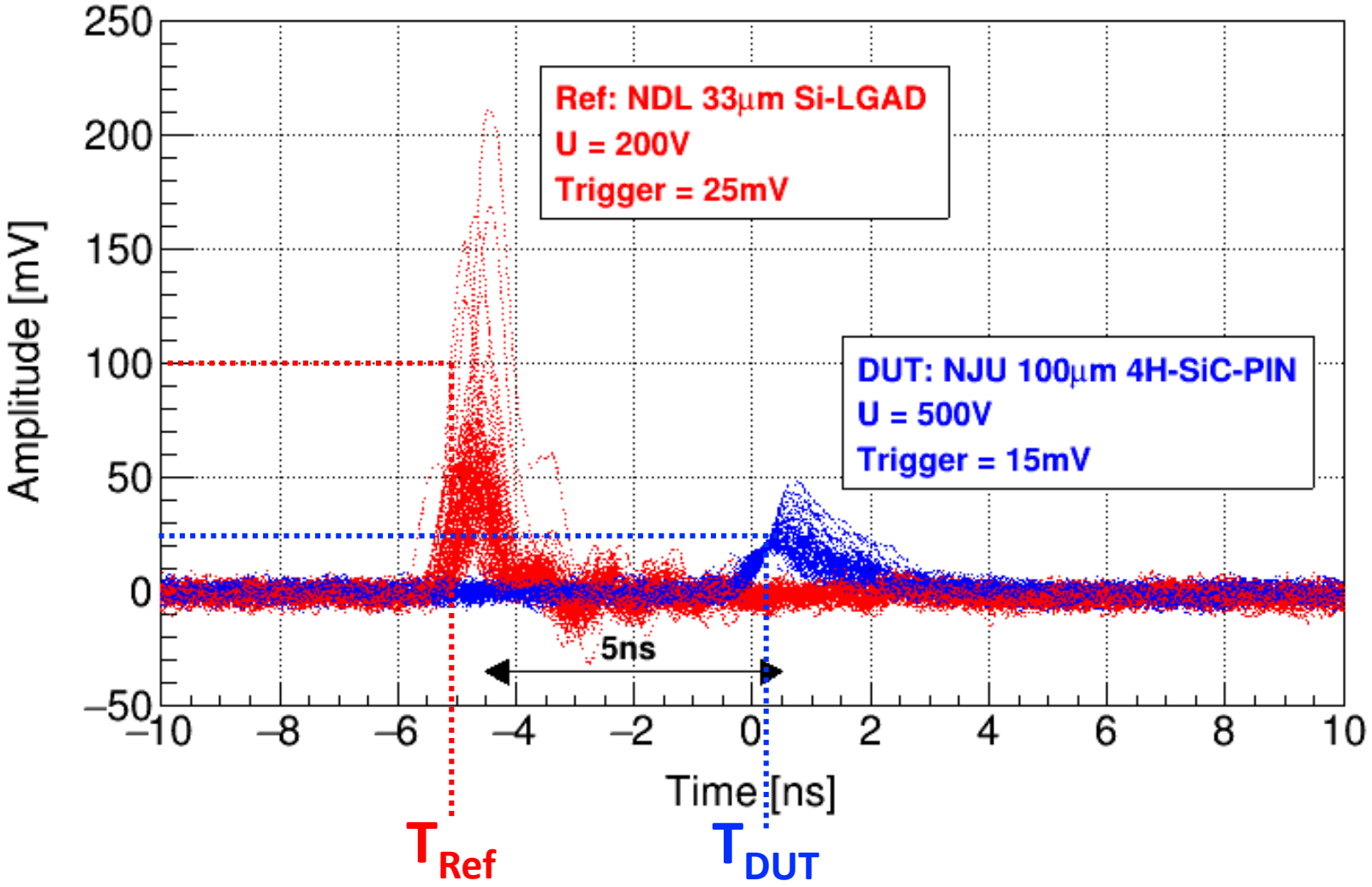
Waveform sampling





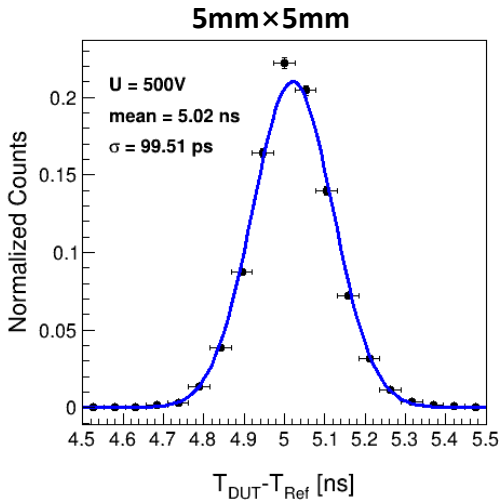
- Select the trigger level to suppress noise.
- Tow obvious pulses from Ref and DUT device by β particle.
- ~ 5ns time delay of 4H-SiC PIN signal.
- **The most of signals for 4H-SiC PIN are lost due to high trigger level .**

Constant Fraction Descriminator (CFD)

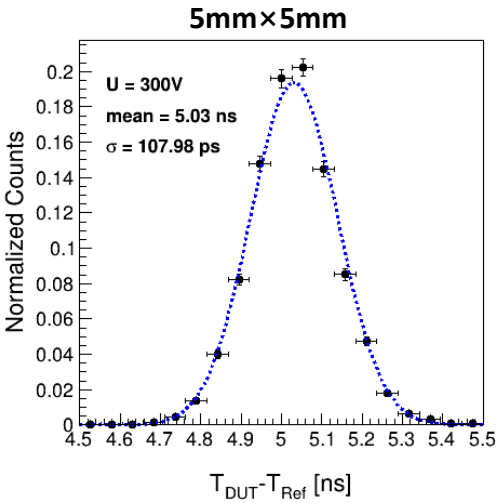


Time Resolution

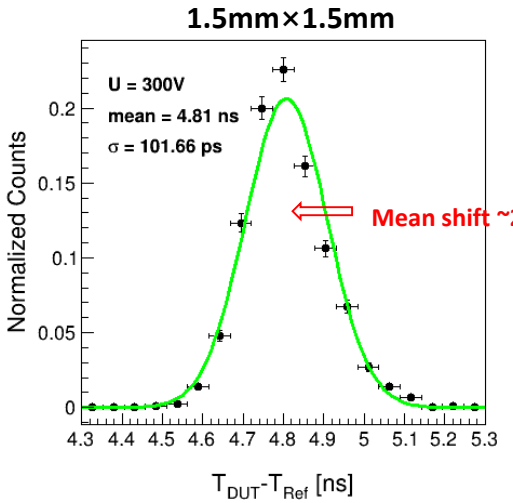
For large size 100 μm 4H-SiC PIN device, the measured time resolution could be smaller than 100 ps.



σ_{DUT} =93.5 ps



$\sigma_{DUT} = 102.5$ps



$\sigma_{DUT} = 95.8$ ps

- Higher reverse voltage (faster carrier velocity) has better time resolution.
- Smaller size device (smaller capacitance) has better time resolution.
- The T_{DUT}-T_{Ref} mean of the 1.5mm×1.5mm device shifts around 200 ps caused by smaller rising time.

Thanks for your attention

Backup

➢ Time shift caused by rising time for different size sensors

The T_{DUT}-T_{Ref} mean of the 1.5mm×1.5mm device shifts around 200ps due to faster rise time than the 5mm×5mm size device.

