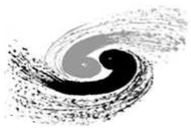
R&D status for vertex detector prototype

Zhijun Liang (IHEP)



中国科学院高能物理研究所

Institute of High Energy Physics
Chinese Academy of Sciences

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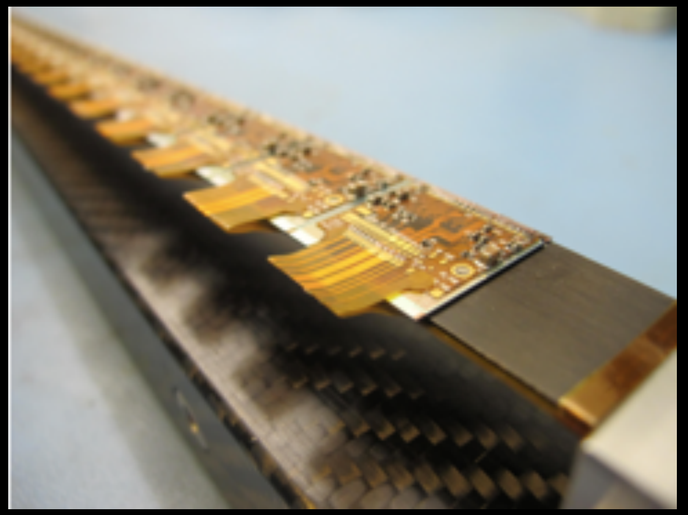
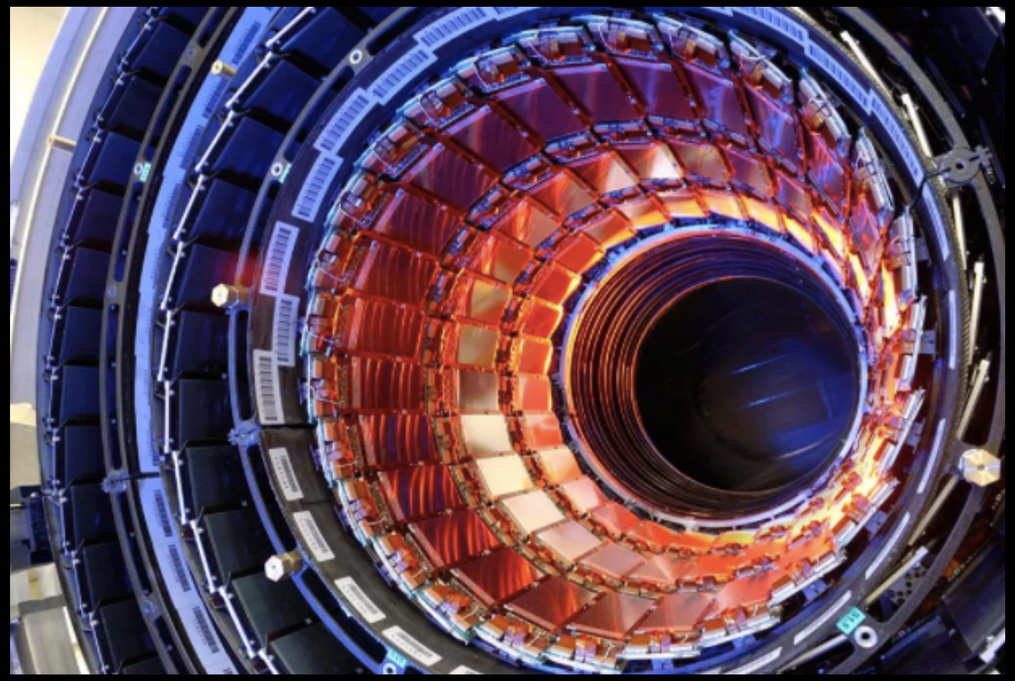
MOST2 vertex detector R & D: Research Goal

- Produce a world class vertex detector prototype
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (>1 MRad)
- Preliminary design of prototype
  - Three layer, module ~1 cm × 12 cm^2

Typical module



Typical tracker



Resolution

ATLAS/CMS upgrade
（~15 μm）

Alice upgrade
（5~10 μm）

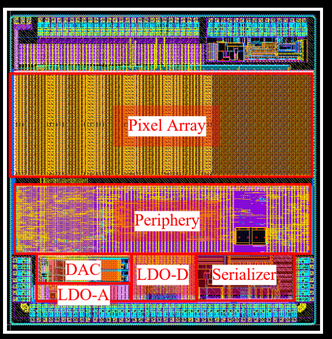
World leading

This project（3~5 μm）

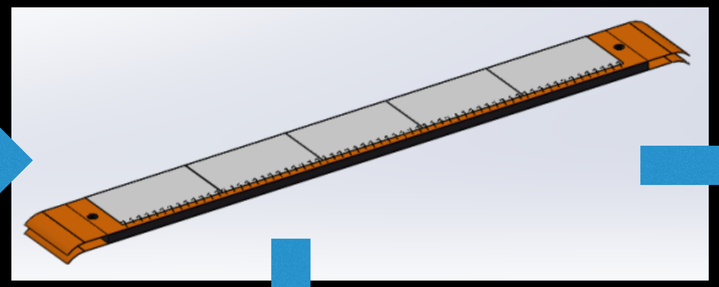
Overview of task2： vertex detector R & D

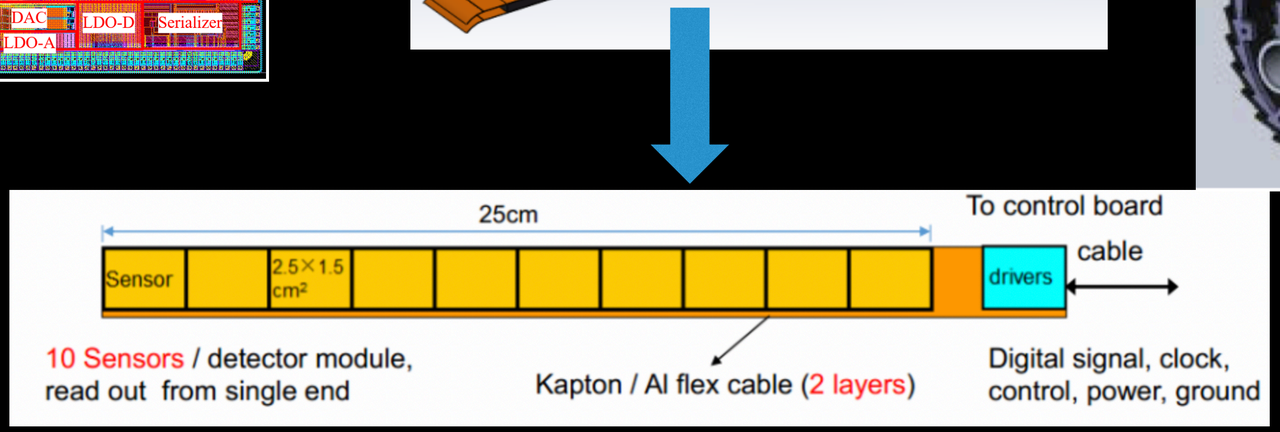
- Can break down into sub-tasks:
  - CMOS imaging sensor chip R & D
  - Detector layout optimization, Ladder and vertex detector support structure R & D
  - Detector assembly
  - Data acquisition system R & D

CMOS imaging sensor prototyping

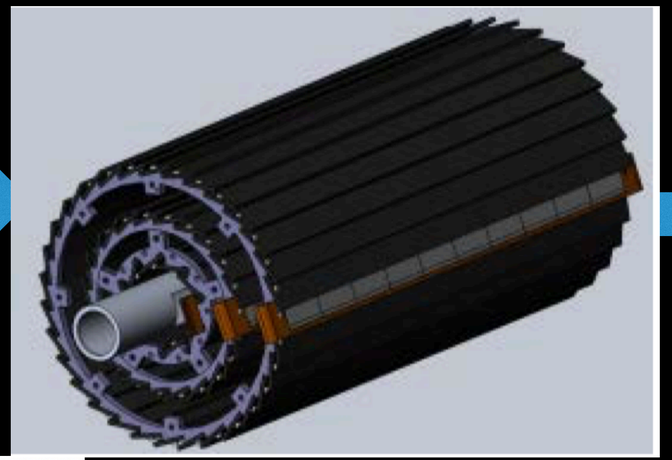


Detector module (ladder) Prototyping

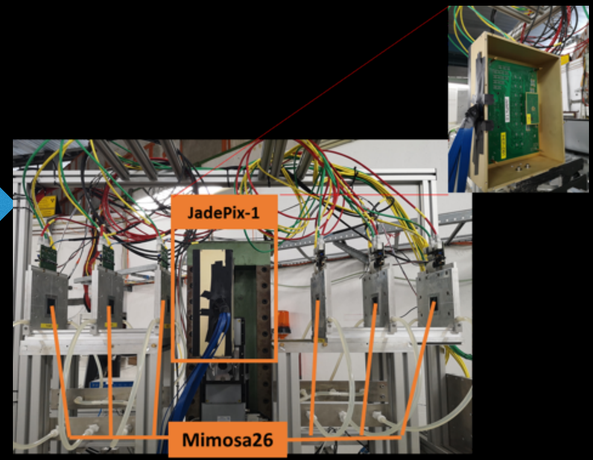




Full size vertex detector Prototype



Beam test to verify its spatial resolution



Achievement Presentation and Assessment Methods

Silicon Detector

考核指标[2]				考核方式(方法)及评价手段[4]
指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	
硅径迹探测器原型机的空间分辨率	无	研制出小型传感器芯片，像素单元尺寸小于或等于25微米 ×25微米。	3-5微米	同行专家评审。(通过束流实验，离线分析数据获得空间分辨率。该测试结果写入原型机设计与测试报告，以供同行专家评审)
所设计的抗辐照硅传感器能承受的总剂量	无	完成传感器的初步设计，通过仿真初步验证其抗辐照性能	1 MRad	同行专家评审 (提供传感器的设计与测试报告供专家评审)

Assessment index

Spatial resolution

- Mid-term: produce **25*25 μm** pixel size chip
- Final : **3-5 μm** resolution in **Beam test**

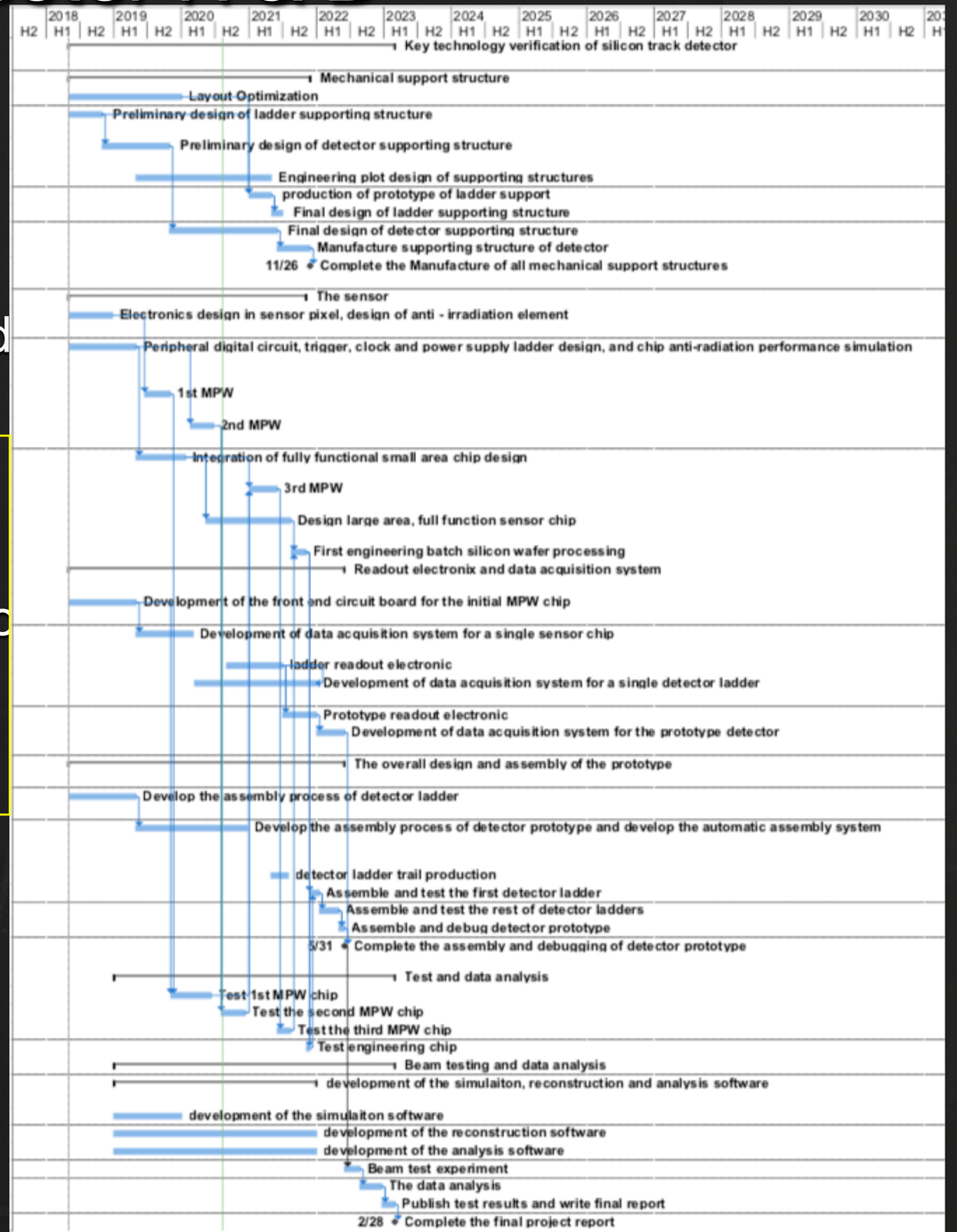
Radiation hardness

- mid-term: verified by TCAD simulation
- Final : Total ionization dose **>1 Mrad**

Overall plan of task2： Vertex detector R & D

- 3rd Year:
  - 3rd CMOS sensor fabricated and tested

  → skipped , since 2nd MPW chip is working well
  - Final support structure engineering design completed
  - Fabricated support structure prototype for ladders
- 4th Year (2021.7 –2022.6) :
  - Competed R & D full-size TaichuPix sensor
  - Manufactured the support structure for whole detecto
  - Assembling and installing the detector prototype
  - Completed DAQ system for whole detector
- 5th Year:
  - Completed detector assembly and commissioning
  - Test beam and data analysis
  - Finish assembling of prototype



CMOS Sensor chip R & D

- The existing CMOS monolithic pixel sensors can't fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - High readout speed (<500ns deadtime @40MHz at Z pole) -> for CEPC Z pole high lumi
  - Radiation tolerance **(per year):** 1 MRad

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

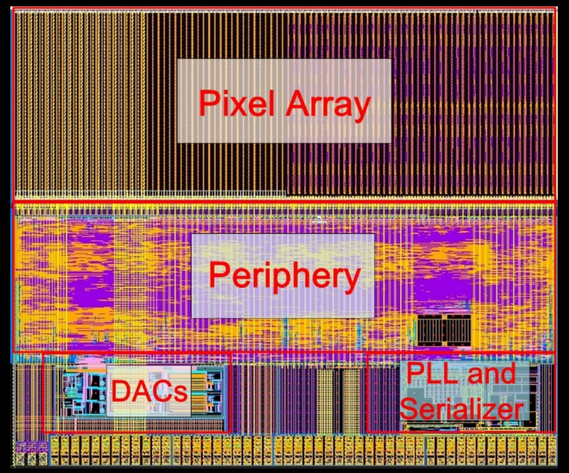
Sensor prototyping

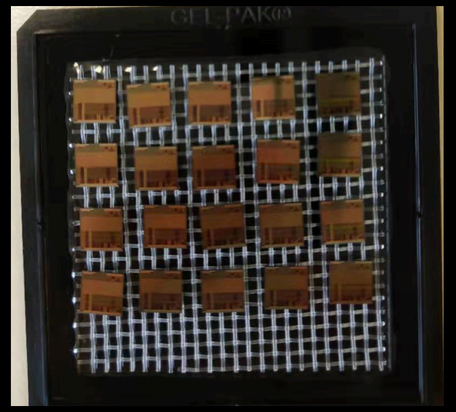
- Completed two round of sensor prototyping
  - 1st Multi-wafer project chip (Taichupix1)
    - Submitted in June 2019, received in November 2019
  - 2nd Multi-wafer project chip(Taichupix2)
    - Submitted in Feb 2020, received in July 2020
    - Major bugs fixed in Taichupix1
    - Radiation hard design (enclosed gate) in pixel analog
    - A full functional pixel array (64×192 pixels)
    - Periphery logics
      - Fully integrated logics for the data-driven readout
      - Fully digital control of the chip configuration
    - Auxiliary blocks for standalone operation
      - High speed data interface up to 4 Gbps
      - On-chip bias generation
      - Power management with LDOs

Taichupix1

Chip size：5mm×5mm

Pixel size：25μm×25μm

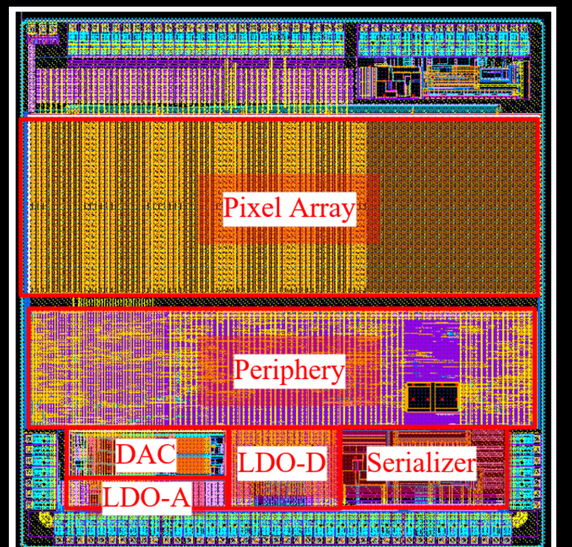




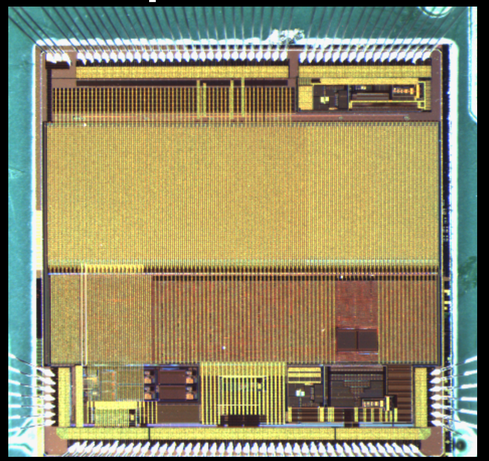
Taichupix2

Chip size：5mm×5mm

Pixel size：25μm×25μm



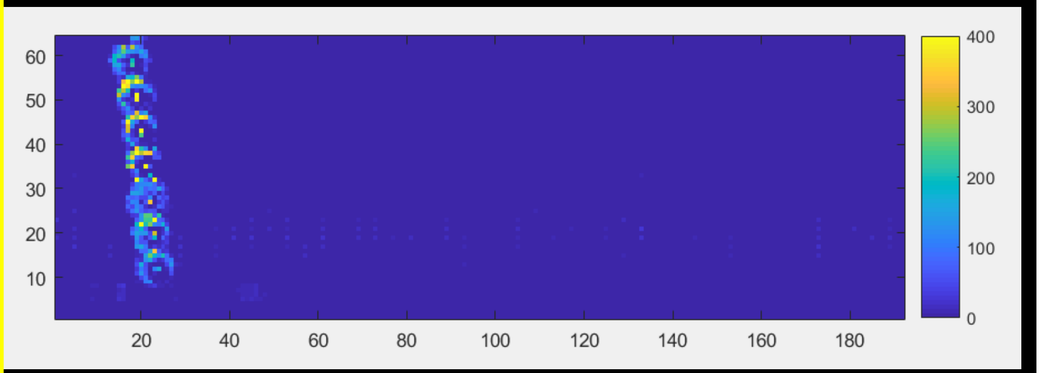
Taichupix2 on test board

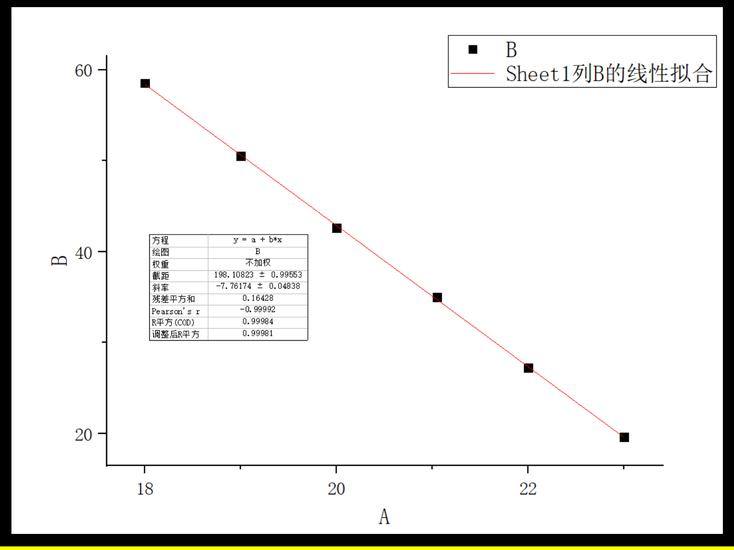


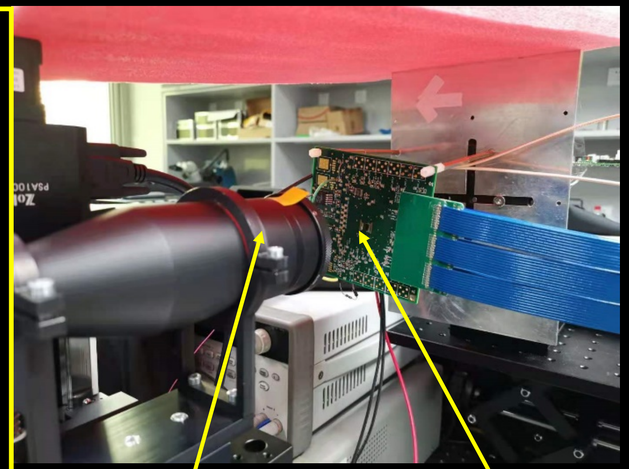
Laser test in last report (coarse scan)

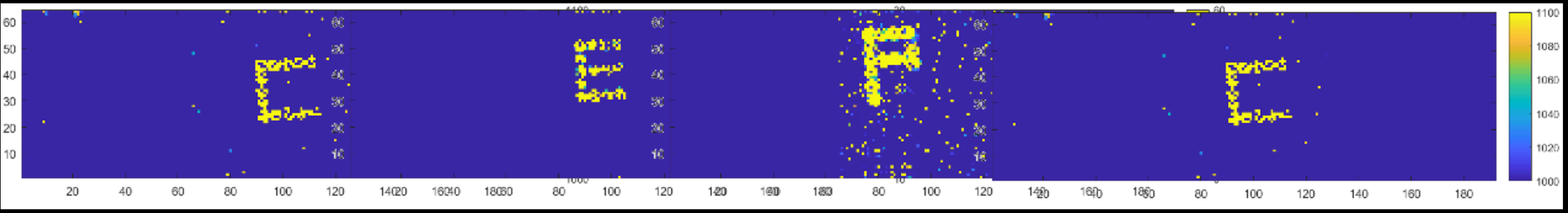
- Triggerless mode was used for the laser test → full readout chain verified
- Measured positions from Taichupix is consistent with expected laser movements

Light spot fitting for laser moving in y-direction with step of 200 *μ*m



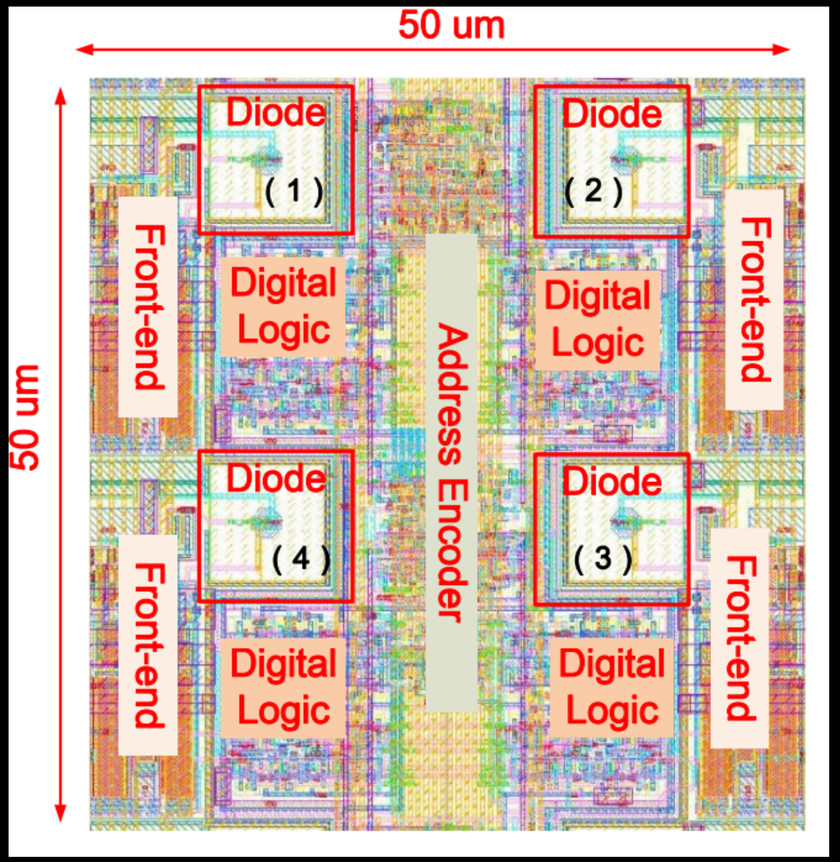


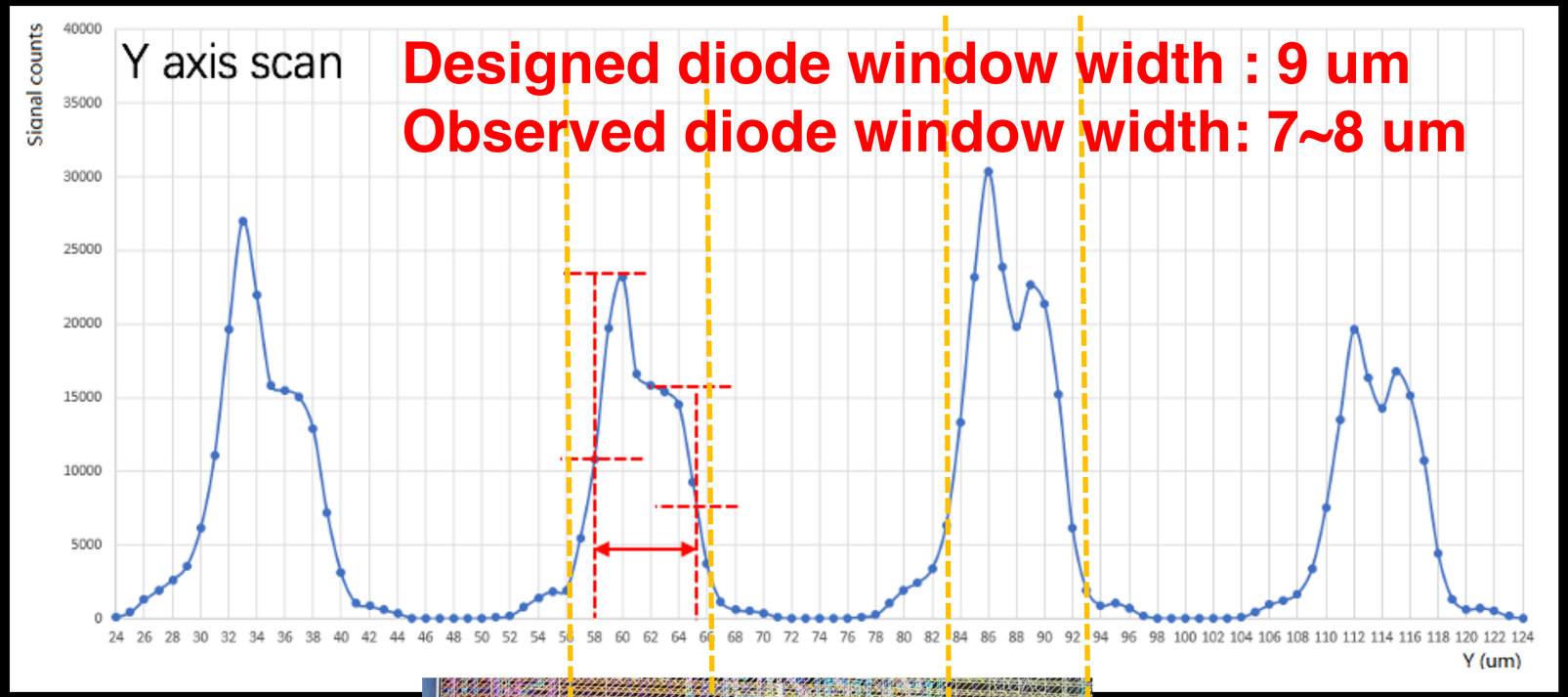


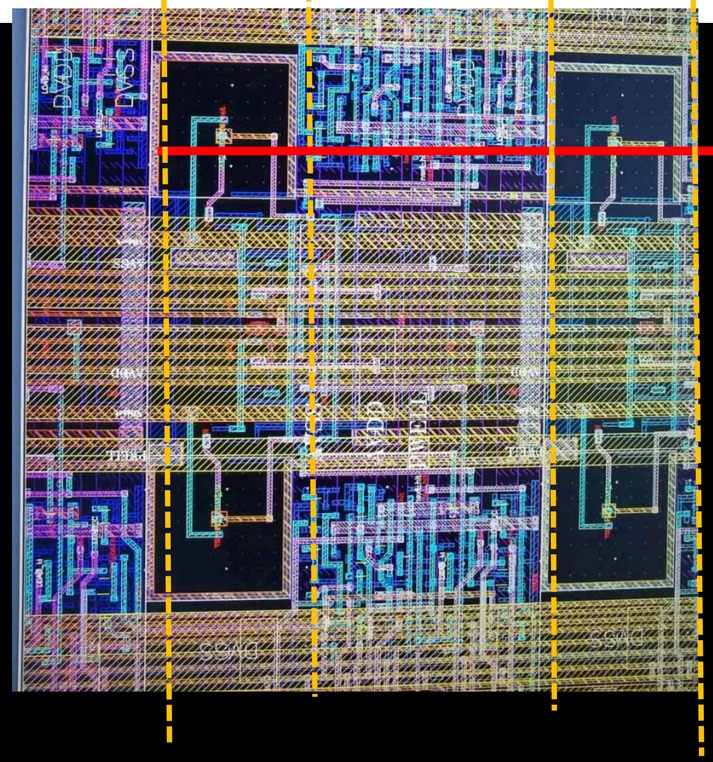


Laser test （fine scan)

- Improved laser setup
  - Beam spot focused to few um
- Study pixel internal structure
- Study Uniformity of response

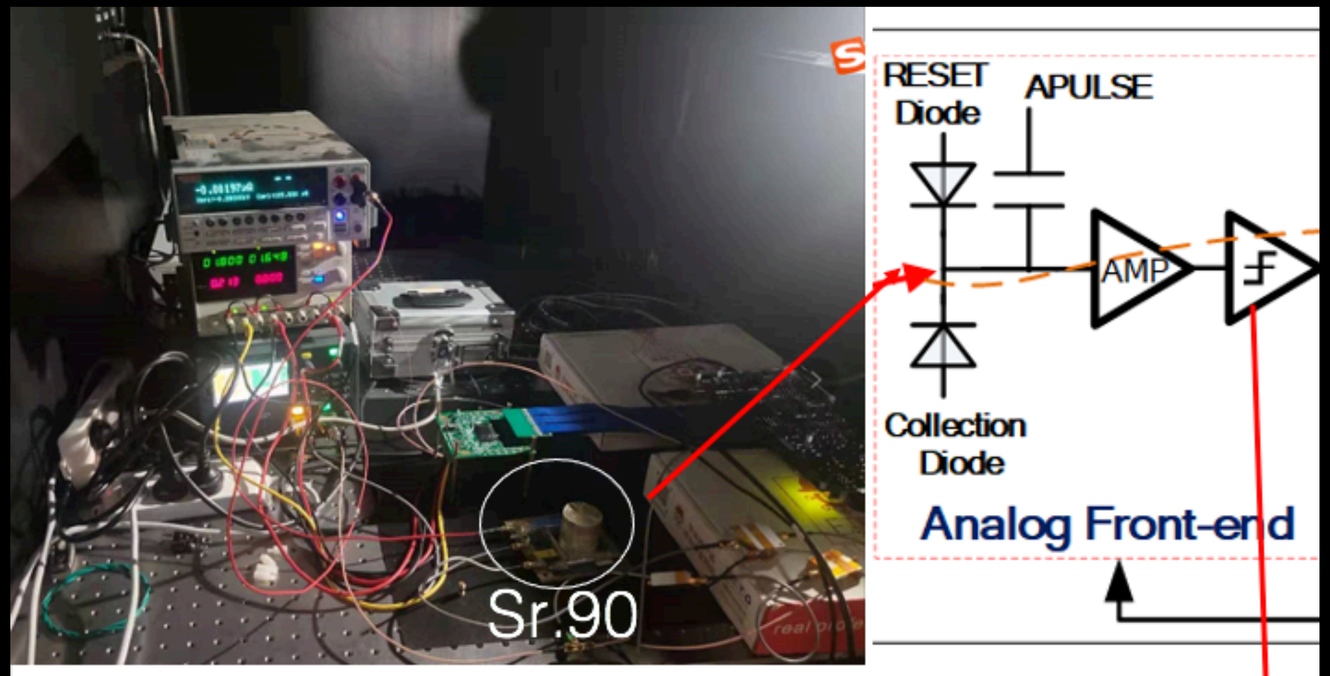




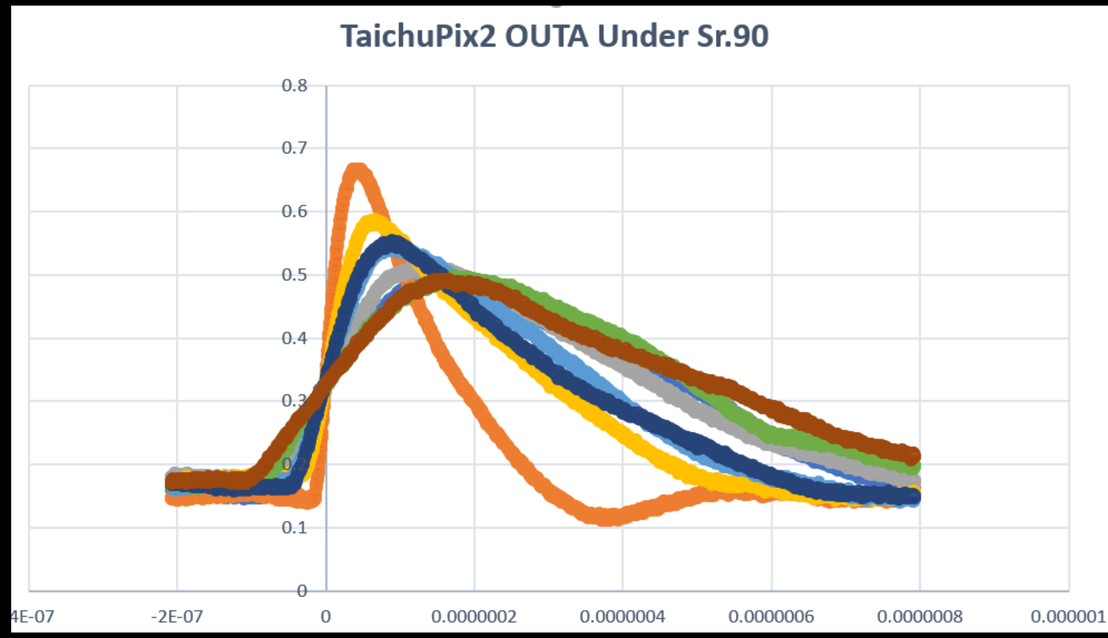


TaichuPix2 test with ^{90}Sr source

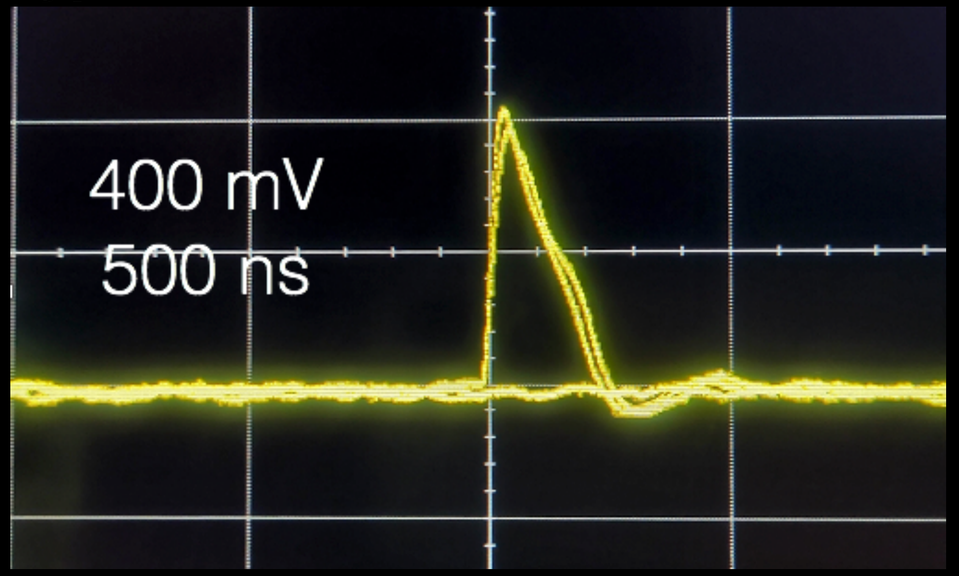
- Digital readout (full chip)
- Analog readout (debug mode for one row of pixel)
  - High signal to noise ratio found in analog readout
- More studies are on-going



Analog waveform in beta tests



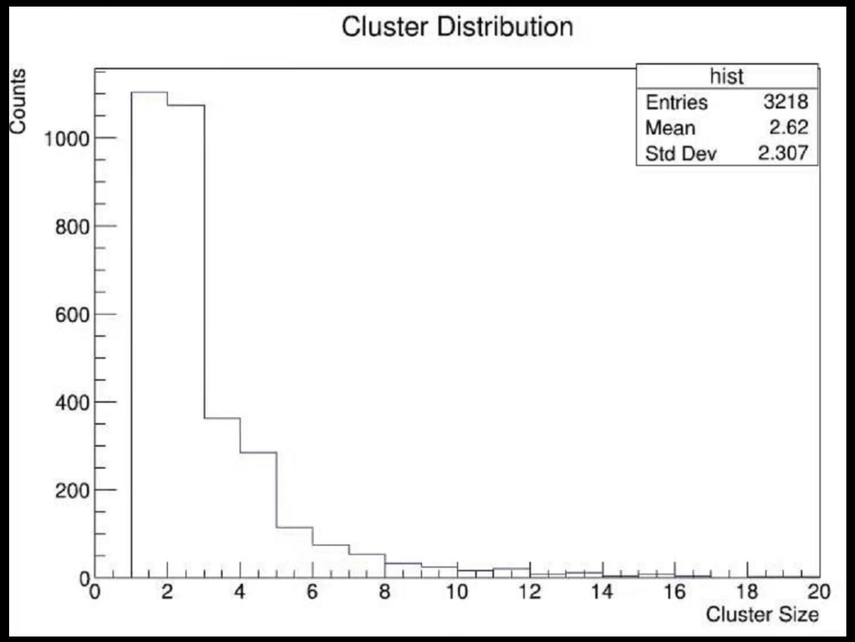
typical waveform in beta tests



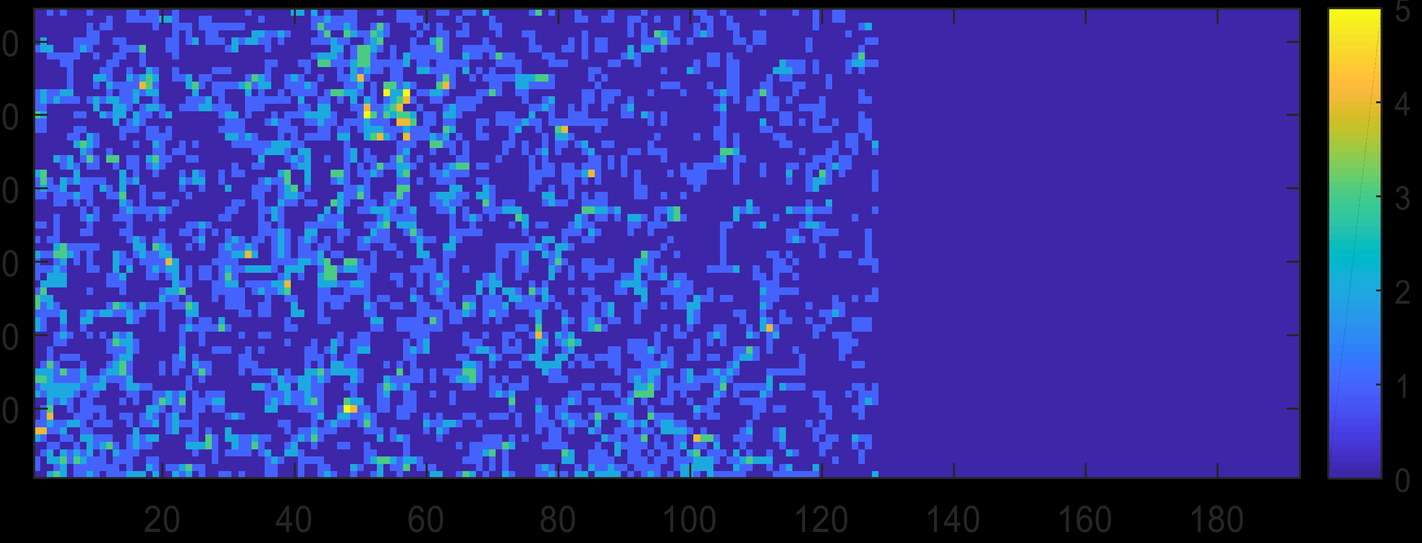
TaichuPix2 test with ^{90}Sr source (2)

- exposure to ^{90}Sr at different threshold (ITHR)
- Finding a cluster for adjacent pixels with a timestamp window of 100 ns
- **Mean cluster size around 3 for different ITHR**

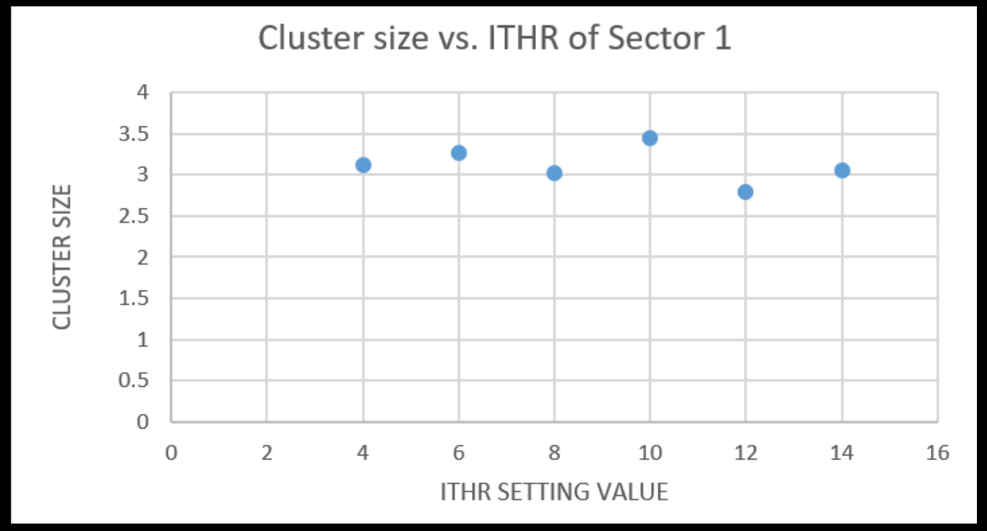
Cluster size distribution



Hit map of TC2 exposure to ^{90}Sr for 400 s



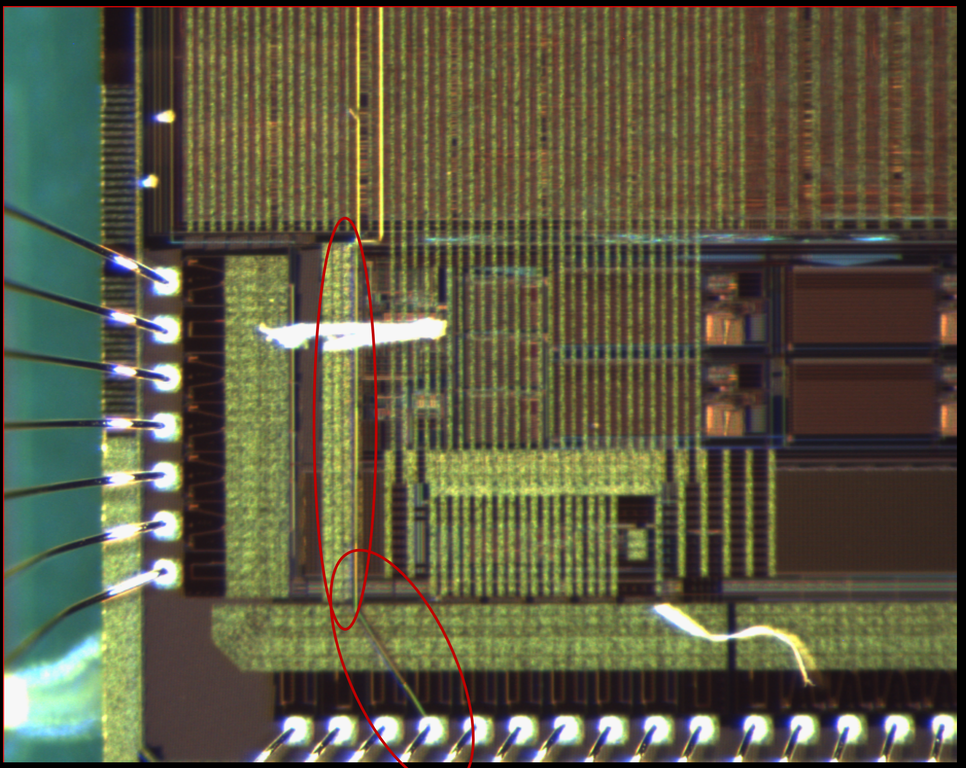
<Mean Cluster size> VS Threshold



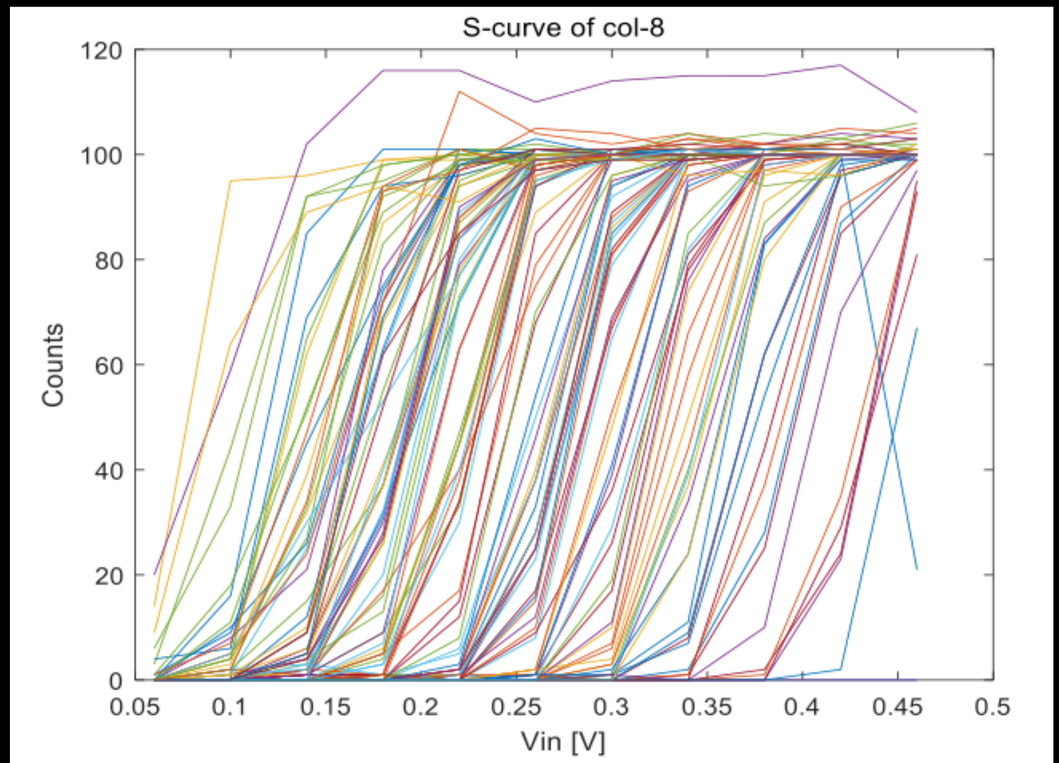
Threshold tuning for TaichuPix2

- For TC2, threshold current ITHR can not be set less than 5.4 nA
  - unexpected from design (nominal design value 4.5 nA).
  - Connected the internal ITHR to an IO-pad through FIB (Focused Ion beam) technology to provide an external ITHR voltage.
  - Applying an external voltage @ Pad-A to tune the ITHR current
  - ITHR can not as low as expected (min. ~7.8 nA) . Need more investigation.

TC2 chip with a Al connection by FIB

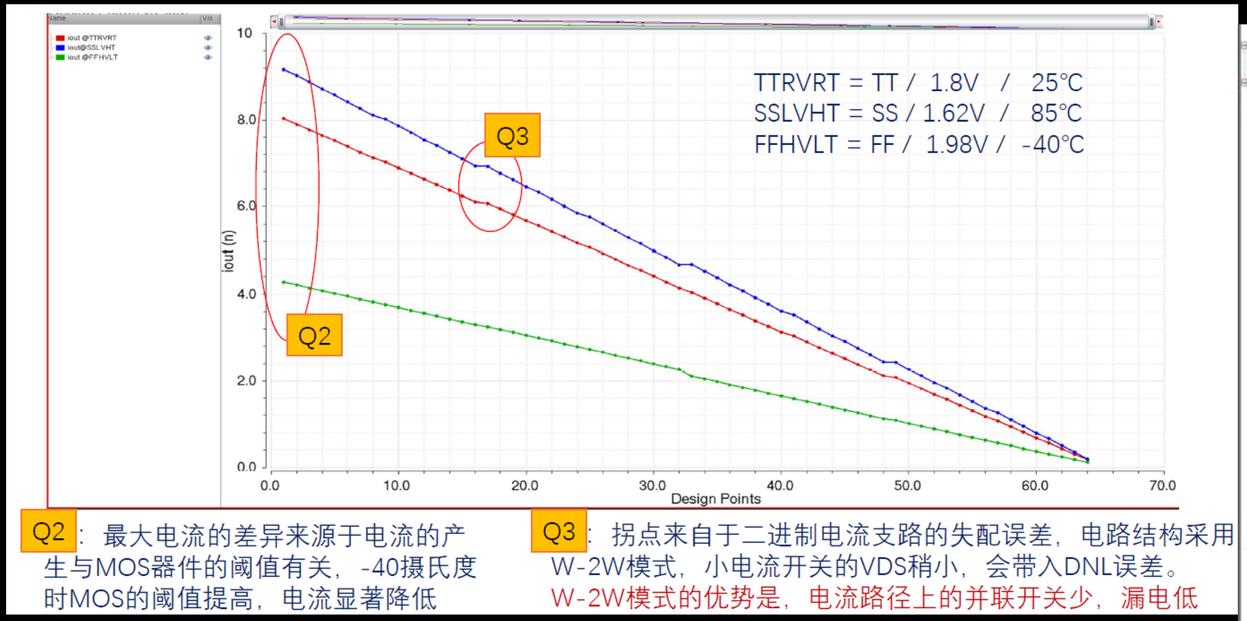


S-curve of one column with external ITHR



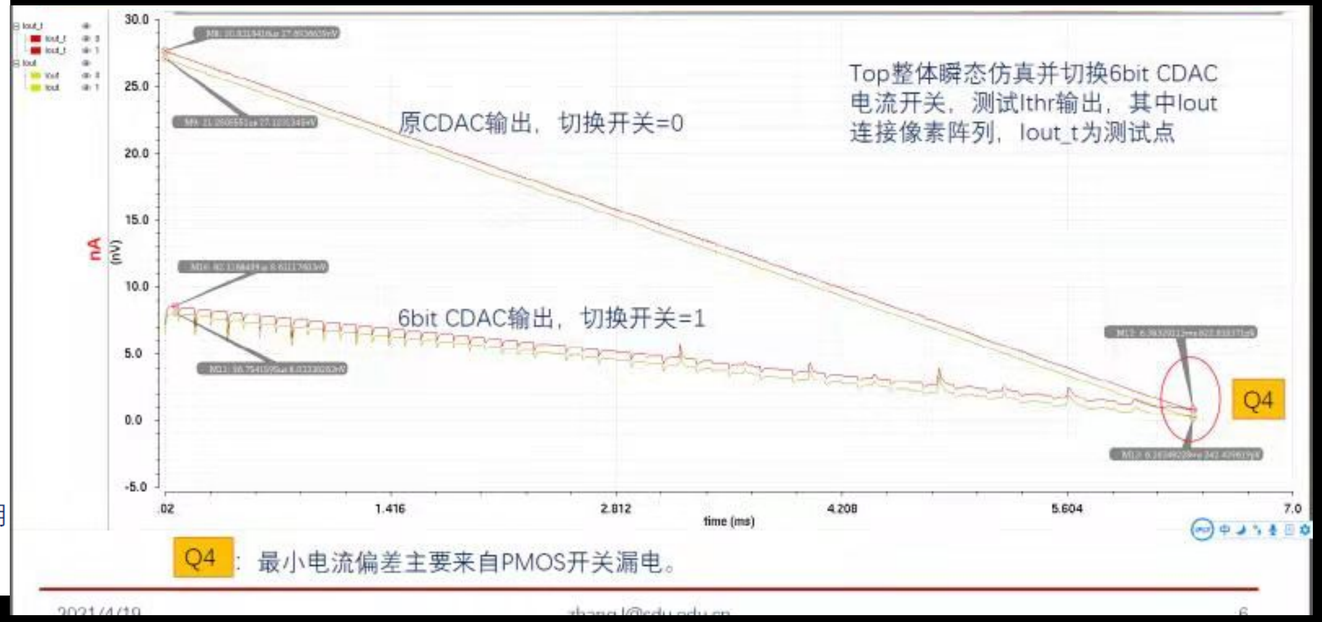
DAC design in the full scale chip TC3

- DAC was also modified by adding a optional 6-bit current DAC for the low current biasing
- Original design suffers from the leakage current and the output range is too large
  - LSB: 0.1nA
  - Aiming at: 2~4nA
- Modified design tuned the output range specifically for small current:
  - Range: 0~8nA



Q2：最大电流的差异来源于电流的产生与MOS器件的阈值有关，-40摄氏度时MOS的阈值提高，电流显著降低

Q3：拐点来自于二进制电流支路的失配误差，电路结构采用W-2W模式，小电流开关的VDS稍小，会带入DNL误差。W-2W模式的优势是，电流路径上的并联开关少，漏电低



Q4：最小电流偏差主要来自PMOS开关漏电。

Simulations on DAC of Taichu3

- TC2 includes two current DACs to provide ITHR
  - One 8-bit DAC same as in TC2
  - An optional 6-bit DAC (design LSB of 0.1nA, range of 0-8 nA)
  - Simulation results indicate the **parasitic resistance increases the DAC output current**, and the parasitic extraction rule effects the value of R and then the simulation result. Have not been understood well.

Name	Input code	Output with Simu-sch.	Output with Parasitic R @extraction rule 1	Output with Parasitic R @extraction rule 2
IBIAS	1011	463.9 nA	551.2 nA	481.8 nA
ITHR_8bit	101100	4.7 nA	9.3 nA	5.5 nA
ITHR_6bit	100011	4.5 nA	7.5 nA	----
IDB	11000	1.02 uA	1.12 uA	1.05 uA

Full-size TaichuPix3 design (engineering run)

- **Full-size Taichu pixel design ready, passed review, ready for submission**
  - **1024×512 Pixel array (25μm×25μm pixel size), Process: Towerjazz 180nm**
  - **FE-I3 like Periphery digital readout , high speed data interface**
    - **Time stamp precision: 25ns-50ns**

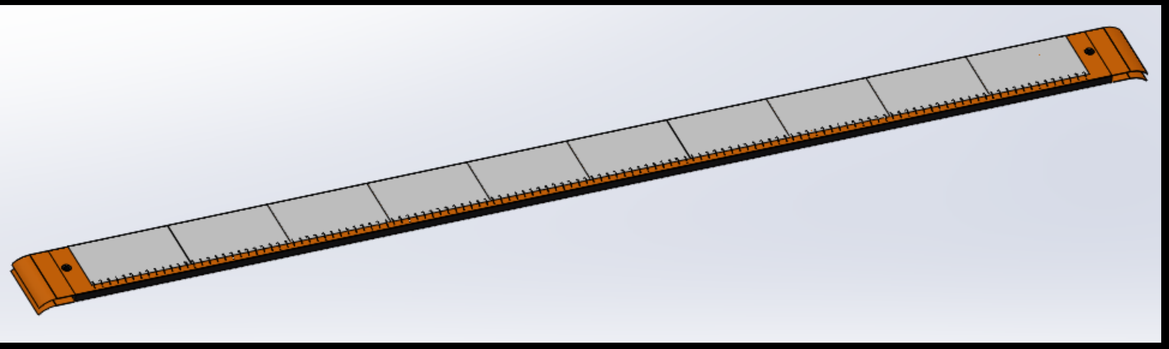
1. Pixel array 1024*512
2. Periphery
3. DAC & Bias generation
4. Data interface
5. LDO (test blocks)
6. Chip inter-connection features
7. Scribe-able top power connection features

- **Process improved for better power supply: 6 Metals to 7M with 1 Thick Top**
  - Will help for the full size chip power integrity
- **25 μm×25 μm pixel, unique design (S1)**
- **A 1024×512 Pixel array**
- **Periphery logics**
  - Unique design for FE-I3 like readout
- **High speed data interface**
  - Optimized for trigger mode and low power: optional low power LVDS port added
- **On-chip bias generation**
  - Bugs detected & solved from the Tcpx2 test
- **IO placement in the final ladder manner**
  - chip interconnection bus features included for ladder
- **LDO will be independently tested as a test block due to the remain issues**

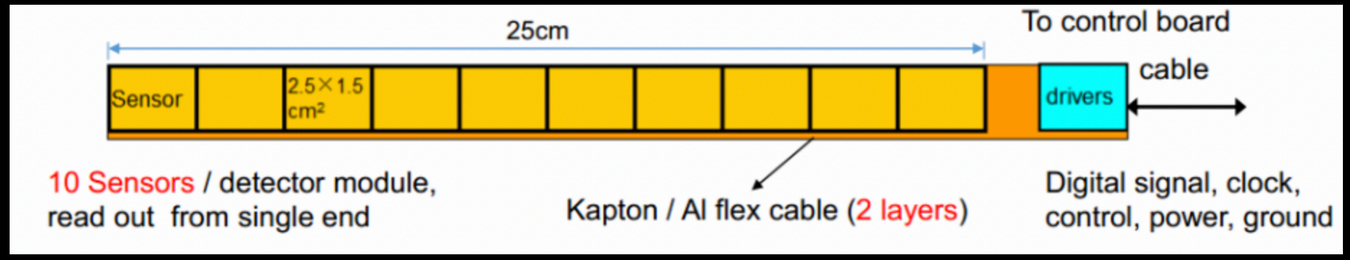
Detector module (ladder) R & D

- Completed preliminary version of detector module (ladder) design
  - Detector module (ladder)= 10 sensors + support structure+ flexible PCB+ control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control , power, ground will be handled by control board through flexible PCB

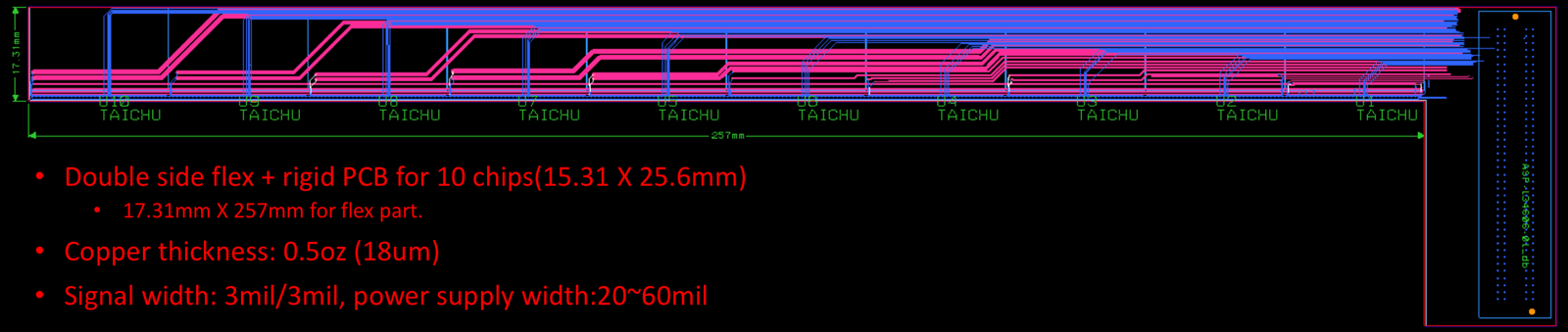
3D model of the ladder



Schematic of ladder electronics



Design of Flexible PCB prototype



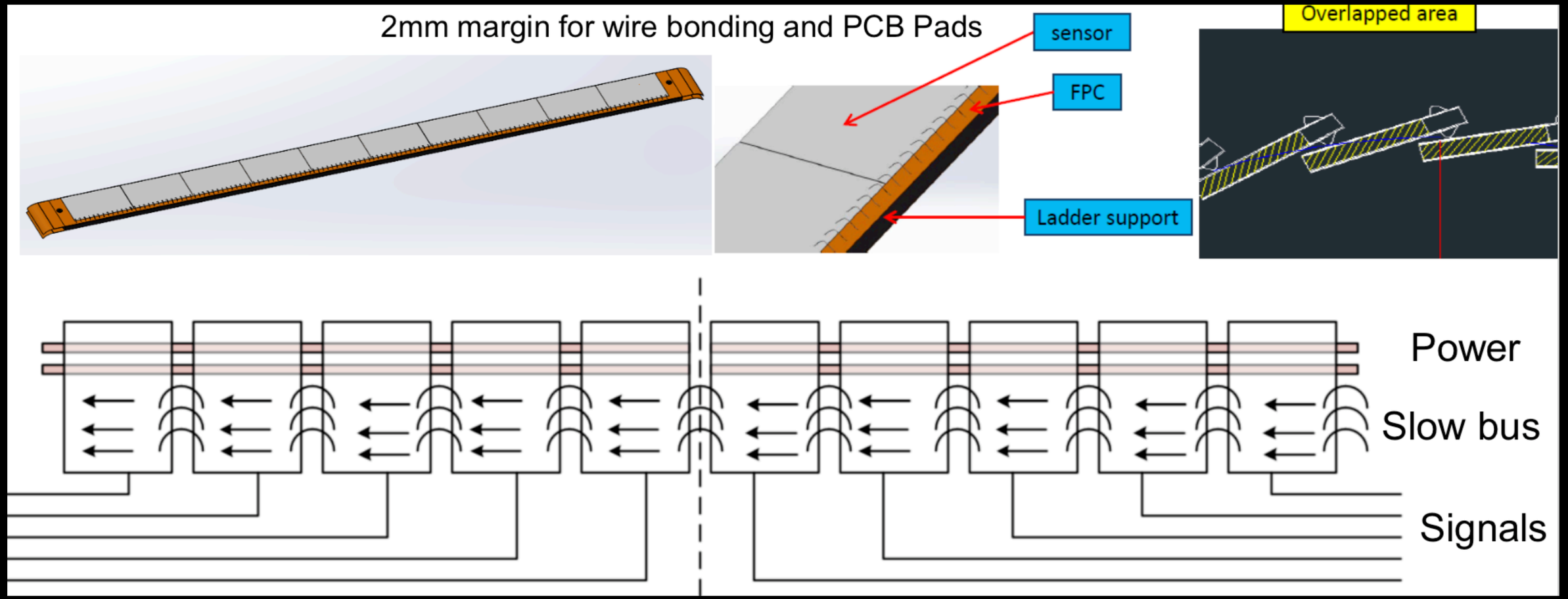
- Double side flex + rigid PCB for 10 chips(15.31 X 25.6mm)
  - 17.31mm X 257mm for flex part.
- Copper thickness: 0.5oz (18um)
- Signal width: 3mil/3mil, power supply width:20~60mil

Profile of flexible PCB

	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

New idea in Taichu pixel design – inter-chip connection

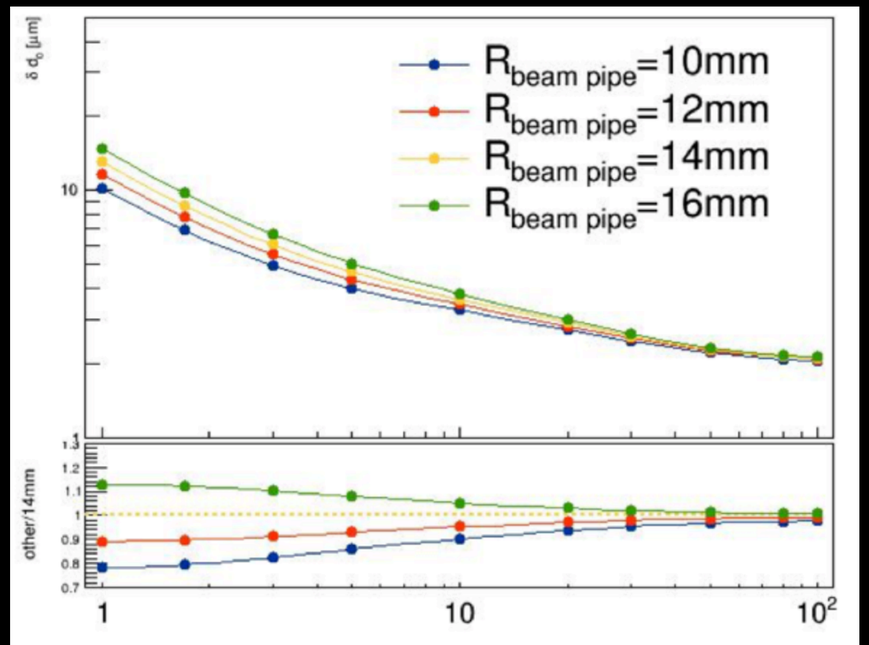
- Inter-chip connection for slow controls through wire bonding
- → Save some metal for PCB (reduce material budget)



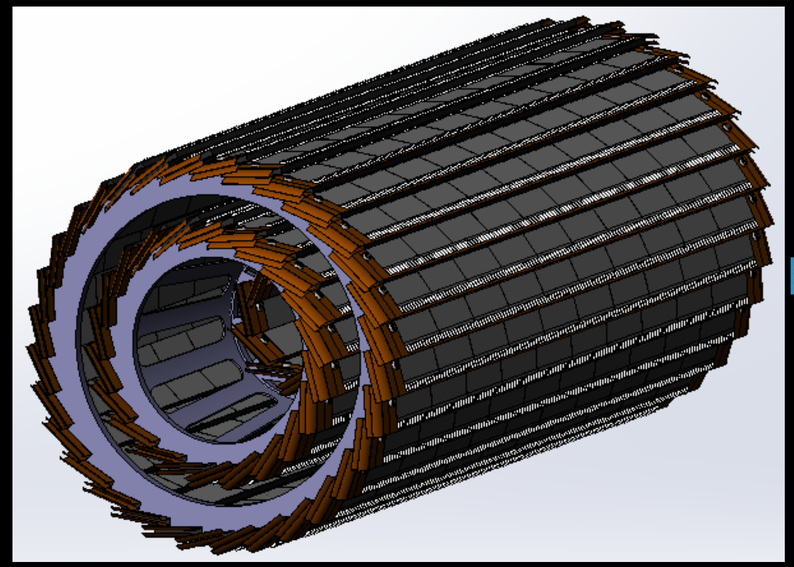
Vertex Detector Prototype R & D

- Completed preliminary version of detector engineering design
  - 3 double layer barrel design
  - 7 modules in inner layer, 22 modules in 2nd layer, 32 modules in outer layer
- Physics simulation to optimize vertex detector layout design.
  - The length of inner layer pixel should be the same as other two layers
  - Inner pixel radium should be as close to beam pipe as possible

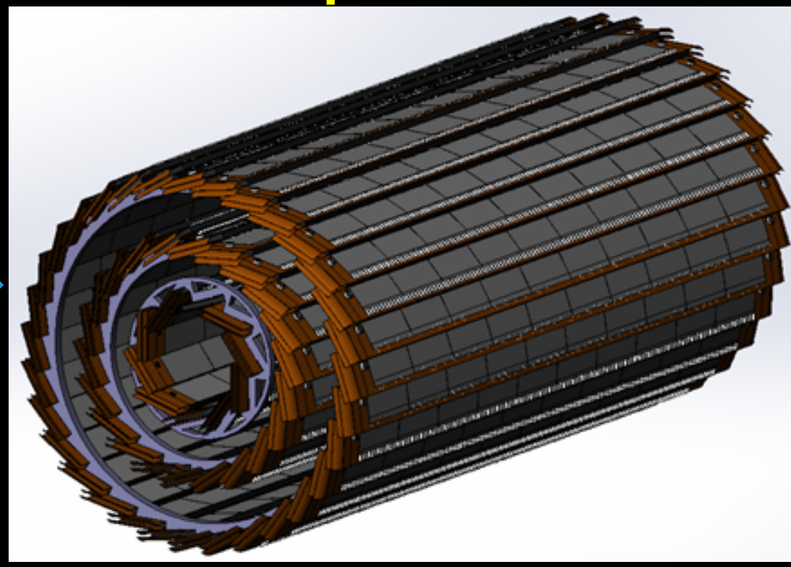
Impact parameter resolution Vs beam pipe radius



Old design



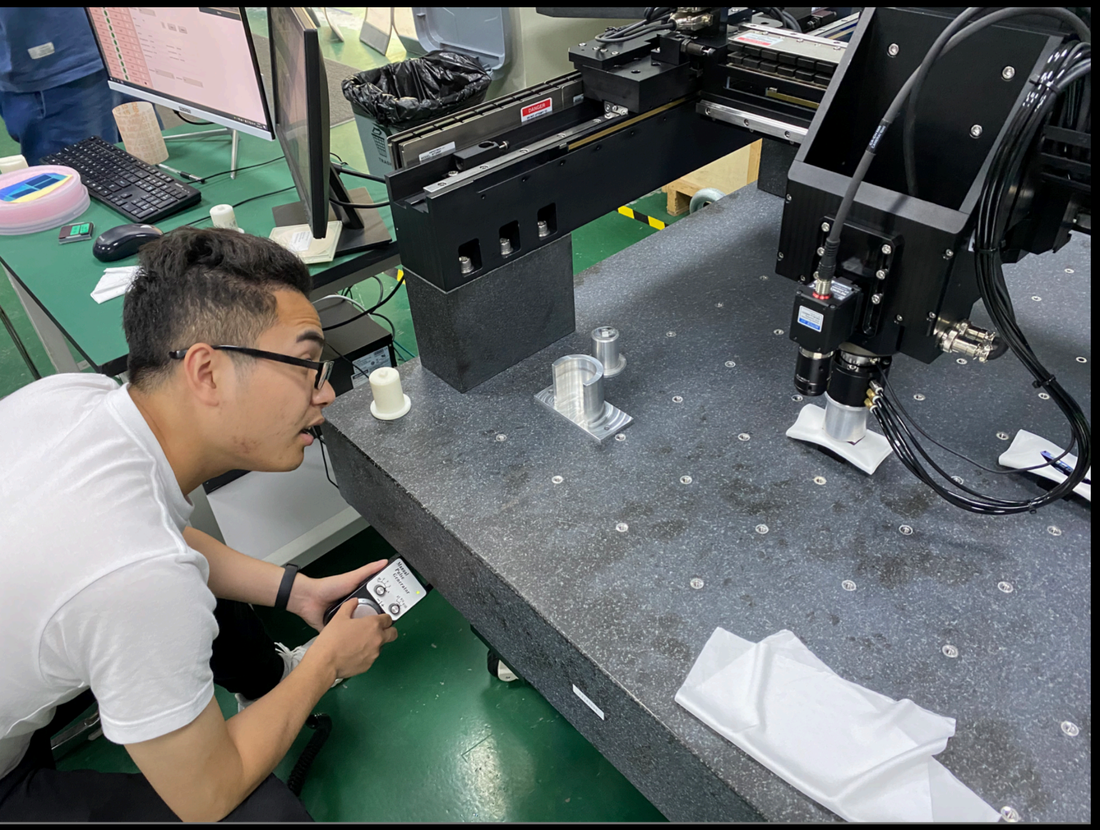
After optimization



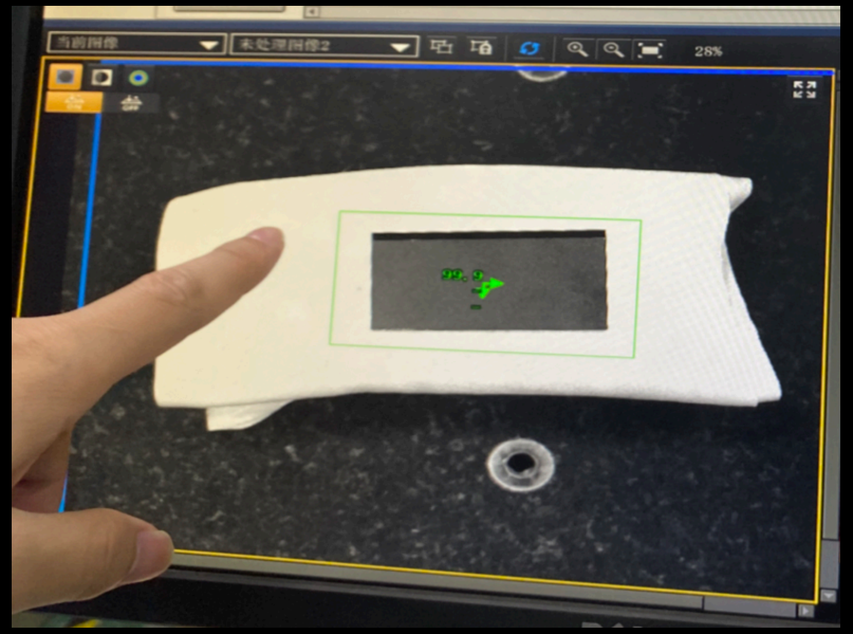
Gantry for vertex detector prototype assembly

- **3~5um good position resolution require high assembly precision**
- **Cooperate with domestic company on R & D Gantry automatic module assembly.**
  - **Pattern recognition with high resolution camera**
  - **Automatic chip pick-up and positioning**
  - **Automatic Glue dispending**

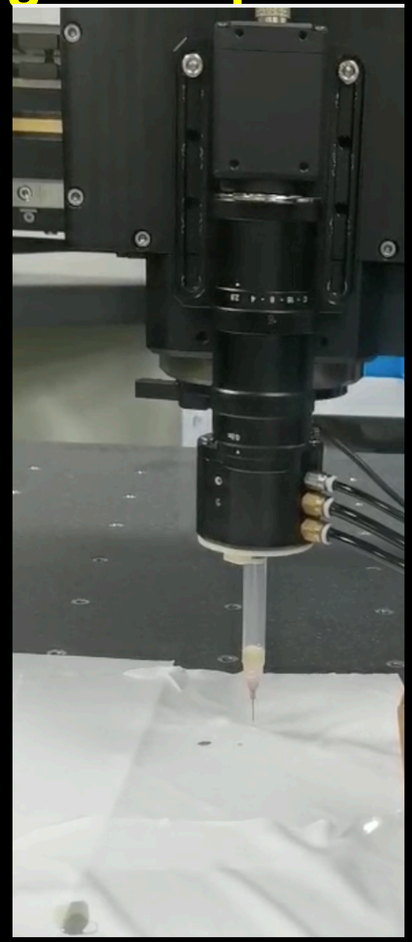
Gantry system



Pattern recognition

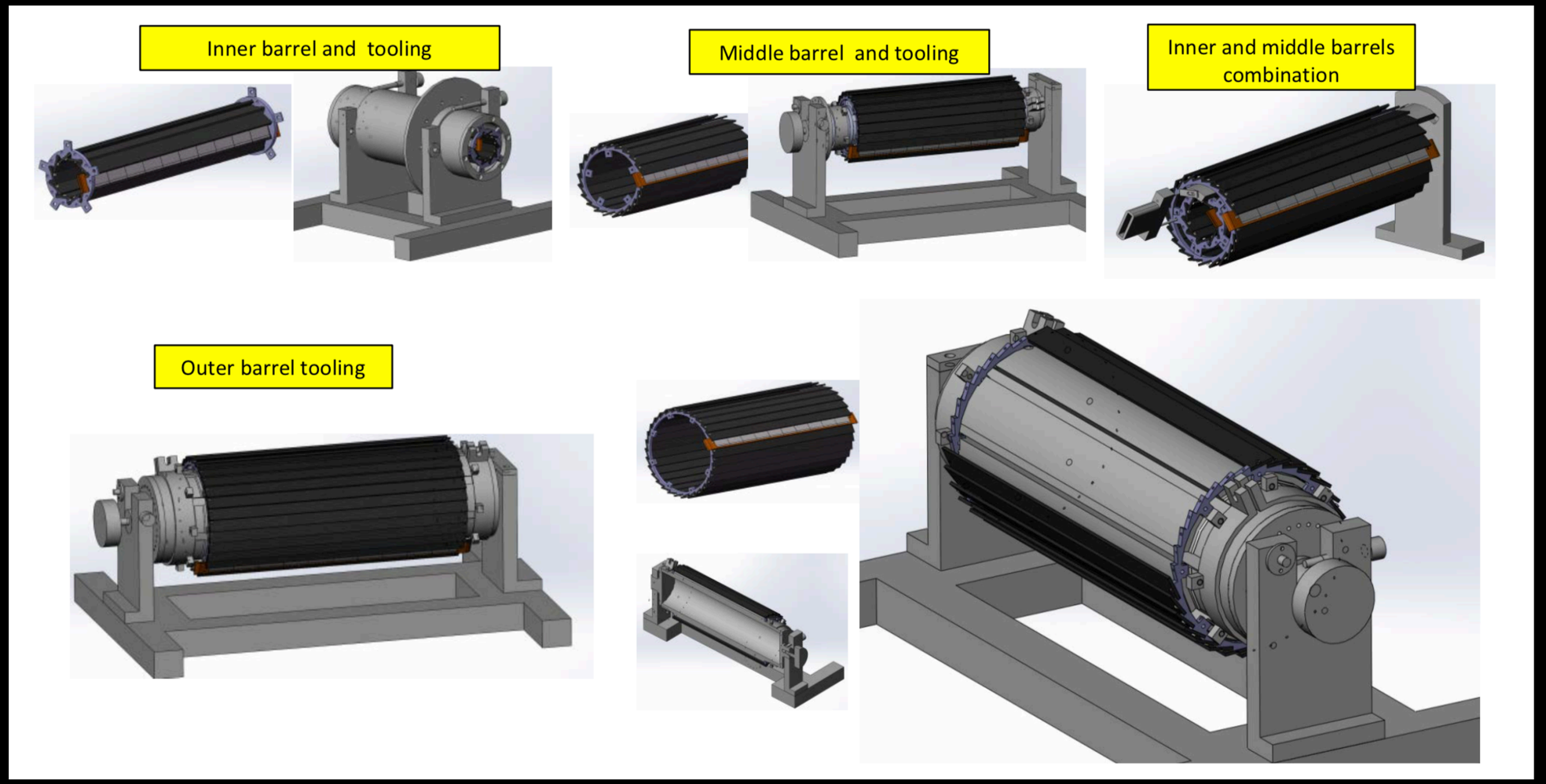


automatic glue dispending



Tooling Design for Barrels Assembling

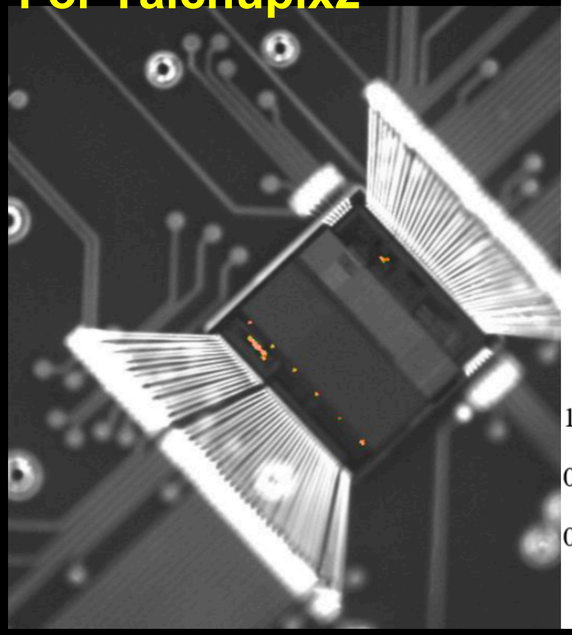
- 3 sets of tooling for 3 layer of barrel assembling.
- Tooling and special tool for inner and middle barrels assembling.



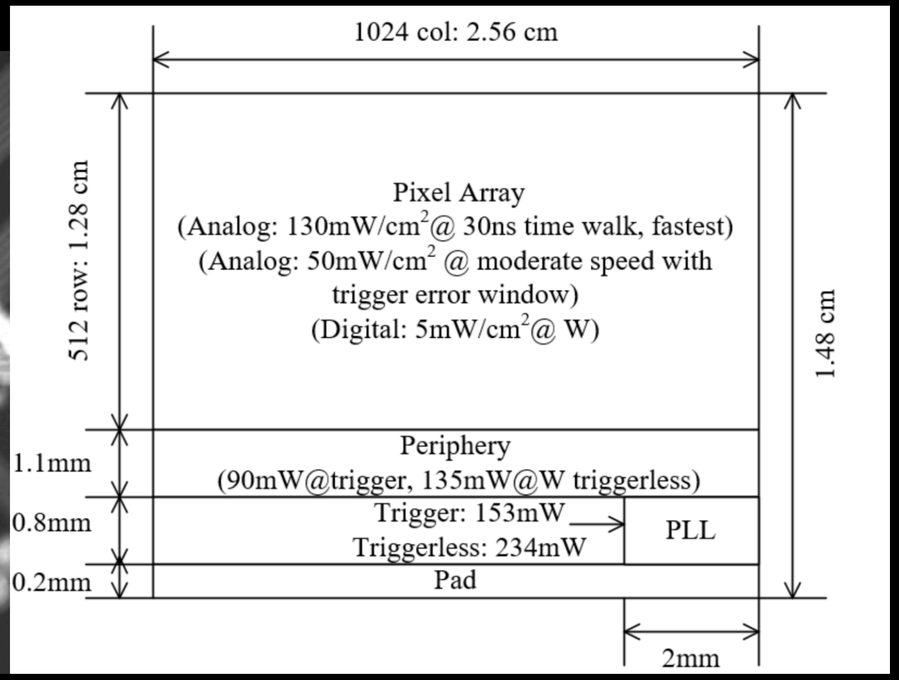
Cooling design

- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix : $\leq 100\ mW/cm^2$. (trigger mode) ; CEPC final goal : $\leq 50\ mW/cm^2$
- Cooling simulations of a single complete ladder with detailed FPC were done.
  - Testbench setup has been designed and built for air cooling , vibration tests

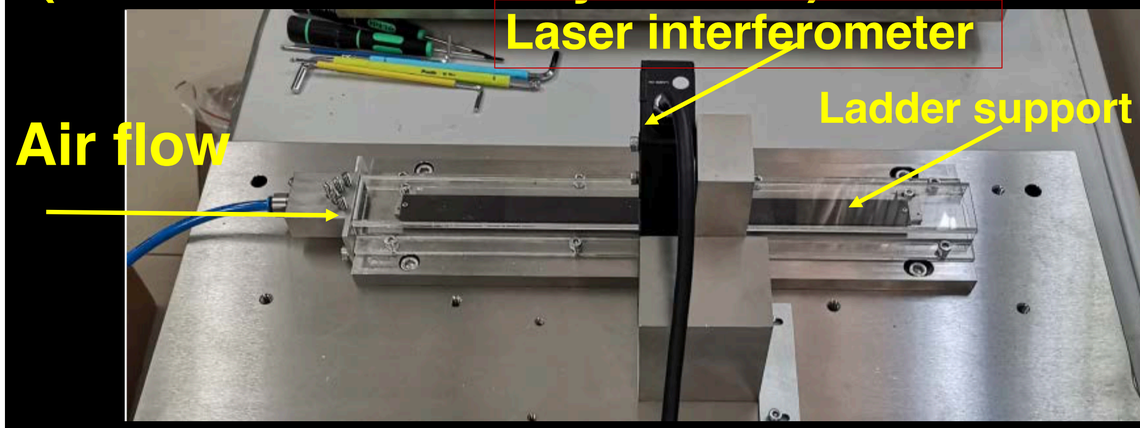
The EMMI (Emission Microscope) For Taichupix2



Power consumption



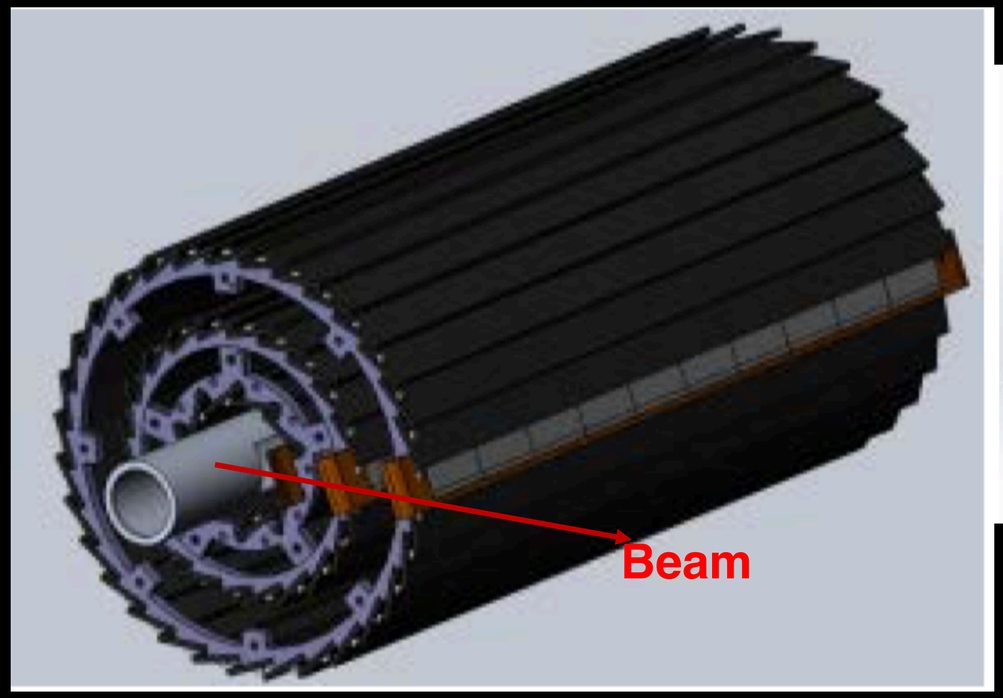
Test setup prototype for ladder cooling
Use compressed air for cooling
(See more from Jinyu's talk)

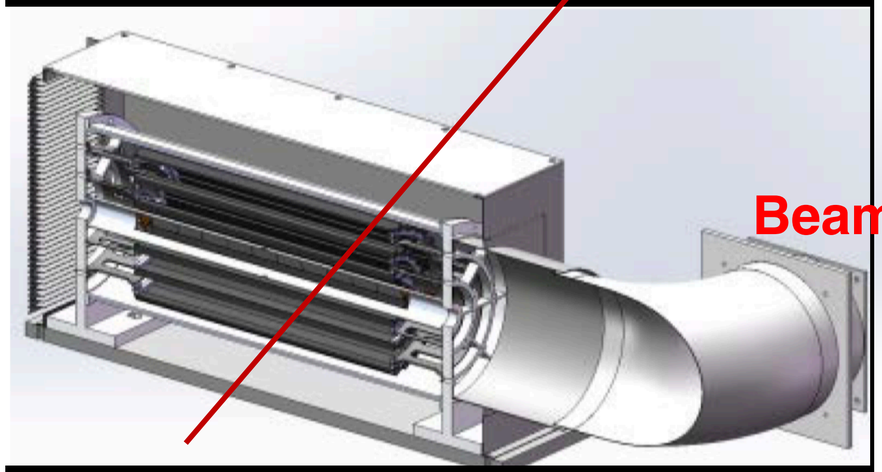


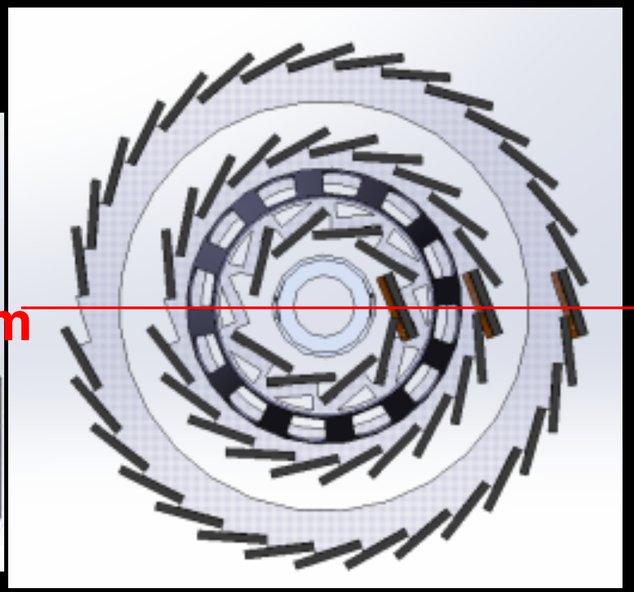
Plan for test beam

- Expect to perform beam test in DESY(3 - 7GeV electron beams)
  - IHEP test beam facility as backup plan (a few hundreds MeV - 2.5GeV electrons)
- Enclosure for detector with air cooling is developed for beam test
  - Beam is shooting at one sectors of vertex detectors

Install one sector of ladder in vertex detector





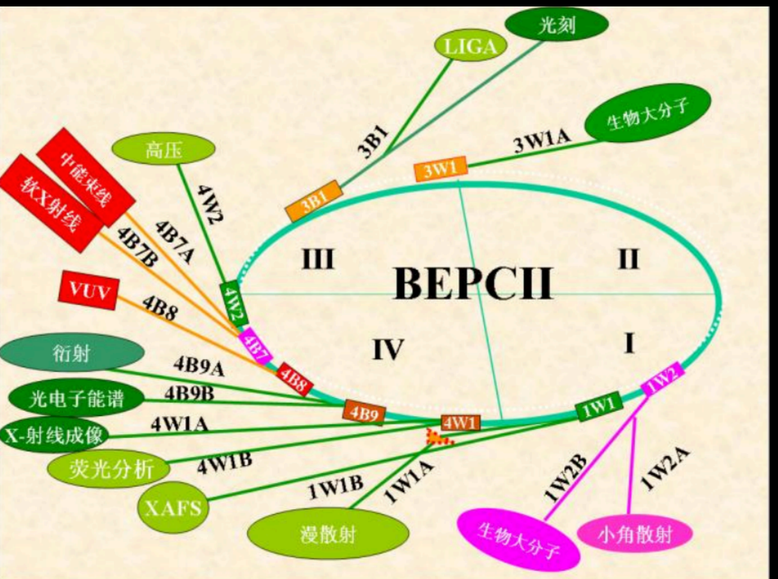


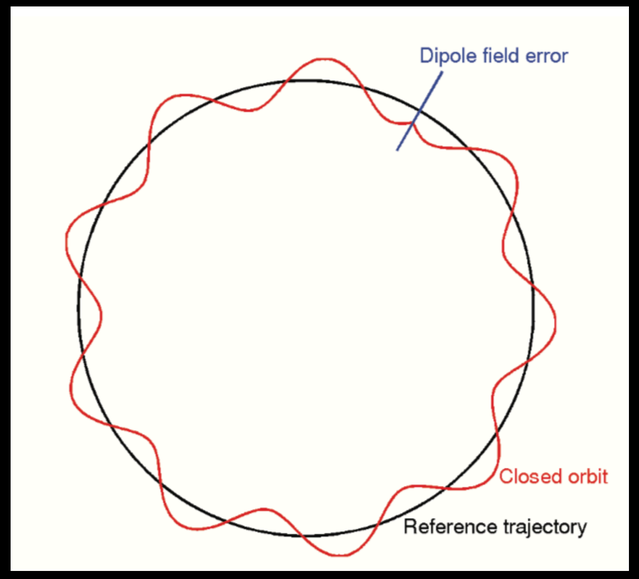
Plan for test beam (2)

New opportunity in Beijing Synchrotron Radiation Facility (BSRF)

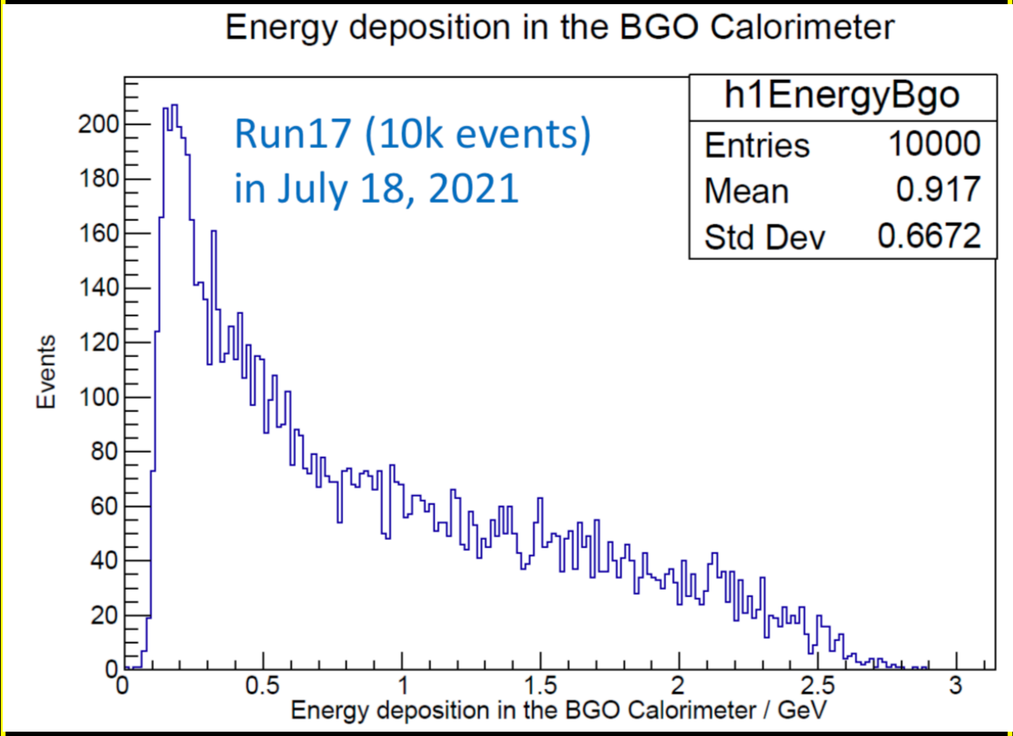
- **High energy electron (0.2~2.5 GeV) leakage from BEPC**
- **High trigger rate (up to 50Hz/cm^2)**
- **Need to filter low energy particles for vertex test beam**

	DESY	IHEP E3 beam	BSRF
Momentum	1-6 GeV	<1 GeV secondary beam	1~2.5 GeV
Particles	electrons	Protons/ Pions/ /Electrons	electrons
Trigger rate	4000 Hz/cm^2	0.6 Hz/cm^2	~50 Hz/cm^2





Energy spectrum measured by calorimeter (by Yong Liu)



Summary

- Sensor:
  - Completed two round of CMOS sensor prototyping, finalized full-size sensor design
  - New readout architecture to reduce pixel size to 25μm*24μm
  - → Reach midterm Assessment index (实现中期指标）
  - First irradiation test up to 30 Mrad >1Mrad total ionization dose radiation
- Mechanics:
  - Build the support structure prototype for ladder prototype
  - Finalize the design for full vertex detector

	Mid-term	Final goal	Status
Spatial resolution	Pixel size less than 25*25 μm	Spatial resolution 3~5 μm	Reach mid-term goal
Radiation hardness	> 1MRad in simulation	>1MRad In radiation test	First test up to 30 Mrad. Chip is still functional

Outlook for the next year

- Competed R & D large area sensor
- Manufactured the support structure for whole detector
- Assembling and installing the detector prototype
- Completed DAQ system for whole detector

2021 年 7 月 | 2022 年 6 月	第四年年初进行大面积、全功能传感器芯片的工程批硅晶圆加工，并在加工完成后工程批芯片对进行全面的测试； 加工探测器原型机的整机支撑结构；开始组装装探测器原型机；研发与调试原型机整机的数据获取系统。	1. 完成探测器原型机整机支撑结构的设计报告，并年底前研制出探测器原型机的整机结构。 2. 完成全功能的传感器芯片的测试，完成测试报告。 3.研发出探测器原型机整机的数据获取系统。	课题年度报告 国际会议报告

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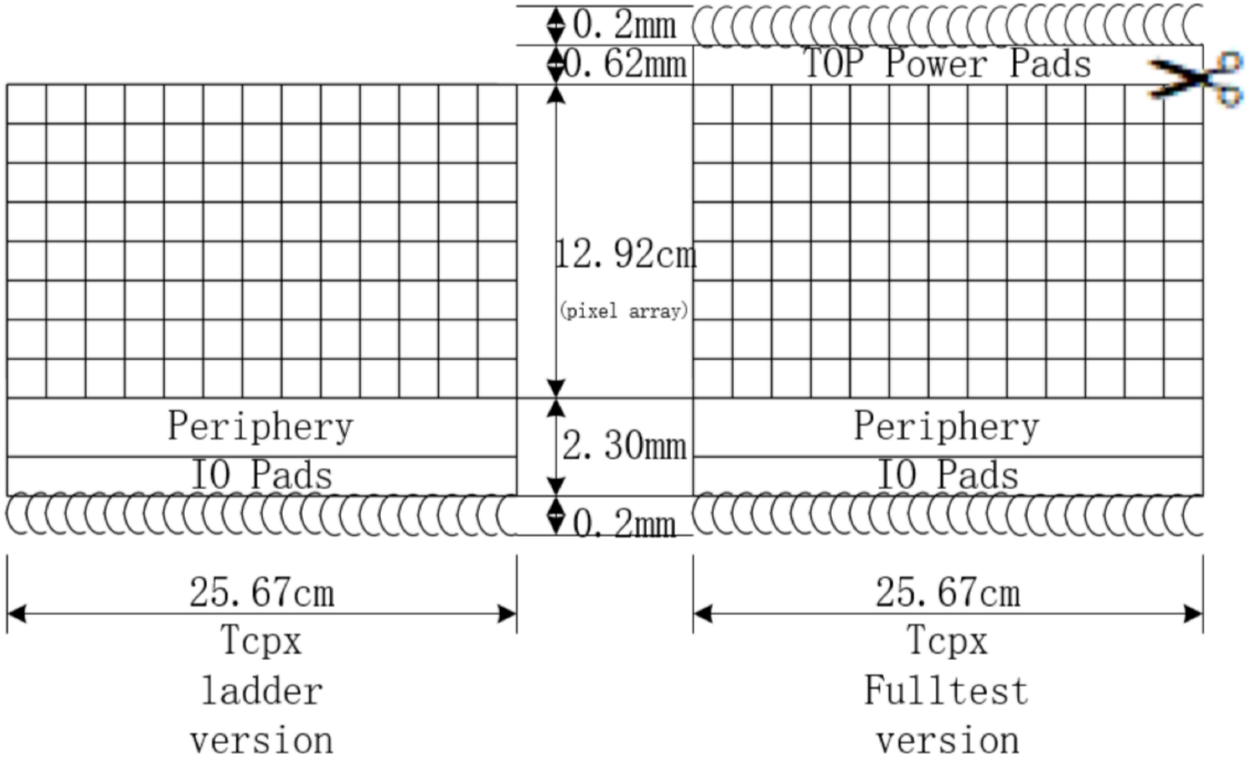
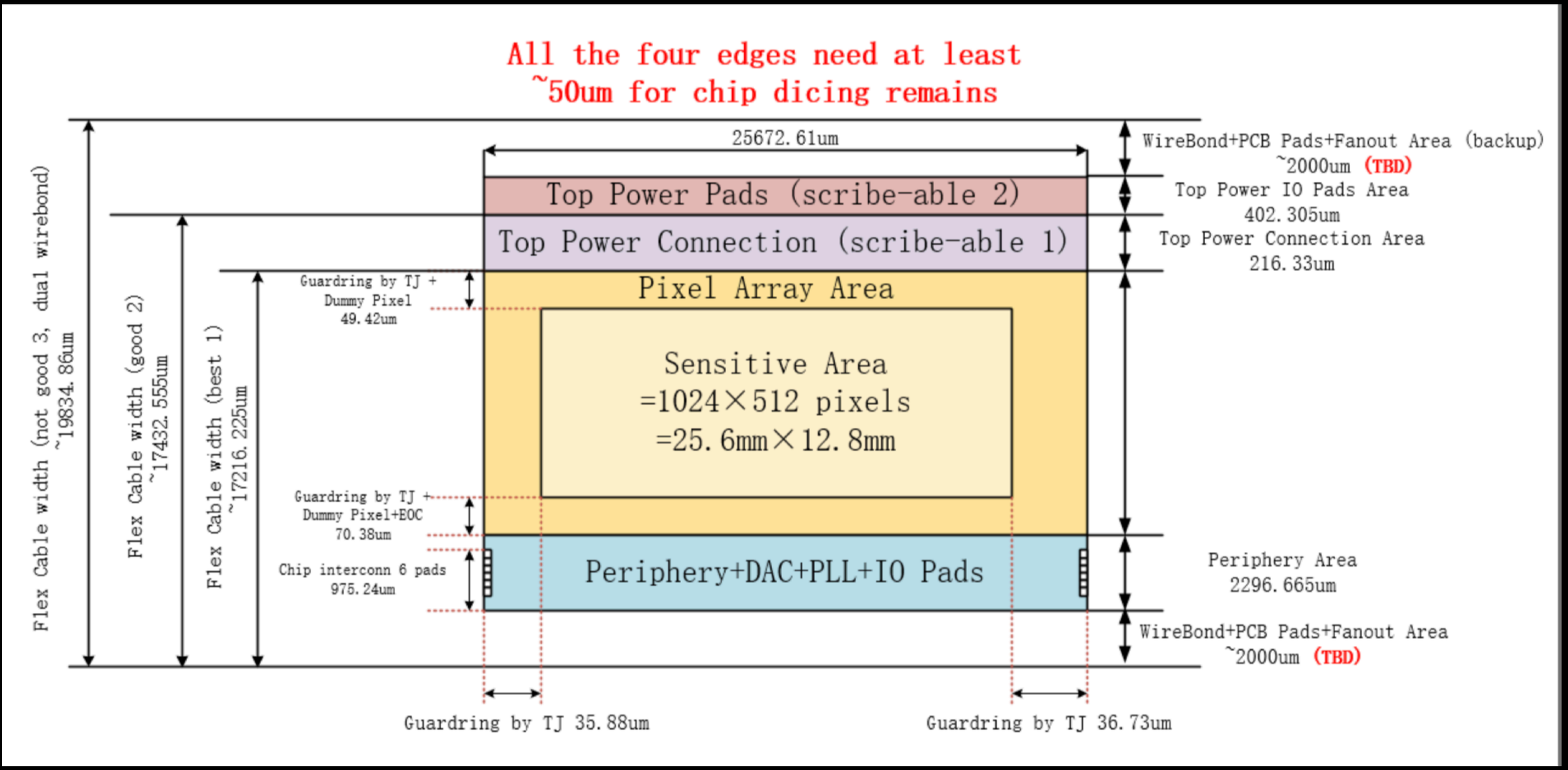
Backup : Preparation for the full size engineering run



- **Two versions possibilities were kept within one tapeout**
  - Fulltest version keeps all test pads features for the chip study before ladder assembly
  - Top power pads & top power bus connections will help for the full chip power integrity, concerning Tcpx is aiming for fast readout with high power
  - Tcpx final ladder version
    - If top power bus not necessary, stays in minimum dead zone
    - If top power bus needed for less IR drop, + 200um dead zone on the top but with a good chip
    - If all needed, we learned by test thanks to the full test features

- **Signal pads/routing on ladders were kept minimum with 9/8 wires, other common bus were routed by chip interconnection features**

Backup : Preparation for the full size engineering run



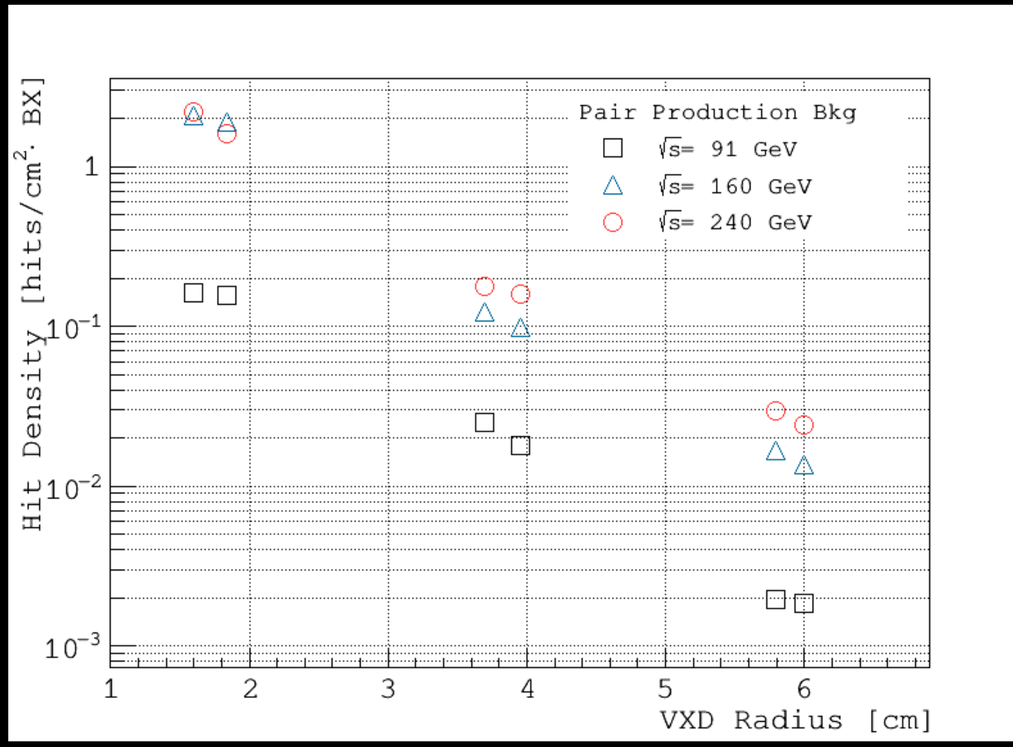
Backup: International collaboration

- **IFAE(Spain): very active in CMOS Sensor design and testing**
- Liverpool (UK): Tracker mechanical design,
- Oxford(UK): CMOS sensor design validation, thermal design
- RAL(UK): Pixel module design
- Queen Mary(UK): module mechanical design (Zero mass concept)
- Strasbourg (FR): CMOS sensor design, Tracker mechanical design
- University of Massachusetts (US): Tracker mechanical design, thermal design

In 2019, we have one engineer visited Oxford and Liverpool for 4 weeks, learned a lots about silicon.

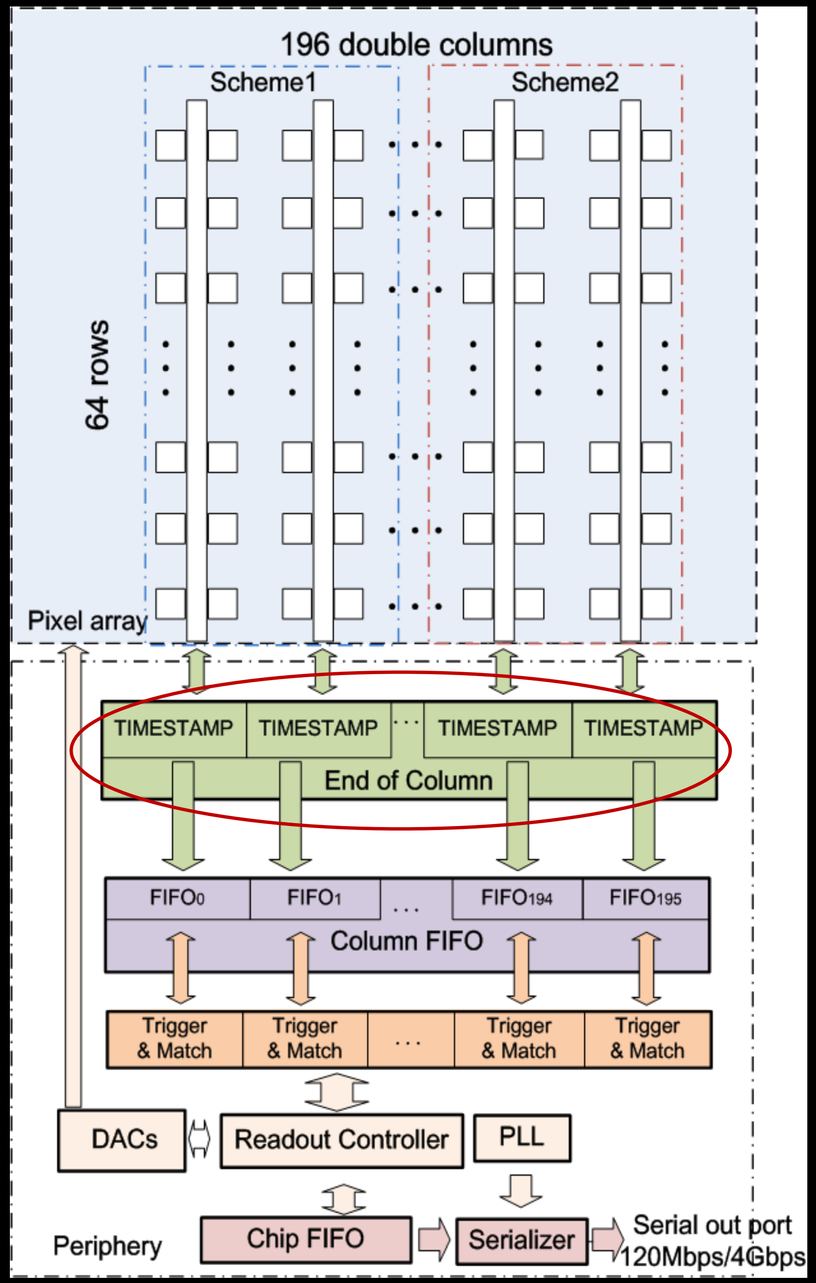
Main specs of the full size chip for high rate vertex detector

- Bunch spacing
  - CEPC Z+Higgs (240GeV): 680ns;
  - WW threshold scan (160GeV): 210ns;
  - CEPC Z pole runing (90GeV) Z: 25ns
- High Hit density
  - 2.5hits/bunch/cm^2 for Higgs/WW runs
  - 0.2hits/bunch/cm^2 for Z pole running



For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

New proposed readout architecture in TaichuPix

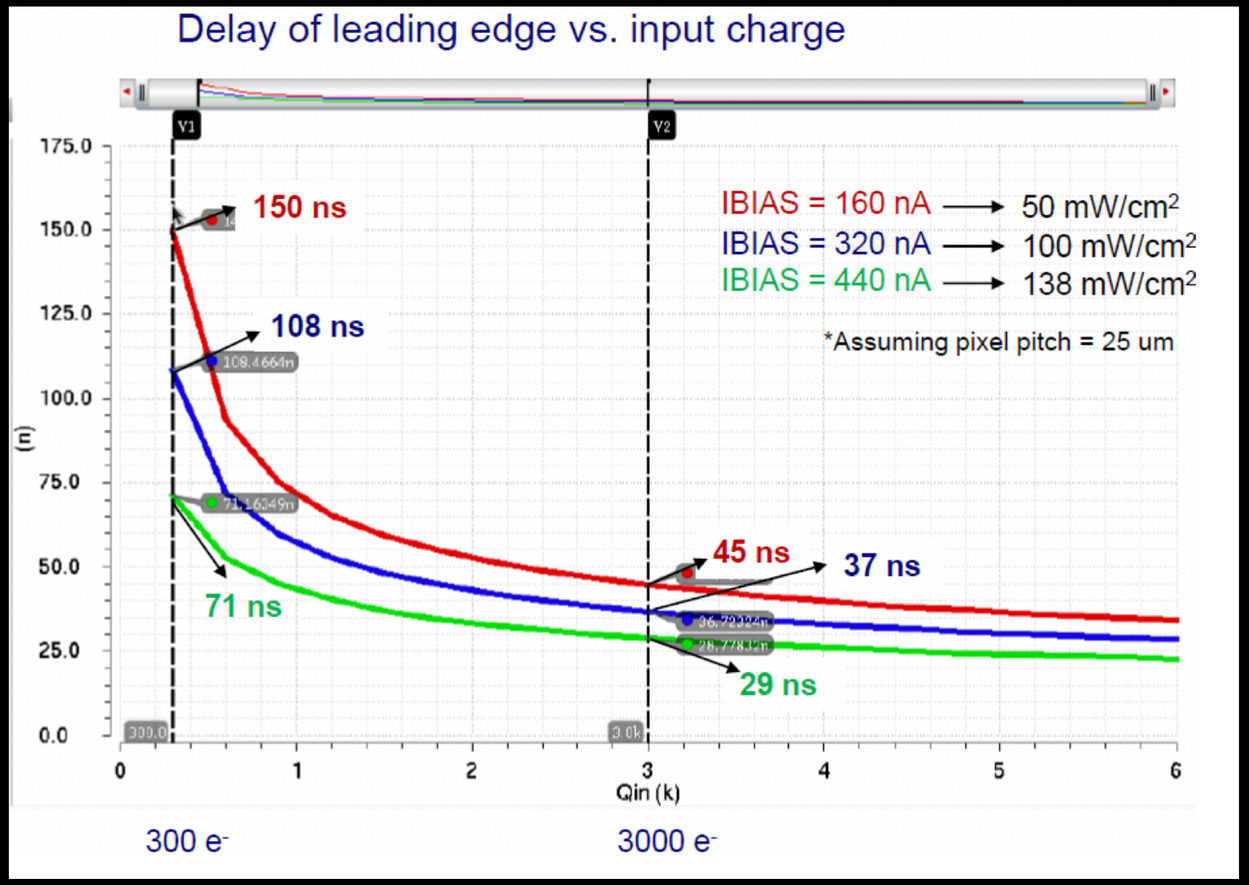


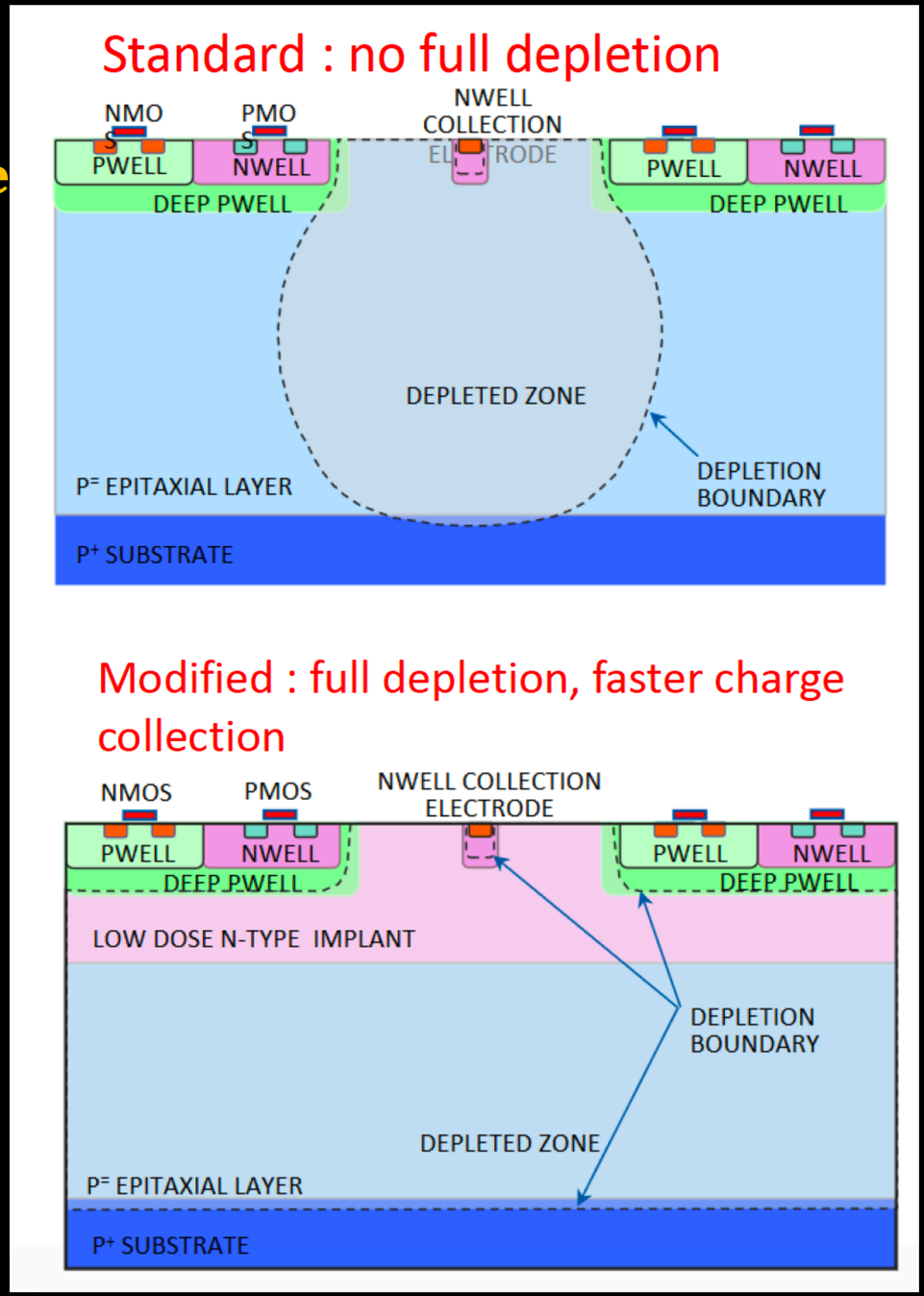
- New readout architecture
- → reduce power consumption and reduce pixel size
- CEPC readout time requirement:
  - <500ns deadtime @40MHZ(Z pole)

- Taichu-1 Column-drain readout
  - Priority based data driven readout; time stamp at EOC
  - Dead time: 2 CLK for each pixel (50ns @40MHz CLK)
  - Two digital pixel designs: FEI3-like and ALPIDE-like design
- 2-level FIFO architecture
  - L1: column level, to de-randomize injecting charge
  - L2: chip level, to match in/out data rate between core and interface
- Trigger readout:
  - Coincidence by time stamp, matched event read out

Pixel Analog design

- CEPC time stamping precision requirement:
  - 25-100ns, better to time stamping each collision at Z pole
- Taichu-1 pixel analog design:
  - 50ns~150ns (based one standard CMOS MAPS tech.)
  - Consider to use depleted CMOS MAPS

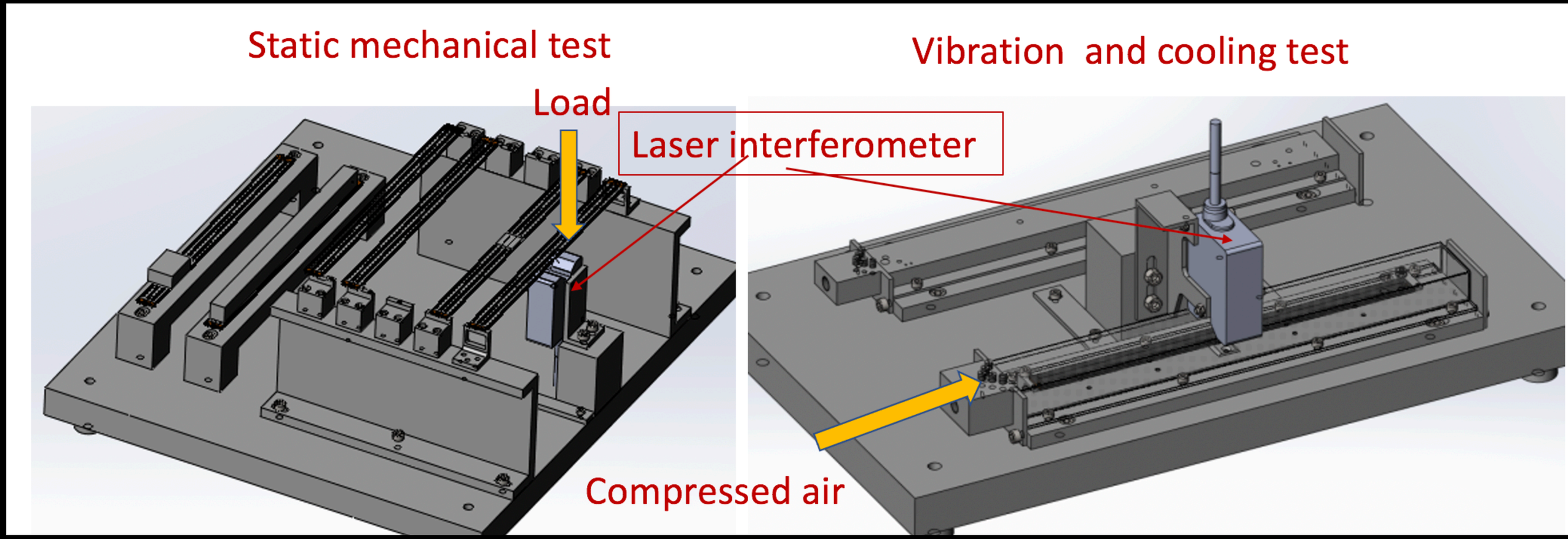




Backup: Ladder Mechanical testing

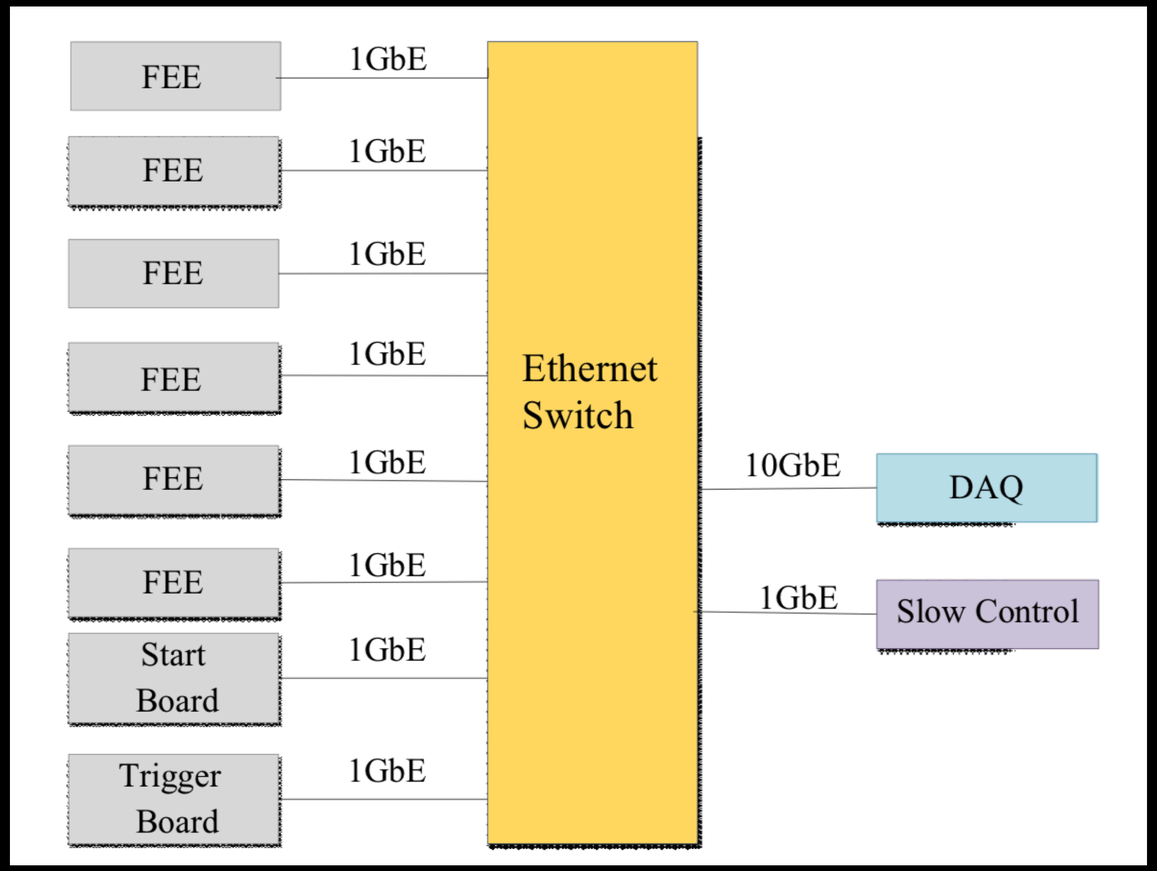
Detailed designs of platform and tooling for different test.

- **Static (different support and load cases)**
- **Vibration and cooling + pressed air (different cases):**
  - **Measure Deformation, temperature, air speed, flow rate, etc.**
- **Goal: Measure vibration to 1μm level with air cooling with laser interferometer**



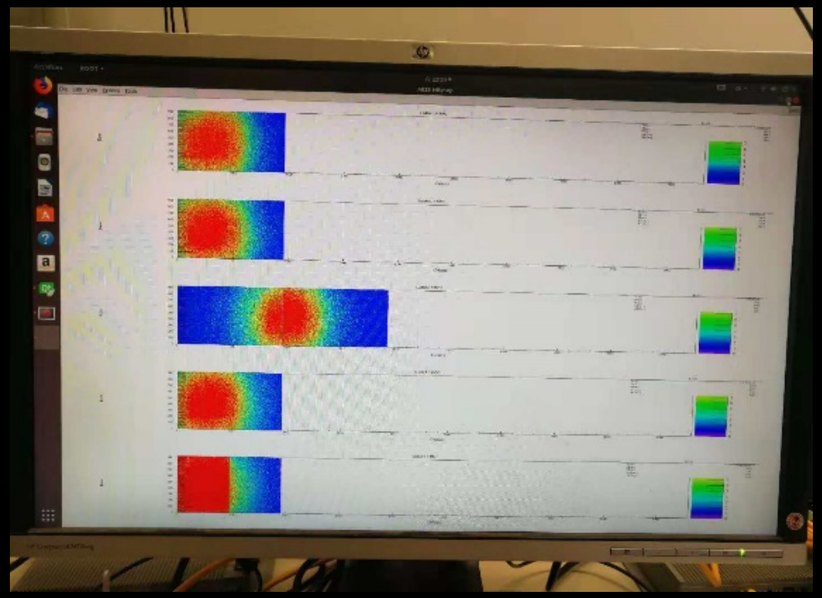
Data acquisition system

- Preliminary design of data acquisition system(DAQ)
  - Ladders are reader by readout boards
  - All readout boards connected to computer through a switch
  - User interface developed
  - DAQ tested in five modules equipped with MIMOSA sensors



DAQ Tests with 5 MIMOSA chips

DAQ system data display
Tested with MIMOSA modules



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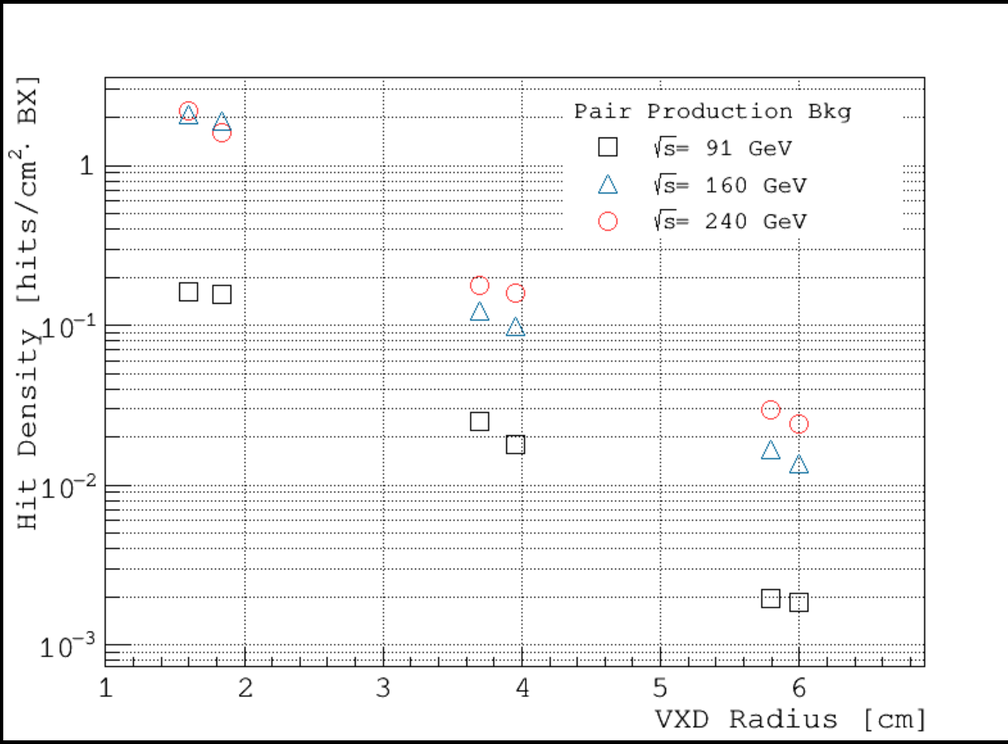

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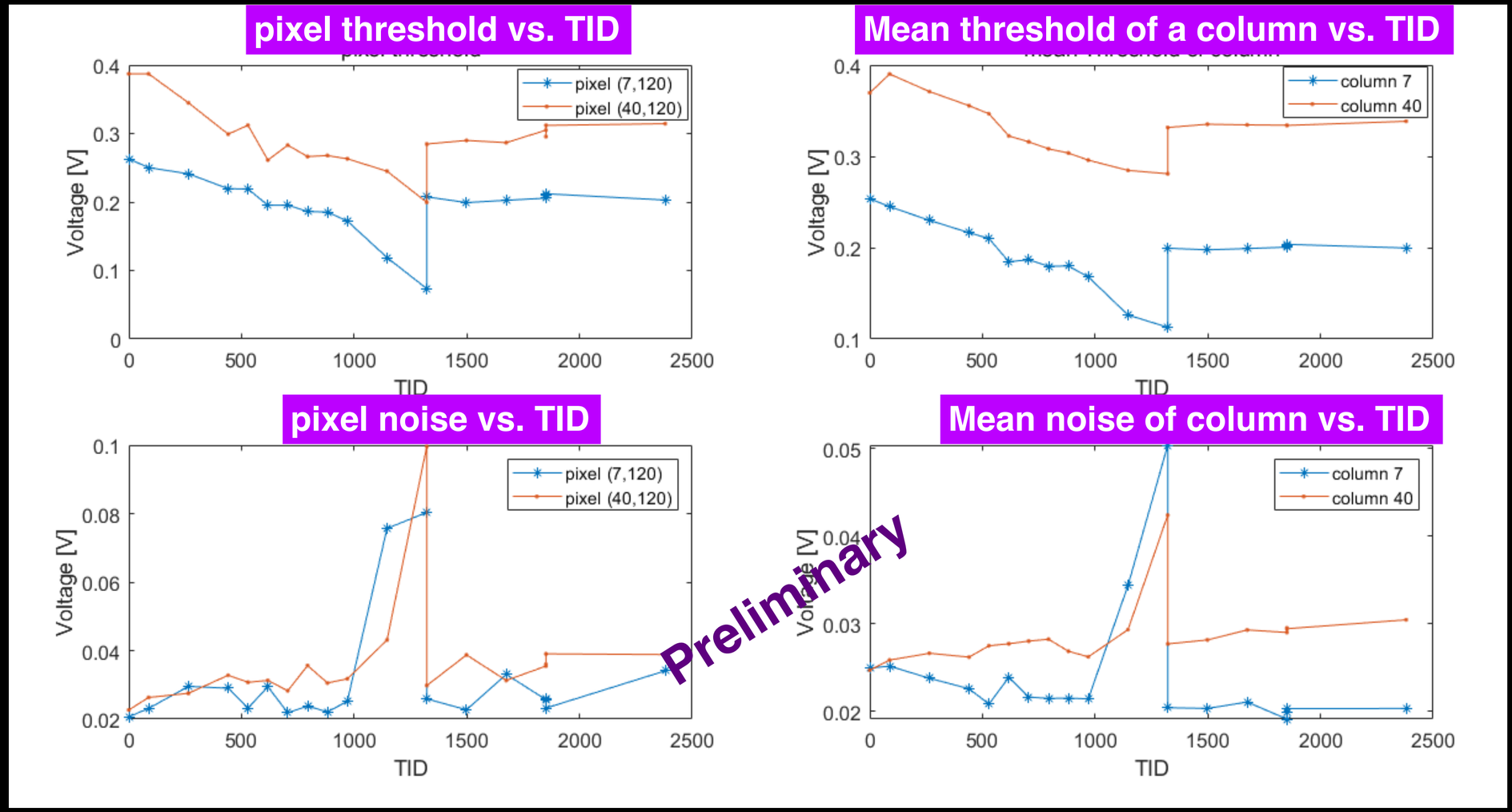
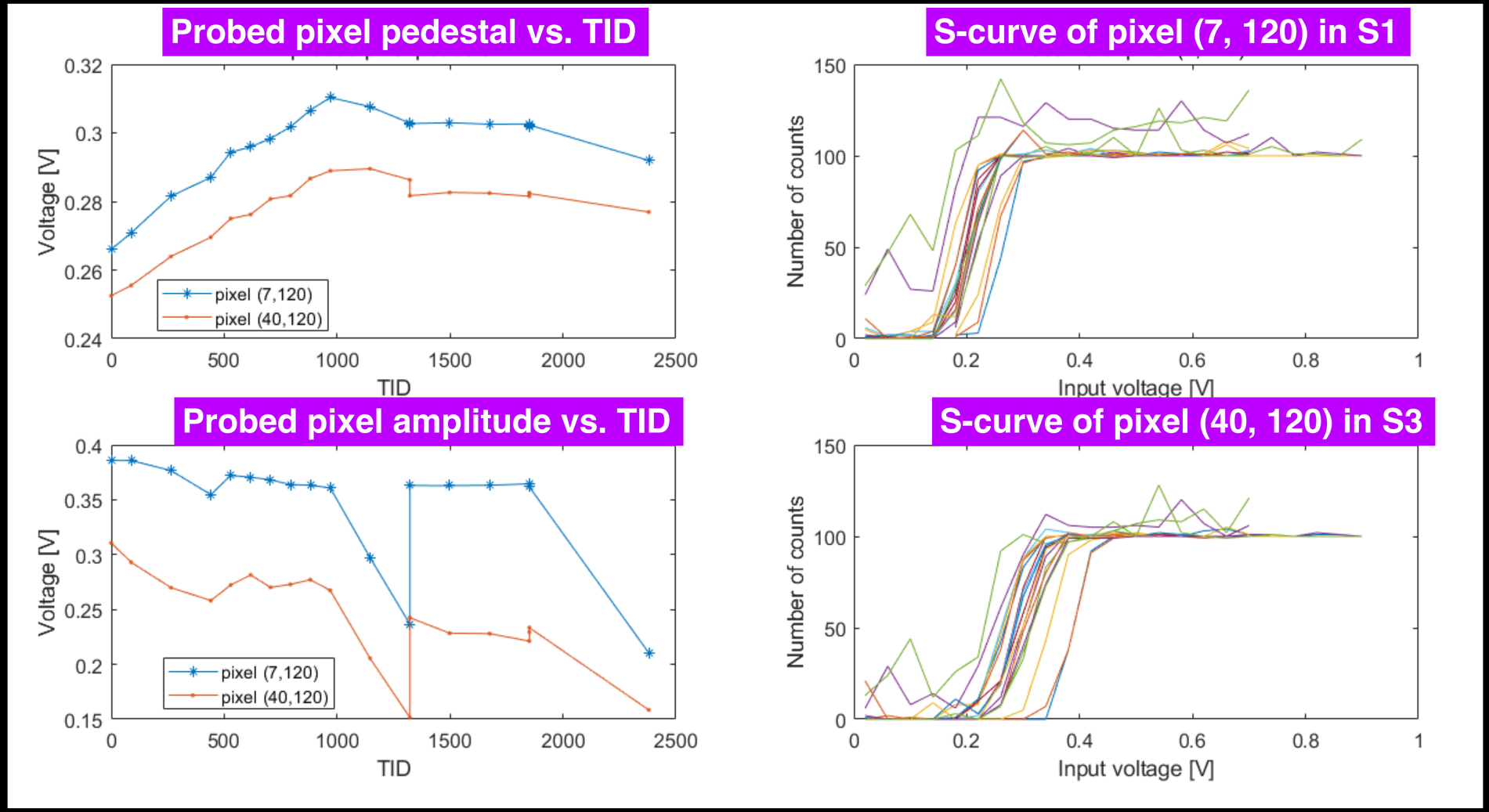
backup :



Good chip function and noise performance proved to 2.5 Mrad,

Backup:



The threshold was initially set at the minimum level. After ~1 Mrad, the pedestal level was shifted to see noise floor in S-curves, so the threshold level was set higher.

Publications and International talks

Publication:

High data-rate readout logic design of a 512 × 1024 pixel array dedicated for CEPC vertex detector

X. Wei,[a,1] W. Wei,[b] T. Wu,[c,d] Y. Zhang,[b] X. Li,[b] L. Zhang,[e] W. Lu,[b] Z. Liang,[b] J. Dong,[e] L. Li,[e] J. Wang,[a] R. Zheng,[a] R. Casanova,[d] S. Grinstein,[d] Y. Hu[f] and J. Guimaraes da Costa[b]

JINST 14 (2019) C12012

A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector

Tianya Wu[1,2], Raimon Casanova[2], Wei Wei[3], Xiaomin Wei[4], Ying Zhang[3], Liang Zhang[5], Xiaoting Li[3], Zhijun Liang[3], Joao Guimaraes da Costa[3], Weiguo Lu[3], Jianing Dong[5], Long Li[5], Wang Jia[4], Ran Zheng[4], Ping Yang[1], Guangming Huang[1] and Sebastian Grinstein[2]

- International conference talks:

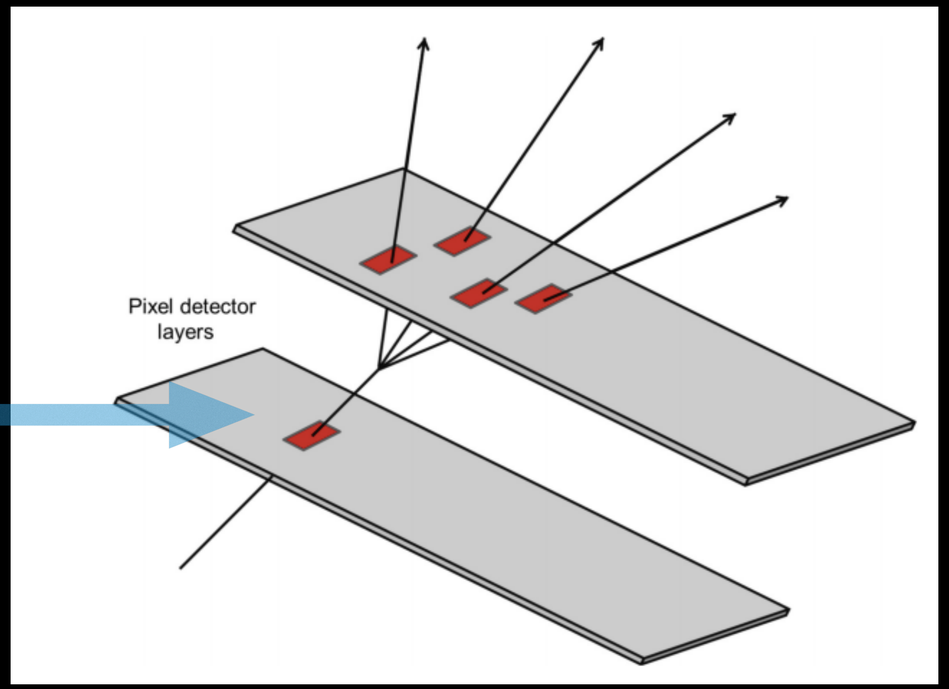
IEEE ICECS (doi: 10.1109/ICECS46596.2019.8965105.)

- Joao Guimaraes Da Costa, CepC phys/detectors, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
- T. Wu , A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector, in proceeding of International Conference on Electronics Circuits and Systems, Nov. 27-29, 2019, Genova, Italy.
- Xiaomin Wei, High data-rate readout logic design for 1024*512 CMOS pixel array dedicated for CEPC experiment, International workshop on radiation imaging detectors, International workshop on radiation imaging detectors, July 2019, Crete, Greece
- Ying Zhang, Overview of the chip design for the MOST2 CEPC vertex project, Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK
- Wei Wei, Full size pixel chip for high-rate CEPC Vertex Detector， Workshop on the Circular Electron-Positron Collider,EU Edition, April 15 - 17, 2019, Oxford, UK

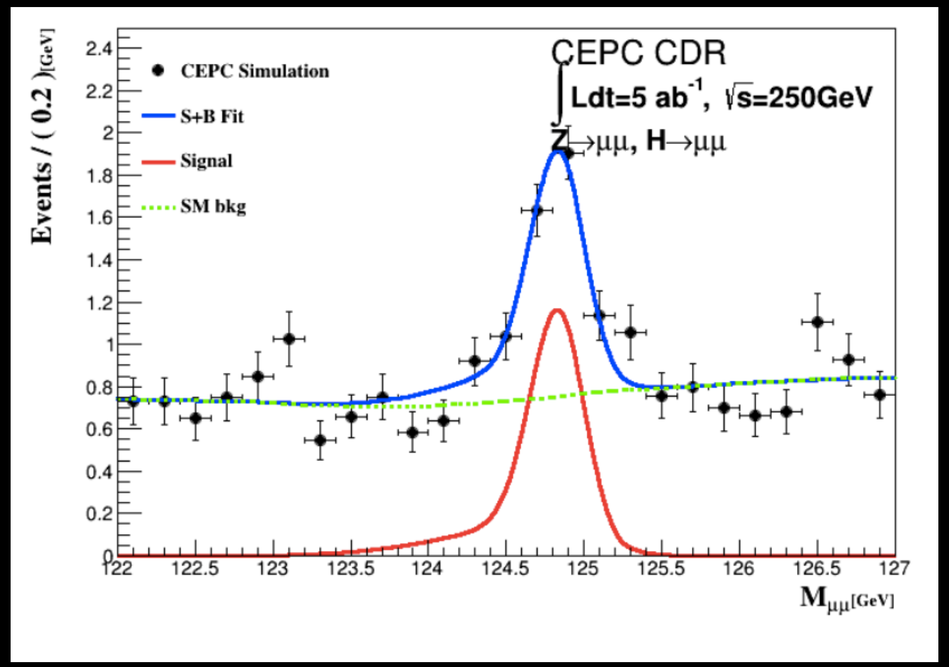
Task 2: Physics goal

- Higgs precision measurement
  - H → bb precise vertex reconstruction
  - H → μμ (precise momentum measurement)

Need tracking detector with high spatial resolution, low material



- Main technology
  - High spatial resolution technology → pixel detector
  - Low-mass detector technology
  - Radiation resistance technology



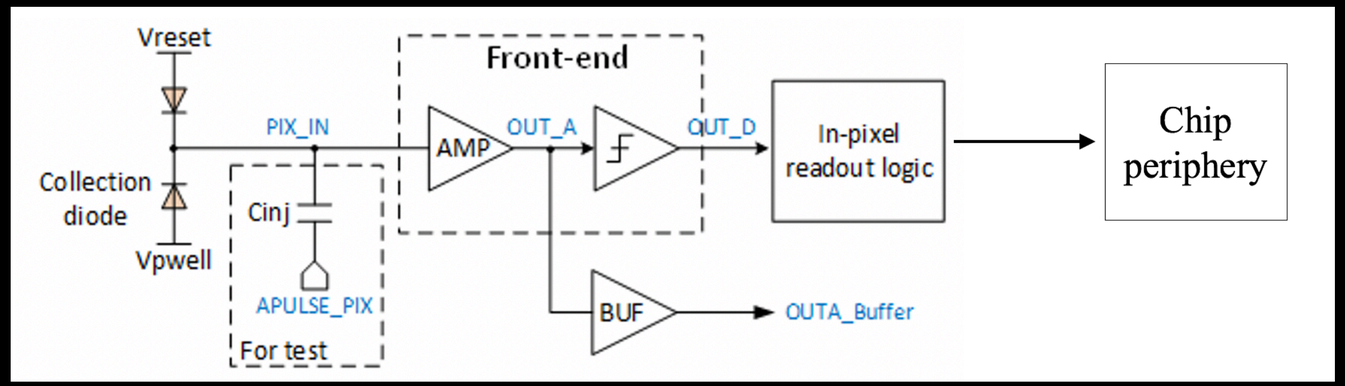
Goal for the third year(2020.7 –2021.6)

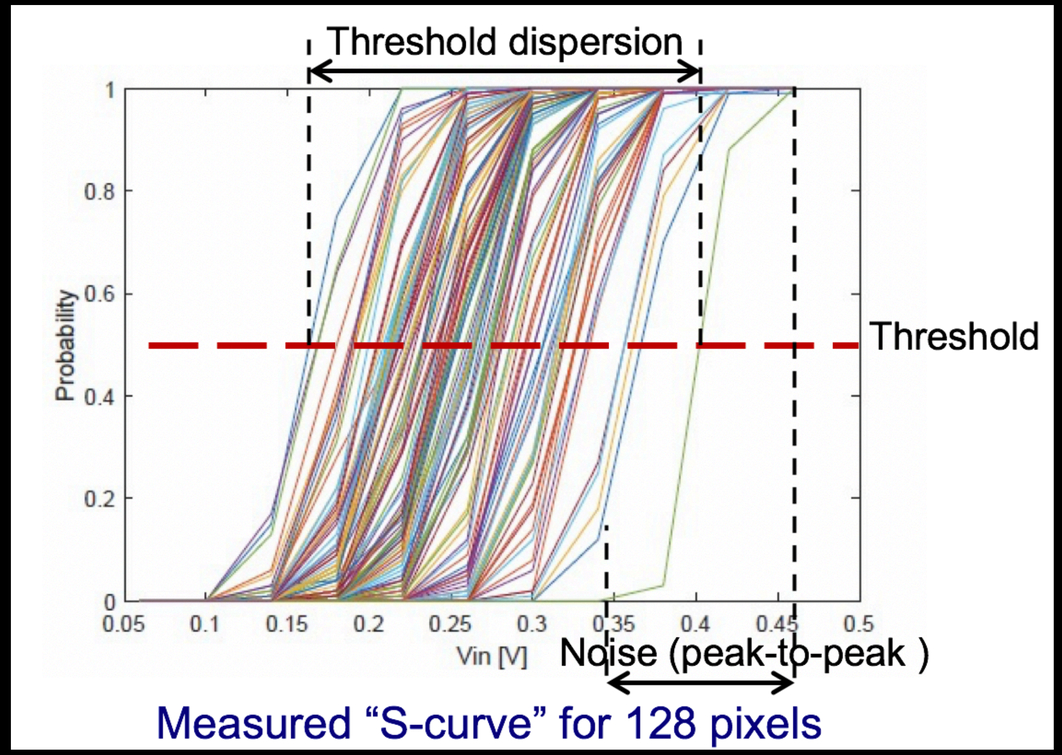
- Achieve the target in task book for the 3rd years
  - Build the support structure prototype for ladder
  - Finalize the full-size sensor design , and write a design report
  - Complete the testing of 2nd MPW Taichu chip, write a testing report
  - Complete initial design of readout electronics and DAQ for vertex detector prototype

2020 年 7 月 | 2021 年 6 月	加工并完成探测器模块单元的结构样品；对第二次 MPW 流片的芯片做全面的测试（包括大剂量的辐照测试）以验证其功能性。根据测试结果，优化外围数字电路设计，并修正像素内前端放大器电路，优化抗辐照电路器件的设计，并整合芯片各模块功能的设计，并提交第三次多项目晶圆（MPW）流片加工，加工后进行快速验证性的测试；设计大面积、全功能的传感器芯片，为大批量的工程批流片做好准备；初步设计探测器原型机整机系统读出电子学的数据获取系统。	1. 研制出探测器单元模块的结构样品。 2.完成全功能的传感器芯片的设计，并完成设计报告。 3.完成第二次的 MPW 流片后芯片的测试，完成测试报告。 4. 完成探测器原型机整机的读出电子学与数据获取系统的初步设计报告。	课题年度报告

Electrical test

- Electrical performance verified by injecting an external charge into pixel front-end

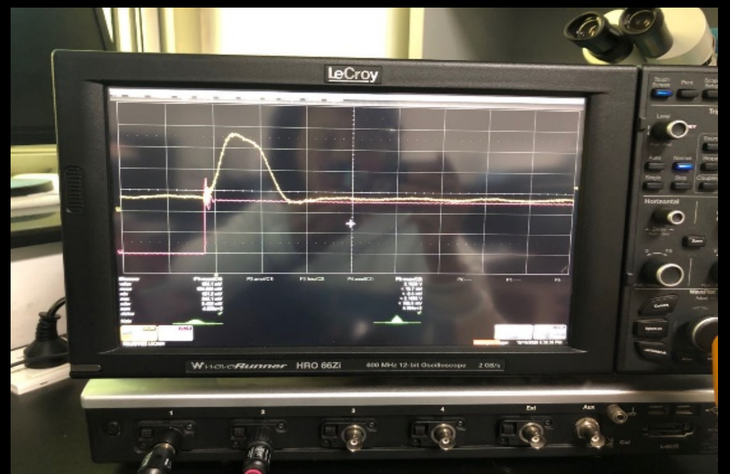




Measured “S-curve” for 128 pixels

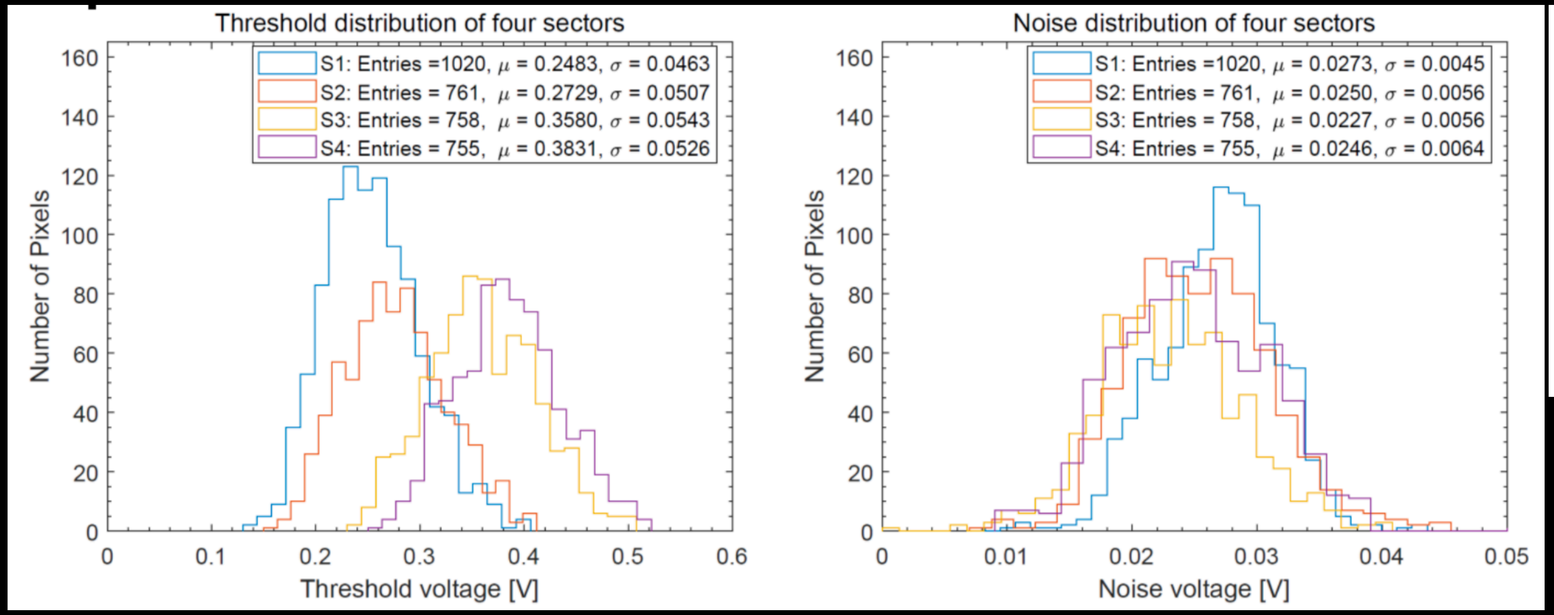
Sector	Pixel front-end	Pixel digital	Pixel size
Sector 1	Same as S1 of TC1, reference design	FEI3-like	25 µm × 25 µm
Sector 2	M6 with guard-ring, PMOS in independent nwell	FEI3-like	25 µm × 25 µm
Sector 3	M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 µm × 24 µm
Sector 4	Increasing M3, M4, M9. M6 in enclosed layout, PMOS in independent nwell	FEI3-like	25 µm × 25 µm
Sector 5	Same FE as S2, with smaller sensor	ALPIDE-like	25 µm × 25 µm
Sector 6	Same FE as S1	ALPIDE-like	25 µm × 25 µm

Analog output of a pixel @ Vin = 0.9 V



Electrical test （2）

- Four sectors with FEI3-like digital logic works well
- and show similar noise performance for 4 different pixel design.
- S1 sector design shows the minimum threshold.



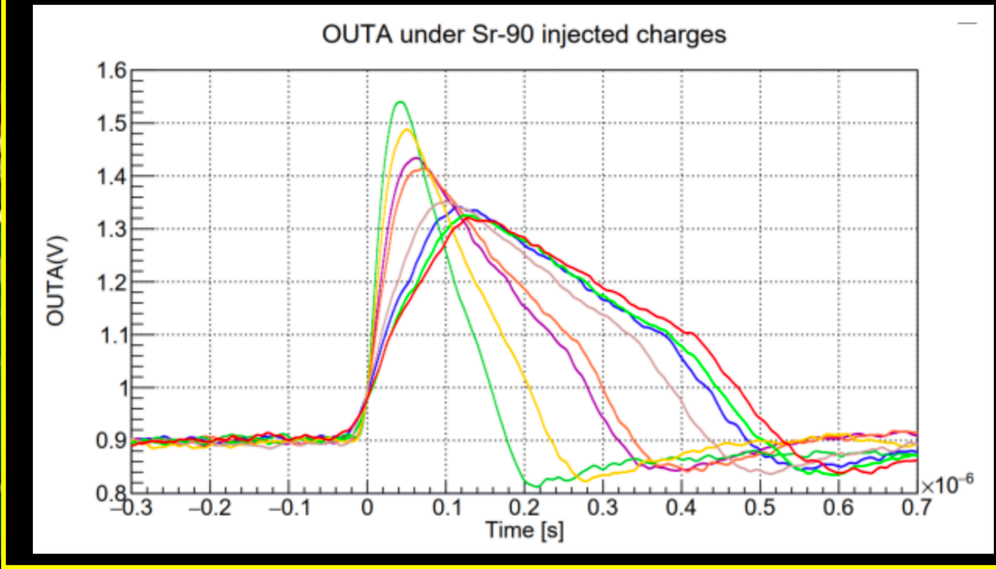
Preliminary

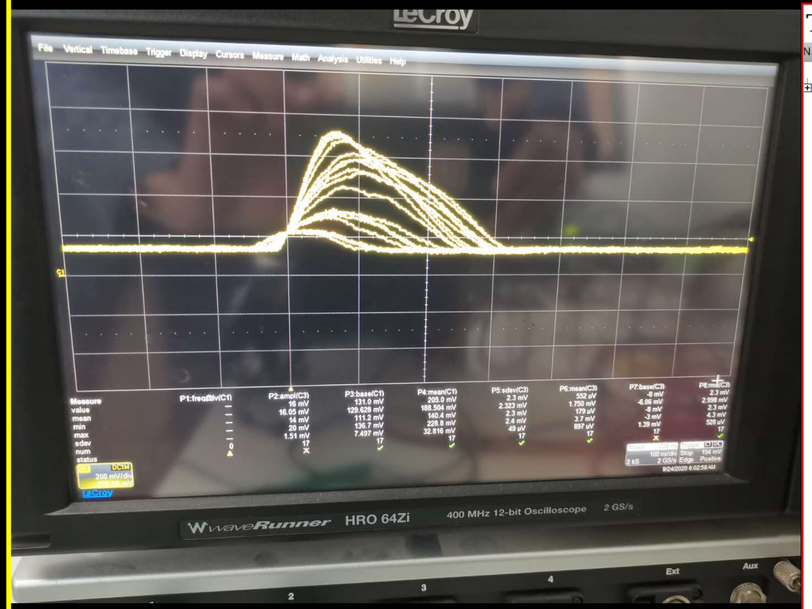
	Threshold Mean (mV)	Threshold rms (mV)	Random noise (mV)	Total equivalent noise (mV)
S1	248.3	46.3	27.3	53.8
S2	272.9	50.7	25.0	56.5
S3	358.0	54.3	22.7	58.9
S4	383.1	52.6	24.6	58.1

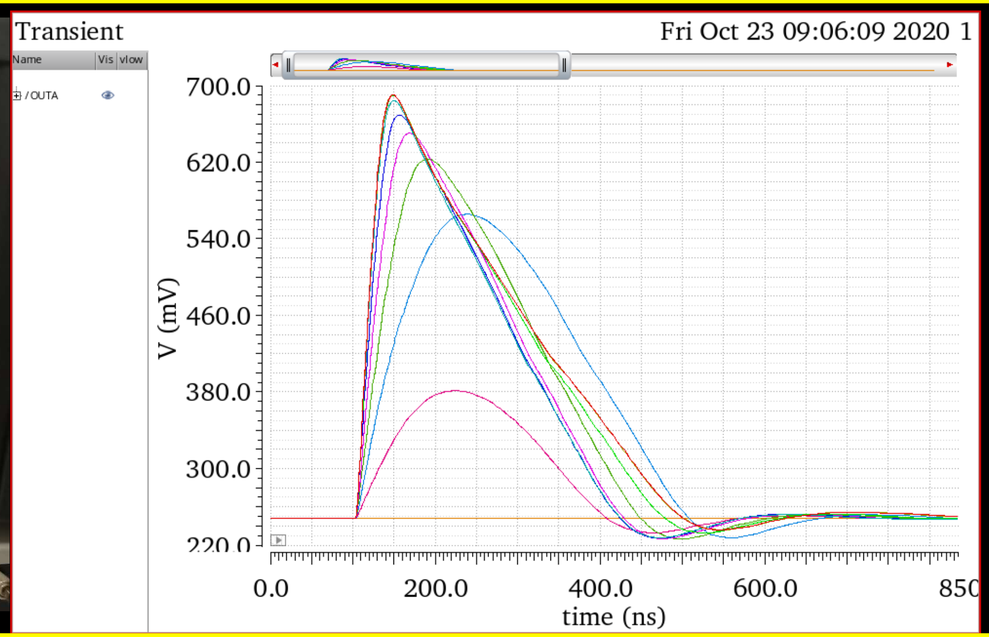
X ray tests and beta source tests

- Analog output waveform agreed with the simulation
- for the small signal, the S/N ratio was also good

Beta source Tests



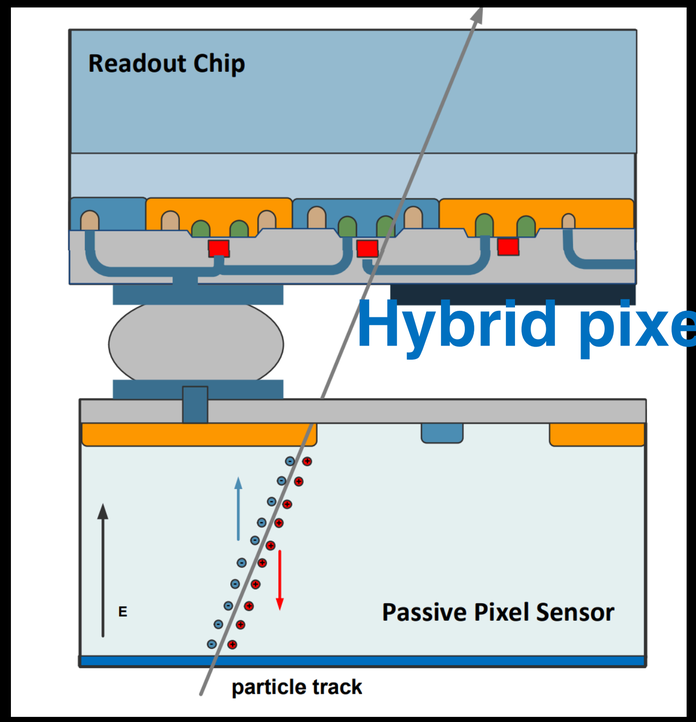


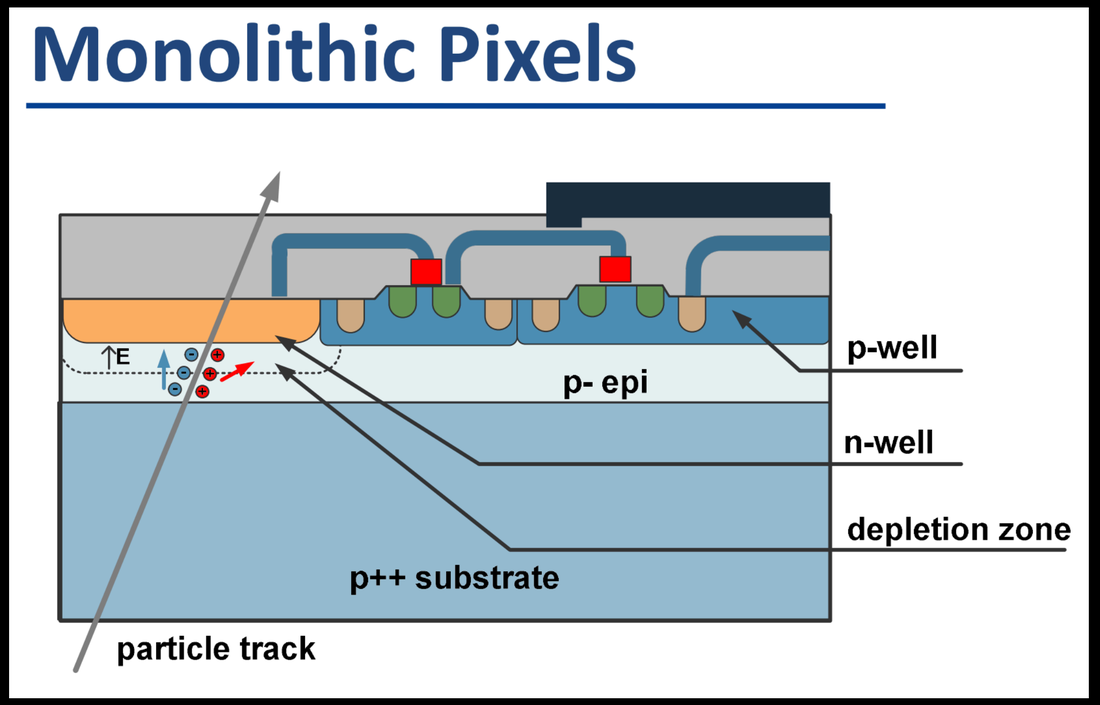


X ray tube test

CMOS Monolithic pixel sensor

- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - low material budget (can be thin down to 50μm)
  - This project use TowerJazz CIS 180nm technology
- Hybrid pixel technology developed by ATLAS and CMS
  - Thickness of sensor is about 200~300 μm
  - Need to bump bonding with readout ASIC (ASIC thickness is about 300μm)
  - Material budget about silicon sensor is about 10 times larger than CIS process





Research Team in task 2

4 institutes

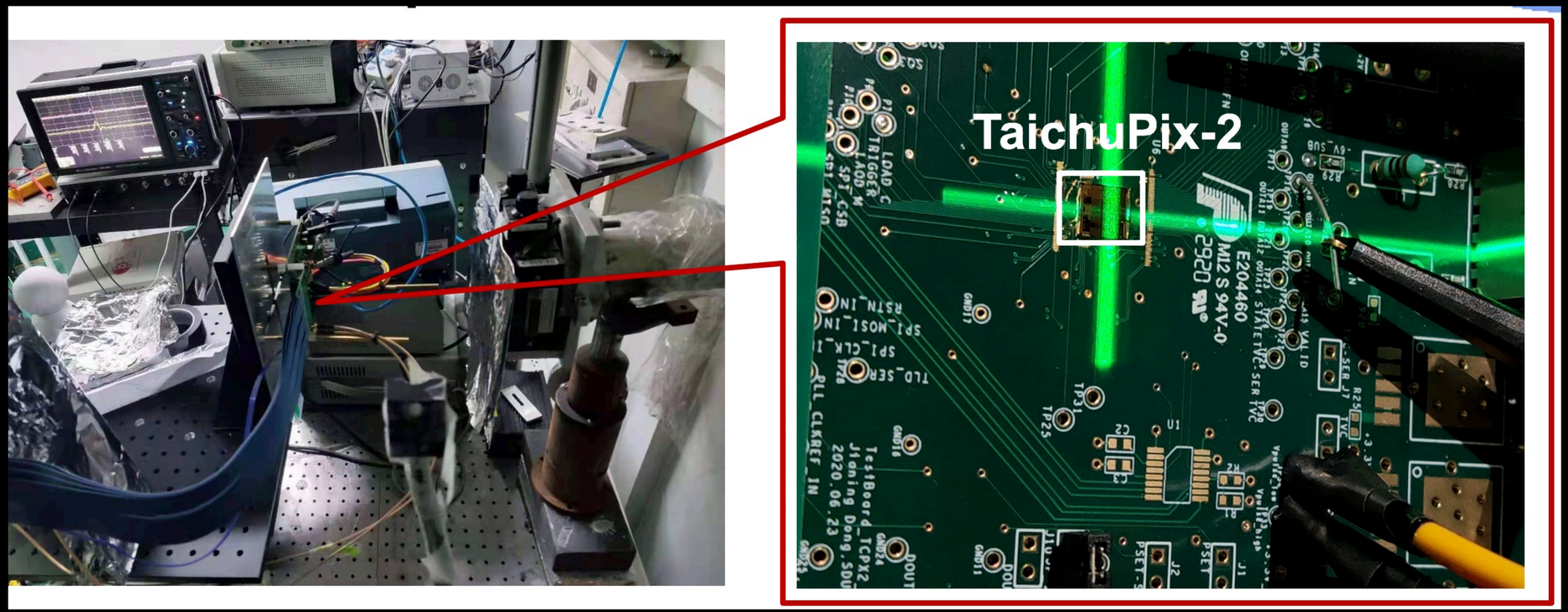
课题2：**IHEP - 中国科学院高能物理研究所**
SDU - 山东大学
NJU - 南京大学
NWU - 西北工业大学

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning
CCNU/IFAE	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
SDU	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
NJU	Irradiation, test beam organization

TaichuPix radiation test

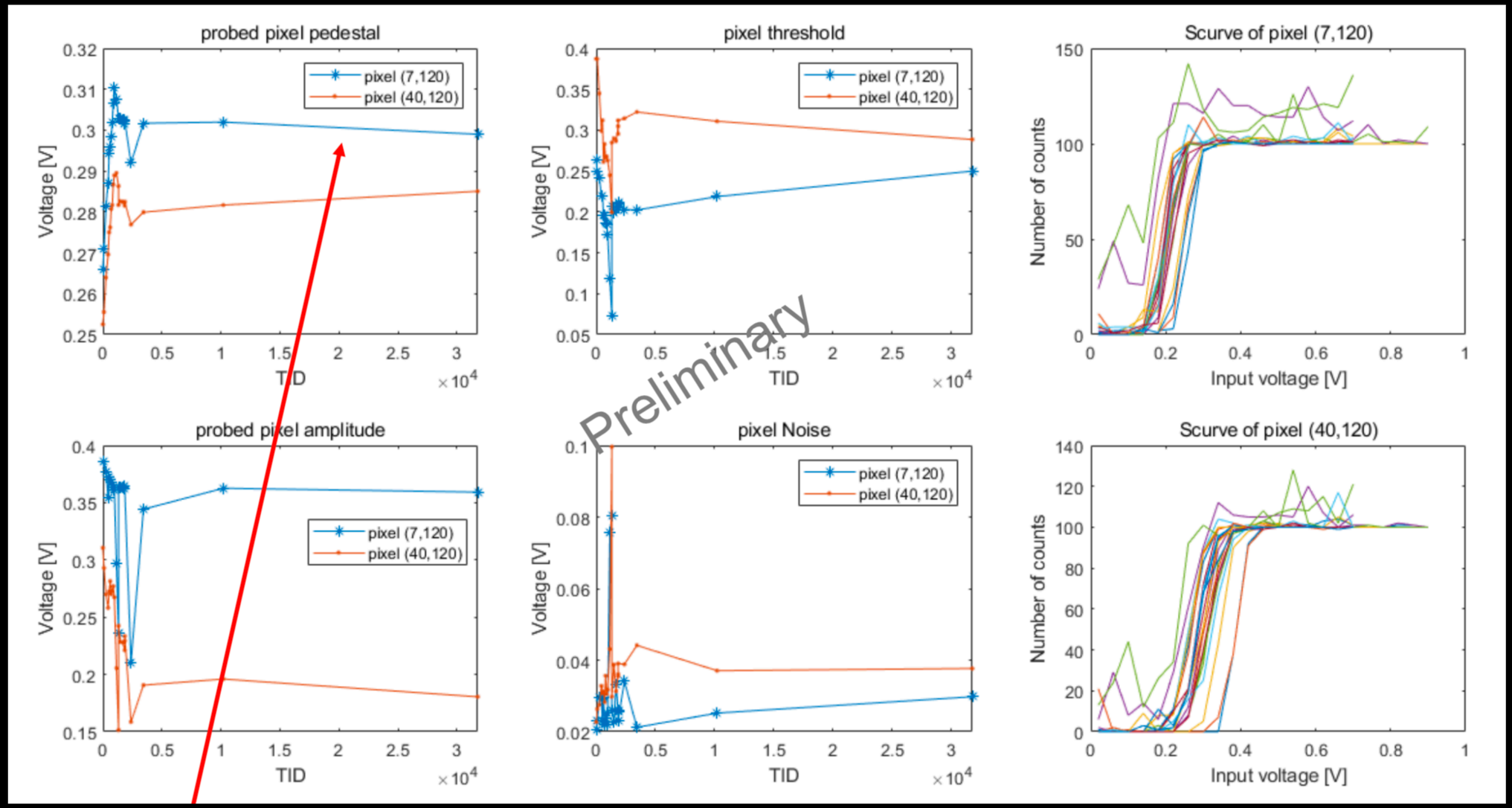
- Completed two round of CMOS sensor prototyping
  - First Radiation test up to 30Mrad at BSRF , TaichuPix2 is still functional
  - TaichuPix-2 irradiated at BSRF 1W2B beamline (6 keV X-ray)
    - Dose rate ~17.63 krad/min for the first 2.5 Mrad
    - then 211.56 krad/min for 51 min, then 1.24 Mrad/min for 15 min
    - Dose rates were calibrated with an ion chamber before test

Radiation test at BSRF for 2nd MPW chip



TaichuPix radiation test (2)

- Good chip function and noise performance proved to 2.5 Mrad,
- no deterioration observed when TID up to 30 Mrad.



TaichuPix radiation test (3)

- No deterioration observed when TID up to 30 Mrad.