CEPC HCAL Progress

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On behalf of CEPC Calorimeter working group

Outline

CEPC AHCAL Status

- Scintillators mass production and test
- SiPM batch test
- ➤ HBU design
- Cooling simulation and Mechanical Design
- ➤ CEPC DHCAL
 - ≻ RPC
 - ≻ RWELL
- Summary and outlook

AHCAL Prototype

Sampling Calorimeter

- 40 layers, ~ 5 N.I.L
- -72 cm \times 72 cm
- Absorber
 - Iron, 2 cm thickness
- Sensitive Detector
 - Scintillator+SiPM, Number:13,960
 - Cell size: 40 mm \times 40 mm \times 3mm
 - SiPM: HPK and NDL

Electronics

- SPIROC2E ASIC Chip



AHCAL Structure

Scintillator mass production and packaging

More than 15000 scintillators were produced based on ejection molding and packaging using ESR film in August







All the packaged scintillators (~15000) have been tested using Sr-90 β-ray source

- ♦ SJTU, USTC
- The automatic displacement platform controls the movement of radioactive source and tests the scintillator one by one



♦14,219 pieces within 10% of 15,524 pieces in total. About

91.6% of scintillators are qualified (within 10% of LY window).





SiPM Procurement and testing

- Two different types SiPM were selected in this prototype
 - ♦ NDL, 1700 pieces
 - ◆ HAMAMATSU, ~13000 pieces



Company	NDL	НРК	
Туре	22-15	S14160-1315PS	
Sensitive area (mm ²)	1.6*4	1.69	
PDE (%)	40	32	
Gain (*10 ⁵)	2.4	3.6	
Pixel No.	7400*4	7284	
Breakdown Voltage (V)	28	38	
OverVoltage (V)	4	4	
Dark Count (kHz)	330*4	120	
Cross Talk (%)	8.5	1.0	

NDL



S14160-1315PS

SiPM bench test system

- Two sets of SiPM batch test systems were developed
 - NDL SiPM
 - HPK SiPM





HPK





NDL

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HPK SiPM Test



Dark Counting Rate

Photon-electron peak

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Darameter	Symbol	S14160				Unit	
Parameter		-1310PS	-3010PS	-1315PS	-3015PS	Onic	
Spectral response range	9	λ	290 to 900		nm		
Peak sensitivity waveler	ngth	λр	460			nm	
Photon detection efficie	ncy at λp ^{*3}	PDE	18		32		%
Breakdown voltage*4		VBR	38±3				V
Recommended operating voltage*4		Vop	VBR + 5 VBR + 4		+ 4	V	
Vop variation within a re	eel	-	±0.1		V		
Dark count rate*5	typ.	DCD	120	700	120	700	kene
	max.	DCK	360	2100	360	2100	kcps
Direct crosstalk probabi	lity	Pct	$\left(\begin{array}{c} <1 \end{array}\right)$		%		
Terminal capacitance at	Vop	Ct	100	530	100	530	pF
Gain		M	1.8 × 10 ⁵ 3.6 × 10 ⁵		< 10 ⁵	-	
Temperature coefficient	of Vop	ΔTVop	34		4		mV/°C

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NDL SiPM





NDL SiPM

I-V curve



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NDL SiPM photon electron spectrum



HG SPS Chip0 Channel10 HG SPS Chip0 Channel10 peak:242.7 o:4.4 60000 333.6 peak:269.0 o:7.6 500 58.82 peak:295.5 c:8.0 peak:320.8 c;8.1 400 peak:349.4 o:12.4 300 200 31.0 V 100 0 100 200 300 400 500 600 700 800 900 1000 ADC







NDL SiPM photon electron spectrum

we found that the SNR of a few SiPM was very small
the photoelectric peaks disappeared with the increase of voltage



At present, these SiPMs account for 7% of the total



HBU-v2 update

- Optimize HBU size and Type-C interface
- Add additional buffer to the sub-board to ensure the signal integrity
- Keep real-time control signal among SP2e equaling to ensure all the SP2e in a same condition







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Cooling simulation

- The power consumption of each layer of HBU is about 4 W
- The main heat sources are electronic chips
- In order to reduce the influence of temperature, we add some fans next to the AHCAL





Fe-Heating source-PCB-Scintillator-Fe

(Fe-Heating source-PCB-Scintillator)*n-Fe

Cooling simulation



- For heating sources: The mean temperature of the origin: 48°C to 58°C. Thermal conductive rubbers reduce the mean temperature by about 20°C. Fans further reduce the average temperature by about 6°C.
- For SiPMs: The mean temperature of the origin: 28°C to 38°C. Thermal conductive rubbers reduce the mean temperature by about 8°C. Fans further reduce the average temperature by about 6°C.

HBU box mechanical design

- In order to facilitate testing and transportation, each HBU has a cassette
- We choose iron as the material of the box, and the mass of this part is directly deducted from the absorber



HBU box mechanical design

- The first version has been processed and is being trial assembled with HBU
- Heat dissipation test shall be carried out after welding of HBU







HBU box mechanical design

Then we can install these cassettes directly into the supporting structure of the prototype



CEPC DHCAL

Resistive Plate Chamber





• Resistive WELL detector (RWELL):



DHCAL Based on GRPC

Size : 1m*1m*1.3m Nbr layers : 48 of RPC Cell Size : 1cm*1cm



(0. $12\lambda_I$, 1. $14X_0$)



Readout Mylar layer PCB pads/ PCB (12m m)+ASICs(1.7 interconnect (1cn/x)Readout ASIC (Hardroc2) mm) 1 cm/ PCB support 16mm) gap Cathode glass Mylar Ceramic ball spacer (1.1mm) Glass fiber frame + resistive coatinge glass (0.7mm) (1.2 mm)(≈1.2mm) + resistive coatir 44 ASICs= 9216 channels/1m 3 mm RPC (glass) ASIC HARDROC (64 ch) 1.2 - 1.4 mm PCB 3-threshold: 110fC, 5pC, 15pC 1.6 mm ASIC

Gas flow simulation for GRPC

- Gas flow has a strong impact on the uniformity, efficiency of GRPC
 - The bigger chamber, the more critical it's become
 - For large GRPC 1820 × 990 mm, simulate the gas flow impact
 - Compare the spacer position, the velocity is more uniform with the shifted design





GRPC construction



Flipping and 2nd glass positionning

Walls positionning



2nd glass gluing gas tightning

Spacers positionning



Walls/spacers gluing







GRPC test

Cosmic ray test



Fabrication of RWELL detector

100cm×50cm RWELL:









Painting the glue

Pumping and drying

Assembling

100cm×50cm RWELL detector

- We make a special PCB and use it as the gluing mask;
- We put glue on both resistive layer PCB and THGEM PCB;
- A vacuum platform was used for gluing;
- 8 pieces of readout PCB are used, there are 25
 - pad(Pad size 5cm×5cm) on each pcb



25 cm \times 25 cm Readout PCB

RWELL performance

• Gain vs HV:



Rate capability: >100 kHz/cm²



Gain Uniformity : RMS/Mean~14.0%@~5175 Gain





• Efficiency : ~95.9%



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Summary and outlook

- The light yield test of all scintillators has been completed.
 - A total of 14219 / 15524 scintillators meet our requirement (the prototype needs 13960)
- Two SiPM test systems are developed and applied to the test
 - One is for SiPM of HAMAMATSU, the other is for NDL
- The new HBU has been tested
- Under the existing power consumption, the influence of air cooling design of AHCAL was simulated
 - The design of fan + thermal conductive rubber pad can effectively reduce the temperature of the AHCAL
- HBU cassette handling is being carried out
- The DHCAL based on GRPC and RWELL are carried out in an orderly manner



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 THANKS



backup



HCAL Baseboard Unit Status

- One layer has 3 sub-HBUs
- One sub-HBU is $78.5 \times 24 \text{cm}^2$
- Flexible boards are used to transmit power and signal between the 3 sub-HBUs and DIF
- Each sub-HBU has 3 SPIROC2E chips
 - The chips were packaged in China





AHCAL



Data InterFace (DIF) board

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Pedestal of HBU

- The pedestal of each channel was calibrated using random trigger
- The pedestal positions are differences between chips
- The channels of the same chip are relatively uniform
- The pedestal width has little to do with the chip



The pedestal of one channel



The pedestal of each channel in HBU

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HBU Support Frame

- A 5mm thick AI support frame is machined for trial assembly and testing with HBU
- The optimization of the support frame will be discussed next step





