Status update on JadePix-4/MIC5

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On behalf of the JadePix-4 design team

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- Motivation
- Design specs
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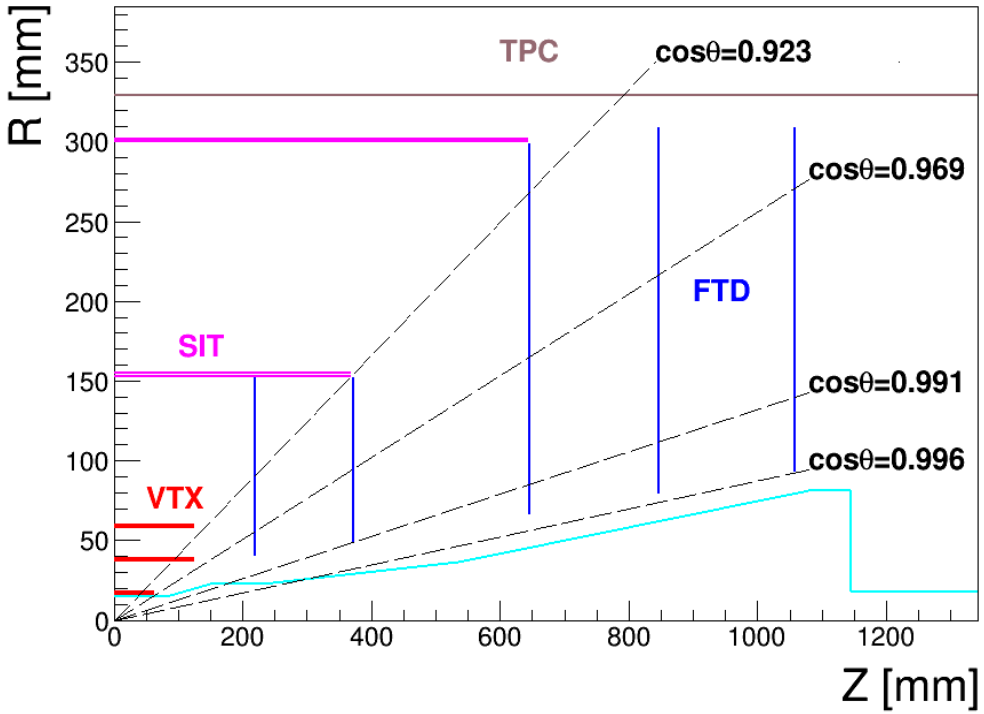
- Implementation
- Readout mode
- Summary

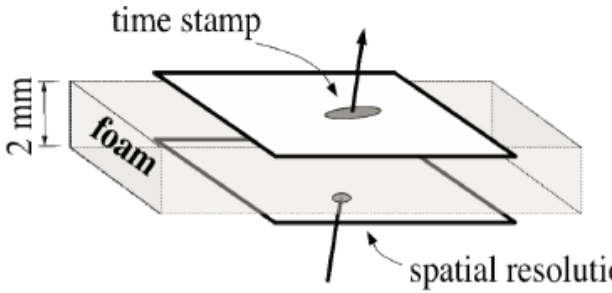
Motivation

Silicon tracking system



- Baseline design in the CDR stage
  - VTX: 3 (mechanical) layers of double-sided pixels
  - Pixel sensor identified as one of the critical R&Ds
  - High resolution, fast readout, low power

- Complementary design for the layer 1
  - Inner side: high resolution and low power
  - Outside: Fast readout and low power



Concept of double-sided structure

Baseline design parameters

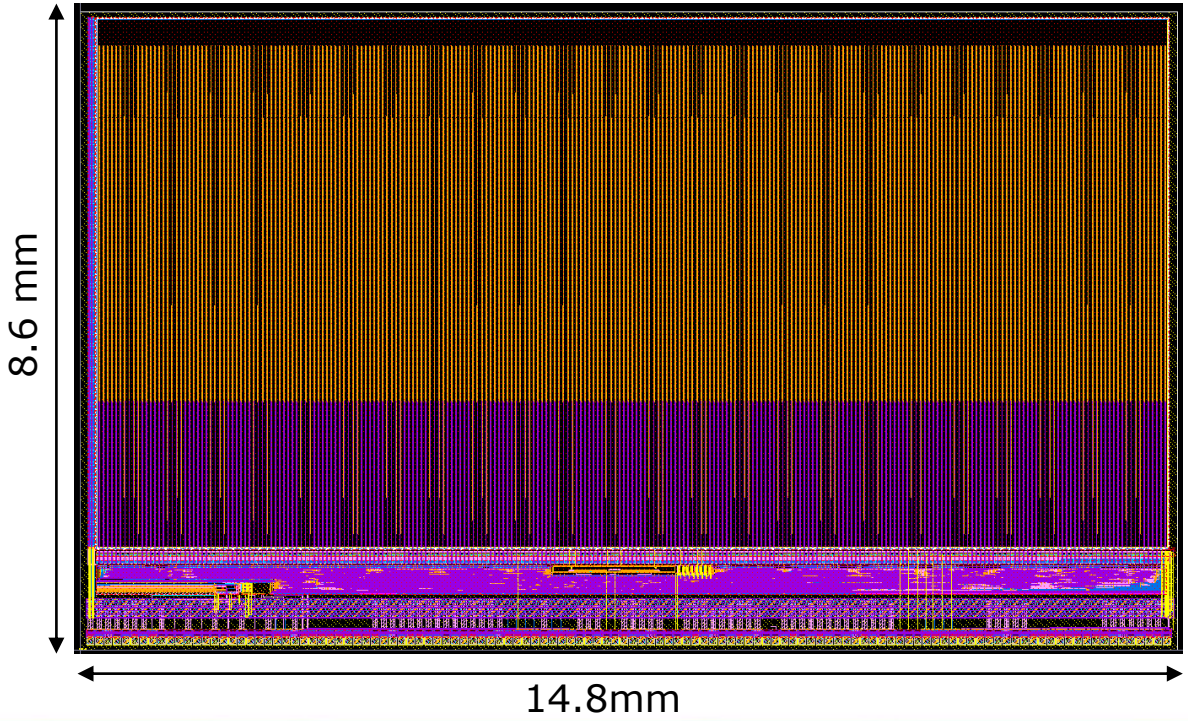
	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	0.15%/X_0
	18	62.5	6	0.15%/X_0
Layer 2	37	125.0	4	0.15%/X_0
	39	125.0	4	0.15%/X_0
Layer 3	58	125.0	4	0.15%/X_0
	60	125.0	4	0.15%/X_0

Design specs

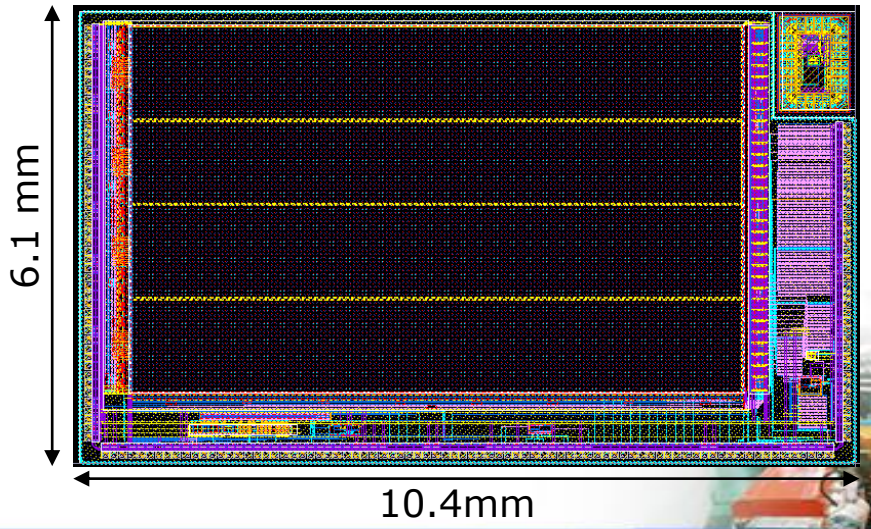
- JadePix-4 optimized for fast readout and low power
  - With pixel size ~ 20 μm × 30 μm,
  - Mask area: 14.8 mm × 8.6 mm

	S.P. resolution	Integration time	Average power
JadePix-4	<5 μm	~1 μs	< 100 mW/cm^2
JadePix-3	<3 μm	<100 μs	< 100 mW/cm^2

JadePix-4 Layout

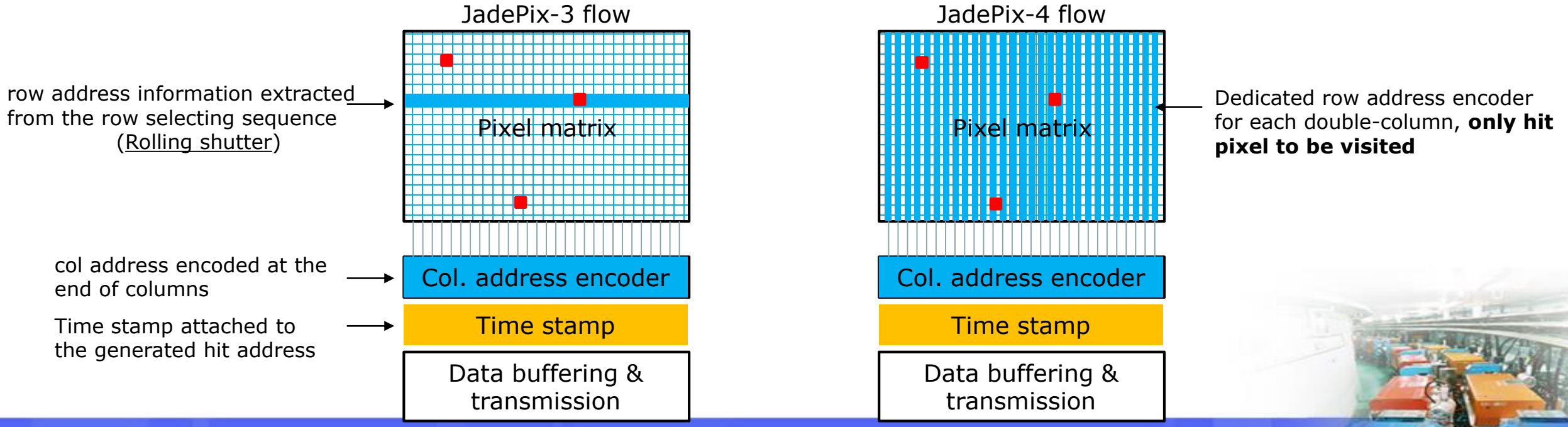


JadePix-3 Layout



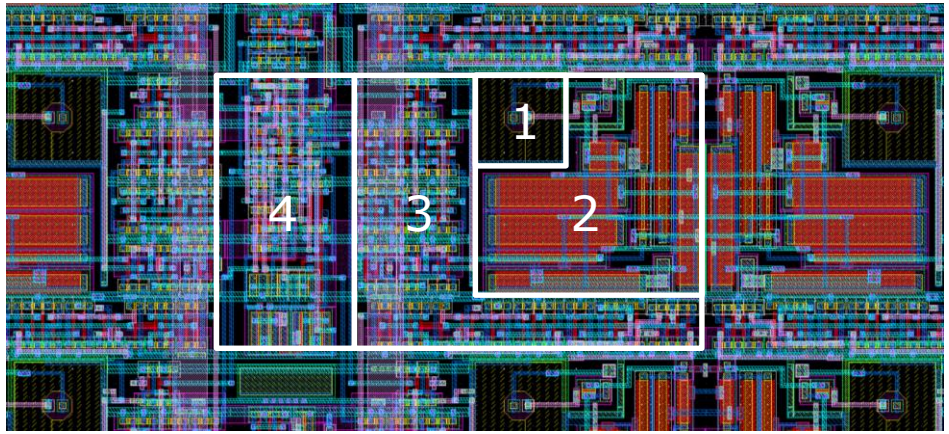
Hit processing flow

- Hit registered in the each pixel needs fast processing
  - Hit position (col. and row address) to be encoded
  - Time stamp to be attached
  - Register to be reset for the next hit
- A major modification on the hit processing flow
  - Row address encoding embedded into the active pixel matrix, which is much faster



Implementation

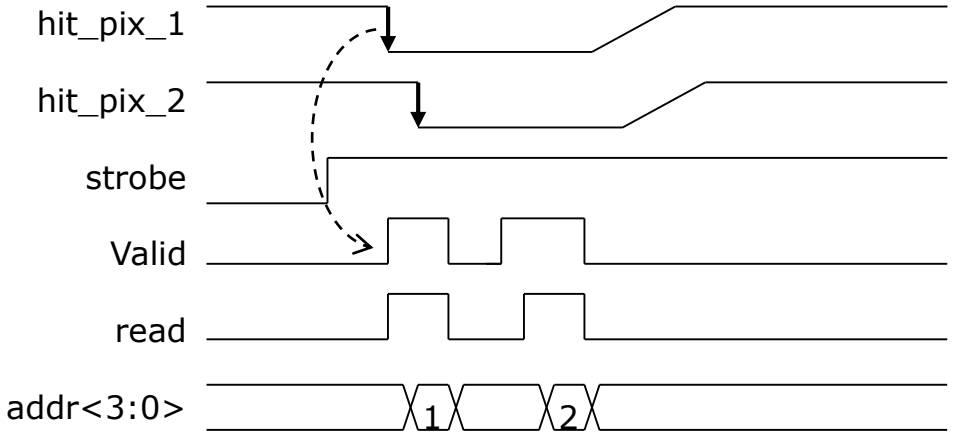
- Tower Semiconductor (Tower Jazz) 180nm CIS process
- Key component verified and reused from JadePix-3
  - Diode
  - Analog frontend
  - Hit register
- Asynchronized Encoder and Reset Decoder (AERD)
  - Analog design flow for the row encoding (Human intuitive)
  - Digital design flow for the col. encoding (Algorithm driven)
- Final layout of pixel matrix
  - pixel array: 356 row × 498 col.
  - Pixel size: 20 μm × 29 μm

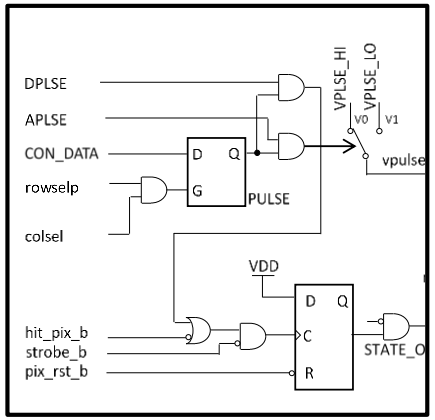


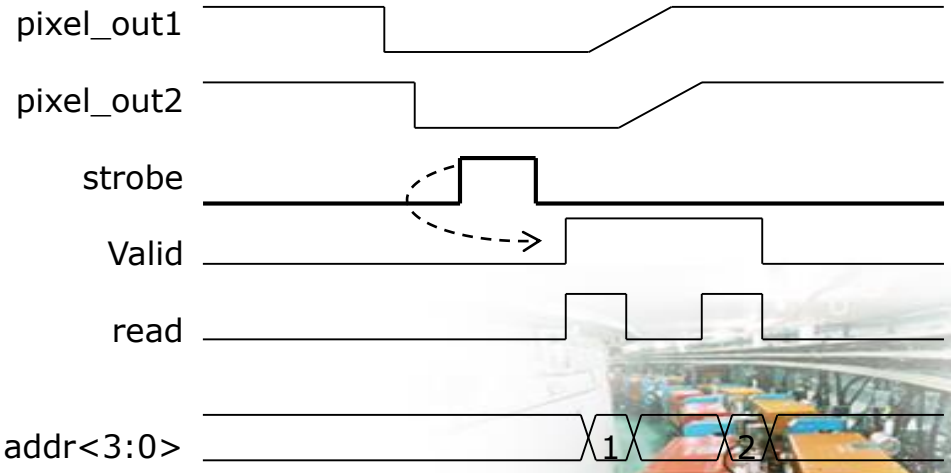
JadePix-4 pixel layout
(MET4 and above not shown)
1. Diode
2. Analog frontend
3. Digital logic
4. AERD shared by 2 col.

Readout modes

- Triggerless mode
  - Global gate signal, **strobe==1**
  - All hits registered at their leading edge
  - 0.2 hits/μs per double col. with the Estimated hit density of inner most layer
  - Occupancy 0.02% @ integration time = 1 μs
- Trigger mode
  - Global gate **controlled by trigger signal**
  - Hits registered only when overlapped with a trigger
  - Capable to handle very high hit density with a dead time for readout, 50 ns/hit







Summary

- JadePix-4/MIC5 is a complementary design to the JadePix-3
  - To complete the R&D for the double-sided concept

	JadePix-3	JadePix-4/MIC5
Pixel size	16 μm × 23.1 μm	20 μm × 29 μm
Integration time	98.3 μs	~ 1 μs
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	356 row × 498 col.
Mask area	10.4 mm × 6.1 mm	14.8 mm × 8.6 mm

- Submitted to a shared engineering run last week.

Design team

- IHEP: Yang Zhou, Ying Zhang, Yunpeng Lu, Qun Ouyang (Project leader)
- CCNU: Ping Yang, Le Xiao, Chaosong Gao, Di Guo, Xiangming Sun
- Dalian Minzu University: Zhan Shi

Thanks for your time!