Status update on JadePix development

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On behalf of the JadePix team

2021/12/22

- Overview of pixel development
- Highlights of JadePix-3
- Design of JadePix-4
- Summary

Physics process and performance requirement

- Efficient tagging of heavy quarks (b/c) and τ leptons

→ impact parameter resolution $\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}(\mu m)$

- Performance requirement
  - High resolution → small pixel pitch
  - Low material → Thinning, low power
  - Close to the IP → Fast readout, radiation hard

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV})\times\sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

physics process and performance req. on CEPC

Physics driven requirements		Running constraints		Sensor specifications
$\sigma_{s.p.}$	2.8 μm			→ Small pixel ~16 μm
Material budget	0.15% X_0 / layer			→ Thinning ~50 μm
		→ Air cooling	→	Low power <50 mW / cm^2
r of Inner most layer	16 mm	→ beam-related background	→	Fast readout 1 ~ 100 μs
		→ radiation damage	→	Radiation tolerance

3.4 Mrad / year

6.2×10^{12} n_{eq} / (cm^2 year)

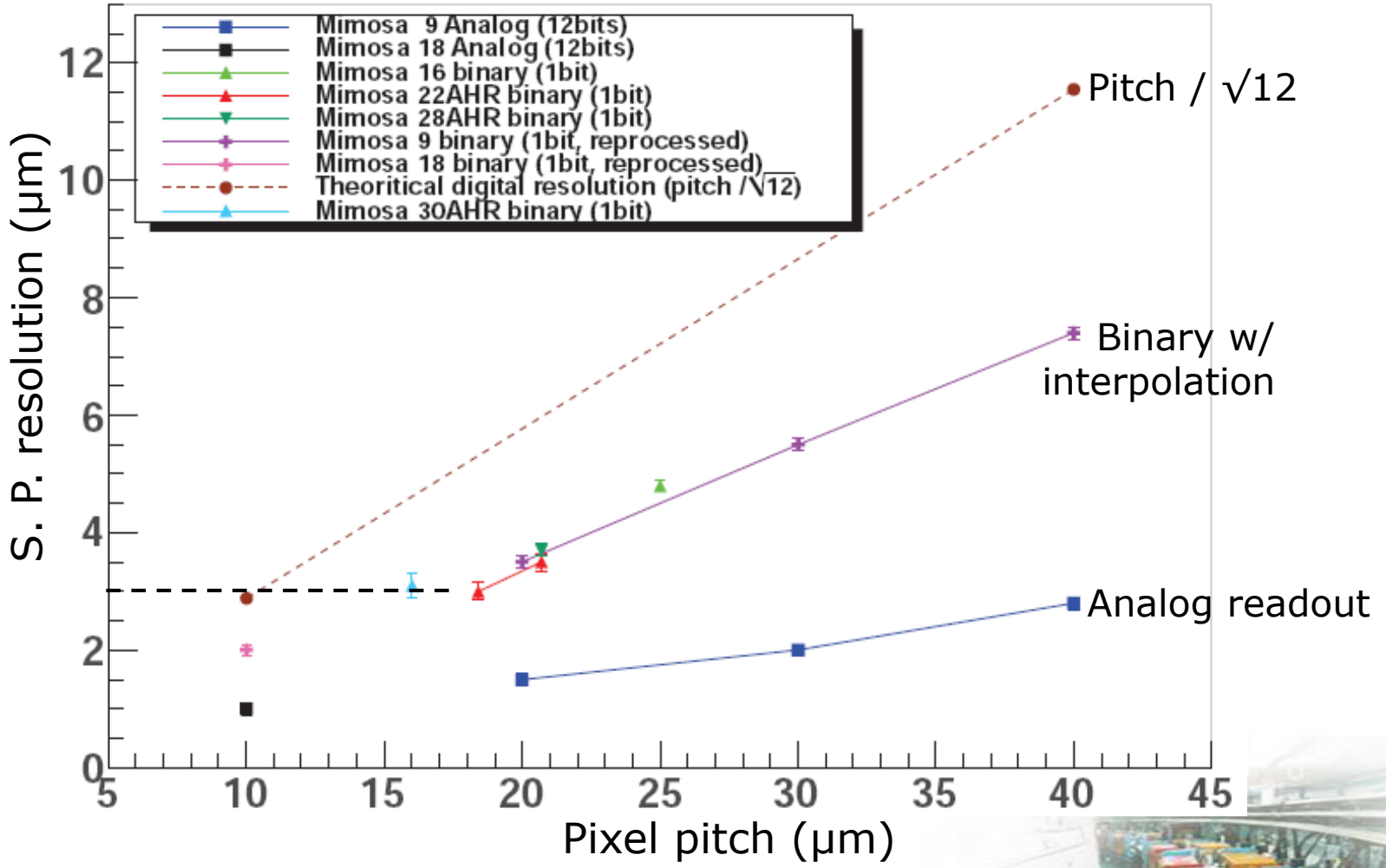
Single point resolution

- Pixel pitch dominant, with interpolation on the hit cluster
  - Binary w/ interpolation:

Pitch **16~18 µm** required

  - Analog readout:

Best resolution with a cost on power & readout speed



Investigated by the Mimosa series (IPHC, France)

Power and readout speed

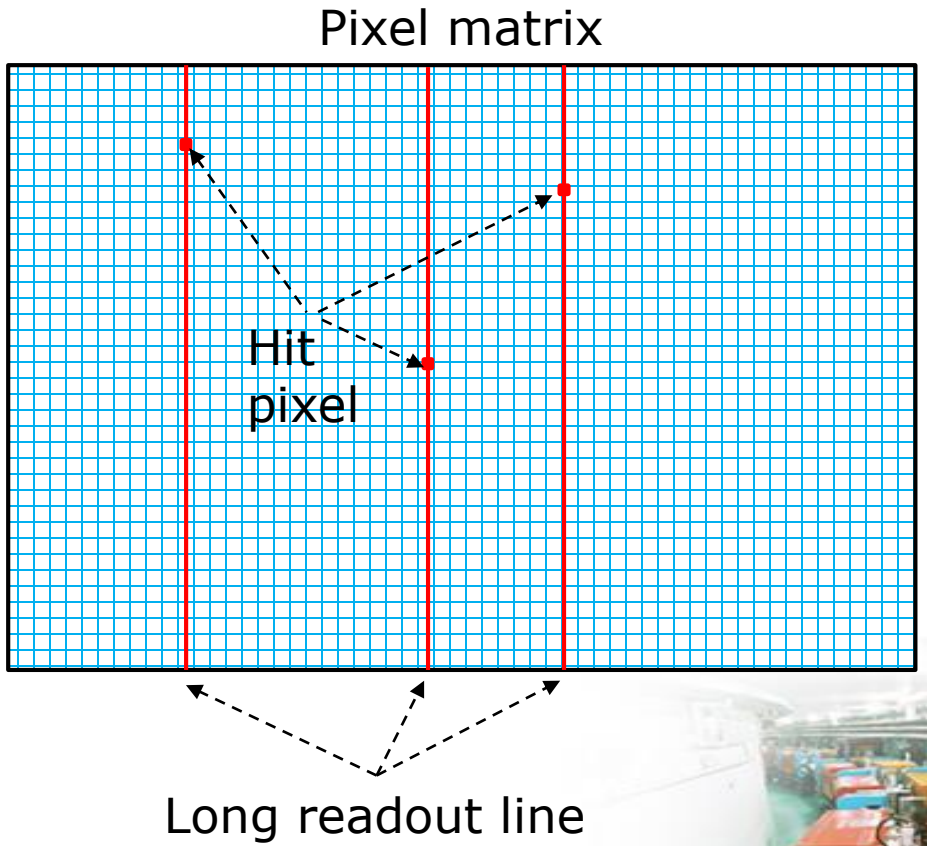
- Readout architecture dominated
  - Low power FE w/ **in-pixel discr.**, O(10) nA/pixel
  - Hit-driven **logic in the active matrix** to extract hit position

} Contradictory to small pixel pitch

fast enough

- Long readout line is a **heavy capacitive load**, 2 pf/cm
  - Analog buffer is slow and needs large current
  - Digital buffer preferred but complex FE of large layout footprint

- Charge Coupled Device ~ O(1 s)
- CMOS imaging sensor ~ O(1 ms)
- CEPC vertex detector ~ O(1 μs)
  - to keep the **hit occupancy** << 1%



How to meet the CEPC requirement

- Within the constraints of present sensor technology
  - Implementing the full specs **in a single design** seems impossible
- Either <u>to split the specs</u> or <u>to develop new technology</u> are necessary

Monolithic pixel sensors for running experiments

	STAR / Mimosa-28	BELLE2 / DEPFET	ALICE / ALPIDE
S. P. resolution < 3 μm	**X**	**X**	**X**
Thinning ~ 50 μm	√	√	√
Low power ~ 50 mW/cm^2	X	X	√
Fast readout ~ 1 μs	X	X	√
Rad. hard ~ 3.4 Mrad/ year ~6.2×10^{12}n$_{eq}$/ (cm^2 year)	X	√	X

CDR study

- Sensor options and critical R&D
  - SOI → 3D-SOI
  - 180 nm CMOS → 65/55 nm CMOS

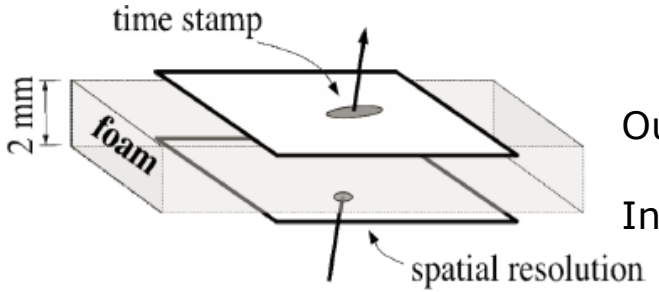
} Aiming at smaller pitch w/o compromise on low power or fast readout

International review report on the Vertex detector (CDR)

Vertex Detector

Findings: there is active R&D and groups are making good progress, building on large effort by the international community. Compared to other efforts toward precise and transparent vertex detectors, CEPC (with its 100% duty cycle) should place stronger emphasis on power management. Advanced processes like 65 nm CMOS or 3D-integrated devices should be pursued actively and can have a big impact on the vertex detector performance.

- Double-sided structure: fast time stamp and spatial resolution separated for **layer 1**



Outside

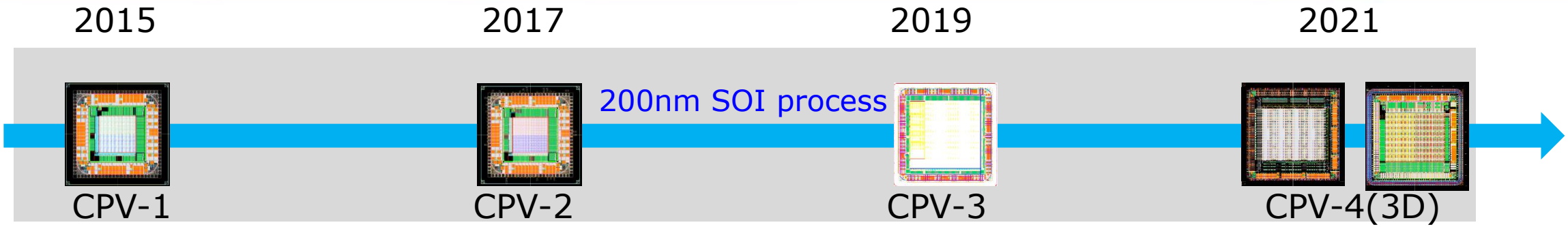
Inner side

Concept of double-sided structure

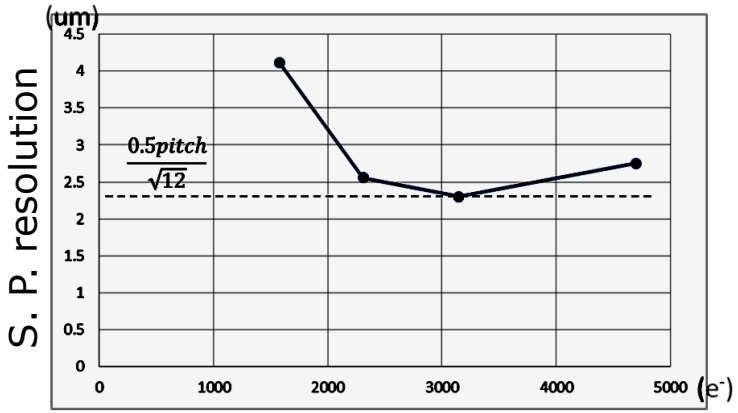
Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	0.15%/X_0
	18	62.5	6	0.15%/X_0
Layer 2	37	125.0	4	0.15%/X_0
	39	125.0	4	0.15%/X_0
Layer 3	58	125.0	4	0.15%/X_0
	60	125.0	4	0.15%/X_0

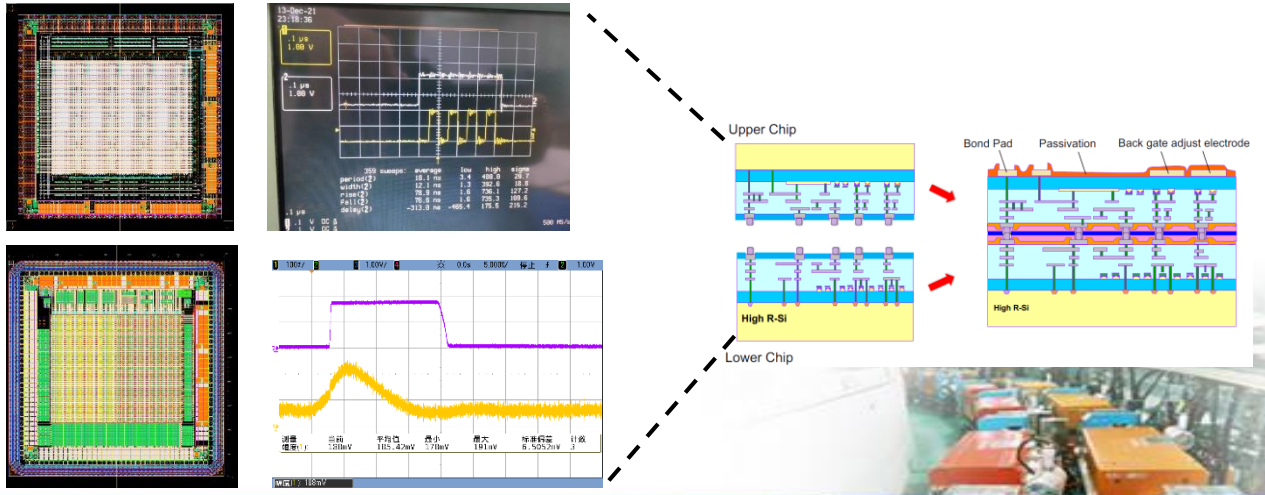
Development of SOI and 3D-SOI



- CPV-1/2/3 dedicated to the study of diode structure and in-pixel discr.
  - Principle verification of $\sigma_{s.p.}$ < 3 μm @ pitch = 16 μm
  - Thinned down to 75 μm successfully
- CPV-4 is a prototype on 3D integration
  - Upper tier: Digital circuit
  - Lower tier: Sensing diode + Analog circuit



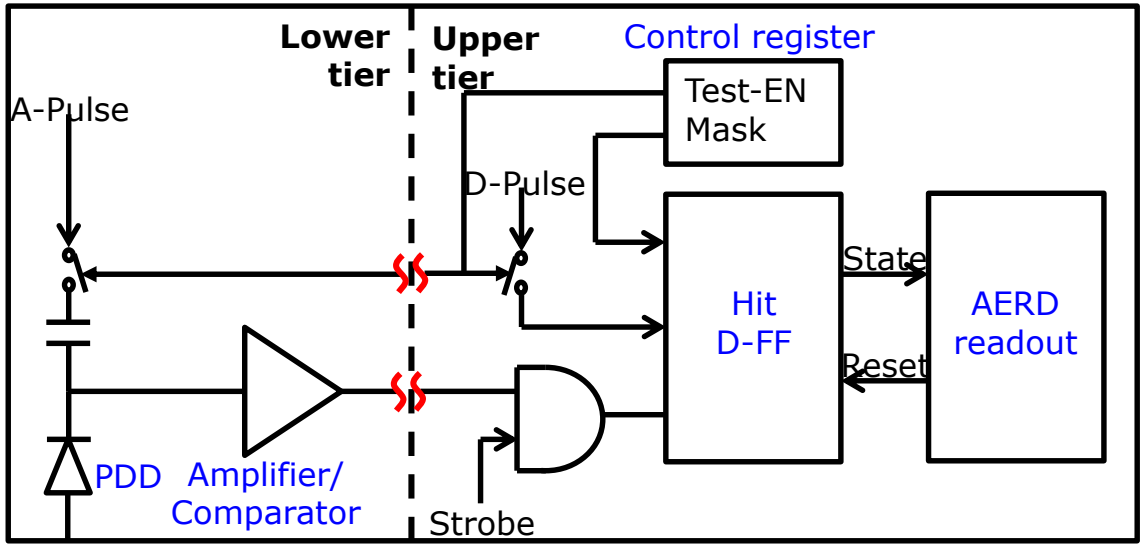
Signal charge of laser beam



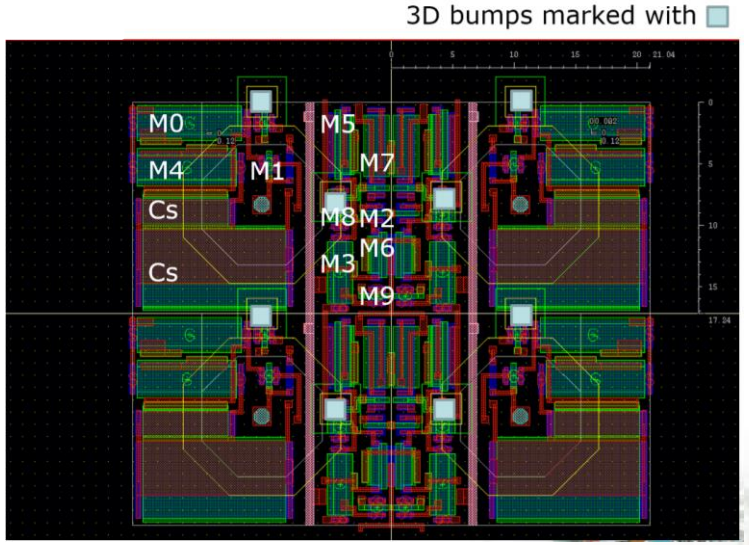
Benefits of 3D-SOI

- Low power FE w/ in-pixel discr., 20nA/pixel
- Hit-driven readout logic w/ time stamp, ~1 μs
- Small pixel layout, 17 × 21 μm²

Unique design enabled by 3D integration



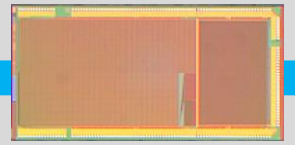
Division of functional blocks for lower & upper tiers

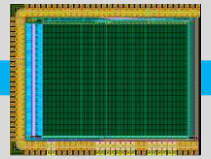
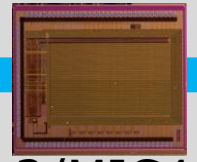


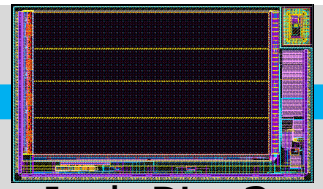
Layout of 2 × 2 pixel array

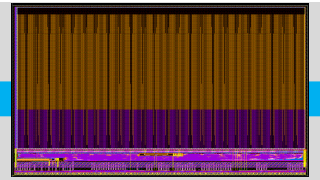
Development of CMOS pixel sensor

2015 2017 2019 2020 2021


JadePix-1

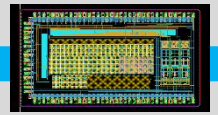


JadePix-2/MIC4


JadePix-3

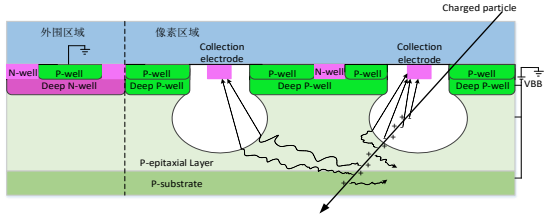

JadePix-4/MIC5

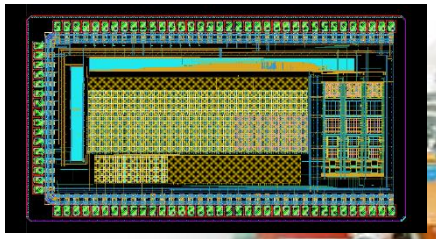
180 nm CIS process

55 nm CIS process

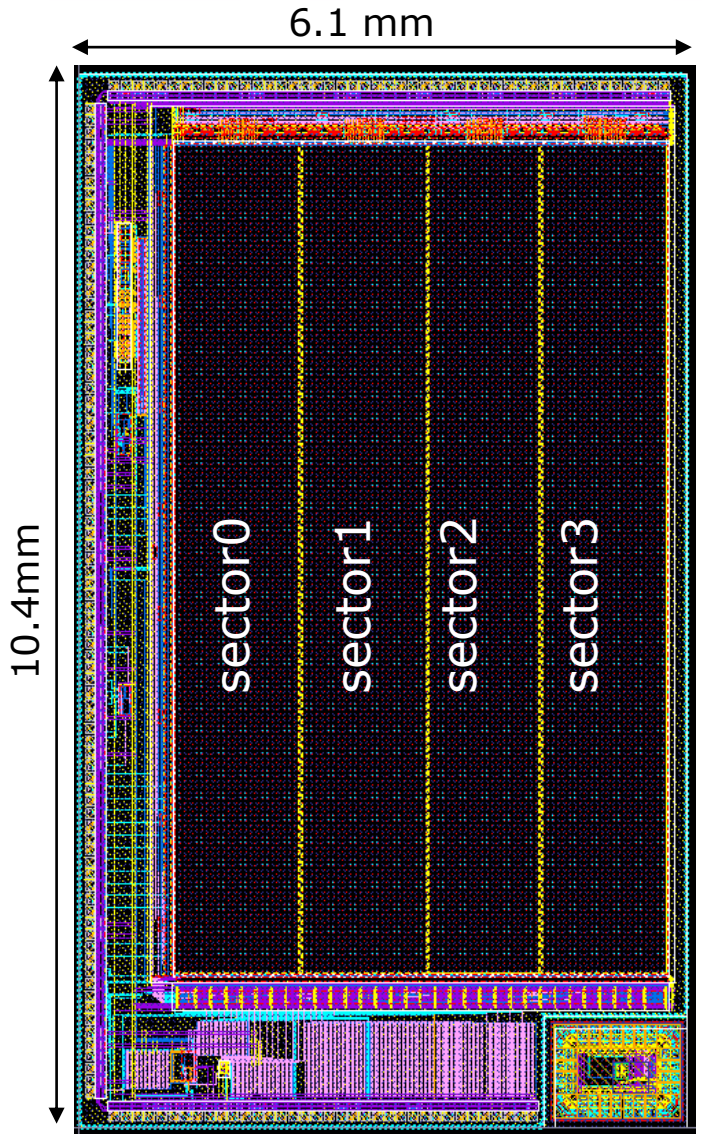

Process test chip

- 180 nm CIS process (driven by the ALICE/ITS2)
  - JadePix-3/4 are designed in line with the concept of **double-sided structure**
  - High resolution and fast readout respectively
- 55 nm CIS process (synergy with NICA development)
  - Targeted on radiation hard and small pixel technology
  - First test chip submitted in June





Pixel array in JadePix-3

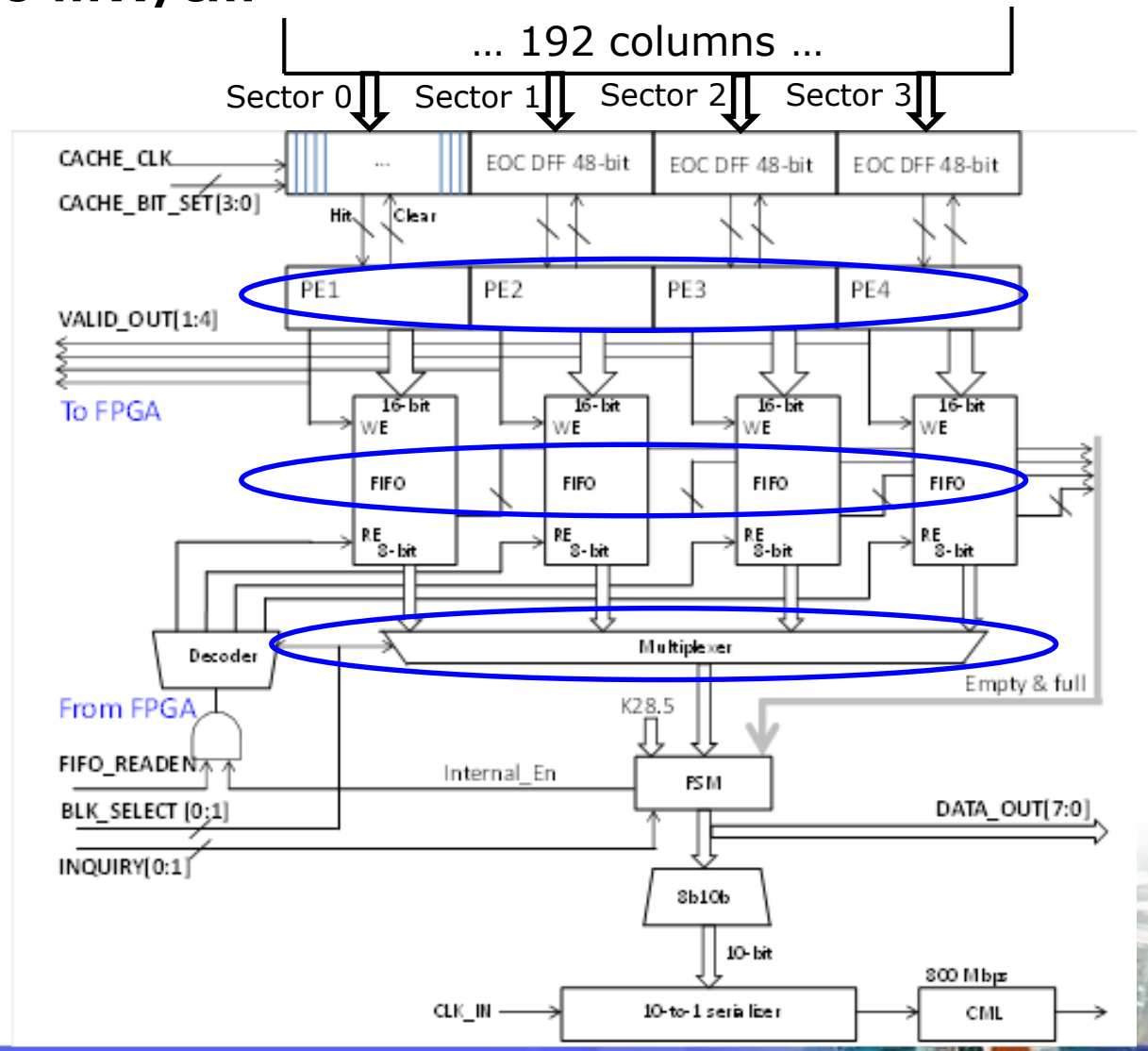


- **Full-sized** in the φ direction
  - Matrix coverage: 16 µm × 512 rows = 8.2 mm
- **Rolling shutter** to avoid heavy logic and routing in the matrix
  - Minimum pixel size: **16 µm × 23.11 µm**
  - Matrix readout time: 512 rows × 192ns/row = **98.3 µs/frame**
- 4 parallel sectors, **scalable**
  - 48 columns/sectors × 4 = 192 columns

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 µm	FE_V0	DGT_V0	16×26 µm²
1	2 + 2 µm	FE_V0	DGT_V1	16× 26 µm²
2	**2 + 2 µm**	**FE_V0**	**DGT_V2**	**16× 23.11 µm²**
3	2 + 2 µm	FE_V1	DGT_V0	16×26 µm²

Lower power design of JadePix-3

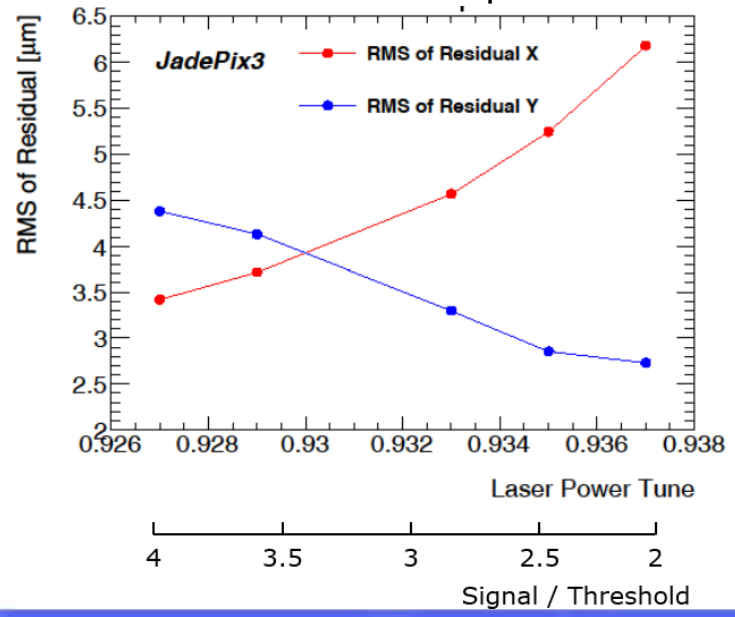
- A low power frontend of 20 nA, equivalent to **9 mW/cm²**
  - Except for the sector 3, where 60 nA used for the comparison of radiation tolerance
- Zero suppression at the bottom of matrix
  - HIT address extracted by Priority Encoder (PE)
  - **Compress the bit flow** dramatically
- Flexible FIFO control scheme allowed to
  - Study the **optimal size of FIFO**



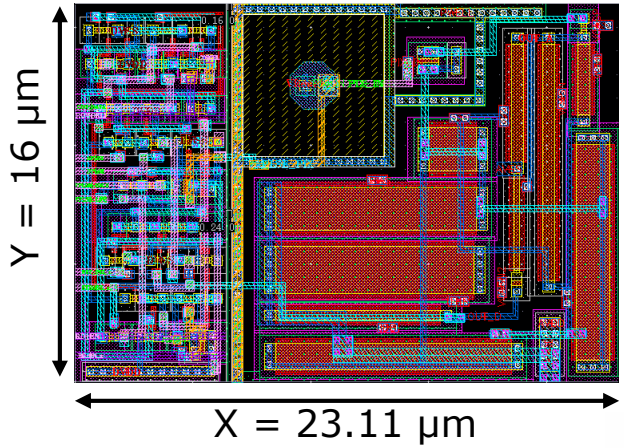
1-D Spatial Resolution of JadePix-3

- Measured with micro-focused laser beam (1064 nm)
  - Laser power carefully tuned for 2 ≤ signal / thr. ≤ 4
  - Threshold set to 220 e-
- 1-D spatial resolution on X and Y
  - **Minimum 3.4 µm and 2.7 µm** respectively

RMS of residual vs Laser power tune

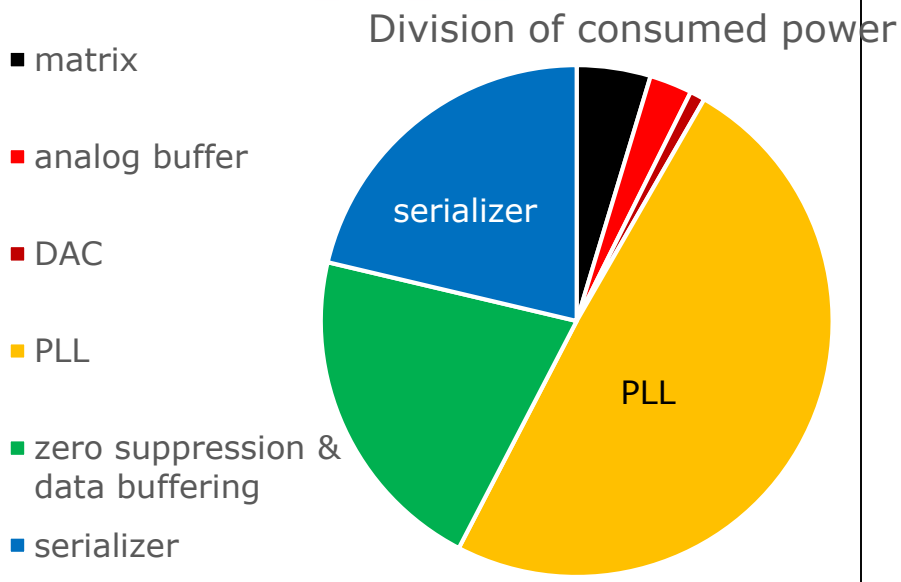


Layout of pixel undertest



Power consumption of JadePix-3

- Average power consumption **46.9 mW/cm²**
  - PLL and Serializer not included (parallel data link)
- Extrapolated to a full size chip of 1 cm × 2.56 cm
  - Average power **91.44 mW/cm²**
  - PLL and Serializer included (serial data link)
- Need to optimize further on
  - PLL
  - Serializer
  - Data buffering
  - Test function

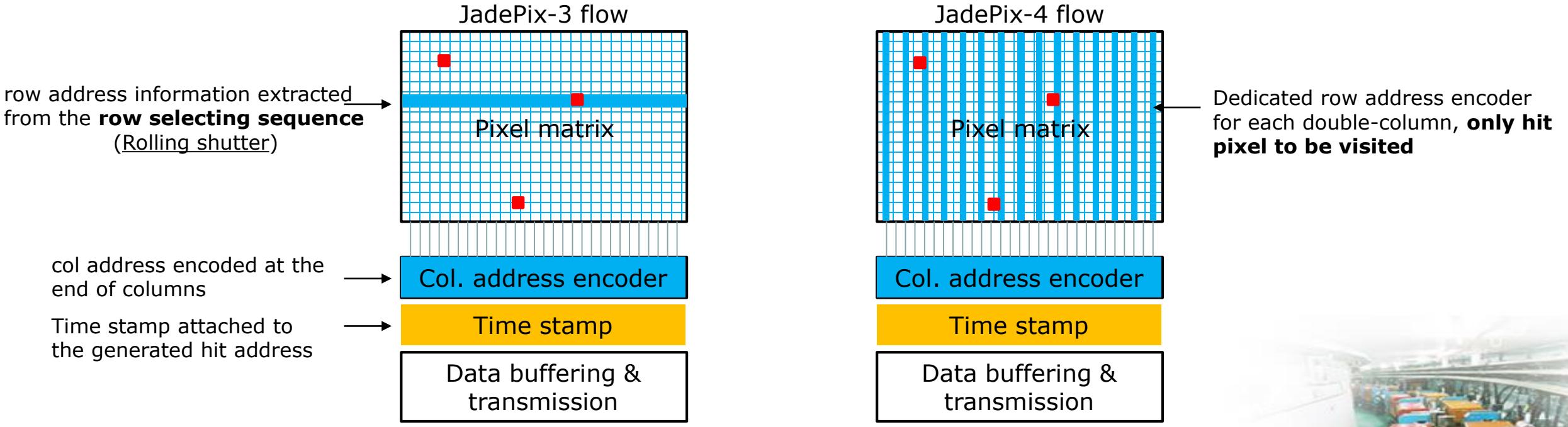


Extrapolation of average power consumption

	512 × 192 (JadePix-3)	512 × 1024 (Full-sized chip)
Matrix	3.15 mA	16.79 mA
Zero suppression and data buffering	12.47 mA	66.47 mA
Other modules	46.82 mA	46.82 mA
Sum	62.44 mA	130.08 mA

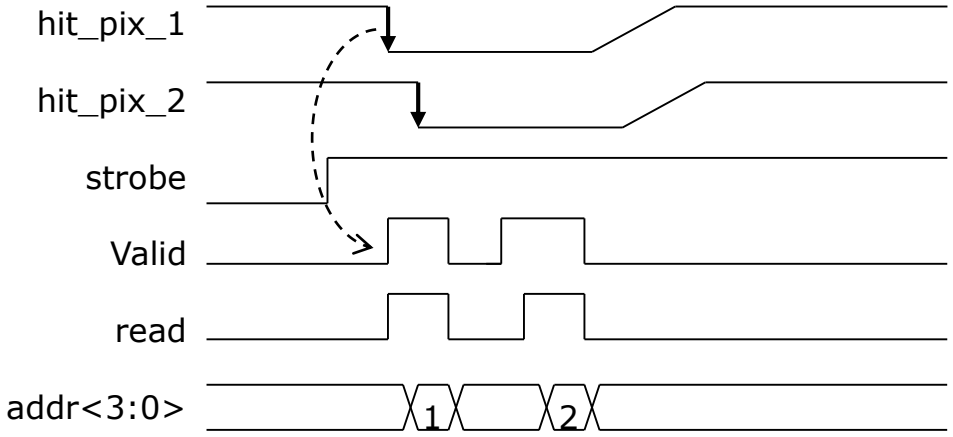
Hit processing flow in JadePix-4

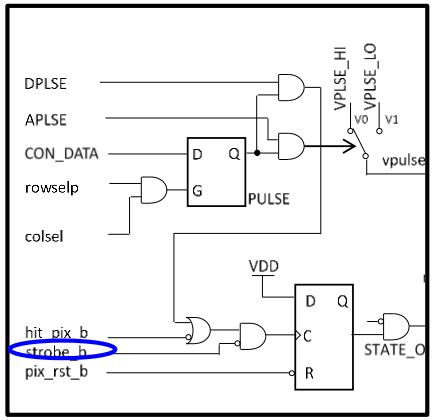
- A major modification: Rolling shutter → Hit-driven readout logic
  - Faster by 2 ~ 3 orders
  - Larger pixel size: 20 μm × 29 μm

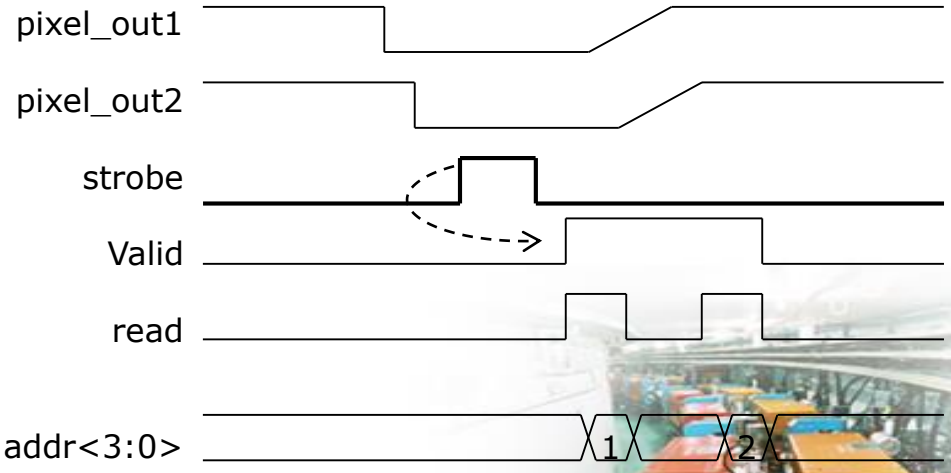


Two readout modes of JadePix4

- Triggerless mode
  - Global gate signal, strobe==1
  - **All hits** registered at their leading edge
  - 0.2 hits/μs per double column estimated
  - Occupancy 0.02%
- Trigger mode
  - Global gate controlled by trigger signal
  - Only **hits coincident** with a trigger
  - Capable to handle very high hit density
  - dead time 50 ns / hit for a double-column





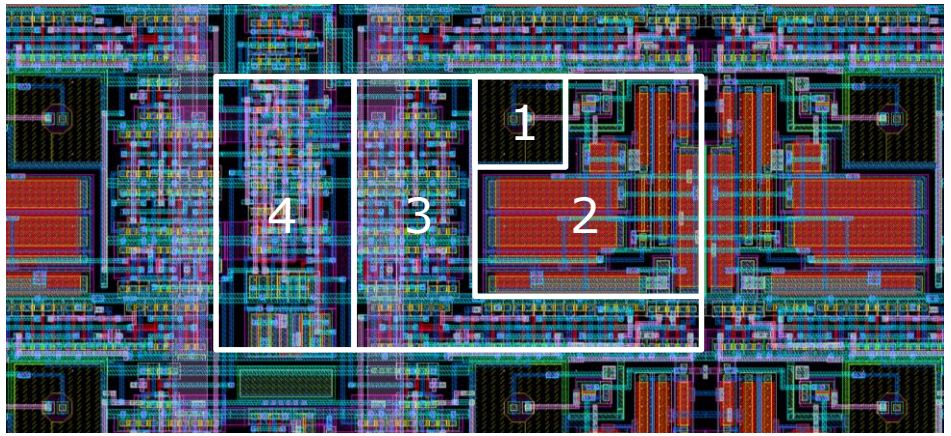


Implementation of JadePix-4

- Key components verified and re-used from JadePix-3
  - Diode
  - Analog frontend
  - Hit register
- Hit-driven readout logic
  - Row address encoder in the matrix
  - Column address encoder outside the matrix
- Final layout of pixel matrix
  - 356 row × 498 col.

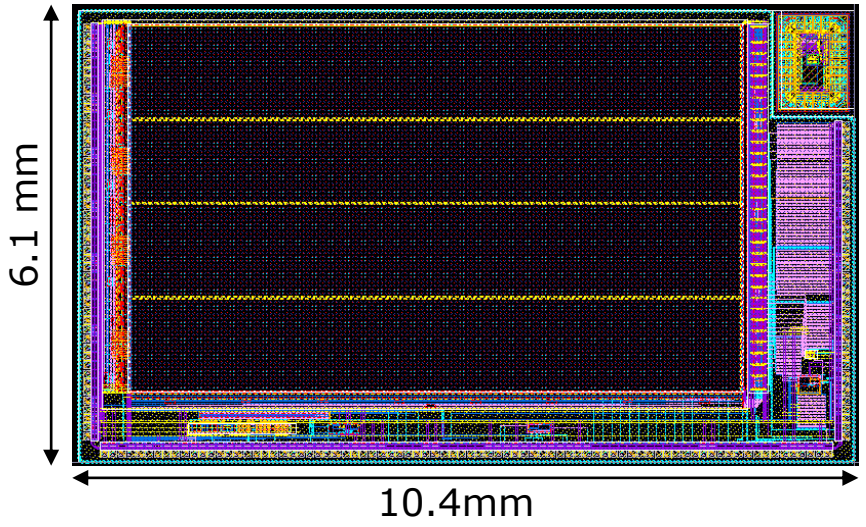
JadePix-4 pixel layout
(MET4 and above not shown)

1. Diode
2. Analog frontend
3. Digital logic
4. Readout logic shared between 2 col.

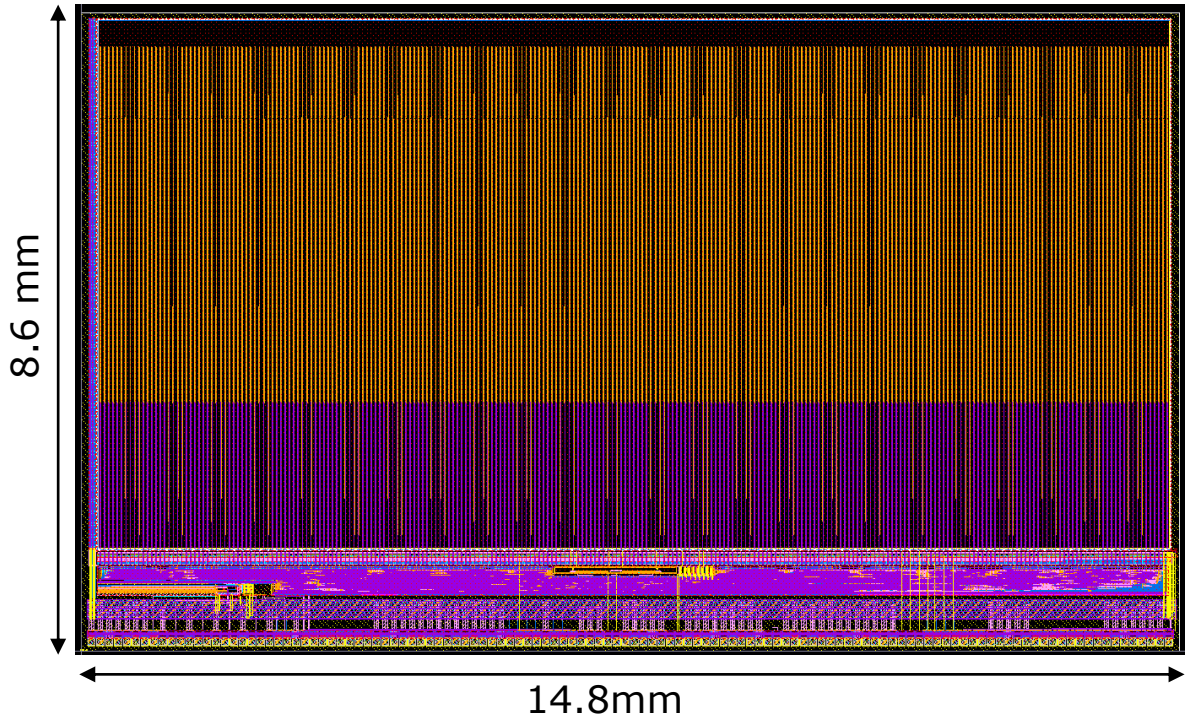


Comparison of JadePix-3 and JadePix-4

JadePix-3 Layout



JadePix-4 Layout



	JadePix-3	JadePix-4
Pixel size	16 μm × 23.1 μm	20 μm × 29 μm
Readout time	98.3 μs	~ 1 μs
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	356 row × 498 col.
Mask area	10.4 mm × 6.1 mm	14.8 mm × 8.6 mm

Summary

- JadePix-4 is complementary to the JadePix-3
  - In line with the concept of double-sided structure in the CDR
  - Separate implementation of fast readout and high resolution on 180 nm CIS process
  - Valuable experience on low power design
- Advanced pixel technologies are gaining momentum
  - 3D-SOI progressed steadily
  - 55 nm CIS process kicked off recently

Design team of JadePix-3/4

- IHEP: Yang Zhou, Ying Zhang, Yunpeng Lu, Qun Ouyang (Project leader)
- CCNU: Ping Yang, Le Xiao, Chaosong Gao, Di Guo, Xiangming Sun
- Dalian Minzu University: Zhan Shi

Thanks for your time!

Backup slides

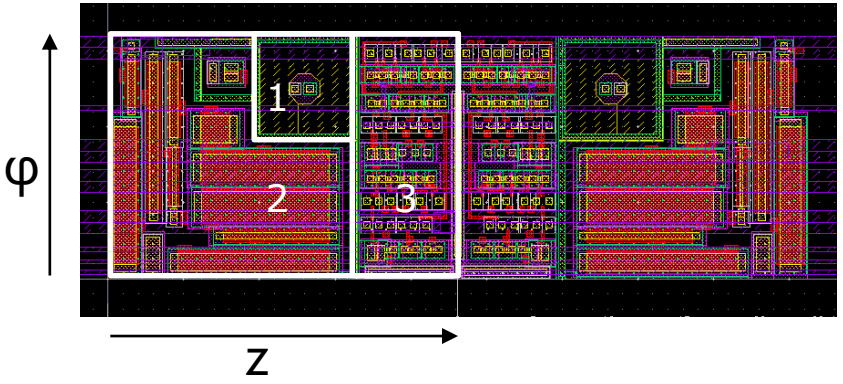
C-tagging performance with different specs

c-tagging performance with different specs

	ε·p ↑ 41%	baseline	ε·p ↓ 22%
	Scenario A (Aggressive)	Scenario B (Baseline)	Scenario C (Conservative)
Material per layer/X_0	0.075	0.15	0.3
Spatial resolution/μm	1.4 - 3	2.8 - 6	5 - 10.7
R_{in}/mm	8	16	23

Zhigang Wu, Manqi Ruan, Qun Ouyang

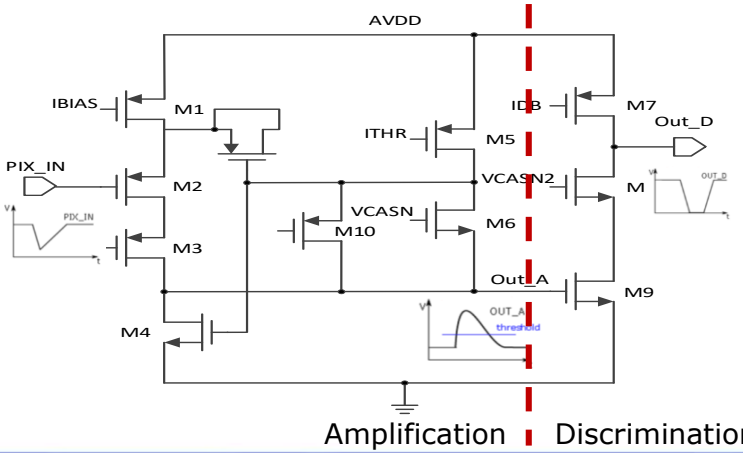
Small pixel implemented in the JadePix-3



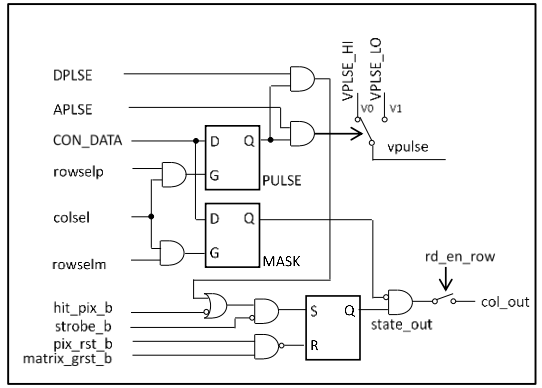
Pixel footprint:
1: Sensing diode
2: Analog frontend
3: digital frontend

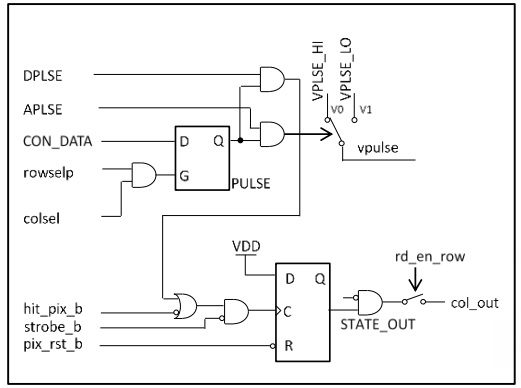
- Fix φ direction to **16 µm** and allow z to vary
  - Sensing diode of minimized geometry verified on JadePix1
  - Analog part with **tradeoff** between layout area and FPN
  - 3 variants of digital part (D-FlipFlop vs RS-latch)
- Mirrored layout to share bias lines between two columns

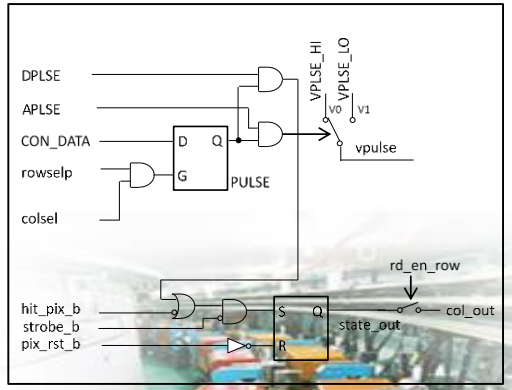
Frontend / analog part



3 variants of digital part

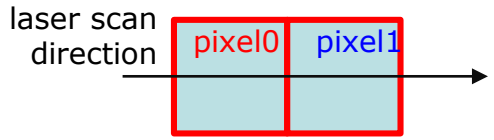




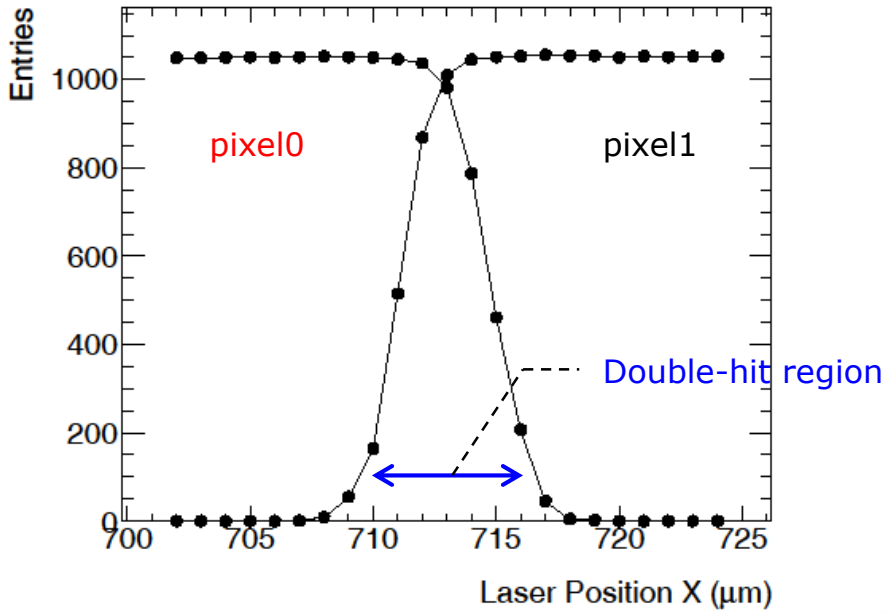


Measurement of position residual

- 1-D scan of laser position
  - Step = 1 μm and repeat 1000 at each step
  - Laser power tune = 93.5% (~520 e^-)
- Distribution of position residual
  - Reference position: motion stage
  - Measured position: weight center of hit pixels
- RMS taken as the 1-D spatial resolution



1-D scan of laser position



Residual distribution