RD53A: a large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors

The 15th Vienna Conference on Instrumentation

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on behalf of the RD53 Collaboration

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RD53 Collaboration and RD53A Chip

- The **RD53 Collaboration** represents a joint effort between ATLAS and CMS communities in order to build large scale pixel readout chips for the Phase II upgrade of ATLAS and CMS
  - 24 Institutions from Europe and US
  - http://rd53.web.cern.ch/rd53/

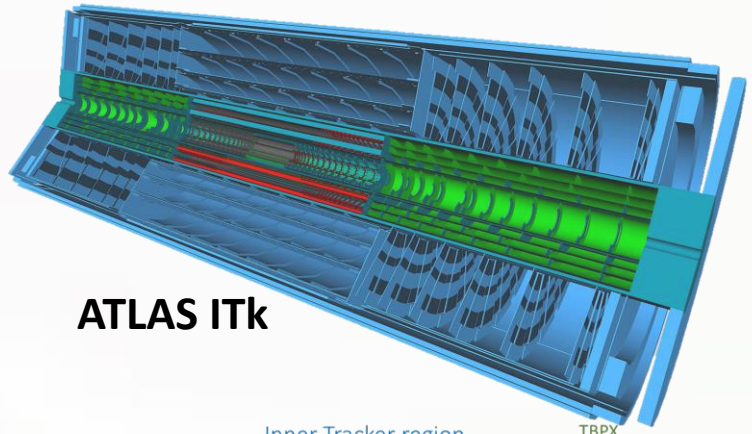


HL-LHC Challenges

- 200 interactions per bc
- Detector lifetime: 4000 fb^{-1}
- Increased trigger rate and latency
- High granularity, Less material

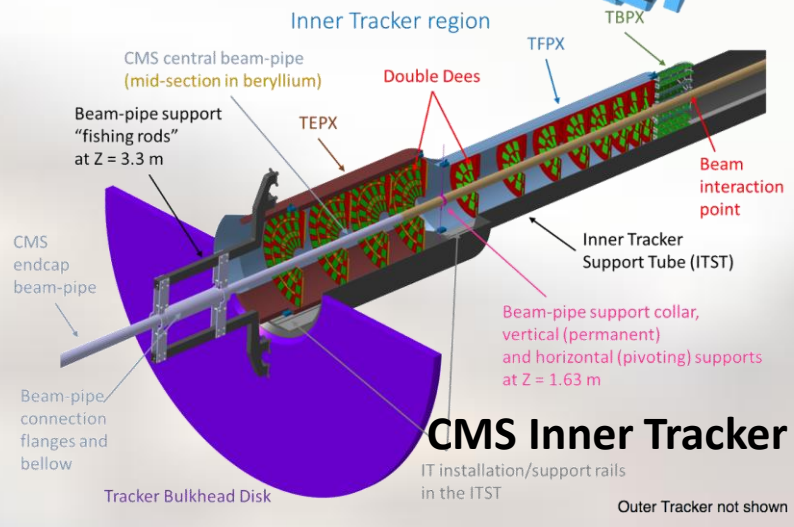
RD53 Requirements

- High hit rates: 3 GHz/cm^2
- 500 Mrad tolerance
- High trigger rate: 1MHz
- Low threshold: 600 e
- 50 x 50 μm^2, Low power



ATLAS ITk

- **RD53A – first prototype**
  - 65 nm technology (high density logic and low power)
  - 20mm x 11.5mm (half size of the production chip)
  - 400 x 192 pixels (50x50 µm pixel)
  - Submission Aug 31 2017, First chip tested Dec 6 2017, First bump-bonded chip test Apr 13 2018
  - RD53A Manual: https://cds.cern.ch/record/2287593/

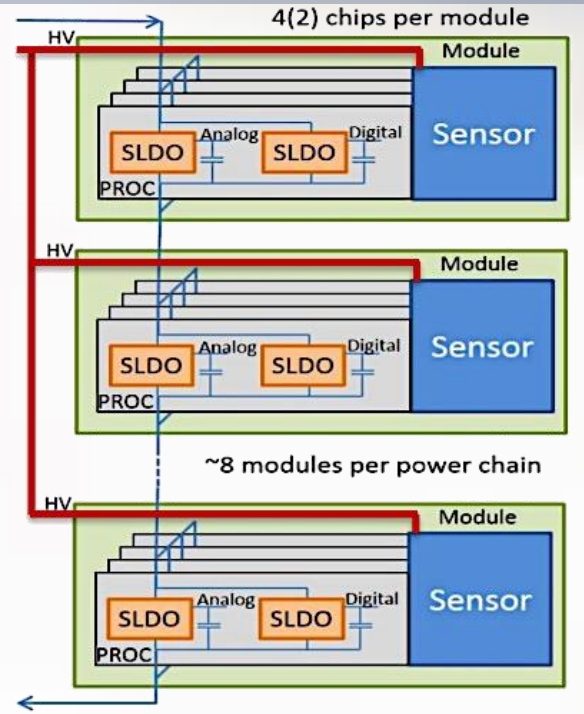


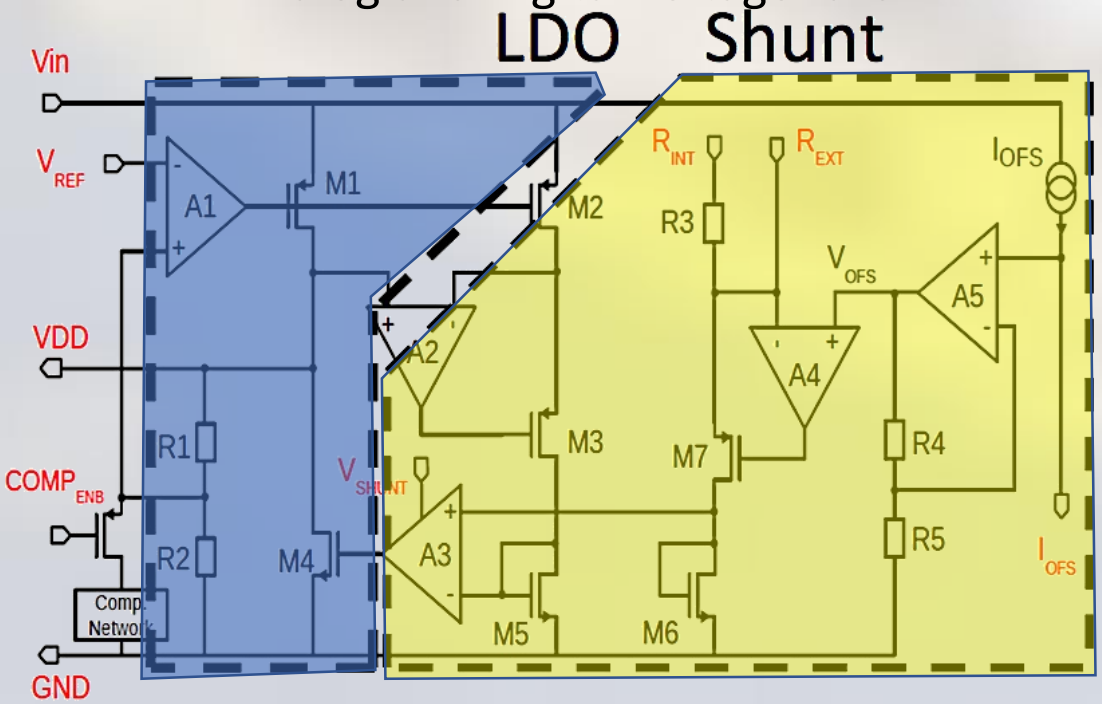
CMS Inner Tracker

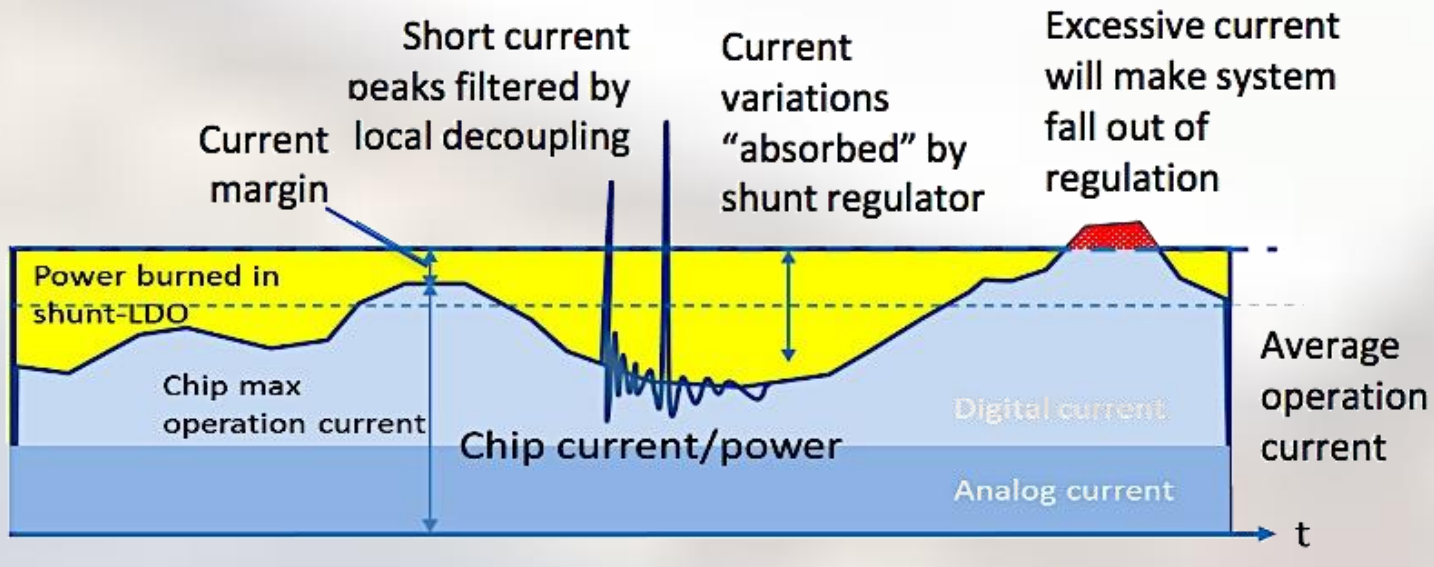
RD53A: Powering

8A (4A), 12V

- **Baseline for powering the ATLAS and CMS HL-LHC pixel detectors: serial powering**
  - Low mass, Not sensitive to voltage drop, Low noise
  - Up to 4 chips in parallel resolve single chip failures
- **RD53A Shunt-LDO regulator**
  - Low-drop linear voltage and a shunt regulator
  - Three operational modes (direct, LDO and ShuntLDO)
  - Analog and Digital voltage rails

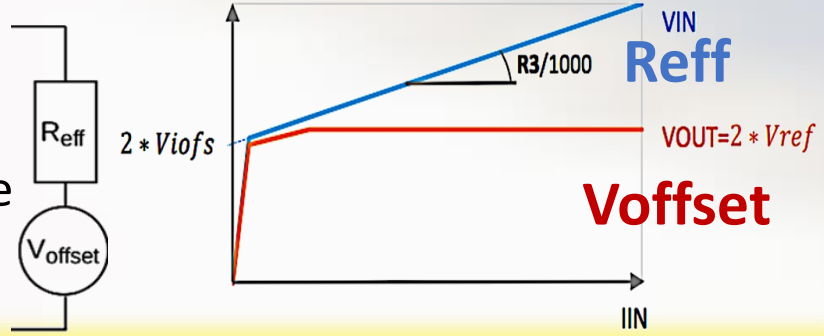


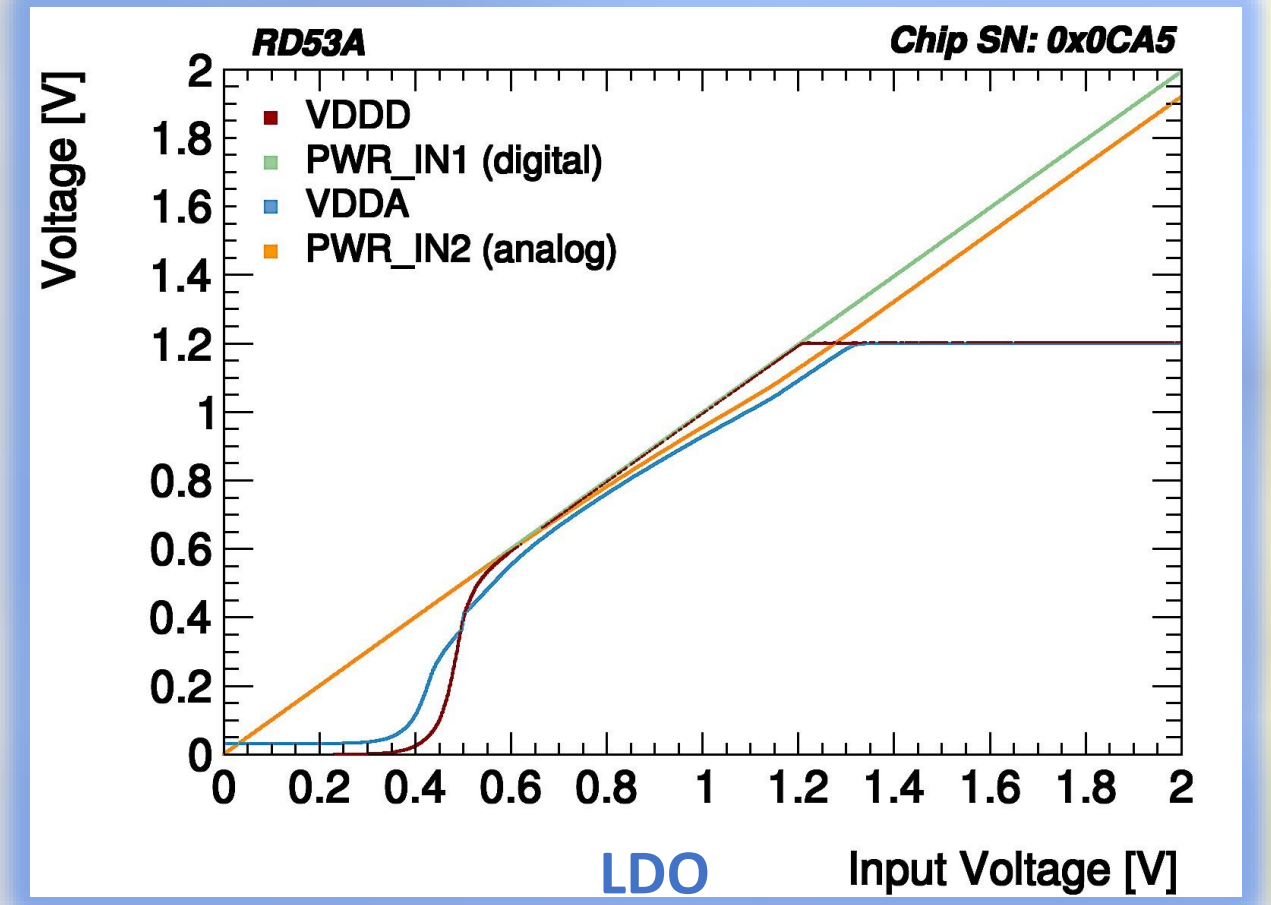


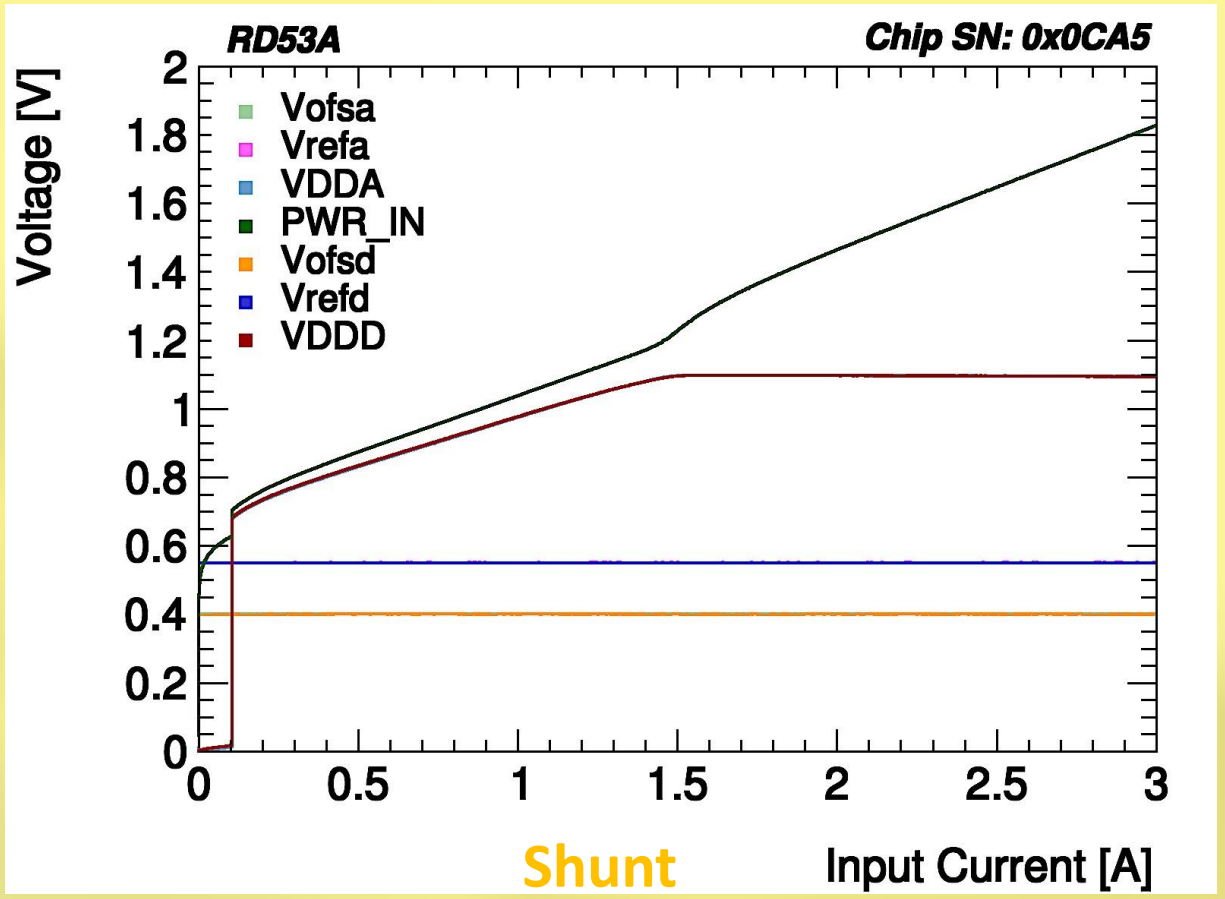


RD53A: Powering

- **Line regulation of the ShuLDO**
  - Shunt-LDO makes power load look like resistor with voltage offset.
  - Power consumption variations inside chip not “visible” from outside
  - Configurable offset voltage and effective resistance.

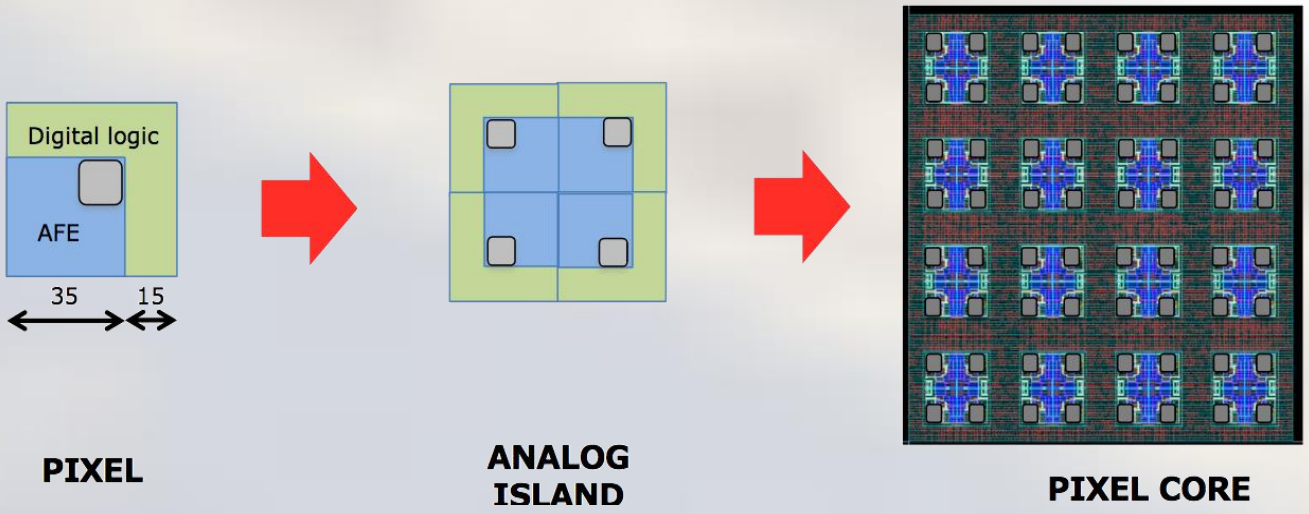


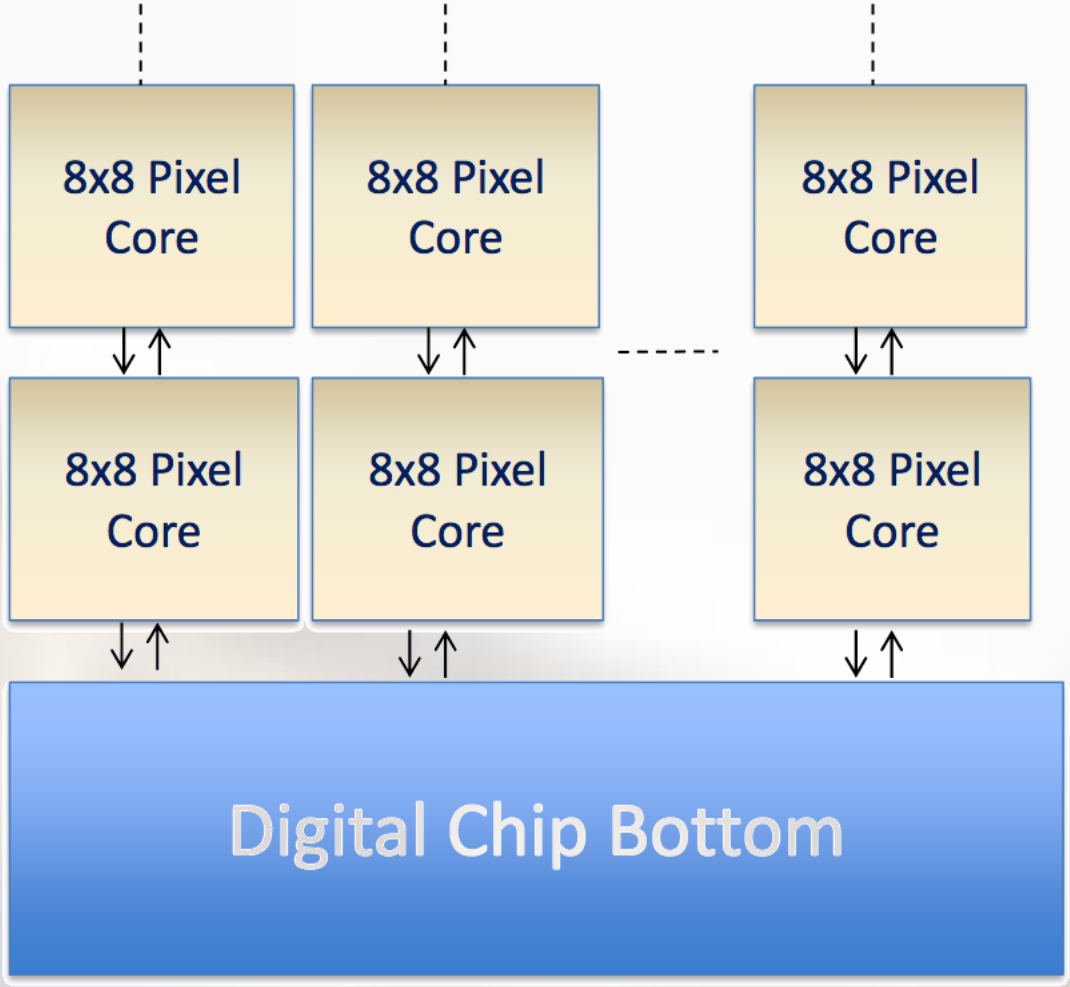




RD53A Pixel Floorplan

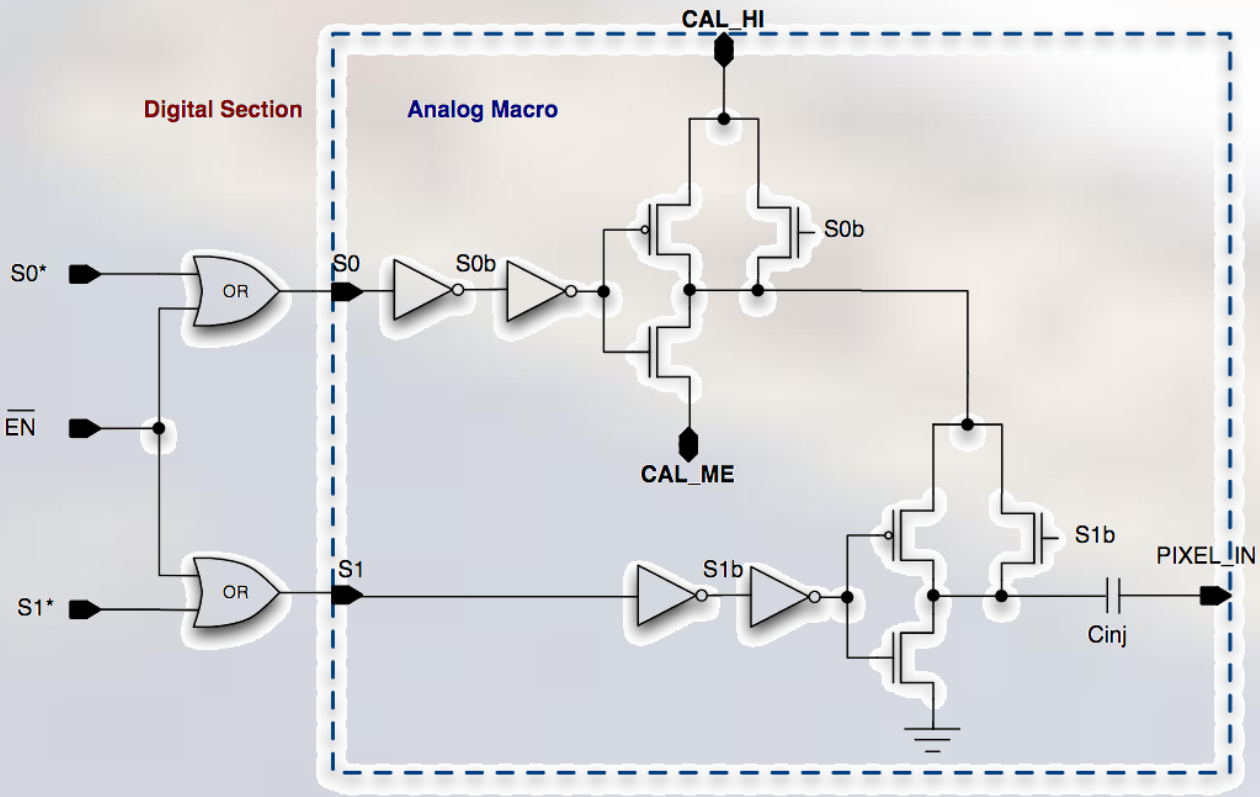
- Pixel matrix build from 8 x 8 pixel cores
- One Pixel Core contains multiple Pixel Regions with shared logic and trigger latency buffering
- FEs are placed as analog islands in the "digital sea" of synthesized core logic
- All cores are identical

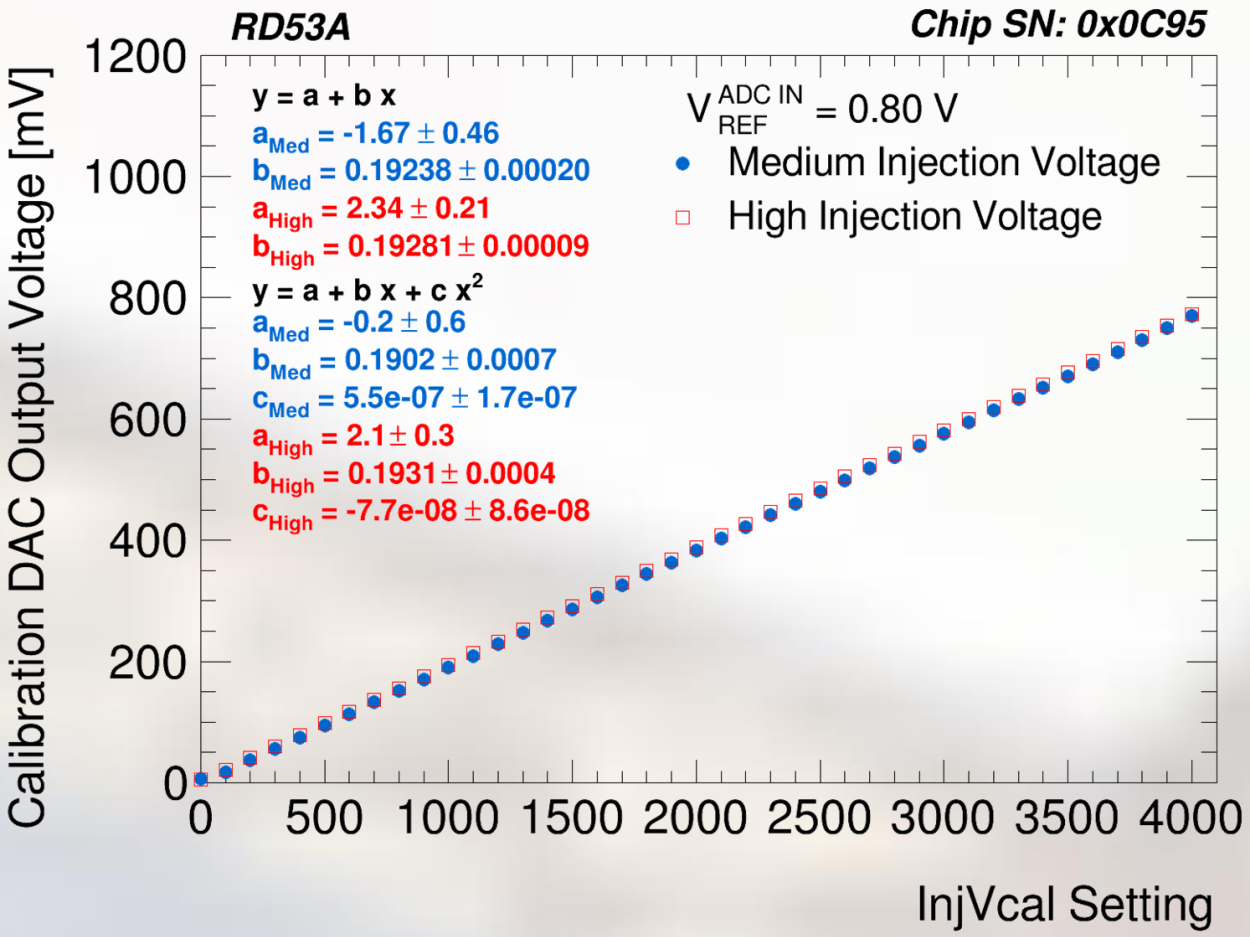




RD53A Calibration Circuit

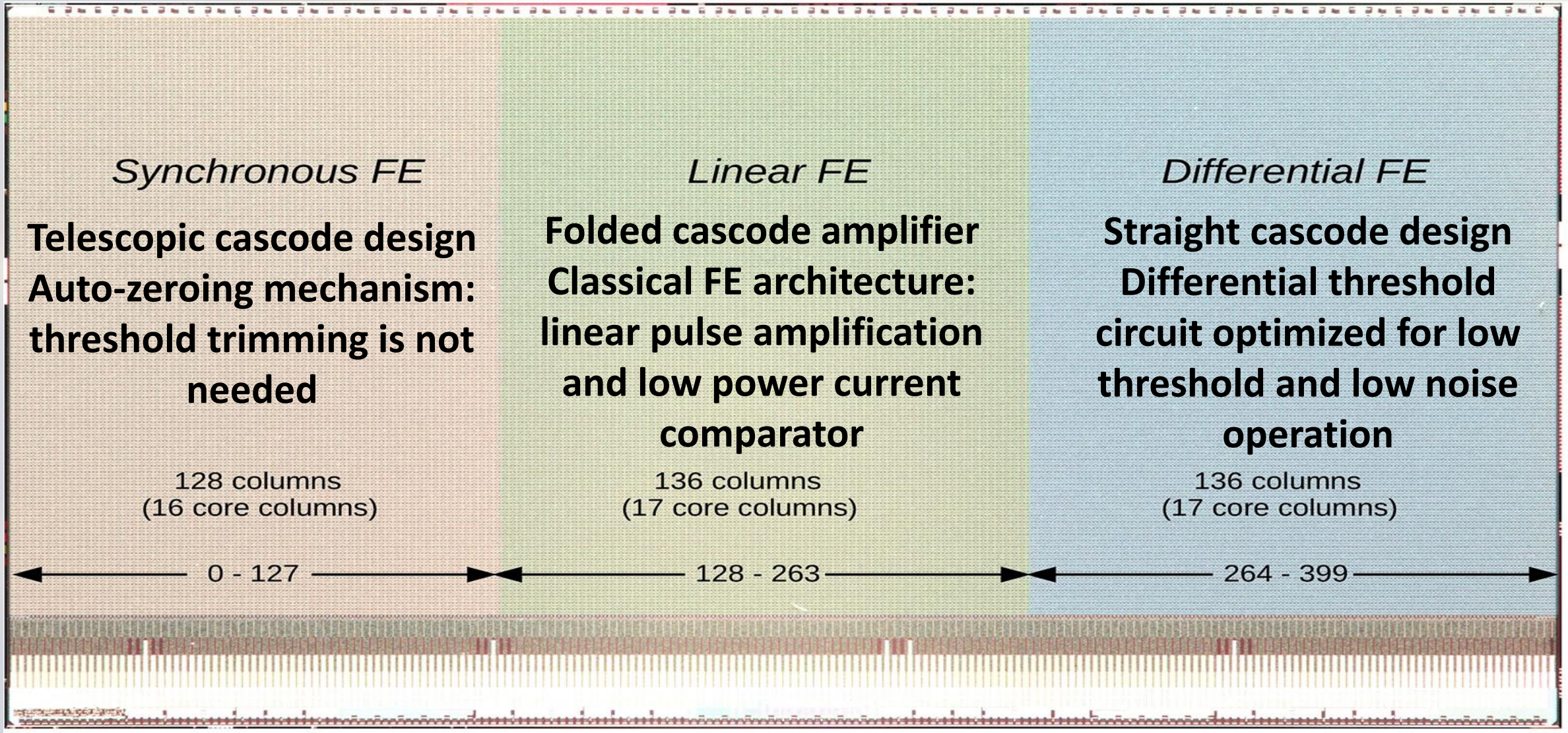
- High and medium injection voltage are generated by 12-bit voltage DAC
- The **linearity** of the calibration injection voltages is confirmed!
- Measured value: 0.196 mV/DAC
  for measured injection capacitance of 8.21 fF (10 e/DAC)
- Simulated value: 12 e/DAC





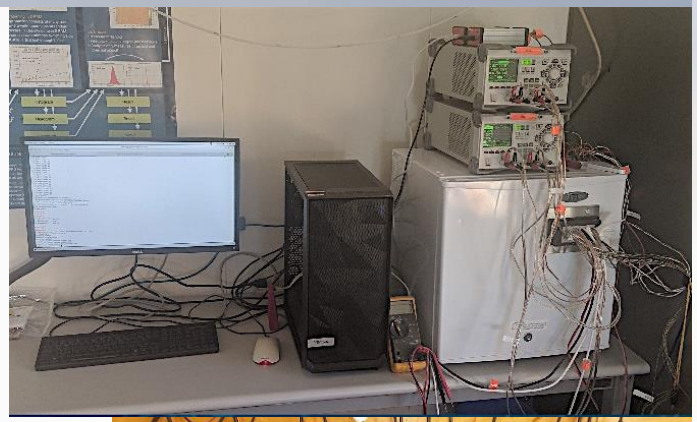
Analog Front-End (FE) Description

- Three different analog FE designs for performance comparisons with same layout area
- Common calibration injection circuit



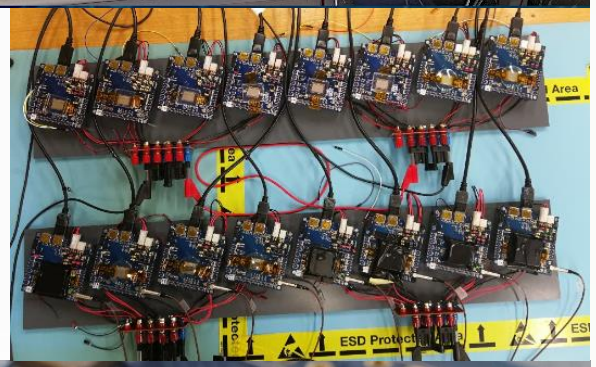
RD53A Testing and Characterization

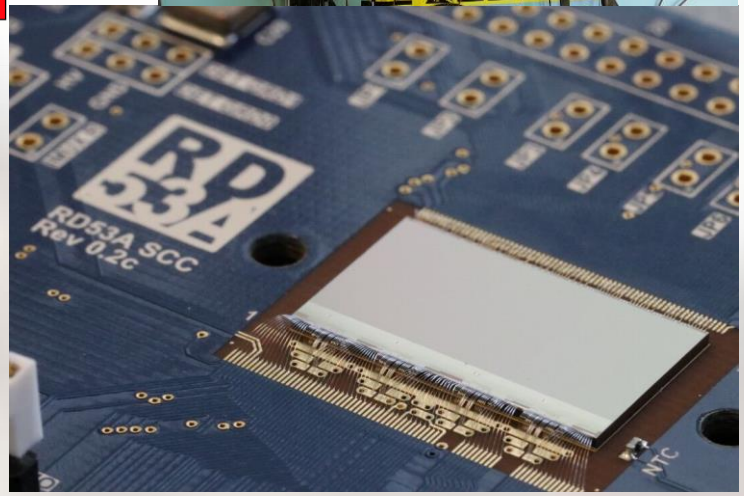
- **Two test systems:**
  - **BDAQ53** (Bonn University) https://gitlab.cern.ch/silab/bdaq53
  - **YARR** (LBNL) https://github.com/Yarr/Yarr



- **RD53A Characterization**
  - Automated wafer probing
  - Radiation campaigns
  - Bump bonding with sensors
  - Studies with radioactive sources and with test beams
  - Serial powering tests
  - All tested chips were loaded on the RD53A single chip card
  - More than **250** chips tested and distributed between institutes
  - About **30** chips irradiated
  - About **150** chips bump bonded to different types of sensors (planar, 3D, 50x50 μm^2 and 25x100 μm^2)
  - All test results shown are in LDO mode, performance in Shunt mode has found to be the same

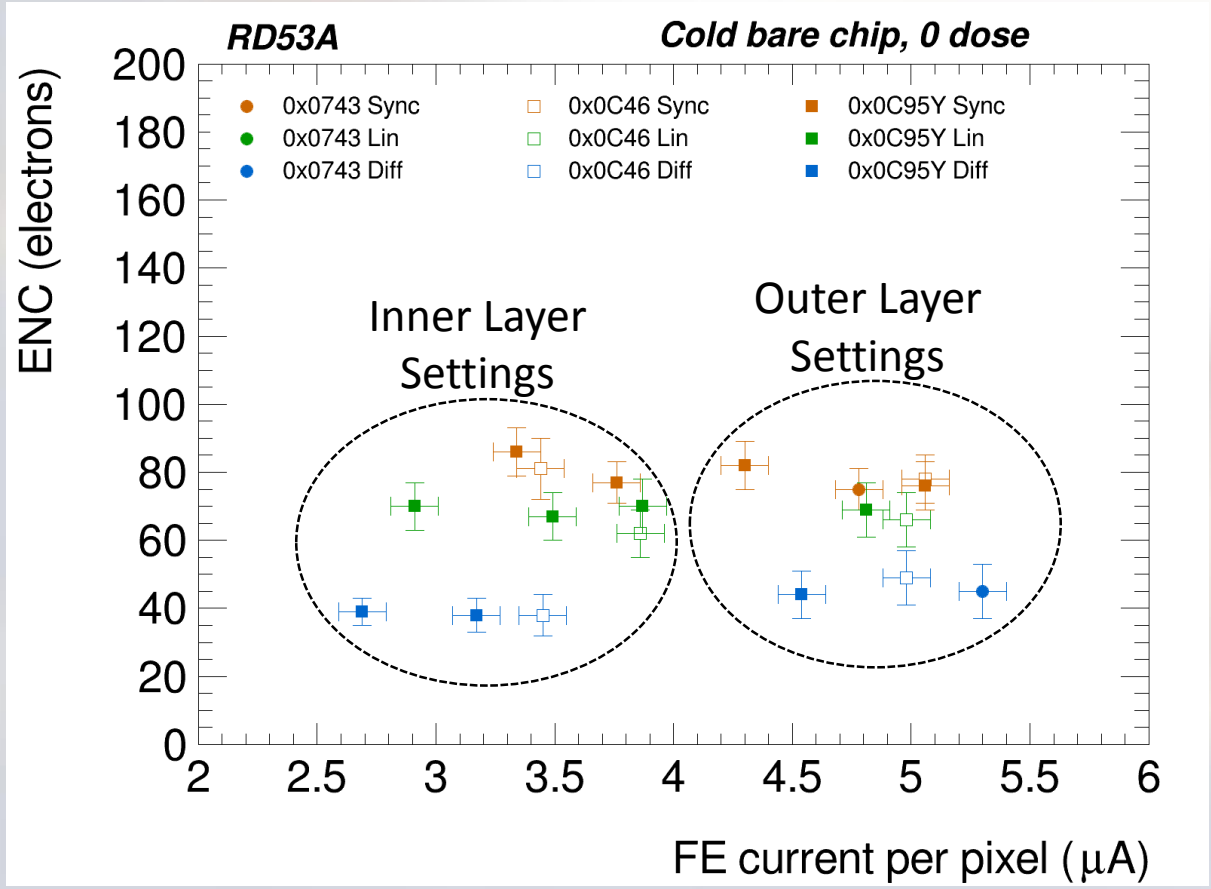


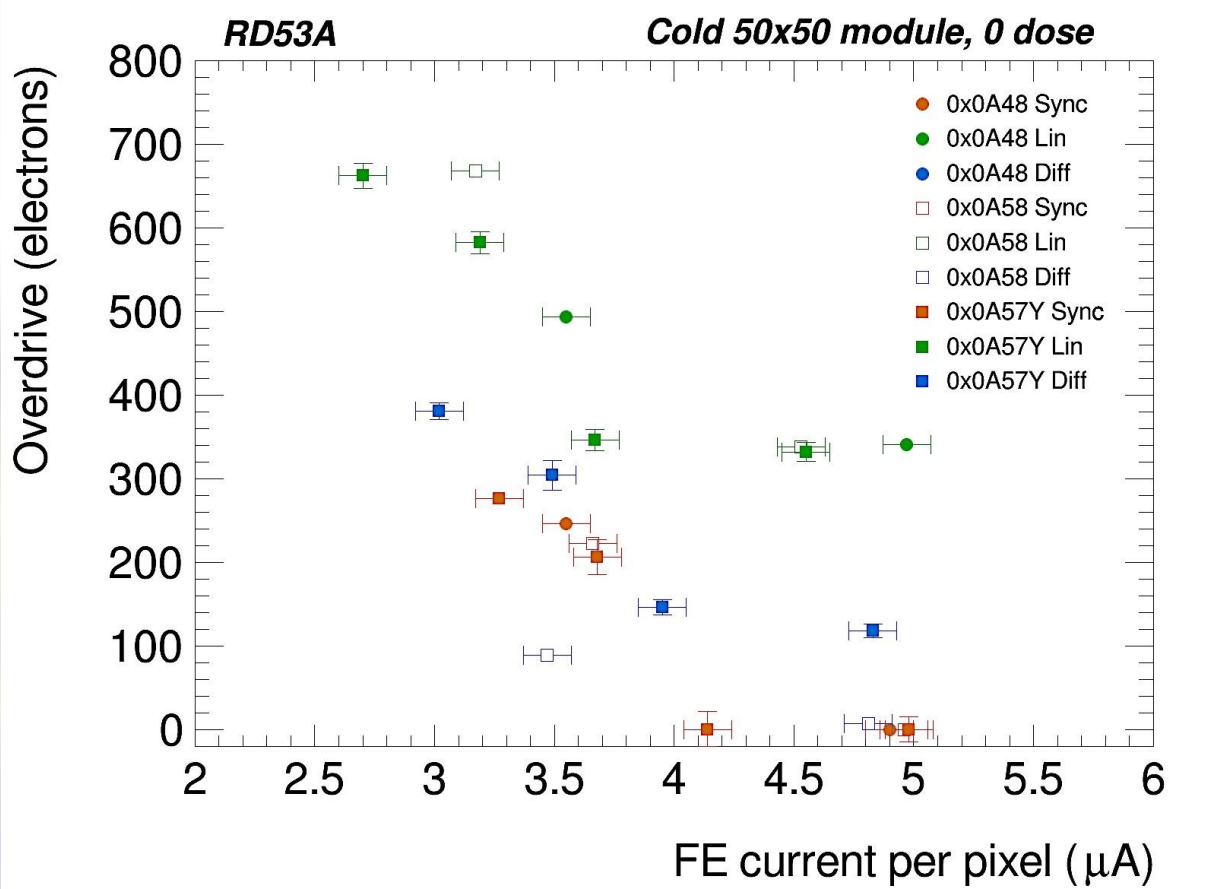




RD53A Results: Analog FE Characterization

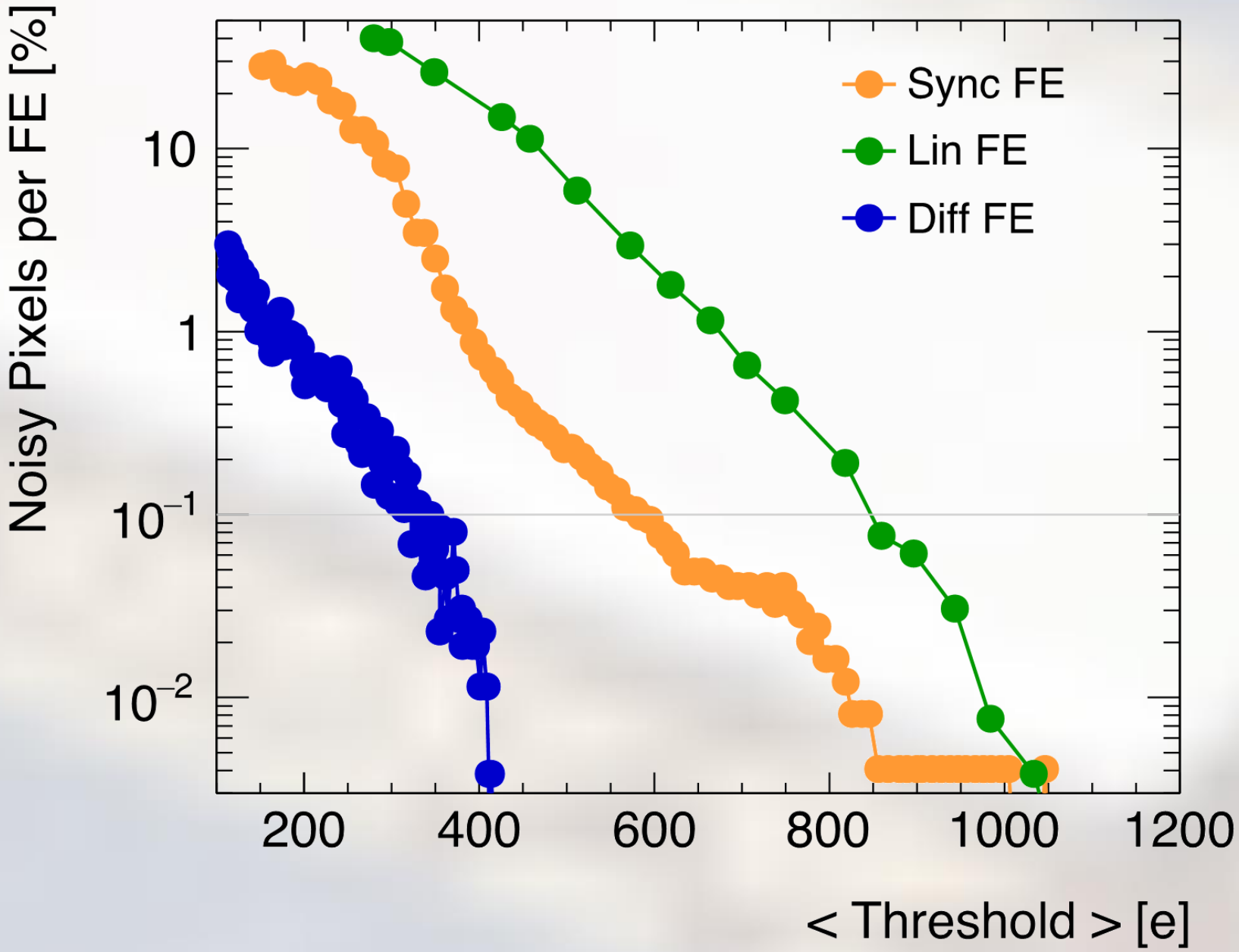
- Verify the functionalities of the three FEs
- Tests with bare chips and 50x50 μm^2 sensors with different settings
- Overdrive: difference between threshold and in-time threshold





RD53A Results: Analog FE Characterization

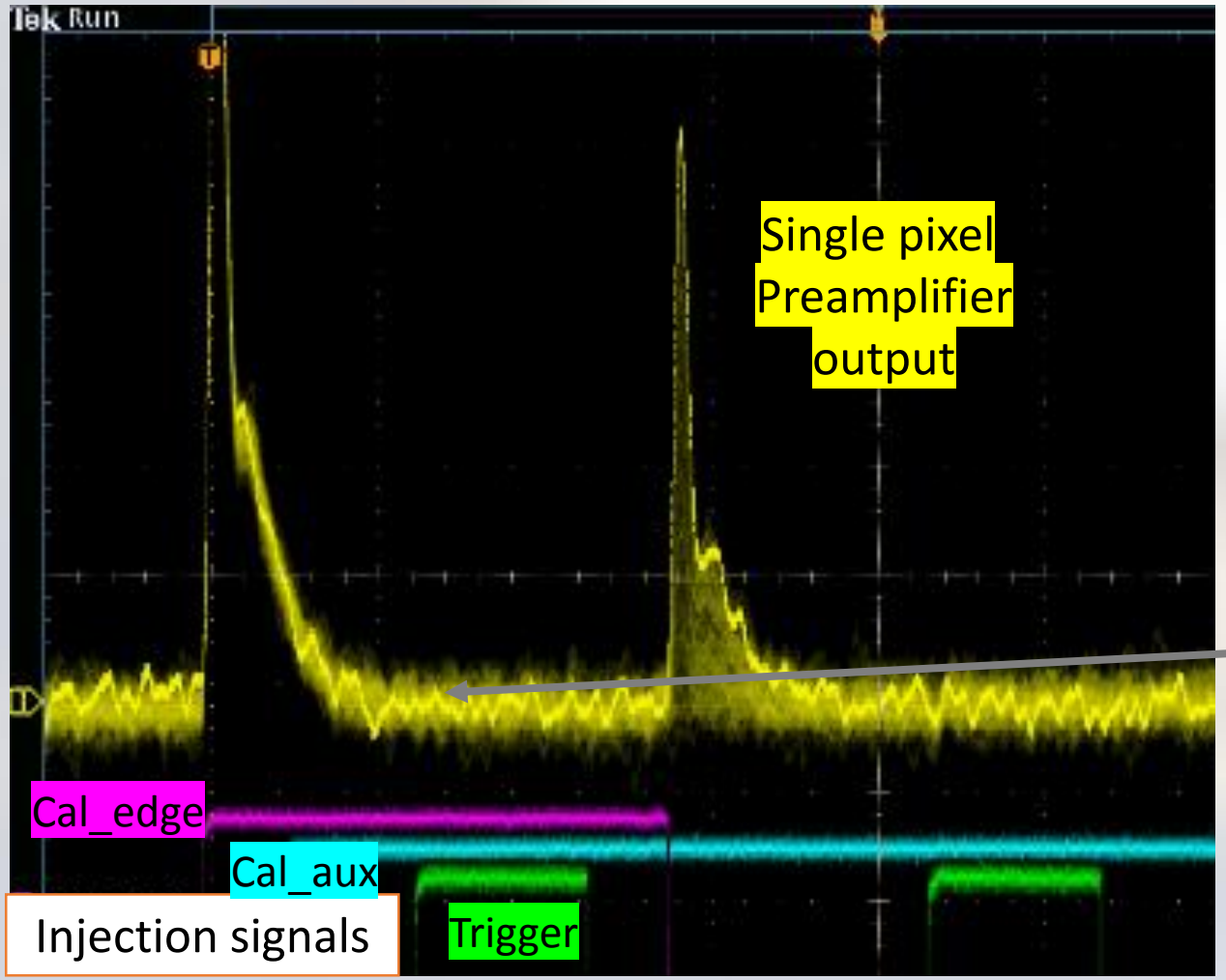
- Measure how many pixels have noise occupancy > 10^{-6} hits/bc as a function of the mean threshold
- Procedure:
  - ✓ tune
  - ✓ lower global threshold
  - ✓ retune pixel threshold (except for the SFE)
  - ✓ measure (in-time)threshold
  - ✓ measure noise
- Dependent on the tuning procedure (assumed that the threshold distributions is Gaussian)
- Cold Bare Chip

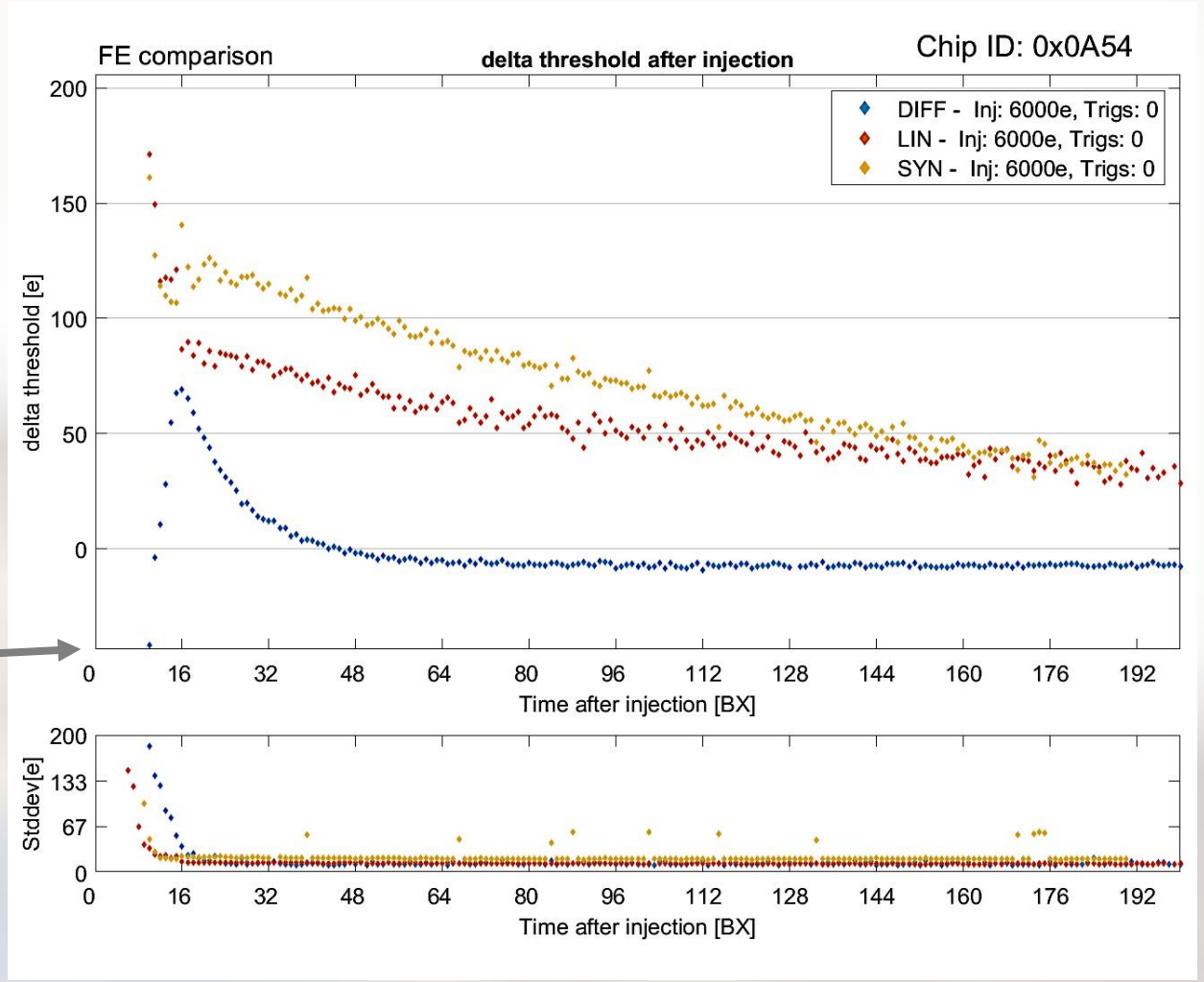


RD53A Results: Double Trigger Scan

- **Double injection** (two charges injected into the same pixel with a variable delay)

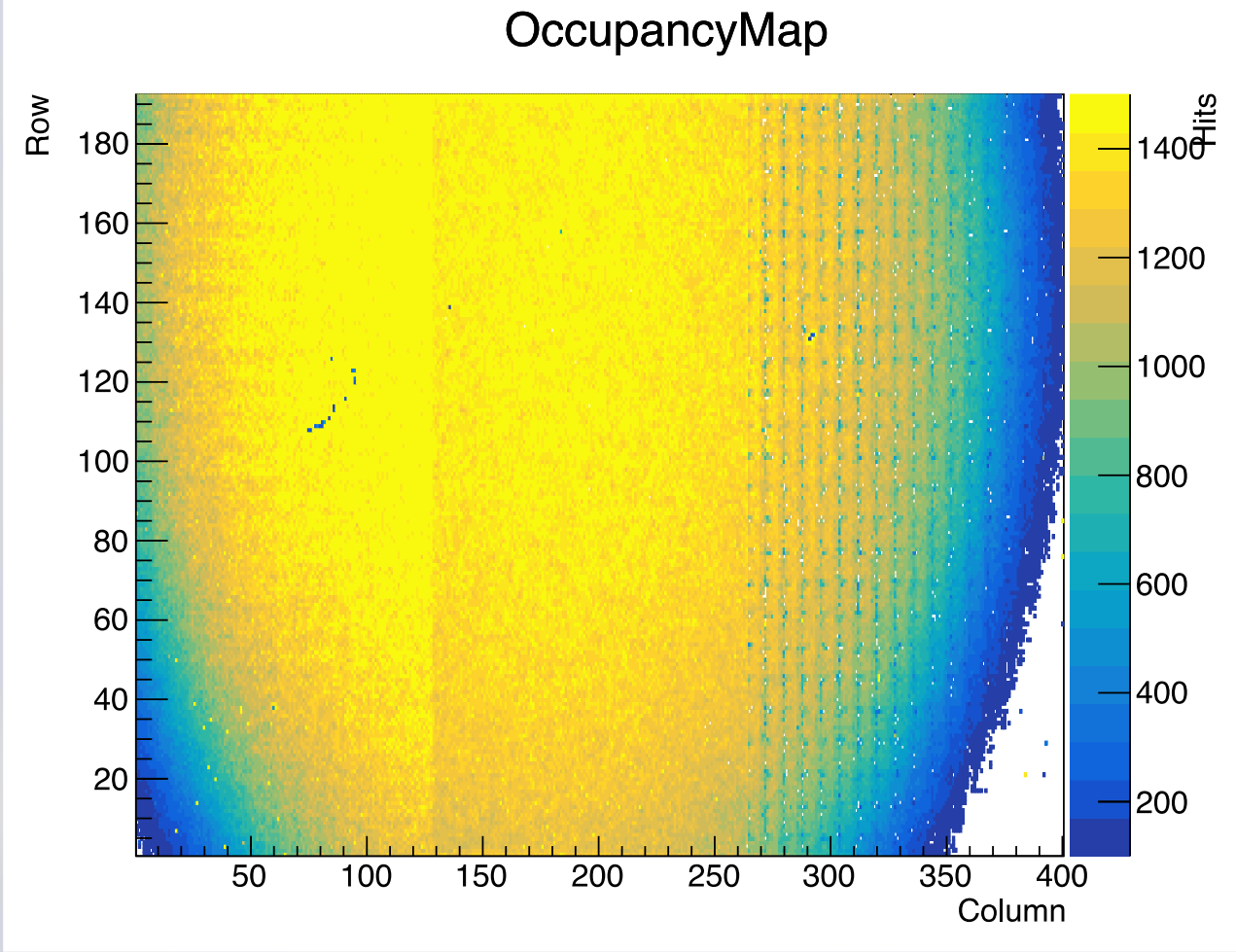
1. Used as *event*: constant charge injection.
2. Used as *probe*: threshold scan to measure the impact of the event.

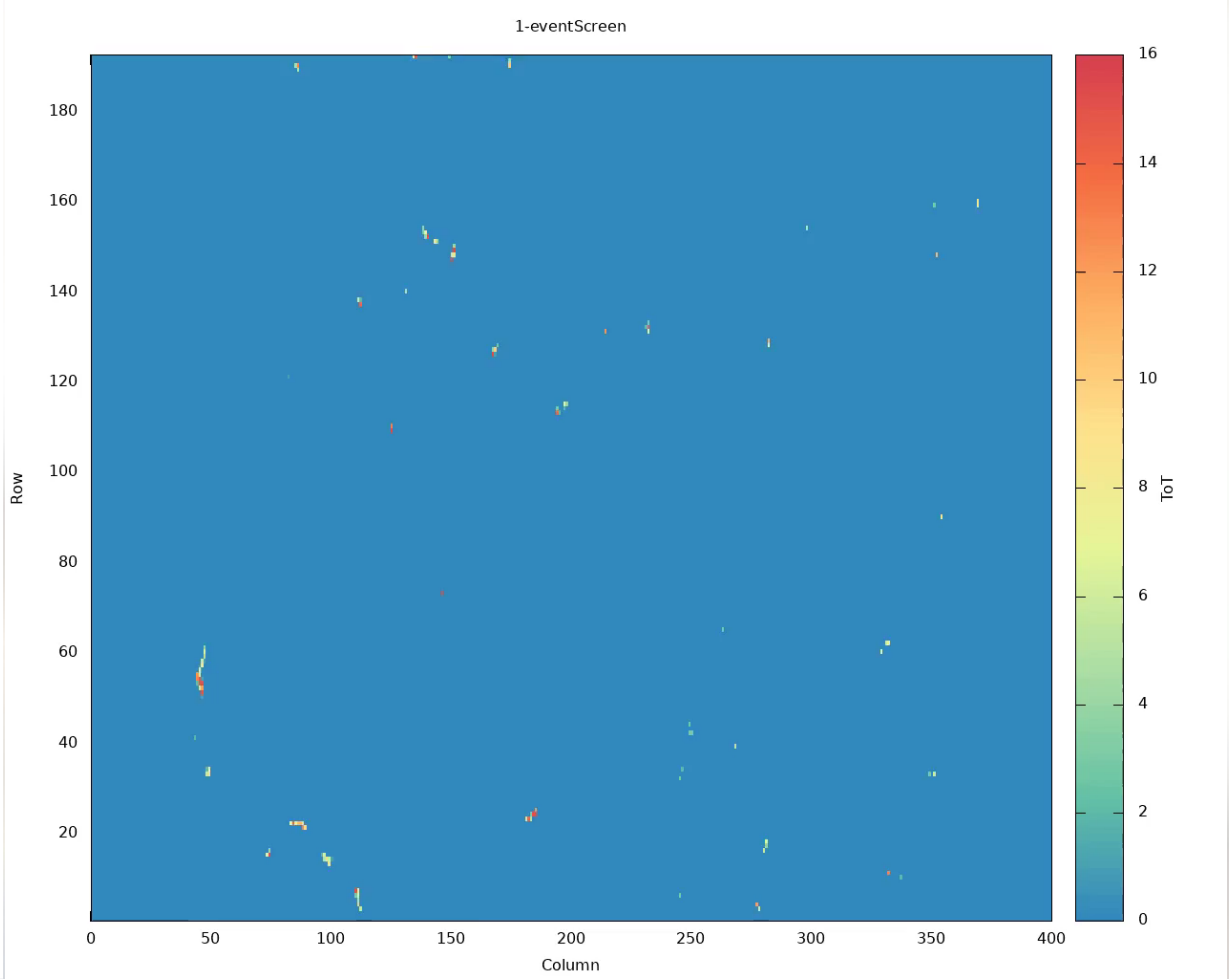




RD53A Results: Realistic Hit Rate

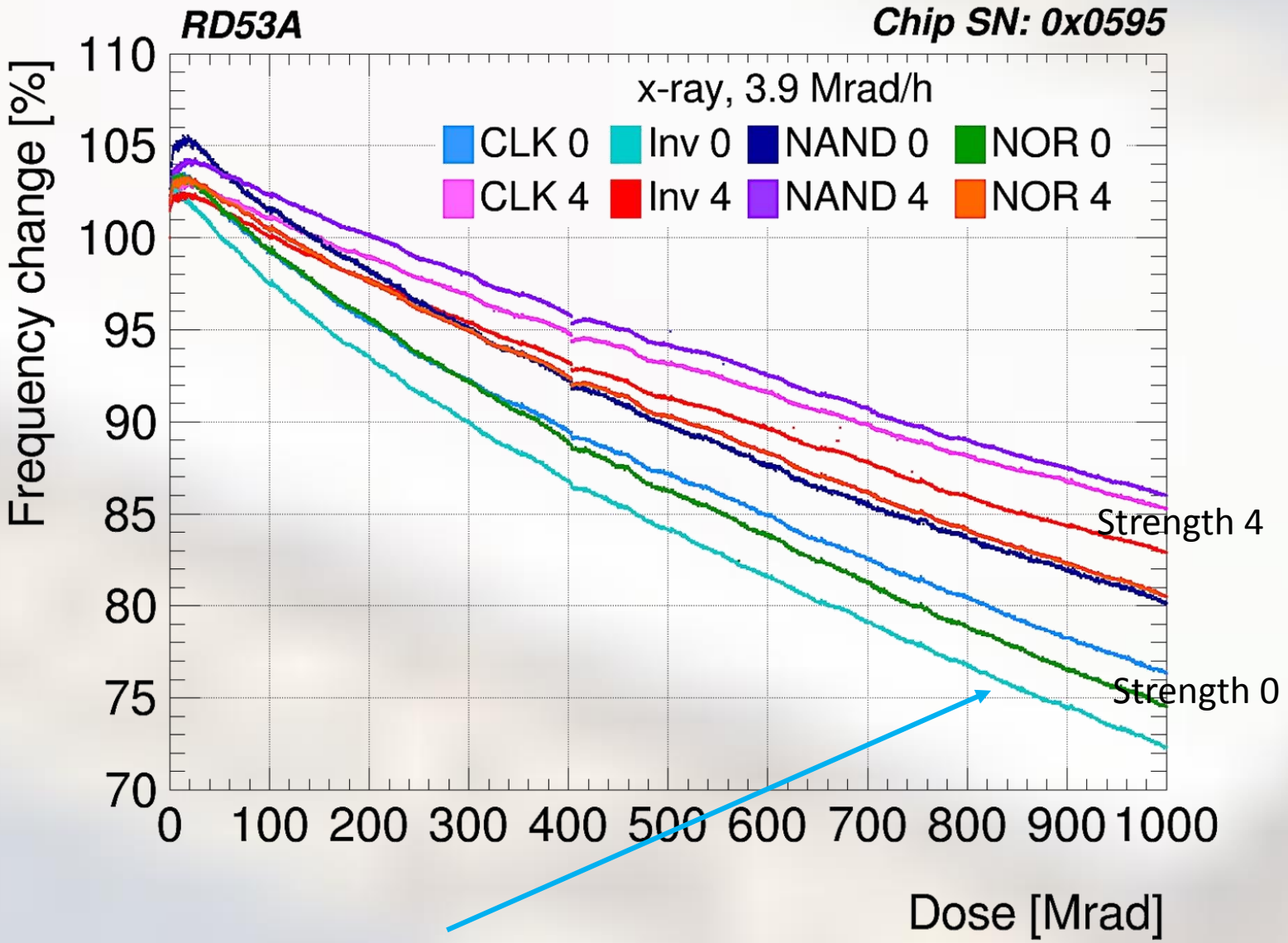
- Kr-85 beta source with activity 60 mCi (opening window 19 mm)
- Estimated hit rate: 7×10^{-4} hits/bc





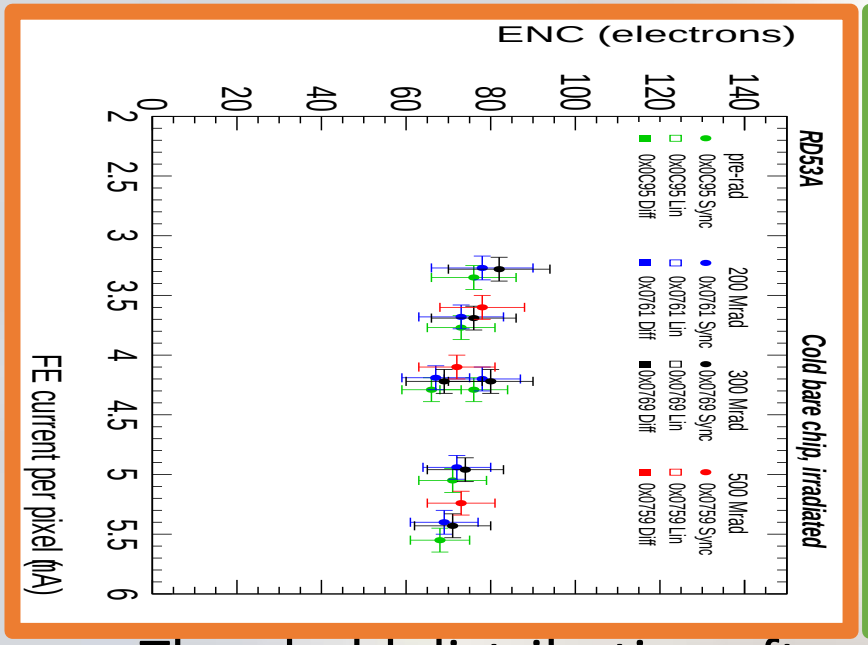
RD53A Results: Analog FE Characterization After Irradiation

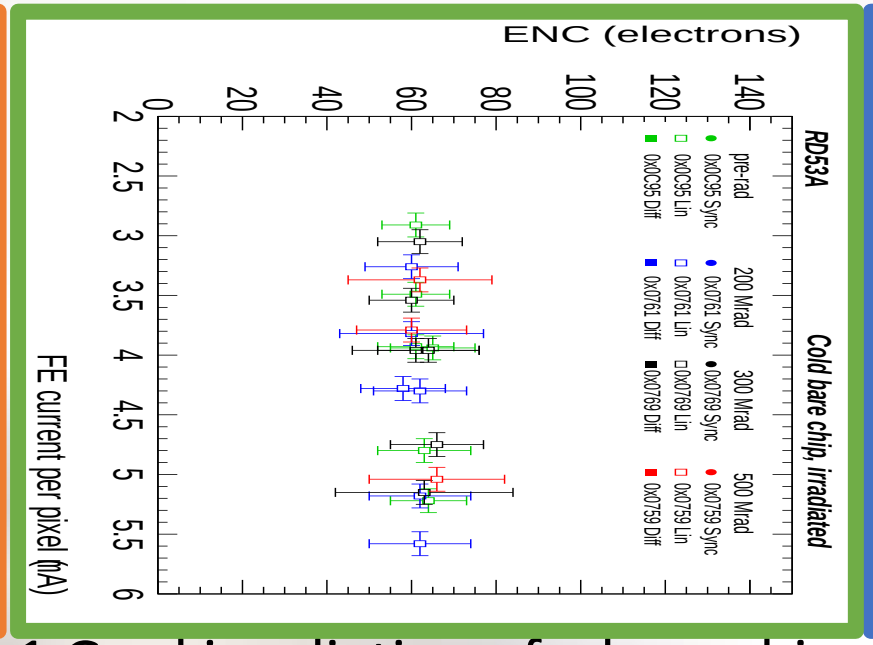
- Multiple irradiation campaigns:
  - ✓ X-ray high and low dose rate irradiation
  - ✓ Non-uniform x-ray irradiation
  - ✓ Low dose rate irradiation (ongoing)
- Eight ring oscillators in the bottom right corner of the chip build with different logic cells
- Each oscillator drives a 12-bit counter, enabled for a known amount of time set by configuration
- **Only 25 % degradation after 1 Grad**

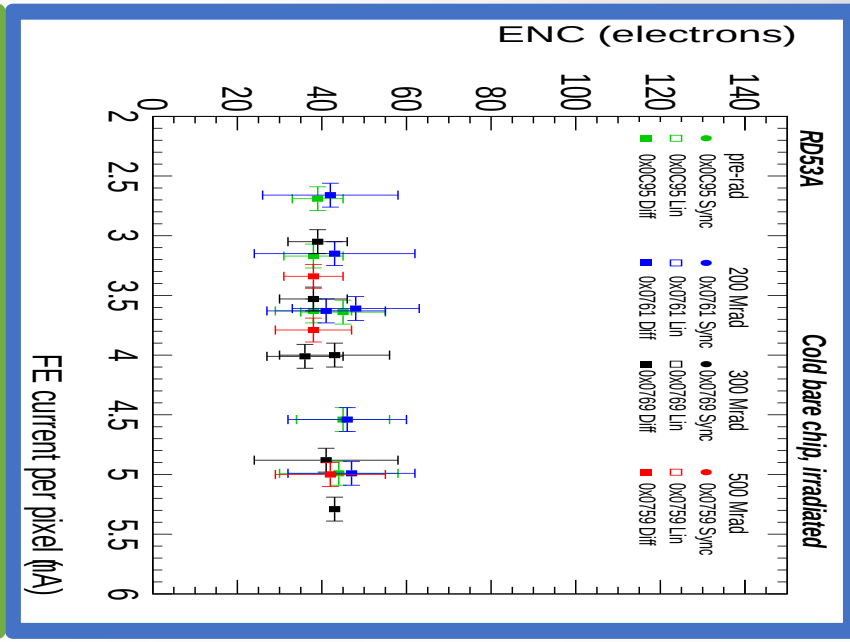


RD53A Results: Analog FE Characterization After Irradiation

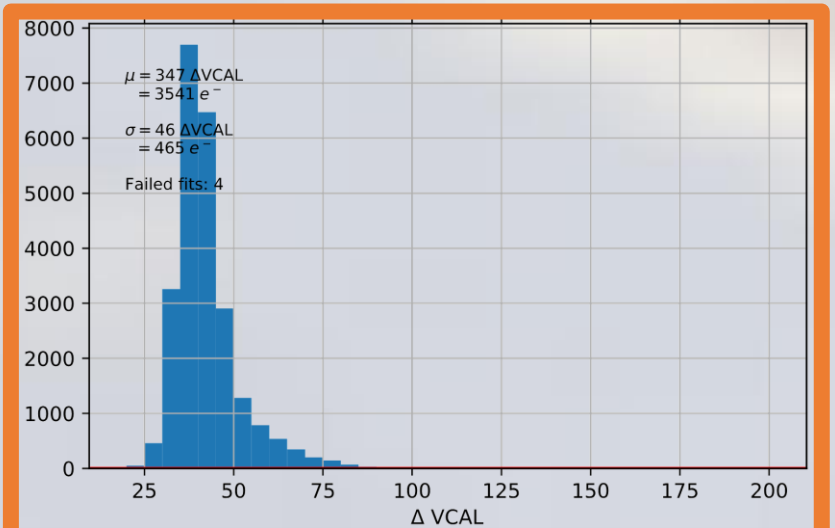
- Noise for different current settings (for 0, 200, 300, 500 Mrad)

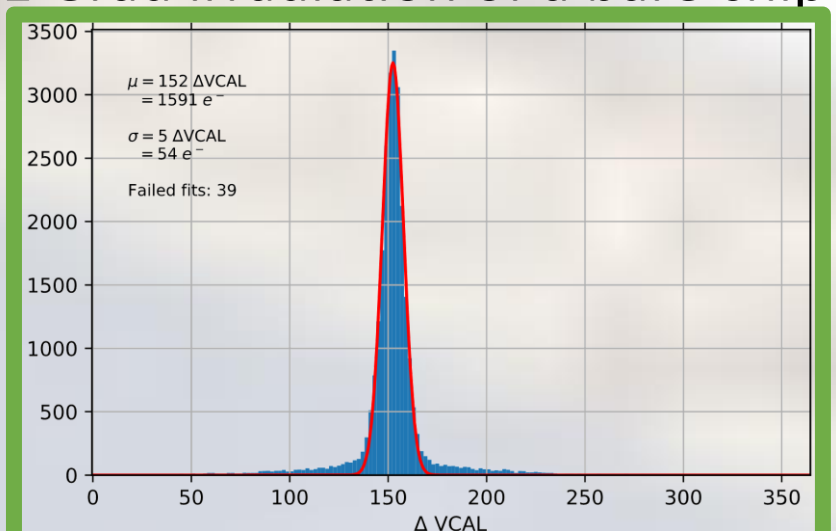


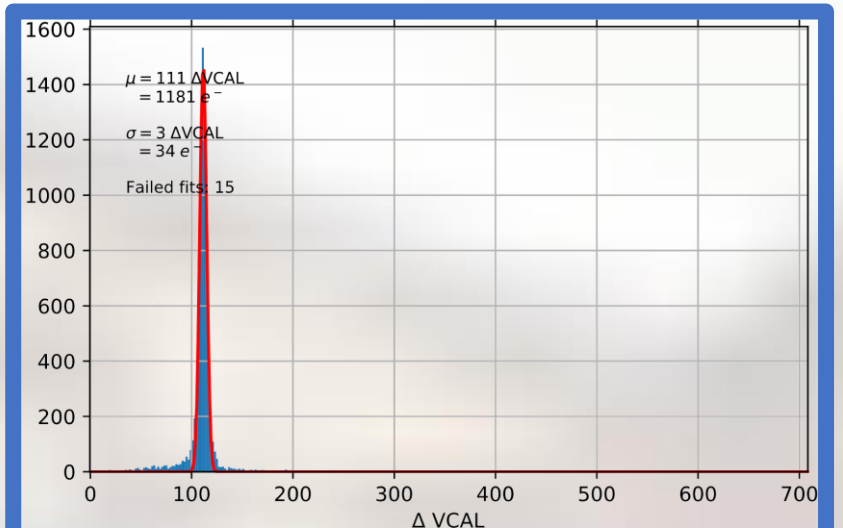




- Threshold distribution after 1 Grad irradiation of a bare chip

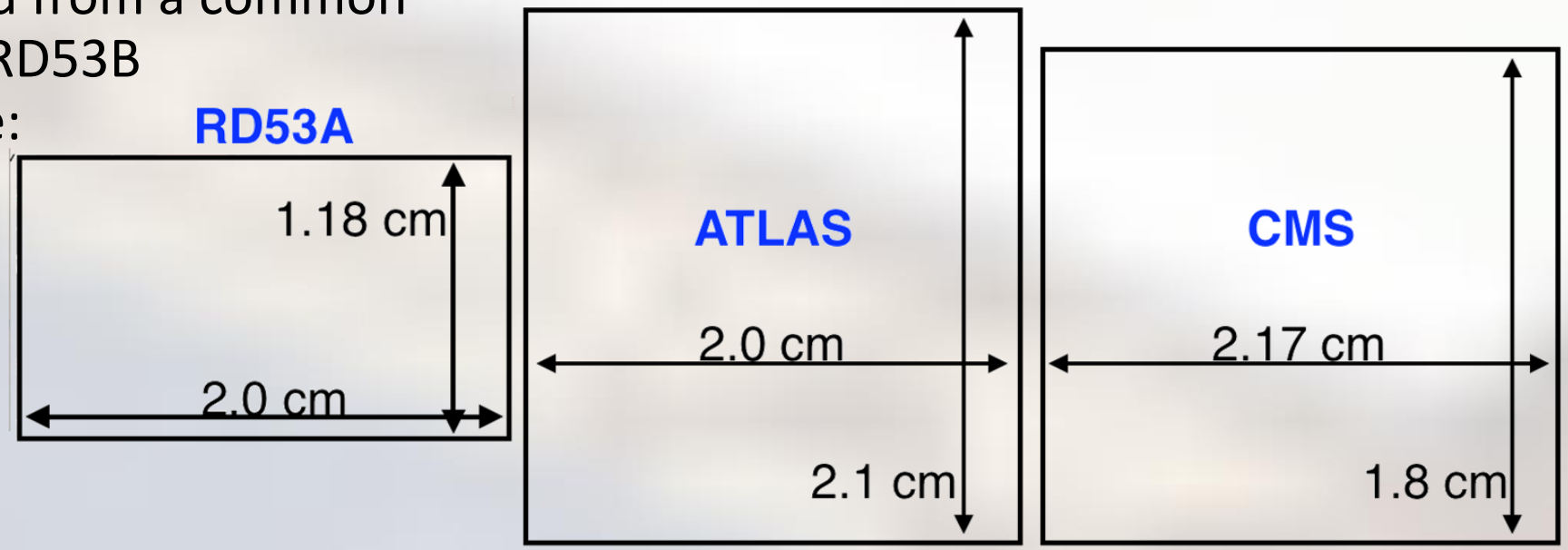




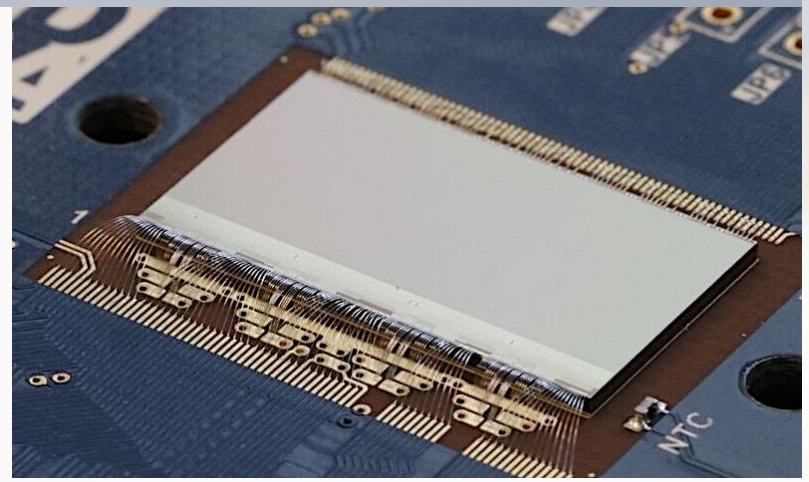


RD53B Development

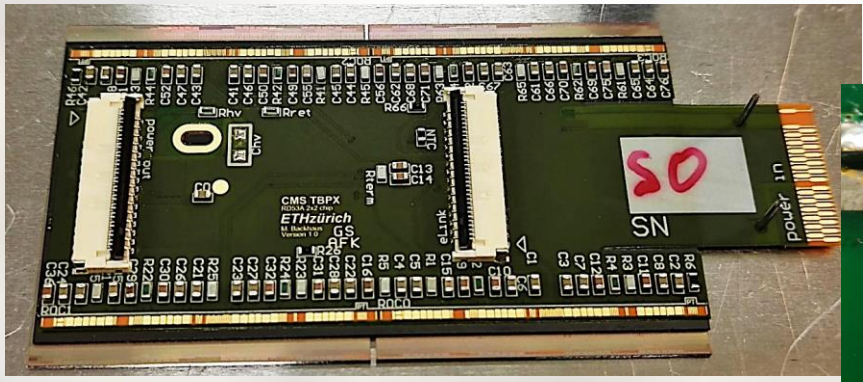
- In parallel with the RD53A characterization,
  the development of the final production chips is already ongoing
- All elements of RD53A with bug fixes and improvements.
- During summer 2018 some small prototypes have been submitted for some blocks requiring major changes.
- ATLAS (CMS) chip submission July 2019 (December 2019).
- Same RD53 team will tape out both chips.
- Both chips are synthesized from a common design framework called RD53B
  main difference is the size:

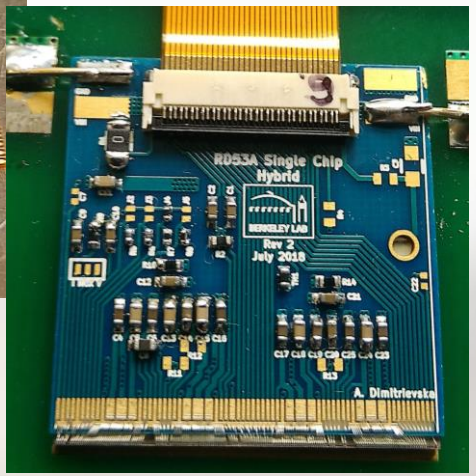


Conclusions and Future plans



- RD53A, a large scale demonstrator chip in 65nm, has been fabricated in fall 2017 and tested in 2018.
- RD53A tests and results show that **RD53A is a solid baseline for final chip development**:
  - ✓ Noise and threshold dispersion values close to simulation results.
  - ✓ Results still improving with optimization of test setups.
  - ✓ First radiation tests show minimal degradation in analog performance up to 500 Mrad at cold temperature (in agreement with simulation using post rad transistor models).
- All analog FE are fulfilling specifications but all need additional modifications for final chip.
- Ongoing modules characterization:
  - ✓ Chip successfully operated with sensor.
  - ✓ Extensive qualification including test-beams.
- Continue with irradiation campaigns.
- Testing of the serial power chain.
- Design and hybrid testing started.



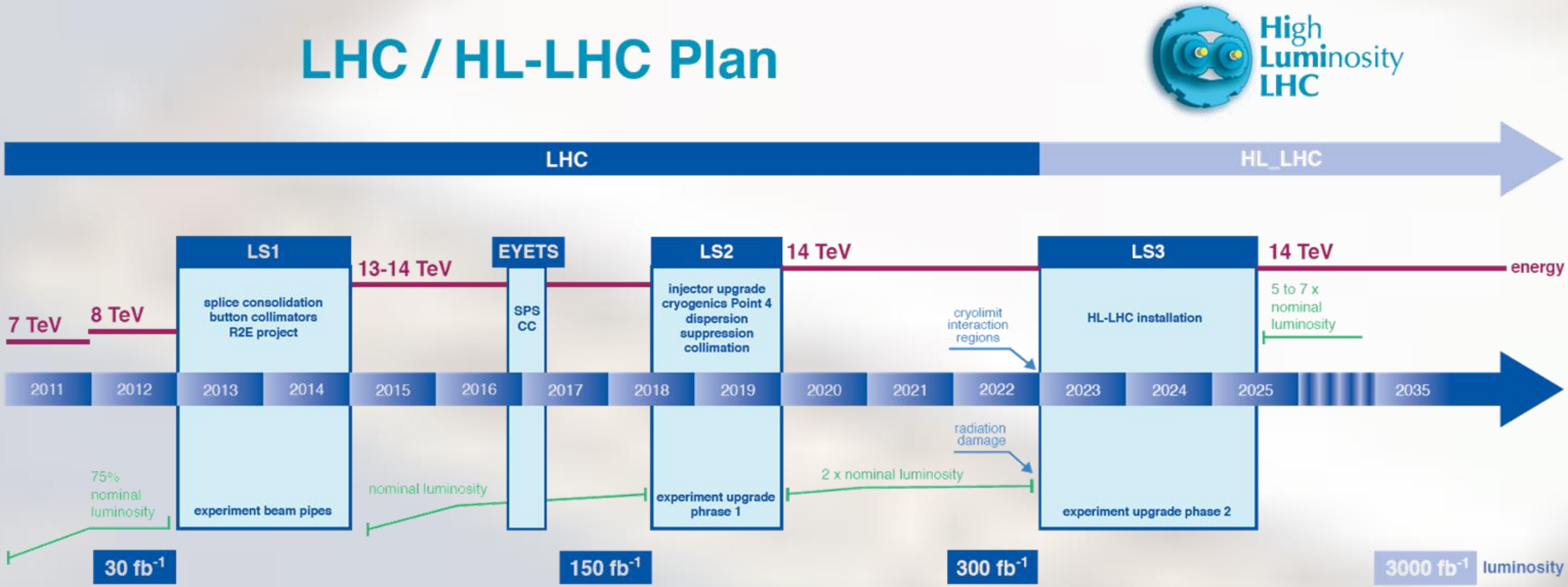


BACKUP SLIDES

Related presentations:

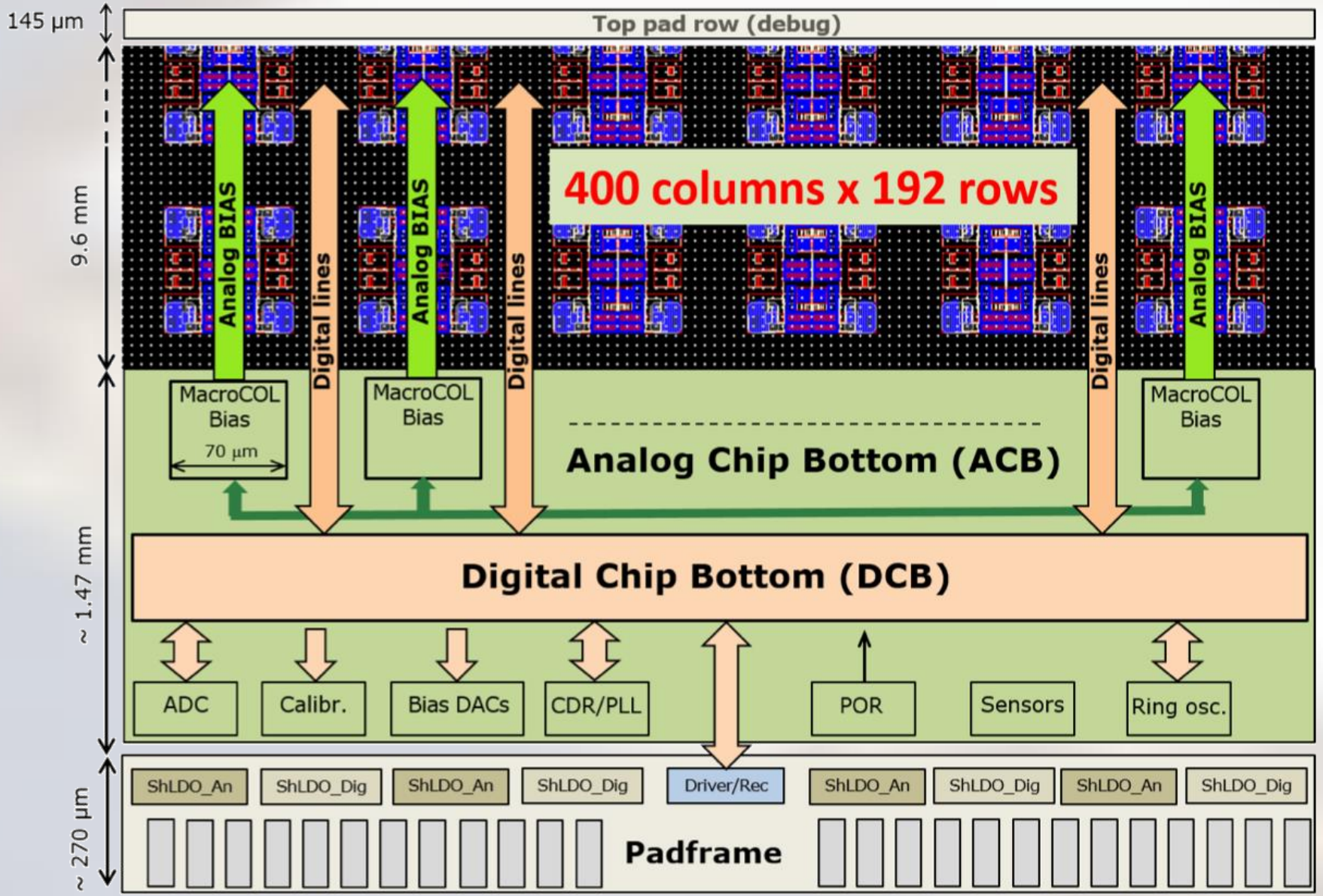
- **T. Flick**: *Module and System test Development for the Phase-2 ATLAS ITk Pixel Upgrade* https://indico.cern.ch/event/716539/contributions/3246646/
- **G. Sguazzoni**: *The CMS Pixel Detector for the High Luminosity LHC* https://indico.cern.ch/event/716539/contributions/3246035/
- **J. Duarte-Campderros**: *First results on 3D pixel sensors interconnected to RD53A readout chip after high energy proton irradiation* https://indico.cern.ch/event/716539/contributions/3246092/

HL-LHC Timeline



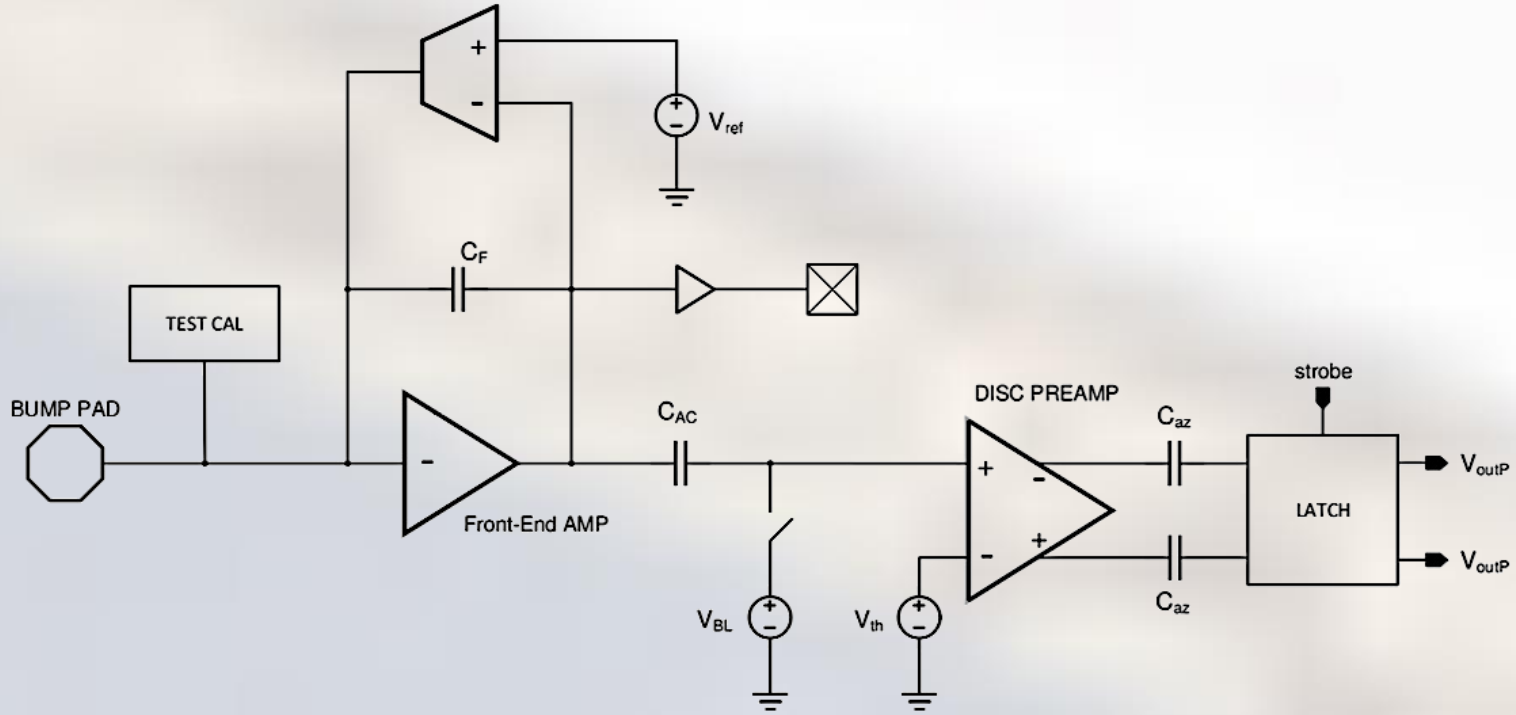
RD53A Floorplan

- Layout and functional view of RD53A floorplan



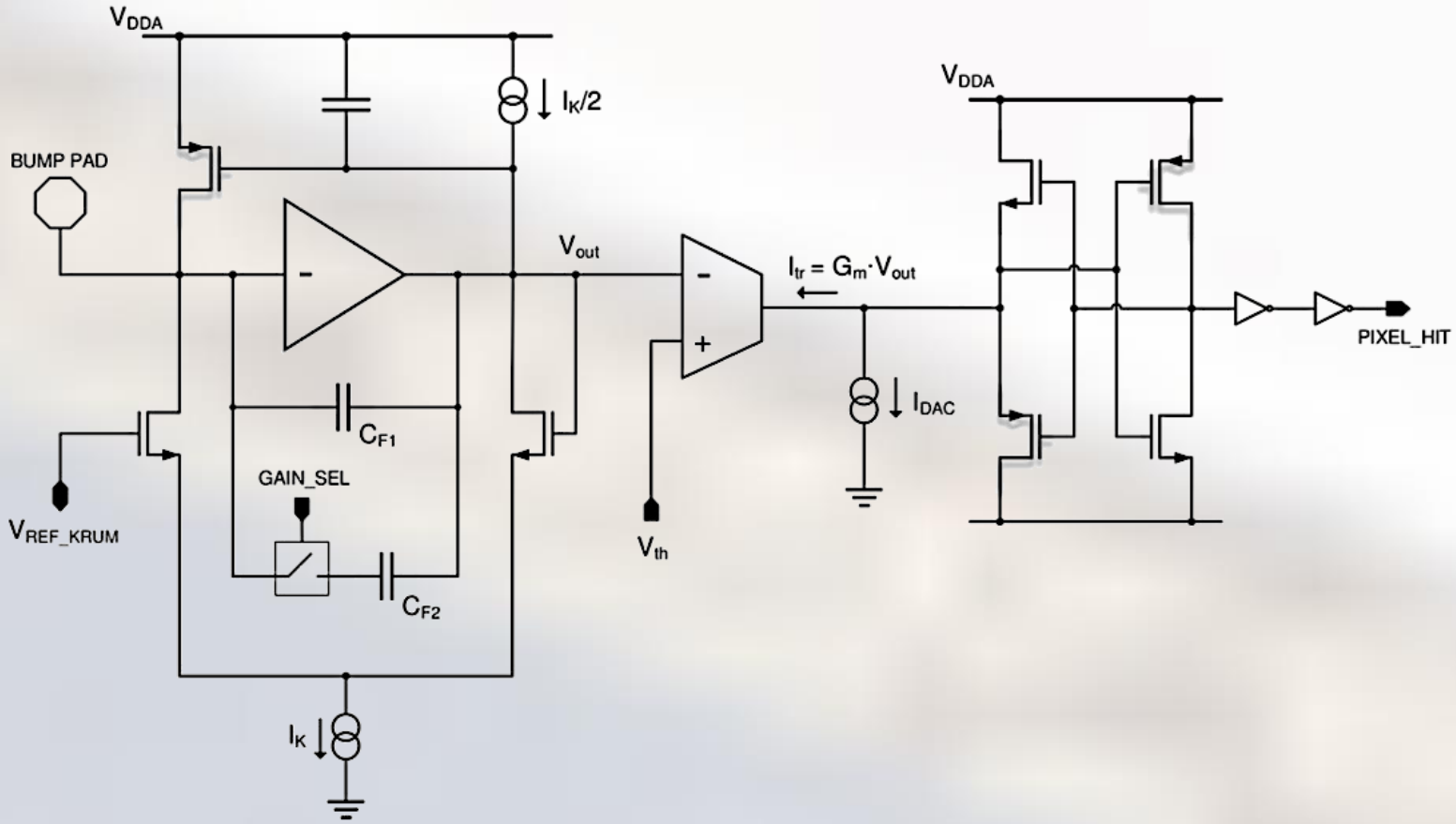
RD53A: Synchronous FE

- Telescopic-cascoded CSA with Krummenacher feedback for linear return to baseline and compensation of DC sensor leakage
- Synchronous hit discriminator with track-and-latch comparator
- Threshold trimming using the auto-zeroing technique (no local trim DAC)
- ToT counting using 40 MHz clock or fast counting using latch as local oscillator (100-900 MHz)
- Efficient self-calibration can be performed according to online machine operations



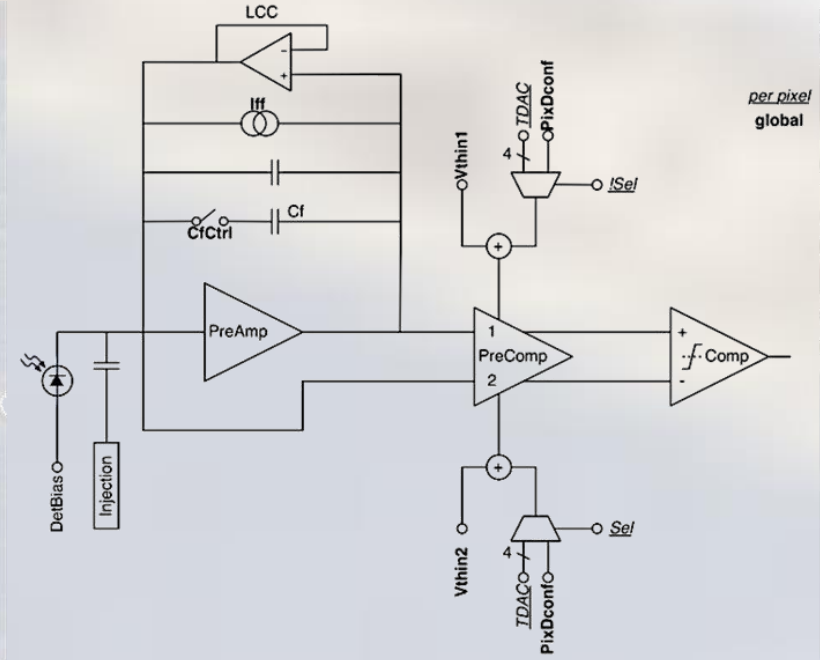
RD53A: Linear FE

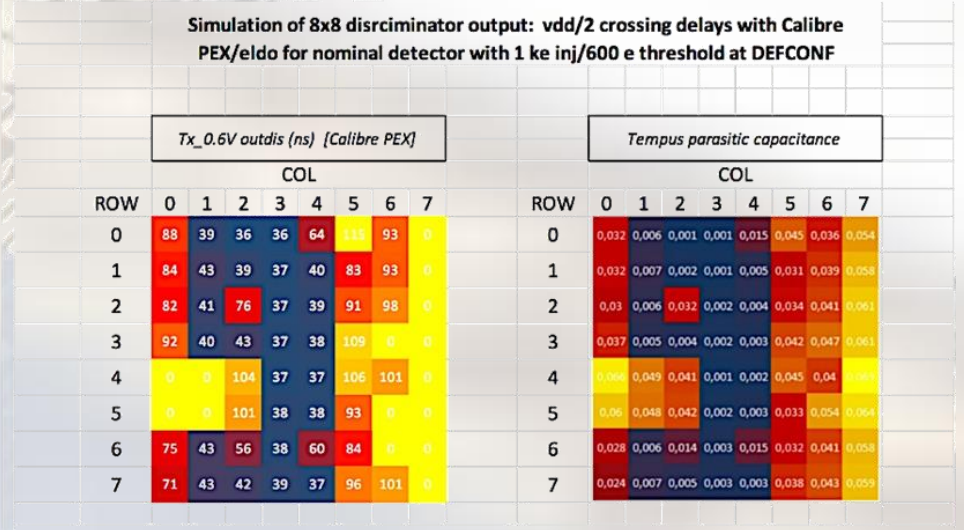
- Single amplification stage with Krummenacher feedback for linear return to baseline and compensation of DC sensor leakage
- High-speed, low-power current comparator 4-bit local DAC for threshold tuning
- 4-bit local DAC for threshold tuning



RD53A: Differential FE

- Continuous reset integrator first stage with DC-coupled pre-comparator stage.
- Switchable low pass filter in feedback for leakage current compensation.
- 5-bit threshold trimming DAC
- Bug in the analog and digital interface: missing P&R constraint on the Differential FE hit output: varying load capacitance on comparator output resulting in systematic variation of delay and ToT (only 12 pixels par core selected as good)
- The bug does not prevent the full characterization of the Differential FE





Simulation of 8x8 disrciminator output: vdd/2 crossing delays with Calibre PEX/eldo for nominal detector with 1 ke inj/600 e threshold at DEFCONF

Tx_0.6V outdis (ns) [Calibre PEX]

ROW \ COL	0	1	2	3	4	5	6	7
0	88	39	36	36	64	115	93	0
1	84	43	39	37	40	83	93	0
2	82	41	76	37	39	91	98	0
3	92	40	43	37	38	109	0	0
4	0	0	104	37	37	106	101	0
5	0	0	101	38	38	93	0	0
6	75	43	56	38	60	84	0	0
7	71	43	42	39	37	96	101	0

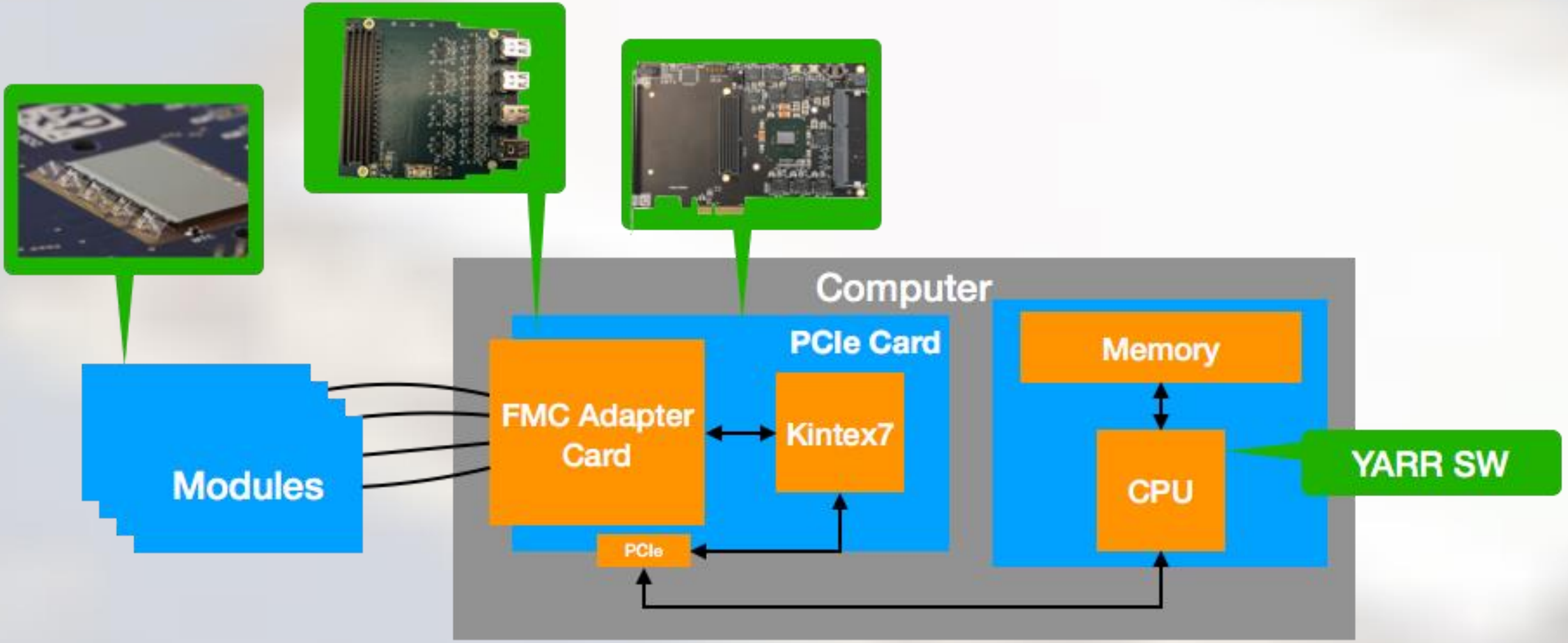
Tempus parasitic capacitance

ROW \ COL	0	1	2	3	4	5	6	7
0	0,032	0,006	0,001	0,001	0,015	0,045	0,036	0,054
1	0,032	0,007	0,002	0,001	0,005	0,031	0,039	0,058
2	0,03	0,006	0,032	0,002	0,004	0,034	0,041	0,061
3	0,037	0,005	0,004	0,002	0,003	0,042	0,047	0,061
4	0,056	0,049	0,041	0,001	0,002	0,045	0,04	0,059
5	0,06	0,048	0,042	0,002	0,003	0,033	0,054	0,064
6	0,028	0,006	0,014	0,003	0,015	0,032	0,041	0,058
7	0,024	0,007	0,005	0,003	0,003	0,038	0,043	0,059

RD53A Features

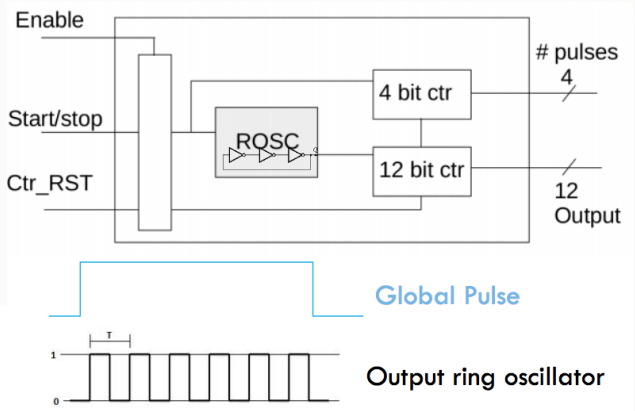
- **Start-up issues**: PLL not locking
  - *V*DD (from which PLL is powered) has to be >1.12V for PLL to work
  - *V*DDA and *V*DDD decrease with lowering temperature O (1mV/1C)
- **Synchronous FE**: auto-zeroing produces noise on power lines.
- **Linear FE**: untuned threshold dispersion is very large
- **Differential FE**: pixel-pixel variation of the parasitic capacitance at the comparator outputs, good pixel matrix has to be applied for time-sensitive measurements
- Source scans requires all four HitOrlanes.

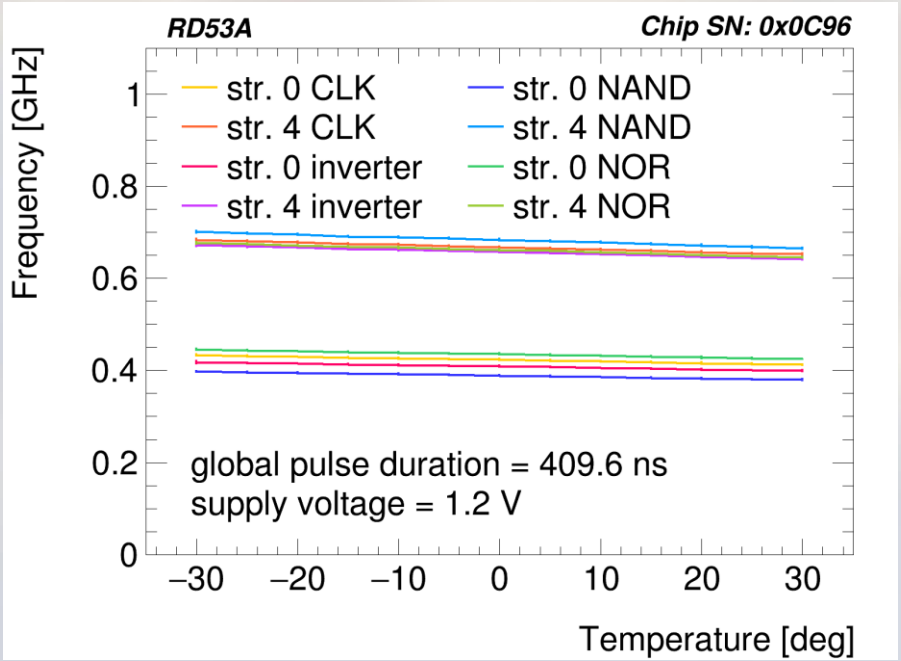
RD53A Testing: YARR

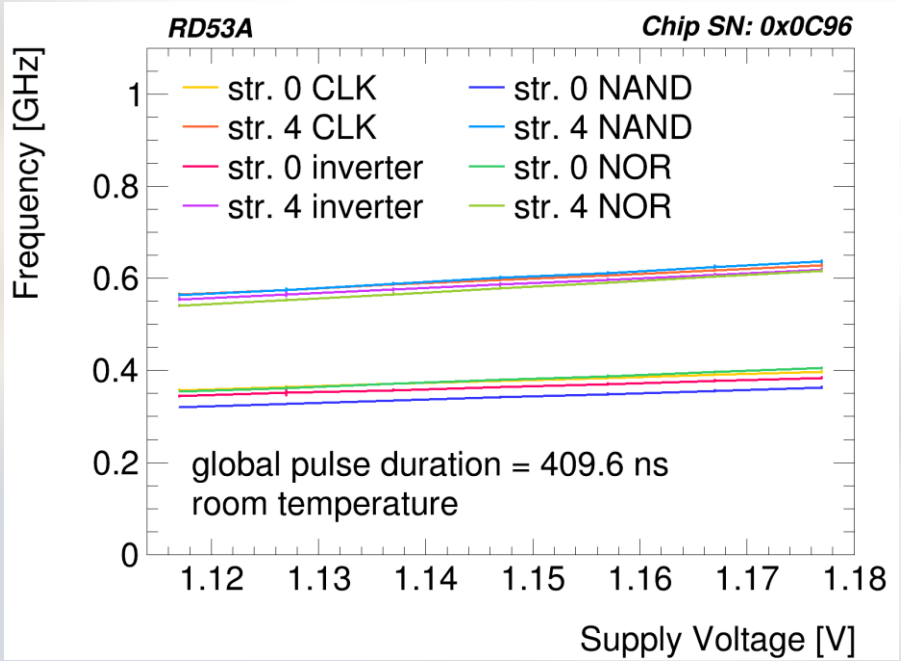


RD53A Characterization: Register Readback Tests

- Readout registers same command for both global and local registers, and register frames are received containing requested registers
- Differential and linear front end have 8-bit, while synchronous has 3-bit registers RD53A has read-only registers for some tests and monitors,
- Ring Oscillators shown here:
  - Scan the duration of global pulse
  - Oscillator frequency depends on temperature and voltage

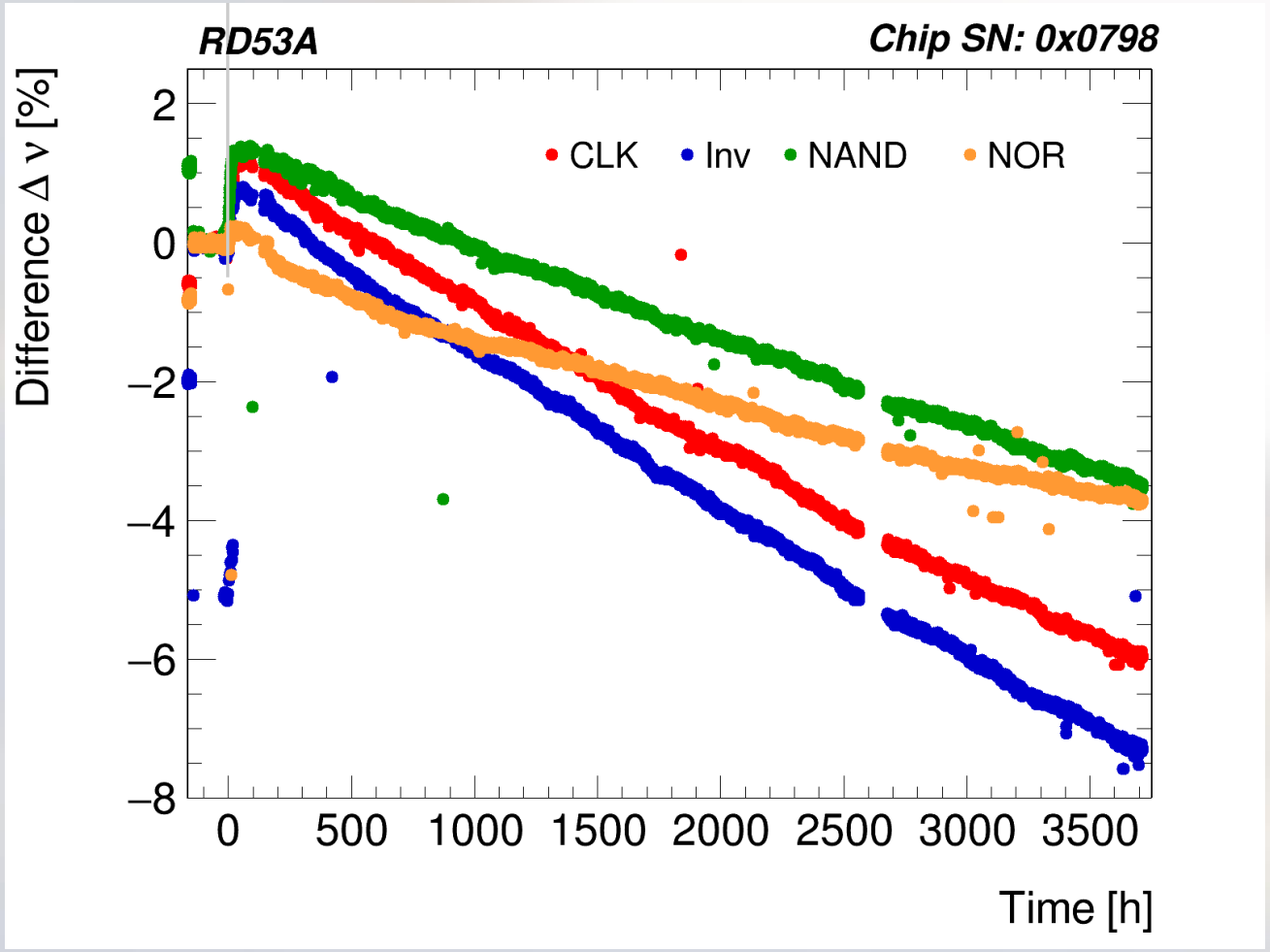


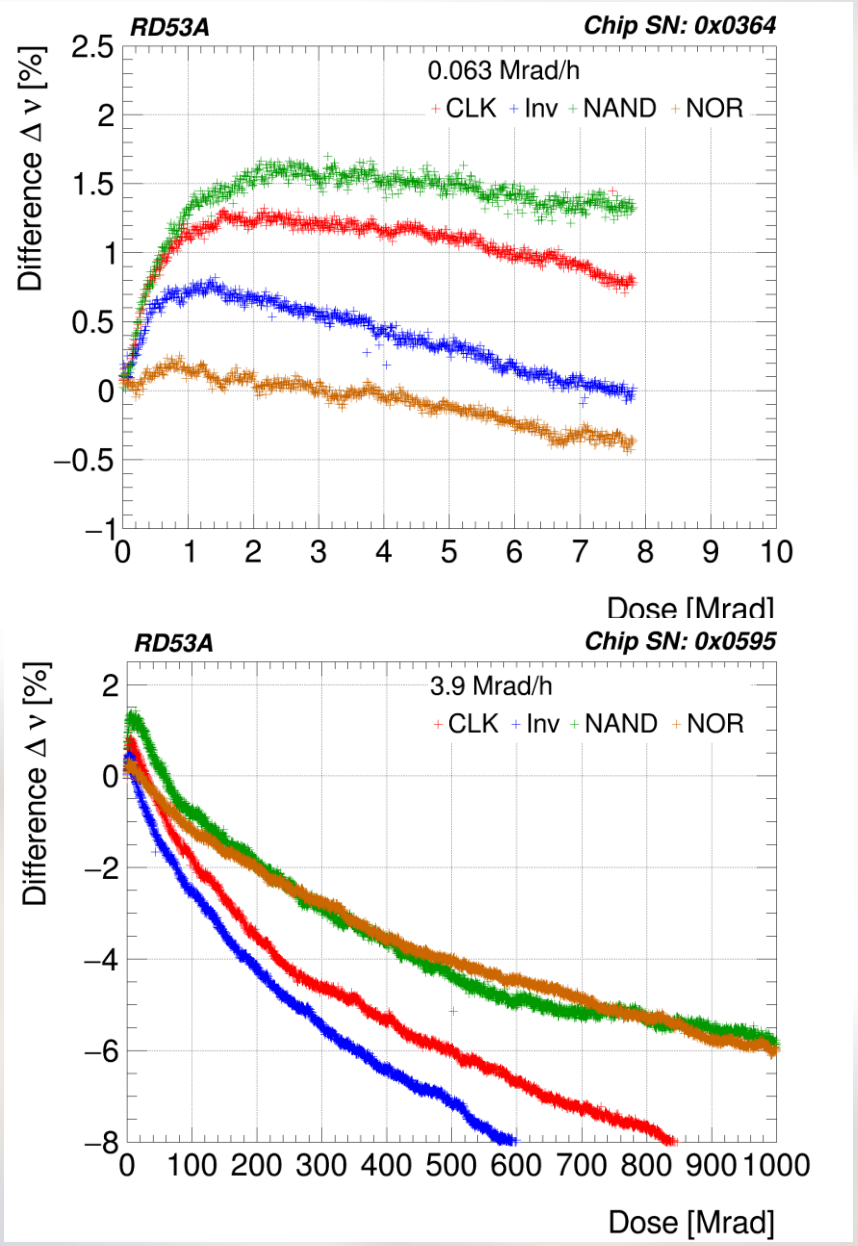




RD53A Characterization: Ring Oscillators

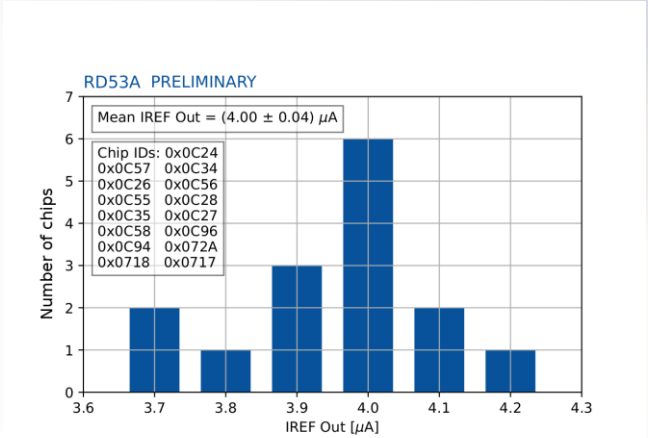
- Low and high dose rate comparison
- Difference between gates of different strengths



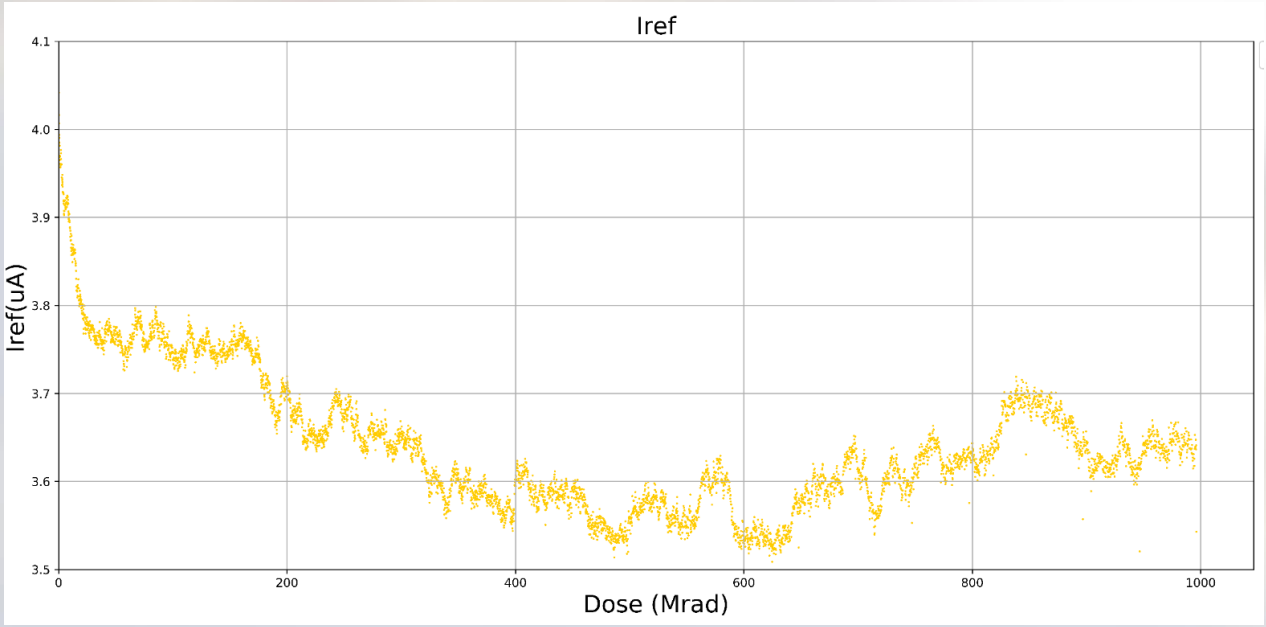


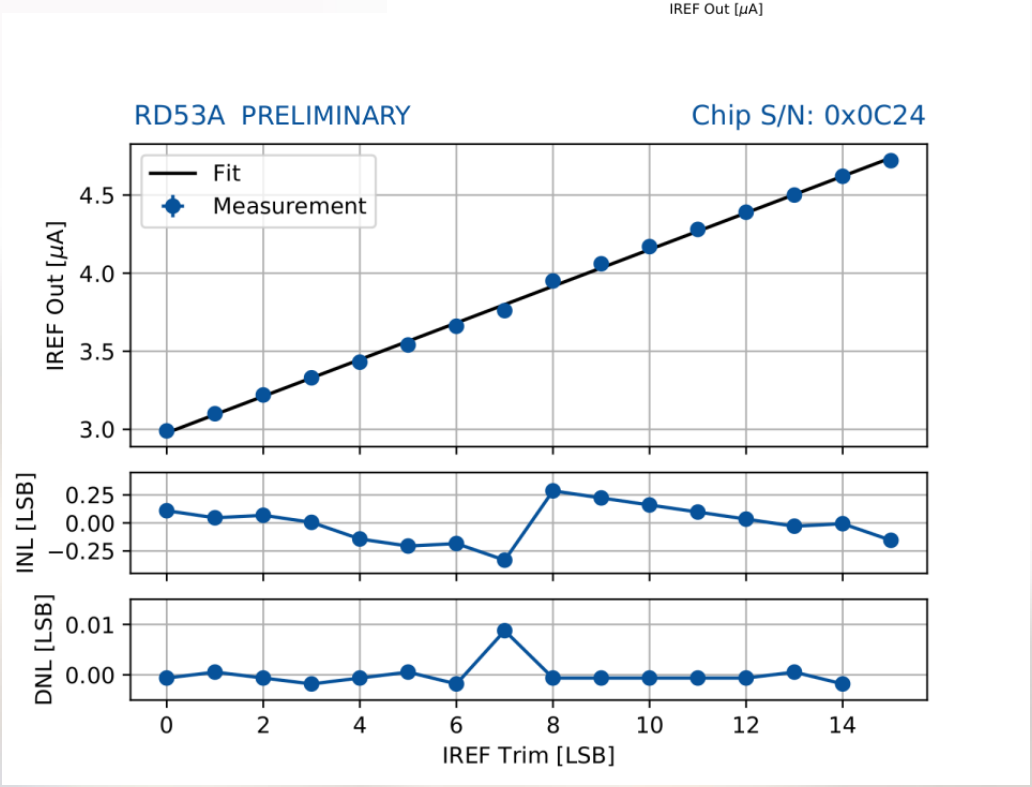
RD53A Characterization: Reference Current

- Nominal internal reference current is 4 µA
- Has to be trimmed in order to compensate for process variations
- Trimming can be done with 4-bit code set by wirebonds
- *The nominal current value correspond to setting 6 - 11*



- After irradiation:



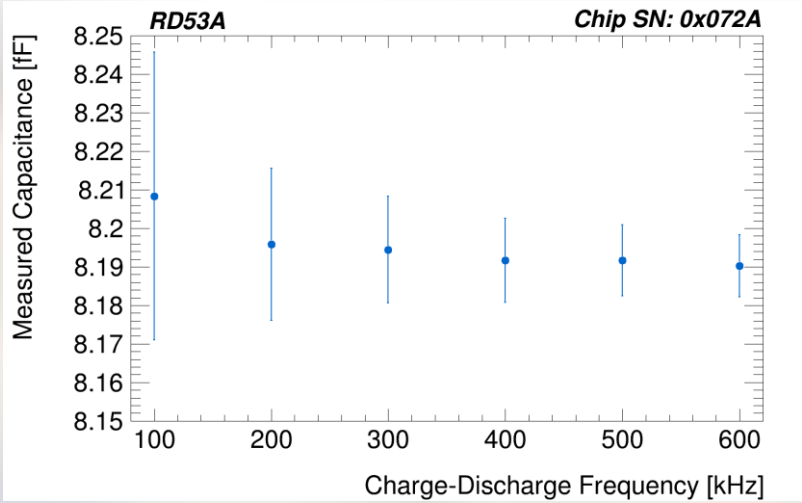


RD53A Characterization: Injection Capacitance

- Two banks of 100 parallel injection capacitors for the purpose of measuring the capacitance (left and right side)
- The capacitance is measured from the frequency and measured current when the banks are cyclically charged and discharged
- 0x072A:
  - injection capacitance is measured form multiple charge-discharge cycle frequencies
  - left side bank shown, parasitic capacitance is subtracted
  - parasitic capacitance measurement circuit is broken for right side
- Average: 8.21 fF
- Difference between banks:
  0.04 fF, left side has slightly larger capacitance
- **Nominal value** 8.5 fF

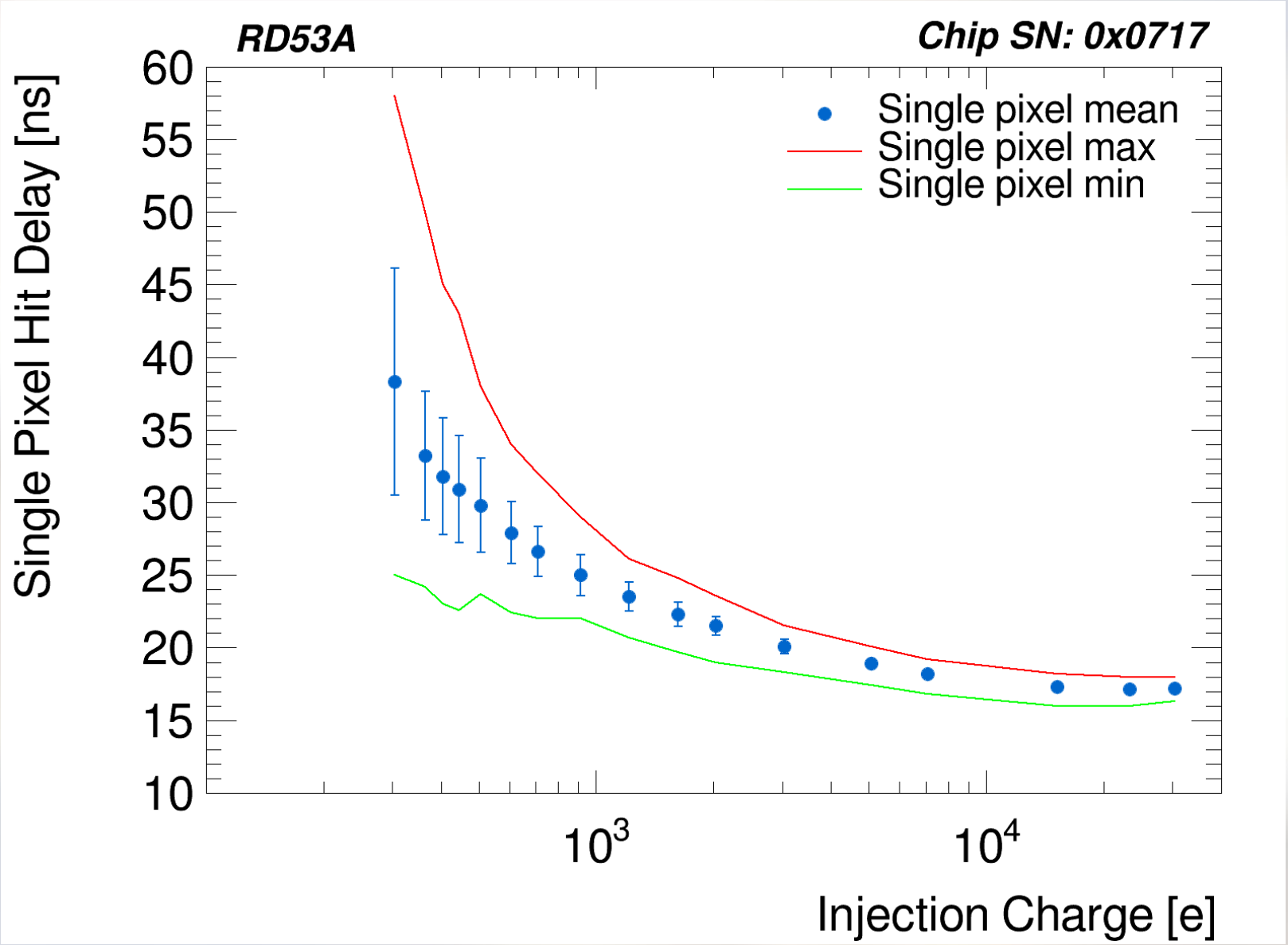
	Left Side	Right Side
0x072a	8.20fF	Unknown
0x0c96	8.12fF	8.35fF
0x0717	8.28fF	8.11fF
0x0718	8.30fF	8.12fF
0x0c94	8.22fF	8.15fF
0x0c95	8.25fF	8.25fF

All uncertainties +- 0.01fF



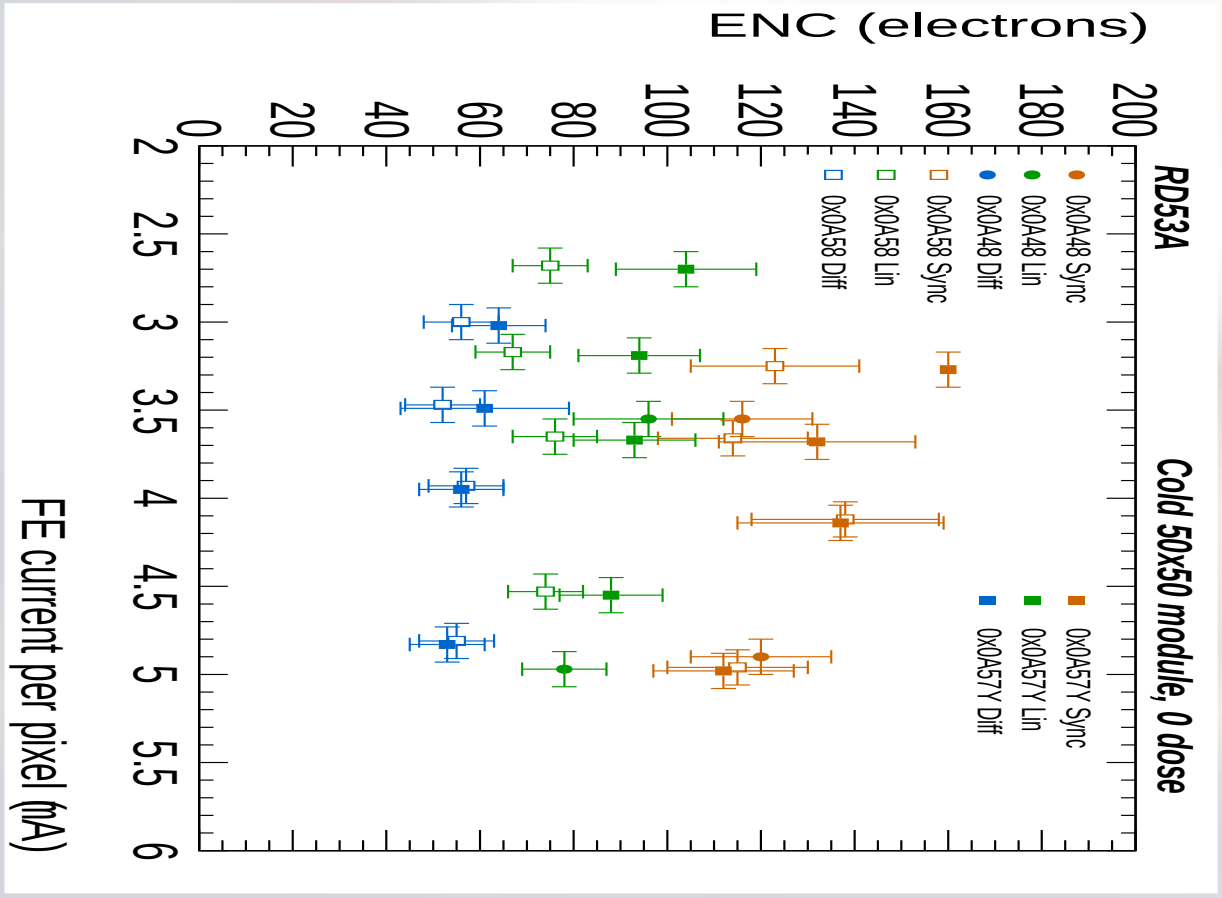
RD53A Characterization: Time-walk

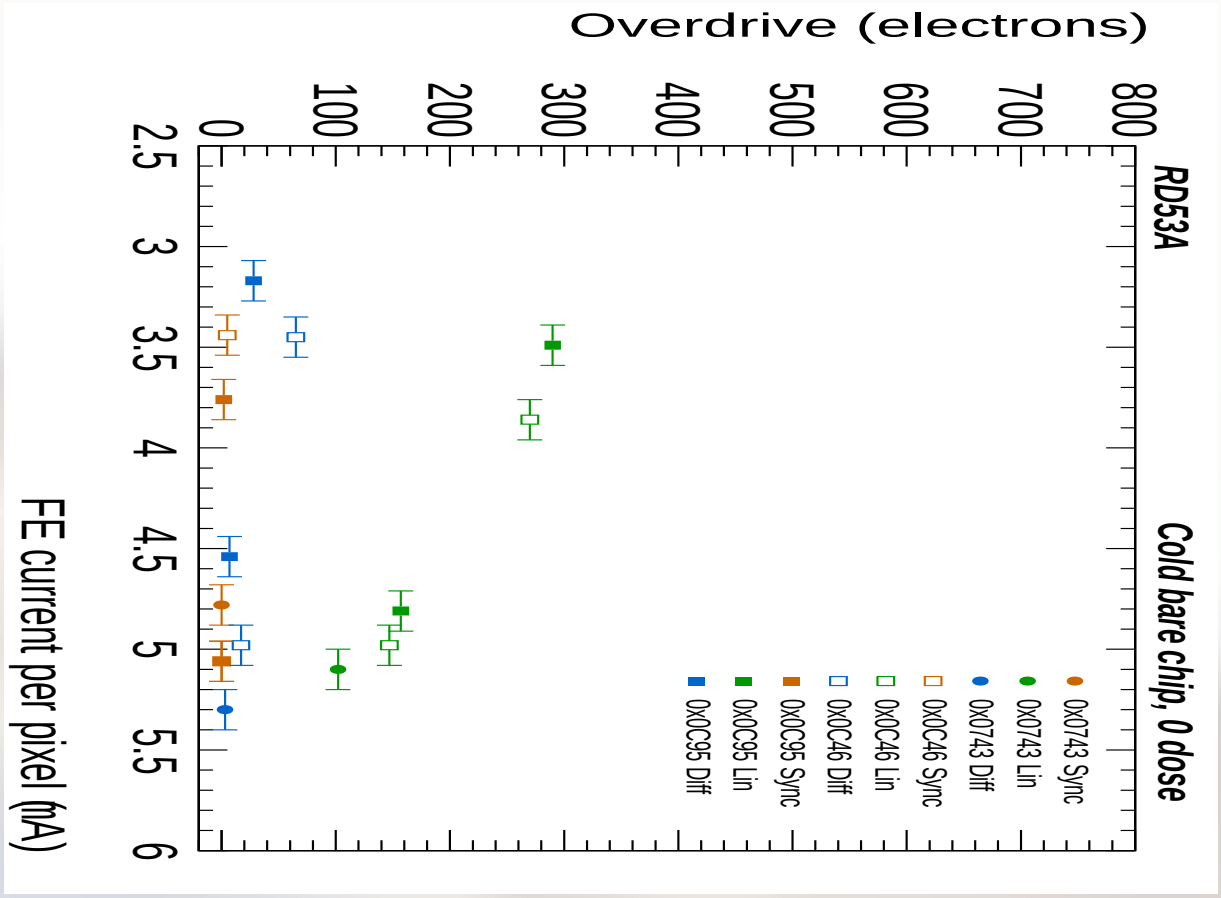
- Measure analog FE trigger output delay as function of the injected charge
- Set the injection voltage, trigger on the injection signal and measure the delay until the HitOr rising edge
- Repeat the measurement for different injection voltages
- Delay should decrease with the number of injected electrons



RD53A Results: Analog FE Characterization

- Verify the functionalities of the three FEs
- Tests with bare chips and 50x50 μm^2 sensors with different settings
- Overdrive: difference between threshold and in-time threshold





RD53 Characterization: Analog FEs

