Status of the Silicon Tracker

Yiming Li (IHEP, CAS)
On behalf of the CEPC silicon tracker community

CEPC Day, 29 Jan 2022

Si Tracker for CEPC

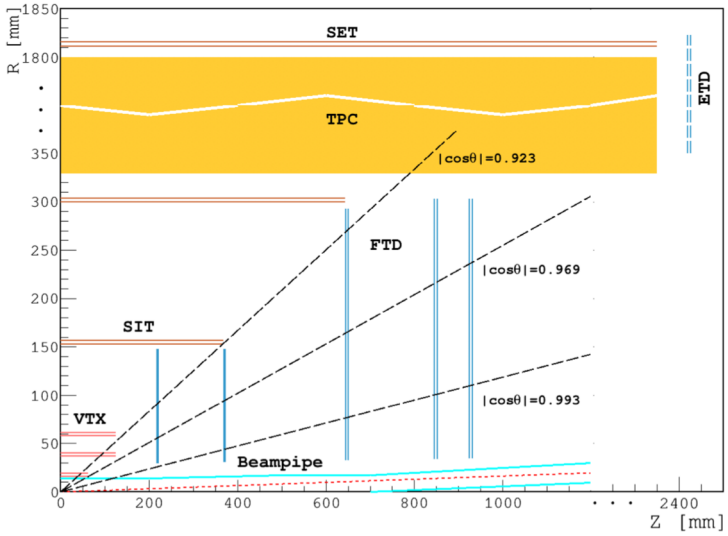
- CEPC requires a high-resolution and low-material tracking system
- Large area of silicon!
  - > 70 m^2 for baseline design: Silicon + TPC
  - ~ 140 m^2 for Full Silicon Tracker

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

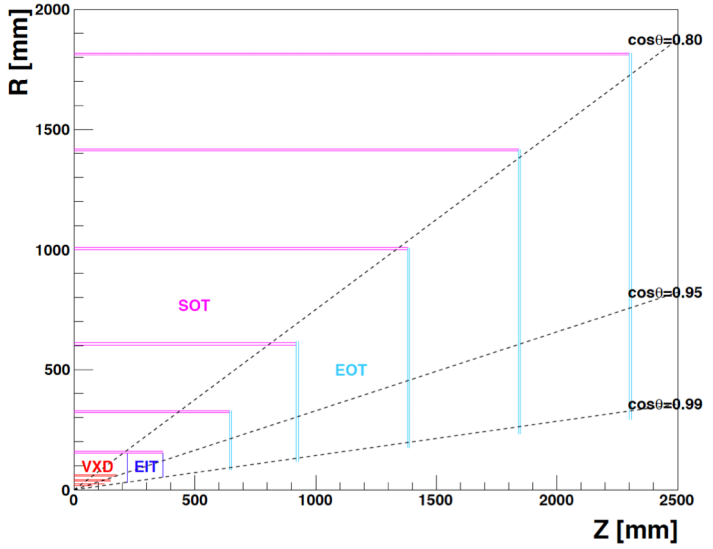
$$a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1}$$

$$b \sim 1 \times 10^{-3}$$

- CMOS is the promising technology for cost effectiveness and performance



Baseline design



Full Silicon Tracker

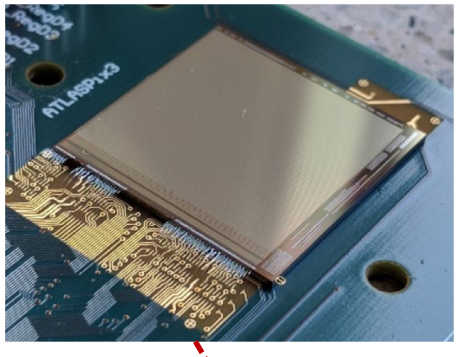
CMOS Si tracker collaborators

Convenors: Harald Fox (U. Lancaster), Meng Wang (SDU)

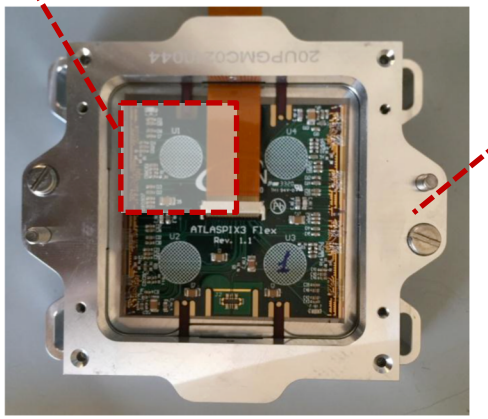
- Australia
  - University of Adelaide
- China
  - Harbin Institute of Technology
  - Institute of High Energy Physics, CAS
  - Northwestern Polytechnical University
  - Shandong University
  - T. D. Lee Institute – Shanghai Jiao Tong University
  - University of Science and Technology of China
  - University of South China
  - Zhejiang University
- Germany
  - Karlsruhe Institute für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisa e Università di Pisa
  - INFN Sezione di Torino e Università degli Studi di Torino
- UK
  - Lancaster University
  - Queen Mary University of London
  - STFC – Daresbury Laboratory
  - STFC – Rutherford Appleton Laboratory
  - University of Bristol
  - University of Edinburg
  - University of Liverpool
  - University of Oxford
  - University of Sheffield
  - University of Warwick

Prototyping Overview

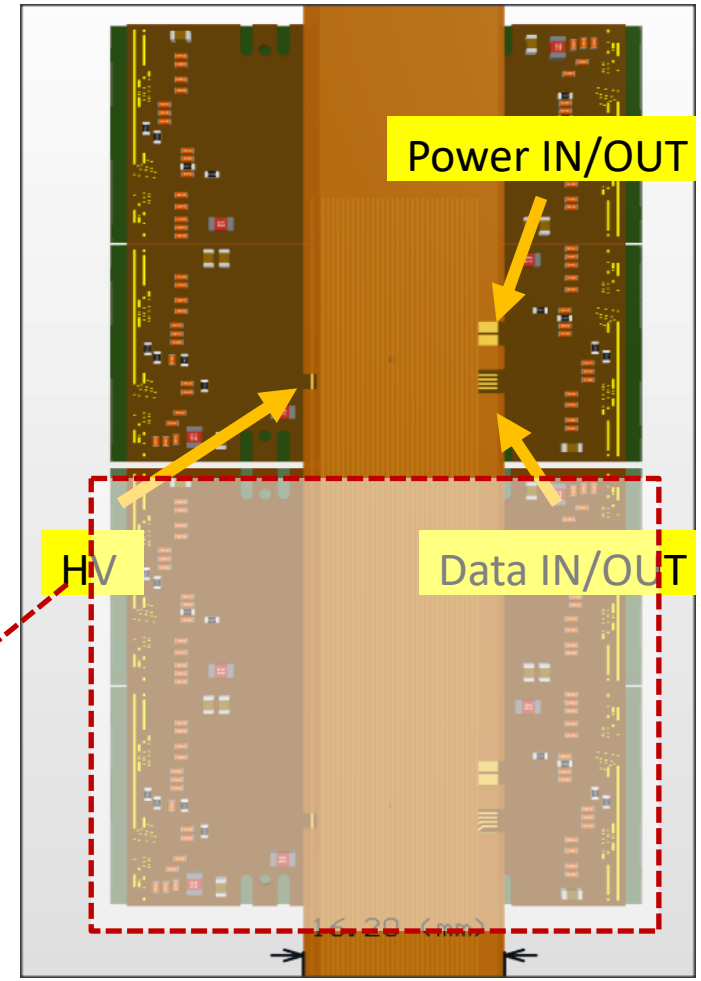
Single chip



Quad module



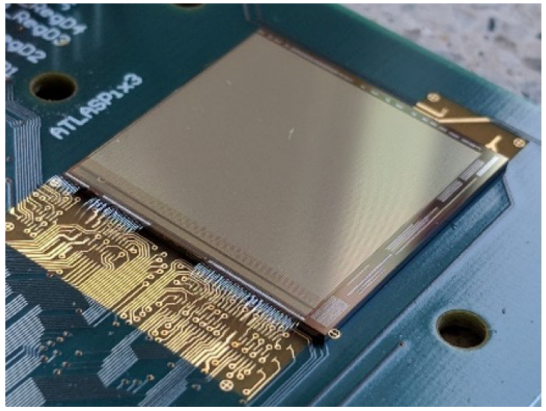
Stave(let) ⋮



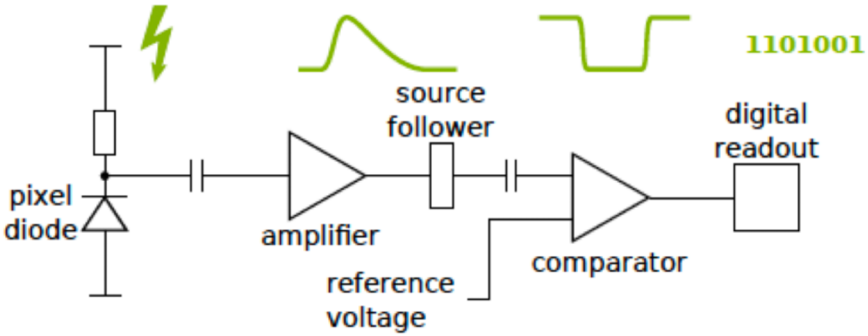
⋮

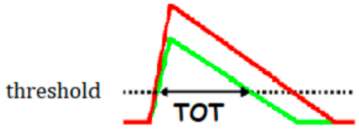
ATLASPix3 sensor

- TSI 180nm HV process on 200 Ωcm substrate
- Pixel size 50 × 150 μm²
- 132 columns × 372 rows (20.2 × 21 mm² chip)
- Triggerless/triggered readout possible
- Binary with ToT information
- Power consumption ~140 mW/cm²



I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021 https://ieeexplore.ieee.org/document/9373986





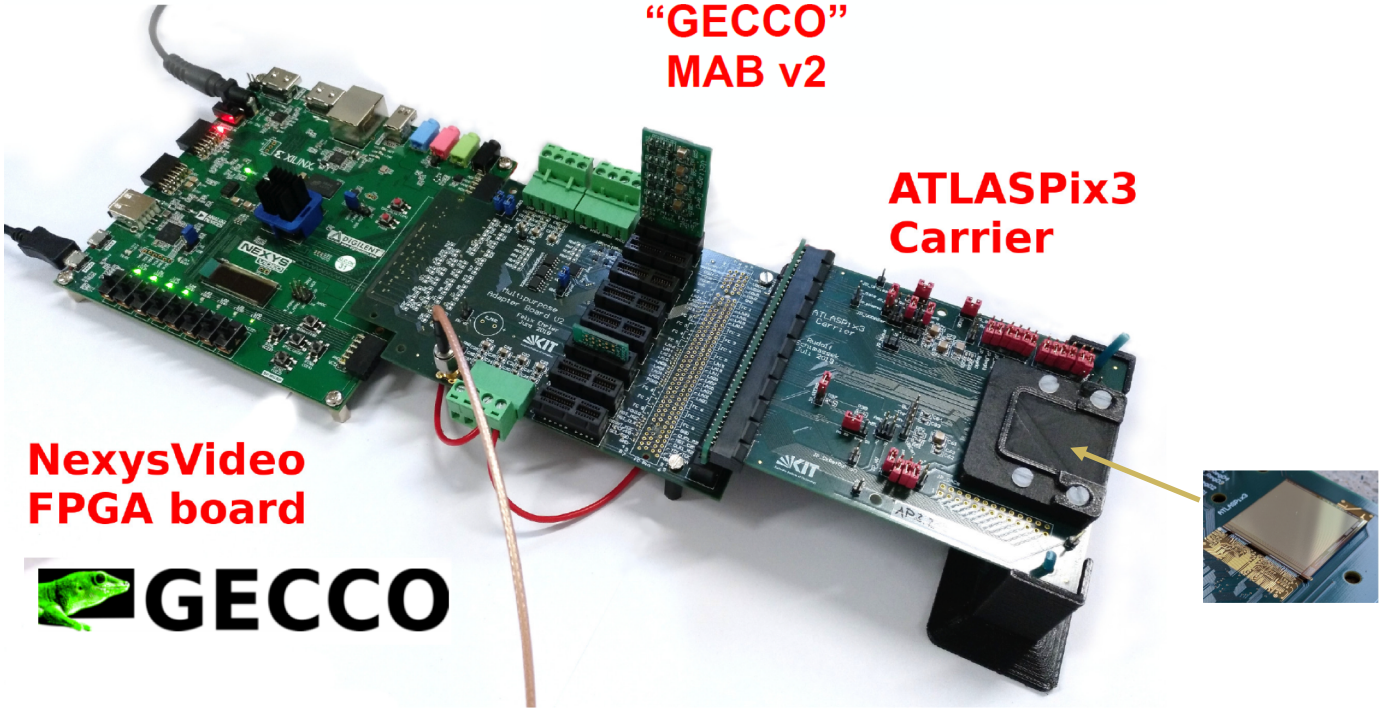
Time-over-Threshold (ToT) as proxy of signal amplitude

Mainly working with ATLASPix3.0 (some thinned to 150um)

ATLASPix3.1 delivered in Feb 2021

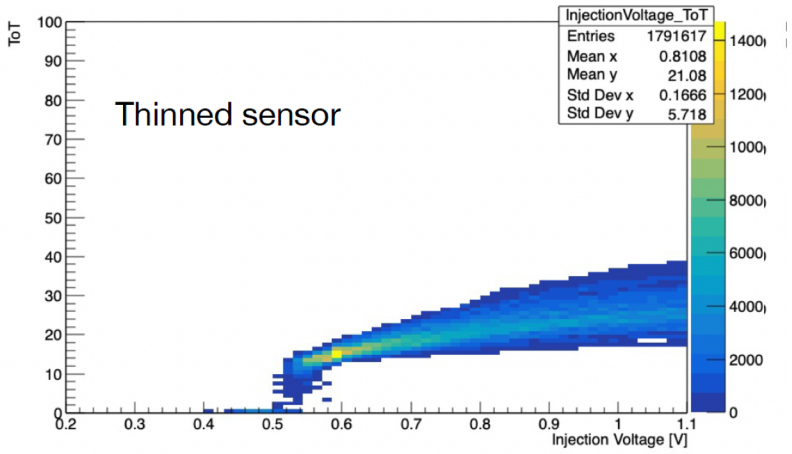
Single-chip programme

- Experience gained with single chip tests (up to last CEPC Day)
  - GEneric Configuration and COntrol System - designed at KIT
  - LFP-FMC connection to Nexys FPGA, PCIe x16 to DUT, allows extensive tests
  - Carrier board for ATLASPix3 single-chip
- O(65) GECCO boards and carrier boards produced in China
- Chips & boards distributed globally and multiple institutes set up lab tests

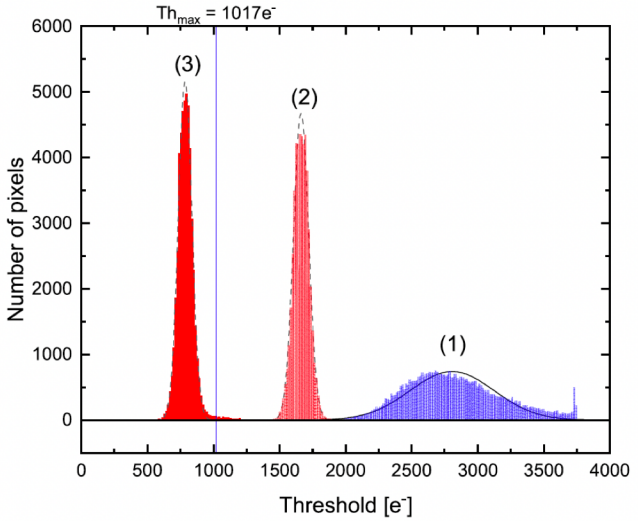


Single chip tests

- ATLASPix3 responses to cosmic ray or various radioactive sources (^{55}Fe, ^{90}Sr, ^{241}Am) are observed at different sites
- Thresholds at 800e noise <~ 80e



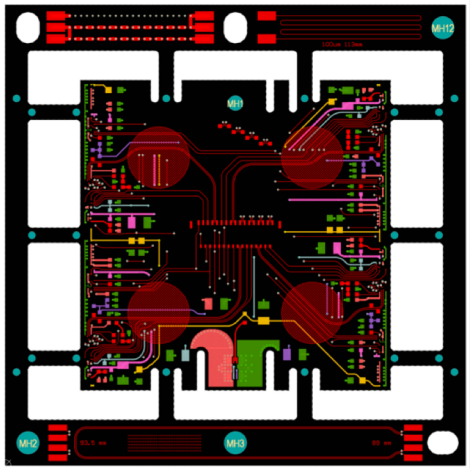
ToT response

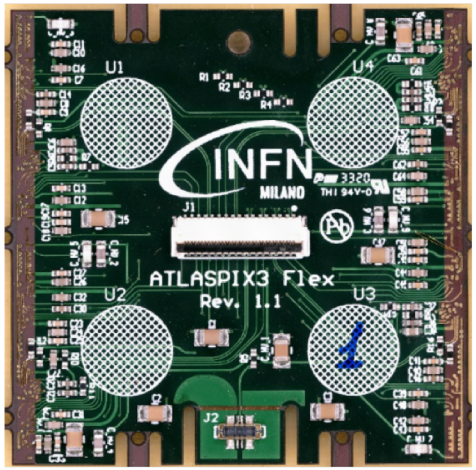


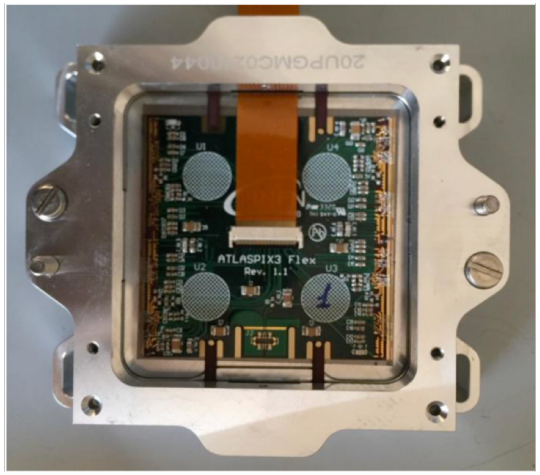
Test with injection charge: (1) untuned (2, 3) tuned with higher / lower thresholds

Quad module

- Four chips sharing services by common power connections and configuration lines
- Inspired by ATLAS ITk quad module concept for large area application







Bianca Raciti, PSD 2021 poster

Quad module test

- Data flex and power cables designed by INFN Milano, under verification
- Adapter card for connecting to GECCO
- 9 quads with ATLASPix3.0 assembled, test ongoing
  - All chips can be configured on a quad
  - Single chip responsive to radiative source

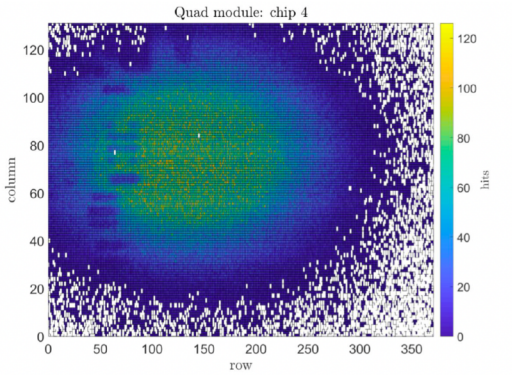
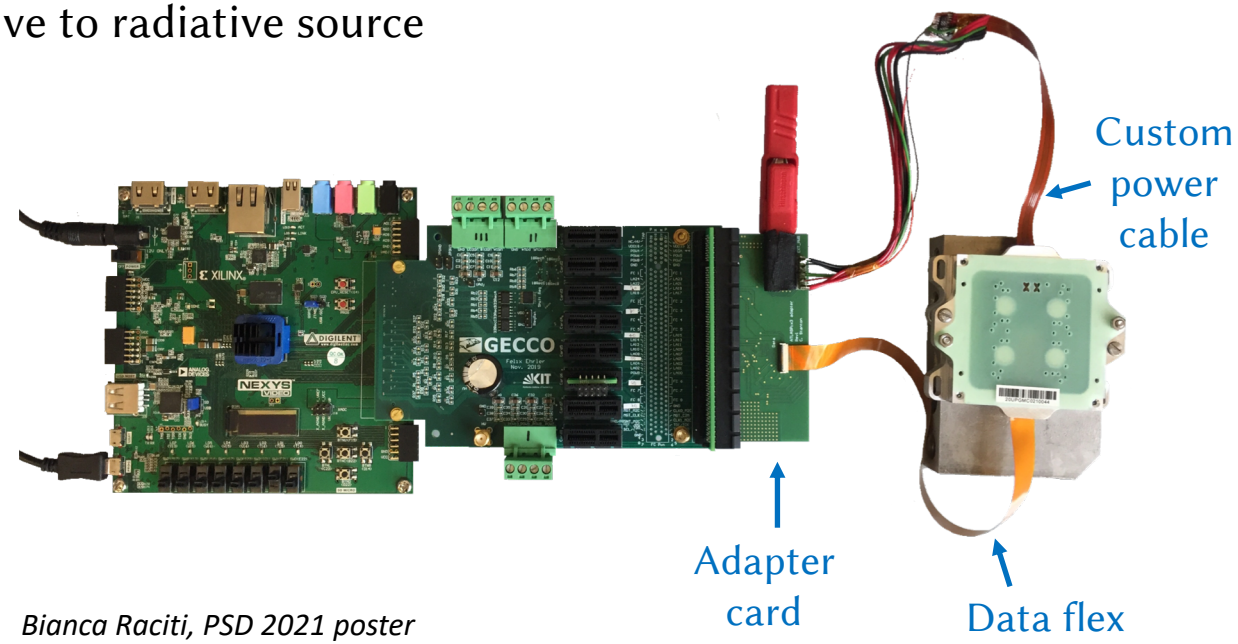


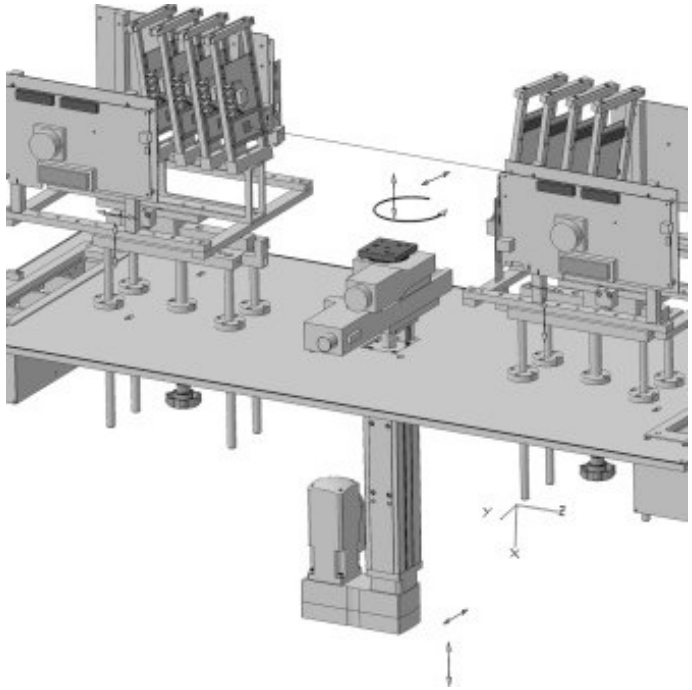
Fig. Hit map of a source run with ^{241}Am on chip 4.



Bianca Raciti, PSD 2021 poster

Plan for testbeam

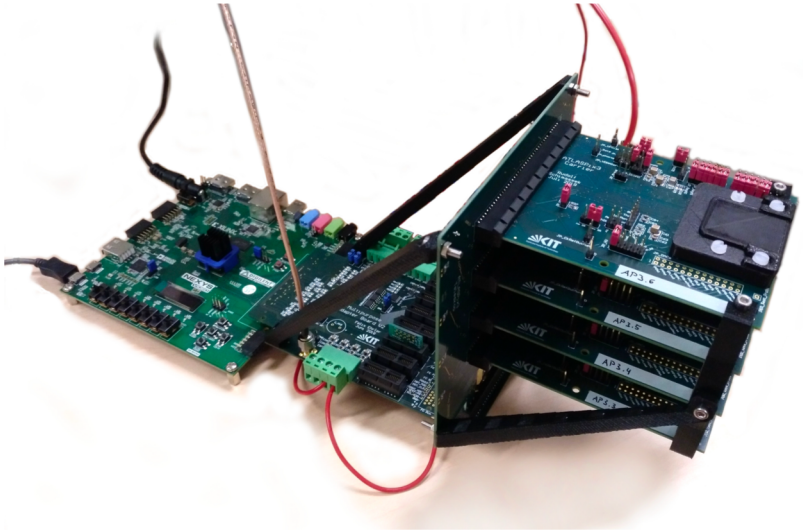
- Motivation:
  - Ultimate test of a sensor system
  - Measure efficiency and position resolution
  - Study performance with angled tracks
- Beam time at DESY booked for 4th April

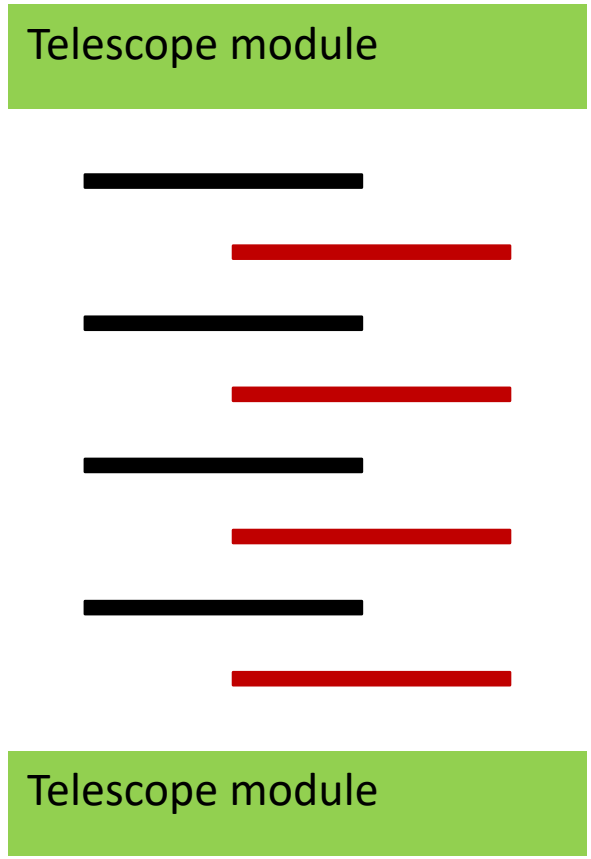


Jaap Veltuis, talk at SiTracker meeting 20 Jan 2022

DUT configuration

- KIT produced telescope cards carrying 4 sensors with ~2.5 cm spacing
- Two stations of 4-sensors in zipper configuration – closest as possible
- No need for trigger: each sensor provides hits and time stamps
- Test setup being assembled by Bristol/Edinburgh/Lancaster

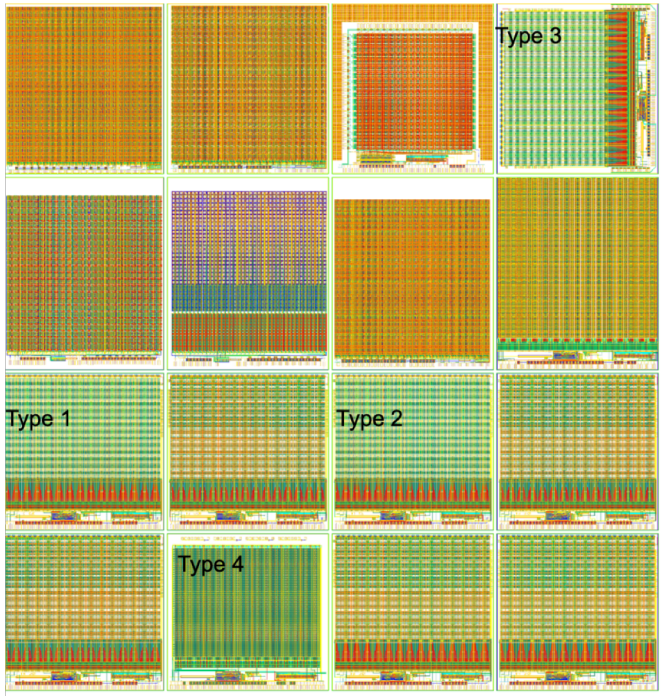




New sensor development

- Improved sensor designs for tracking at electron colliders
  - Joint engineering run with LHCb 2020
  - Designs for CLIC, CEPC, DESY telescope upgrade (TELEPIX)
  - Pixels 25µm X 165µm
- Key improvement
  - Reduced pixel size
  - Different amplifier/comparator types
  - Reduced power consumption

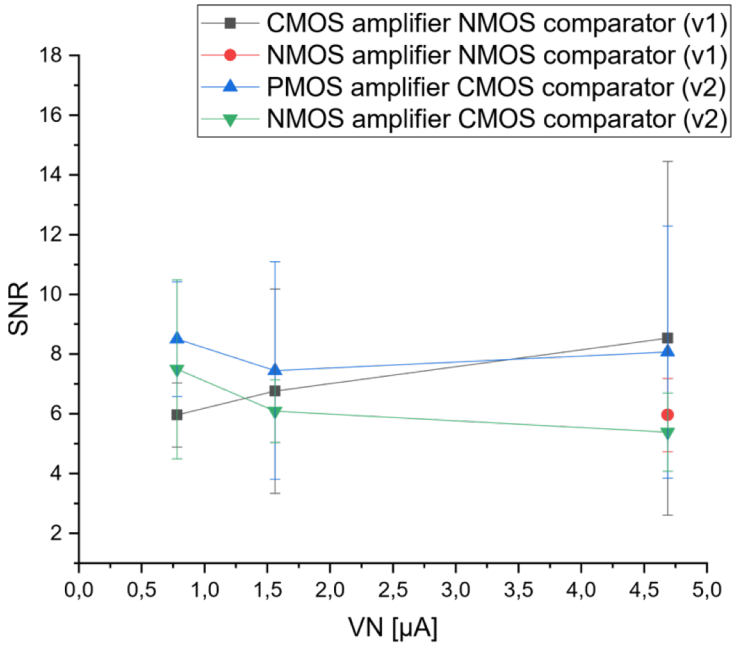
Matrix	Pixel size µm	Pixel type	Amplifier	Comparator
1	25x165	HVCMOS	N/C MOS	NMOS
2	25x165	HVCMOS	N/P MOS	CMOS
3	25x165	HVCMOS	NMOS	distributed
4	25x35	DMAPS	NMOS	CMOS

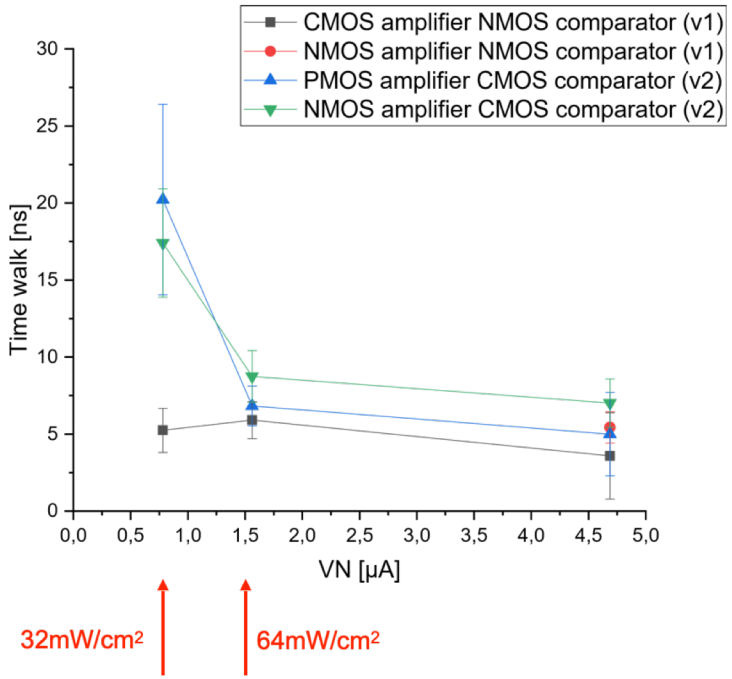


Ivan Peric, UK-CEPC tracker workshop, https://indico.ph.ed.ac.uk/event/103/

Preliminary measurements and implications

- Pixel matrices with three amplifier types have been operated with smallest possible threshold
- Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured
- CMOS amplifier has smallest time walk
- Low power consumption is possible (up to factor of 4 reduction compared with ATLASPix3)



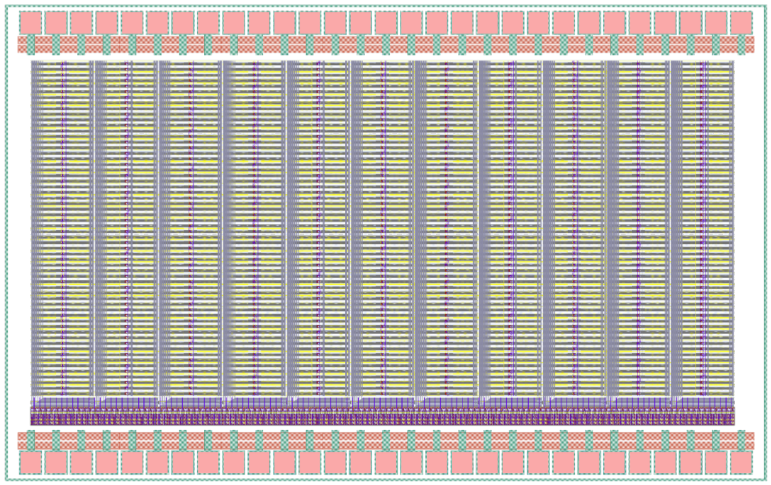


Ivan Peric, UK-CEPC tracker workshop, https://indico.ph.ed.ac.uk/event/103/

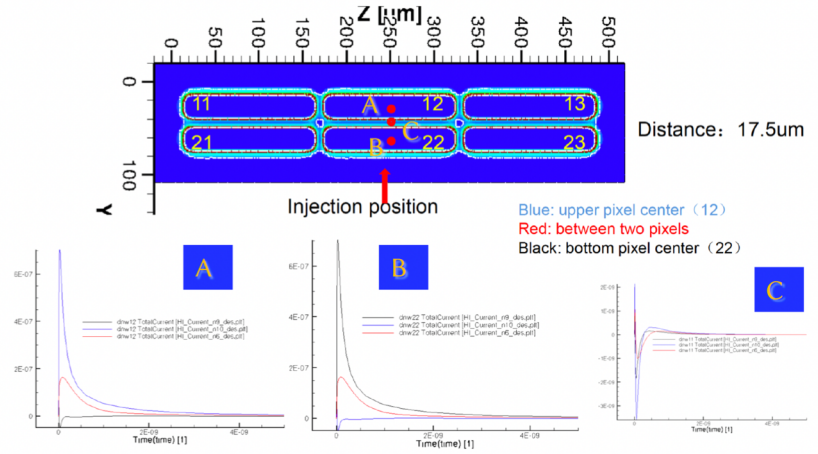
ATLASPIX3: 140mW/cm²

Sensor in 55nm technology

- HLMC (上海华力) offers 55nm technology with similar layers as TSI
- Test sensors designs will be submitted within a MPW run
- Originally planned for Aug 2021, seeking opportunity in Mar 2022
- An area of 3mm*4mm is targeted



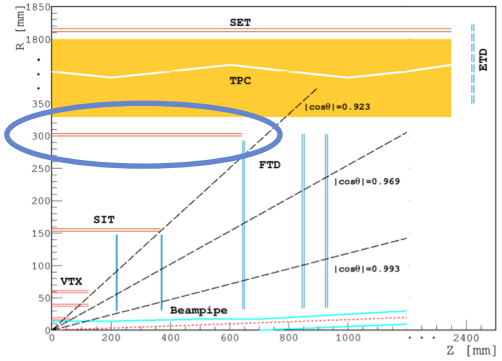
KIT design for test sensors

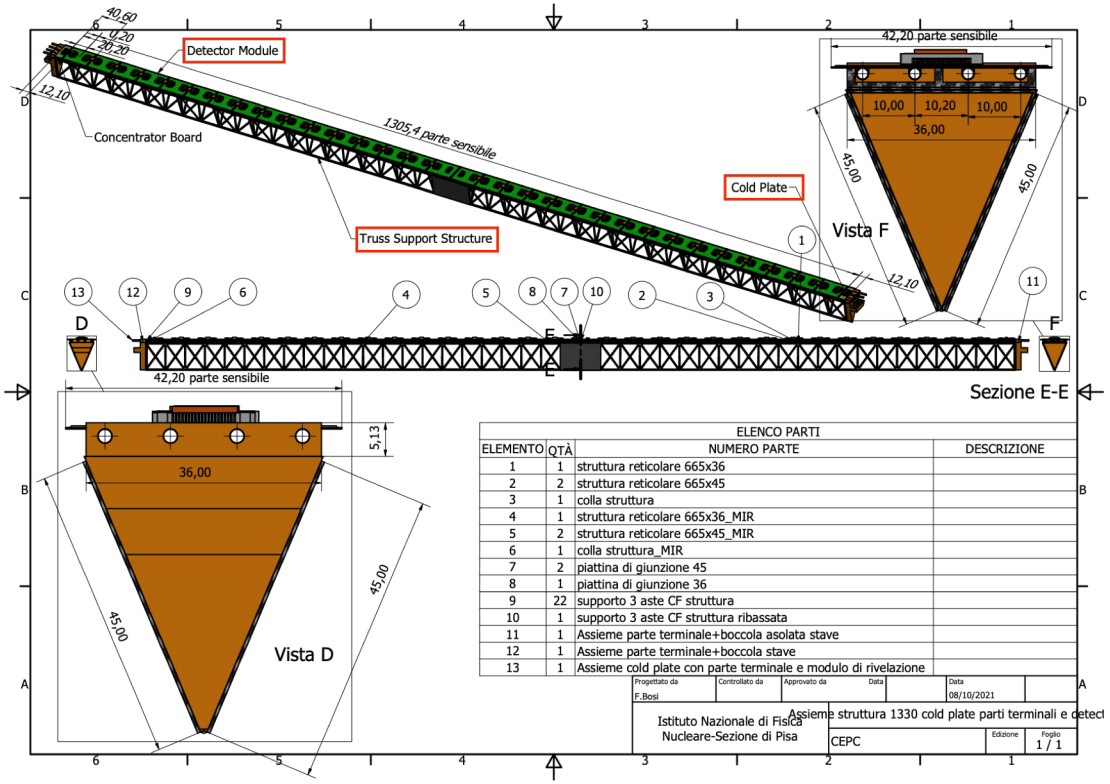


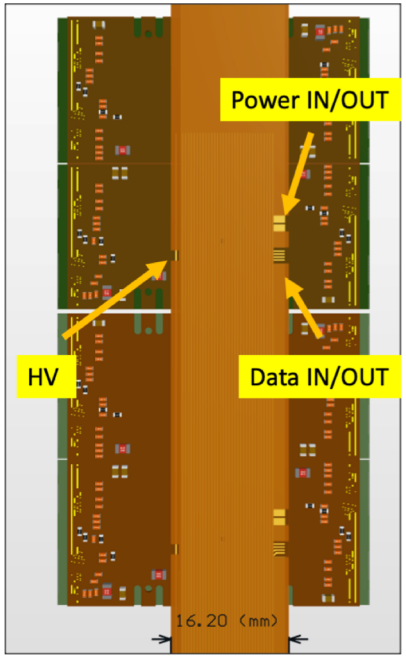
IHEP simulation for 6-pixel test structure

Mechanics design

- System design concept (SIT2)
  - Truss structure for long stave hosting 16 quads
  - Distribute power and data signals along the stave





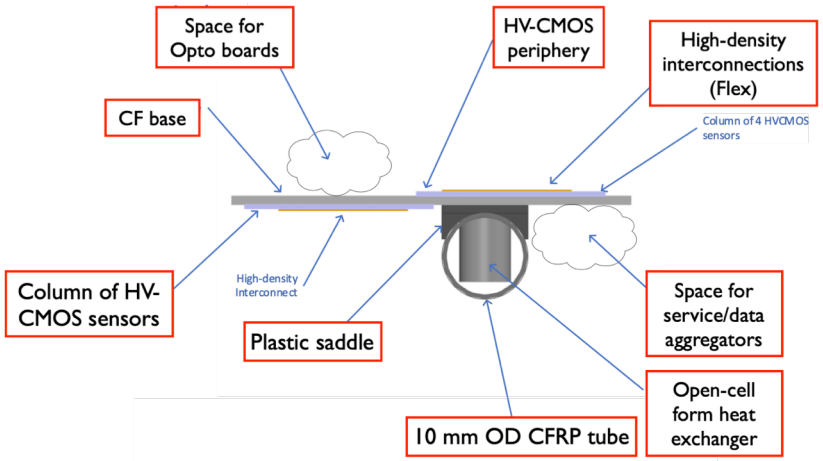


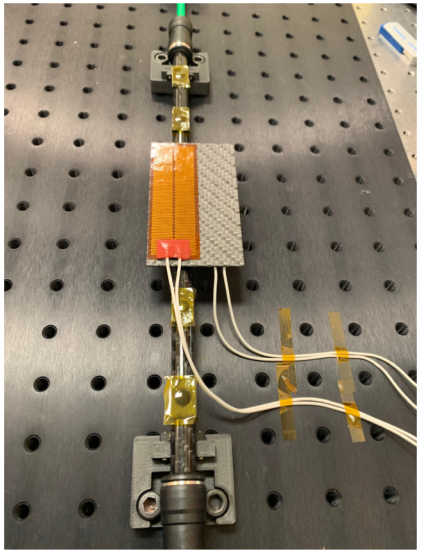
F. Palla, F. Bosi, A. Andreazza, F. Sabatini, UK-CEPC tracker workshop, https://indico.ph.ed.ac.uk/event/103/

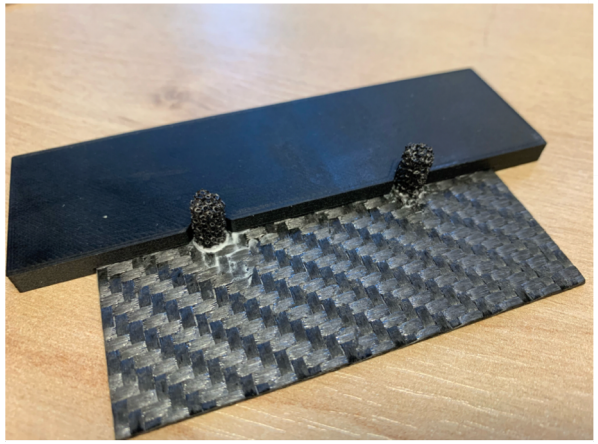
Mechanics prototyping (for SIT-I)

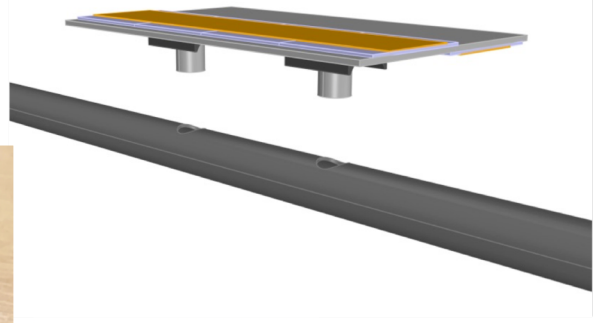
- Sensors glued to CF base
- Base attaches to support tube via saddles
- Saddles have apertures through which the foam heat exchangers pass and glue to the base

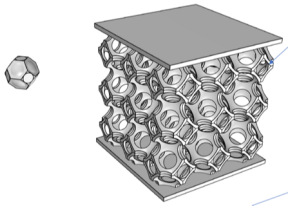
- Thermal performance of foam under study
  - Pre-prototyping ongoing
  - Thermal conductivities under characterization
  - FEA models under development







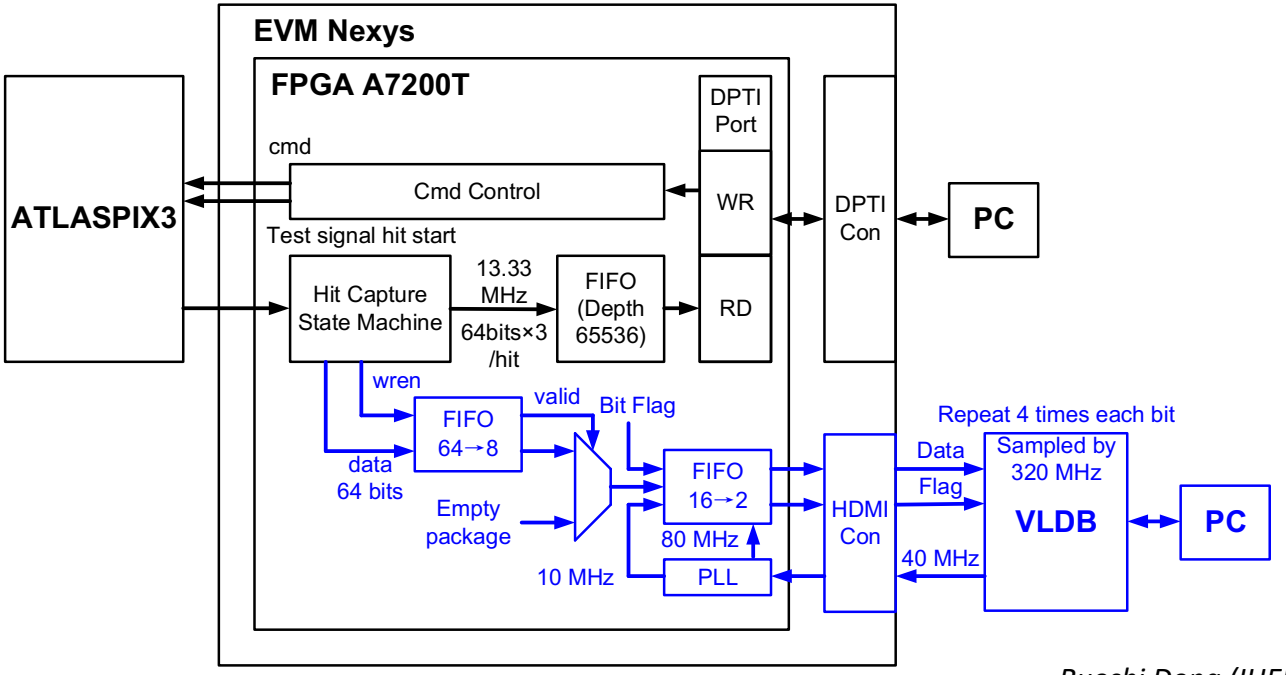




T. Jones, UK-CEPC tracker workshop, https://indico.ph.ed.ac.uk/event/103/

DAQ development

- GECCO works in prototyping phase but not solution for the system
- Efforts ongoing to investigate the feasibility of other readout system
  - VLDB: used for LHCb upgrade, successfully commissioned in real beam
  - Now managed to read the data stream by "hacking" the data stream in FPGA
  - In synergy with LHCb upgrade efforts



Ruoshi Dong (IHEP-KIT joint postdoc fellow)

Summary

- The SiTracker community has accumulated a lot of experience with single chip ATLASPix3 sensors
  - Progress are being made with quad modules towards a demonstrator stavelet
  - The system will be tested at real beam in April
  - New ATLASPix3.1 sensors are being distributed, new results expected
- New sensors are under development dedicated to CEPC need
  - Hopefully with 55nm technology
- Mechanical design for the system and pre-prototyping are progressing

http://cepc.ihep.ac.cn/~cepc/cepc_twiki/index.php/Si_Tracker

BACKUP

ATLASPix3 readout electronics